Evolution of System Electrical Interfaces Towards 400G Transport

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Agenda

Next Generation Interconnect Framework Document and OIF Projects
400G Challenges
Potential Advantages of Architectural Solutions
Chip to Module Interfaces for 400G
Module Architectures
OIF Activities
OIF’s Next Generation Interconnect Framework

Provide an overview of the market drivers for a higher data rate

Identify technical challenges that exist for a next generation data rate including:

- Power dissipation
- IO densities on chips, connectors, and equipment
- Channel characteristics
- Electrical link reach

Identify the application spaces that might benefit from Implementation Agreements

- Both Electrical and Optical
- As short as 15mm and up to 2km
Next Generation Interconnect Framework

Identify the application spaces that might benefit from Implementation Agreements

Die to Die
Chip to chip over a backplane

Inter-Chassis
Chip to chip interface e.g. OIF CEI SR/MR IAs
Chip to chip across a back/midplane interface e.g. OIF CEI MR/LR IAs

Input/Output to card
Chip to Module interface e.g. OIF CEI VSR IAs
What’s Going On In The OIF?

CEI-28G-VSR - very short reach chip to module
CEI-28G-MR - medium reach chip to chip
CFP2 coherent - pluggable module for 100G coherent
Gen 2 100G Long Haul DWDM module
Gen 2 Integrated Coherent Receiver
Integrated Dual Polarization Quadrature Modulated Transmitter Assy

Next Gen Interconnect Framework Document
56G VSR Project - chip to module
56G Ultra short Reach - 10mm reach for chip to chip
56G Close Proximity Reach - 50mm reach for package to package
Mid Board Optics - electro-mechanical footprint
Thermal Management - module to heat sink optimization
400G Long Haul - transponders
Challenges

Traditional Channel Issues:

- 0.75 m reach shows significant dielectric loss/dispersion, even with premium materials
- Even premium connectors exhibit resonances above 12.5 GHz due to chassis tolerances (pin wipe)
- PCB footprints create difficult SI challenges (A/R, finished hole)
- At 56 Gbps:
  - Any skew kills 18 ps NRZ UI
  - System SNR minimal by 25 GHz

Alternative architectures can improve all parameters
Challenges

Chip Technology Issues:
- Current edge rates too slow:
  (Improve 18.5 ps to 12.7 ps)
- Current jitter too high:
  (Decrease $R_{J_{RMS}}$ from 0.35 ps to 0.24 ps
  Decrease $D_{J_{p-p}}$ from 3.2 ps to 2.2 ps)
- Gate capacitance too high:
  (Decrease 0.25 pF to 0.17 pF)
- Chip packaging needs to be improved - decrease XTALK

Chip Challenges:
- Increasing equalizer complexity
- Efficient FEC application

DesignCon 2013: Beyond 25 Gbps: A Study of NRZ & Multi-Level Modulation in Alternative Backplane Architectures, Adam Healey, LSI Corporation, Chad Morgan, TE Connectivity, Megha Shanbhag, TE Connectivity
Architectures

Chassis
- Orthogonal
- Cabled
- Optical

Linecard
- Mid board copper
- Mid board optics

IO
- Optimal channel count:
  - 16x25,
  - 8x50,
  - 4x100

Higher Order Modulation

CDFP MSA

OIF Optical Internetworking Forum
Possible Solutions

Alternate signaling strategies may emerge

- Higher-order modulation (QPSK, QAM, etc.)
- Multi-conductor signaling
- Proprietary techniques currently being examined
Architectures

Vertical eye opening with improved chip parameters and FEC

PAM2

1a: Ideal conventional backplane
1b: Conventional backplane w/ connectors

PAM4

2a: Ideal orthogonal backplane
2b: Orthogonal backplane w/ connectors

3a: Ideal cabled backplane
3b: Cabled backplane with current cable & connectors
3c: Cabled backplane with future cable & connectors

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Next Generation Chip-to-Module Interfaces

400G module interface data rates to eventually double from 25 Gb/s per lane
Introduction to 400G Client Module Requirements

Requirements to initially be driven by IEEE 400G Study Group

Expect several variants (or PMD’s) to be standardized according to reach:

- “Short Reach” - 100 m reach over MMF
- “Long Reach” 500m-10 km reach over SMF
- “Extended Reach” 40 km reach over SMF

One key area of focus will be the 400G transceiver’s electrical interface and its specific evolution over time.
Potential First Generation 400G Long-Reach Module Architecture

Architecture based on 4x 100GbE (100G BASE-LR4) components

IEEE “CDAUI-16” physical interface likely to adopt 4x CAUI-4/CEI-28G-VSR

Probably not the long-term solution for 400G but able to leverage today’s technology
Potential Second Generation 400G Module Architecture (1/2)

8x 50G WDM based upon PAM-4 higher order modulation scheme

Electrical interface also potentially based on PAM-4 signaling
Potential Second Generation Module Architecture (2/2)

Second generation module:

• This architecture is able to be implemented with present 25 Gb/s optics thus leveraging the high volume 100 GbE market

• Narrower 8x module electrical interface leading to higher density line cards and lower power consumption

• As well, PAM-4 based retimers would be able to re-use the present CAUI-4 based infrastructure and thus enable similar “chip-to-module” reaches (more on this later)
Potential Third Generation 400G Module Architecture

- 4x 100G WDM based upon PAM-N higher order modulation scheme
  - Other optical modulation alternatives including DMT/QAM approaches leveraging DSP techniques are also possible
- Electrical interface could be based on PAM-4 signaling
  - 100G serial approach will be extremely challenging!
56G Chip-to-Module Channel

Potential 56G channel based upon present CEI-28G-VSR channel

Channel Loss @ 14 GHz = 10 dB

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<th>On-die term.</th>
<th>Device package</th>
<th>VSR host channel PCB Model (2 via transitions + 5” Nelco stripline)</th>
<th>zQSFP+ Connector Model</th>
<th>Module PCB + AC coupling caps Model</th>
<th>Device package</th>
<th>On-die term.</th>
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~ 7 dB       < 1 dB       ~ 2 dB
Typical CAUI-4/CEI-28G-VSR Channel Response

Present CEI-28G-VSR allows for up to 10 dB of loss

- Operating this channel with NRZ signaling at 56 Gb/s doubles channel loss to 20 dB – very challenging!

Crosstalk noise also expected to be a key consideration for this new interface
Typical PAM-4 Waveforms

Wide open eyes at input to slicer!
For VSR types of channels PAM-4 equalization can be largely analog based!
Benefits of PAM-4 Signaling at 25.78 Gbaud

56G NRZ solutions are likely to require a more advanced CMOS technology that is not available today.

NRZ based connectors for 56G may also require focus from the industry which will take time.

56Gb/s PAM-4 transceivers can be implemented with today’s technology; NRZ will require technology advances and higher power.
OIF Interconnect roadmap

CEI-28G-VSR/MR projects nearing completion

- **28G-VSR** to be leveraged by several standards including IEEE 802.3bm and T11 32G-FC

**Several new 56G projects underway with more to come!**