Enabling 56Gb/s Architectures
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Industry Trends and Associated Products

- Trend to 56Gb/s per differential pair as standalone rate as well as a building block to higher rates, ie 56G x 8 = 400Gb/s
- To ensure meeting ecosystem need, multiple 56G reaches are being defined
- Any further optimization of the channel results in access to more flexible architectures
- Additionally, reducing system power by improving channel (but not sacrificing reach)
  - Driving the reach of backplane channels with retimers/equalizers
  - Traditional orthogonal
  - Cabled backplane
  - Chip-to-Chip and Chip-to-World
Conventional Architectures

- Chip to chip interface e.g. OIF CEI SR/MR IAs
- Chip to chip across a Back/Midplane interface e.g. OIF CEI MR/LR IAs
- Chip to Module interface e.g. OIF CEI VSR IAs
- Input/Output to card
- Inter-Chassis
Traditional Backplane and Orthogonal

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<thead>
<tr>
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<th>Power</th>
<th>56 Gbps Reach (PAM4)</th>
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<tbody>
<tr>
<td>Traditional PCB &amp; STRADA Whisper Connector</td>
<td>100% (LR Serdes)</td>
<td>1m</td>
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Full Power Serdes on IC capable of 35 dB channel Loss without need for retimers

Traditional Backplane

Orthogonal Backplane
Cable Backplanes: Margin/Thermal/Reach

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<td>STRADA Whisper Cable Backplane Connector</td>
<td>100% (LR Serdes)</td>
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<tr>
<td>Traditional PCB &amp; STRADA Whisper Connector With Retimers</td>
<td>150% (VSR + AEC)</td>
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Insertion Loss with Different Media

**DAUGHTER CARD**
- Board Material = Megtron6 VLP
- Trace length = 5”
- Trace geometry = Stripline
- Trace width = 6 mils
- Differential trace spacing = 9 mils
- PCB thickness = 110mils, 14 layers
- Counterbored vias, 1 – 6mil stub
- Test Points = 2.4mm (included in data)

**PCB BACKPLANE**
- Board Material = Megtron6 HVLP
- Trace length = 30”
- Trace geometry = Stripline
- Trace width = 6 mils
- Differential trace spacing = 9 mils
- PCB thickness = 200 mils, 20 layers
- Counterbored vias, 1 – 6mil stub
- STRADA Whisper Vertical Header and Right Angled Receptacle

**CABLED BACKPLANE**
- TE-Madison TurboTwin 40G Cable
- 30AWG, 1 meter [39.37”]
- STRADA Whisper Cabled Header and Right Angled Receptacle

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**Diagram**

- Frequency vs. Magnitude, dB
- Data points: 16.9dB @12.89GHz
- Data points: 30dB @12.89GHz

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**Diagram Details**

- Frequency range: 0 to 40 GHz
- Magnitude range: -100 to 0 dB
Optical Backplanes: Density/Reach Extension

½ Power Serdes + E/O + O/E Optical Power. 100M Reach including 2 Optical connectors

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<tr>
<td>STRADA Whisper Cable Backplane Connector</td>
<td>100% (LR Serdes)</td>
<td>3m</td>
</tr>
<tr>
<td>Traditional PCB &amp; STRADA Whisper Connector With Retimers</td>
<td>150% (VSR + AEC)</td>
<td>1.5m</td>
</tr>
<tr>
<td>VCSEL Optical Backplane</td>
<td>150% (VSR + Optics)</td>
<td>100m</td>
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# Mid Board Optics for I/O: Density and Reach

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<td>Traditional PCB w/ Direct Attach Passive Cable</td>
<td>100% Reference</td>
<td>3m</td>
</tr>
<tr>
<td>Traditional PCB w/ Pluggable VCSEL Optics</td>
<td>150%</td>
<td>100m</td>
</tr>
<tr>
<td>Traditional PCB w/ Power Retimers and Direct Attach Passive Cable</td>
<td>150%</td>
<td>5m</td>
</tr>
<tr>
<td>Mid Board VCSEL Optics</td>
<td>150%</td>
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Summary

OIF CEI-56G IAs will enable next generation equipment
PAM4 and NRZ being investigated, next gen connectivity likely to support both modulations
Creative connectivity/packaging solutions will enable enhanced channels
56Gb/s architectures will continue to be heavily based on copper interconnects
Optics will play where reach and/or density dominate the requirement