56G Common Electrical Interface

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Join the OIF
OIF CEI interfaces for 56G
OIF CEI-56G applications for NRZ
  - XSR (Chip to optical engine)
  - VSR (Chip to Pluggable module)
  - MR (Chip to Chip)
NRZ test and simulation results
Conclusion that NRZ is better than PAM4
Why Join the OIF?

- The OIF is the leading the way in the development of 56G electrical interfaces
OIF CEI Interfaces for 56G

LR
Switch card

USR
MR
XSR
VSR
XSR defines chip to optical engine interconnect

OIF CEI-56G-XSR

Courtesy Molex
NG Switch Chip (Design Study) - Double the capacity using ‘traditional’ design for 56G I/O

- Assumes 56Gb/s LR Serdes does not scale
- New Process Node: 28nm -> 20nm
  - Serdes Area hardly scales
  - ~ 30% performance improvement not enough
    ➢ Not feasible
- Two Process Nodes: 28nm -> 16nm
  - ADC, DAC, DSP Serdes Solution
  - Advanced Modulation Schemes add Complexity
  - Power per bit can hardly be reduced (~180W IO)

➢ Power and Area Overkill
NRZ SIMULATIONS for 56G XSR

- TX Vod: 400 mV

- EW: 0.48 UI, EH: 109 mv
CEI-56G-VSR candidate channel

Channel includes:
- Package model
- RX input termination capacitance
- VSR (QSFP) connector model

ILoss @ 28 GHz = -23.2601 dB
CEI-56G-VSR-NRZ eye diagram

VO=37.16 mV HO=0.26 UI DER_{ec} = 2.83e-44

Note: simulations included:
- RX jitter and package
- 3mv rms input noise
- TX jitter
Why NRZ over PAM4

- PAM4 has a 9dB penalty
  - 3 PAM4 eyes in the same voltage swing as 1 NRZ eye
  - VSR channel shows an 8-9dB difference

- NRZ has ‘knobs’ that should be ‘turned’ before we move to PAM4
  - Additional CTLE gain
  - DFE
  - TX equalization
  - Higher performance Printed Circuit Boards
Conclusions

1) The OIF is defining solutions for the next generation electrical interfaces (get on board)
2) NRZ provides the best overall CEI-56G solution