



## **Common Electrical I/O: Building for the Future**

### **Executive Summary**

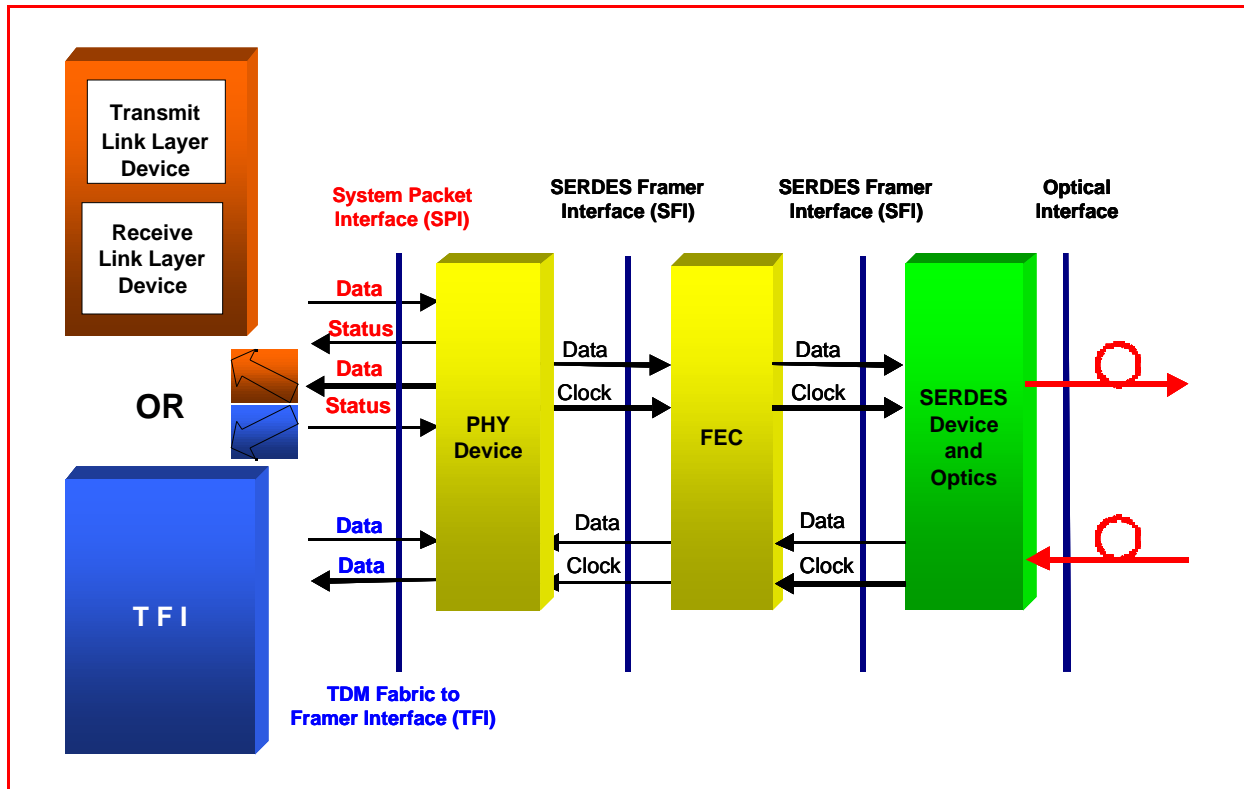
Recognizing industry's need for the entire component level infrastructure to be upgraded to support higher system capacity, the OIF authorized the PLL Working Group to begin a new project, referred to as the Common Electrical I/O (CEI). The goal of the project is to define electrical specifications for 4.976 to 6+ Gigabit and 9.95 to 11+ Gigabit serial signaling for chip-to-chip and board-to-board applications. These specifications will provide the basis for the electrical interfaces that will be used to enable the higher capacities needed for the next generation of systems.

### **Introduction**

The mission of the Optical Internetworking Forum (OIF) is to foster the development and deployment of interoperable products and services for data switching and routing using optical networking technologies. This requires addressing multiple issues related to optical internetworking at the carrier, system vendor, and component vendor levels. This integrated approach strengthens the OIF's ability to fulfill its mission.

The Physical and Link Layer (PLL) Working Group of the OIF specifies implementation agreements (IA) that not only enhance the interoperability of communication links at the optical level but also at the electrical interface, which includes the electrical properties and protocol, between the different components in a typical optical networking application. Figure 1 provides an architectural overview of the various components and interfaces that have been defined by the OIF PLL group.

The SERDES Framer Interface (SFI) defines an electrical interface between a SONET/SDH Framer and the high speed Parallel-to-Serial/ Serial-to-Parallel (SERDES) logic. The SERDES logic typically resides inside the optical module that will carry data traffic but can also be on the host application board. The System Packet Interface (SPI) is between the Physical Layer (PHY) device(s) and the rest of the SONET/SDH System (i.e. between the SONET/SDH Framer and the Link Layer). The SXI-5 specification defines the electrical I/O characteristics for the SPI-5 and SFI-5 interfaces. The TDM Fabric to Framer Interface (TFI-5) Implementation Agreement is an alternative framer interface compared to SPI-5, which is targeted for packet/cell switch fabrics. It operates at the STS-48/STM-16 equivalent bit rate over a backplane.



**Figure 1 - The OIF Infrastructure**

The challenge in designing a system is to maximize its capacity while minimizing size, power and implementation costs. Thus, one of the key factors driving the system's entire internal infrastructure is its I/O capacity, which is the product of the number of cards in a system and the capacity per card. This makes the physical size of an I/O module and its capacity a significant issue to the system architect. Although recent advances to reduce power consumption and reduce package size while increasing signaling speed in fiber optic transceivers are helping to drive up the capacity per card; advances in packaging and electrical signaling are also necessary to reduce the systems overall size.

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## I/O Capacity Explosion

Next generation systems will target higher capacities. The underlying infrastructure will have to be overhauled to support higher aggregate bandwidths to provide a better performance to cost ratio, while simultaneously reducing overall space, power, and cost.

Recently, the XFP 10 Gigabit Small Form Factor Pluggable package definition was completed by the XFP Multi Source Agreement (MSA) Group ([www.xfpmsa.org](http://www.xfpmsa.org)). By using a serial high-speed interface and reducing the necessary number of signal pins, the group was able to reduce the overall width of the package, as demonstrated in Figure 2. Figure 3 provides a comparison of the physical dimensions of various modules, which demonstrates that the XFP has the smallest footprint of competitive 10G serial solutions currently on the market.

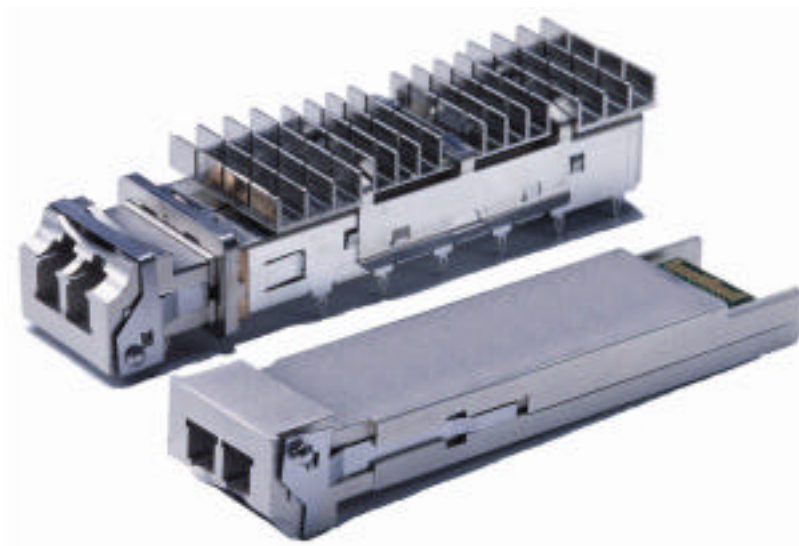


Figure 2 – XFP Module

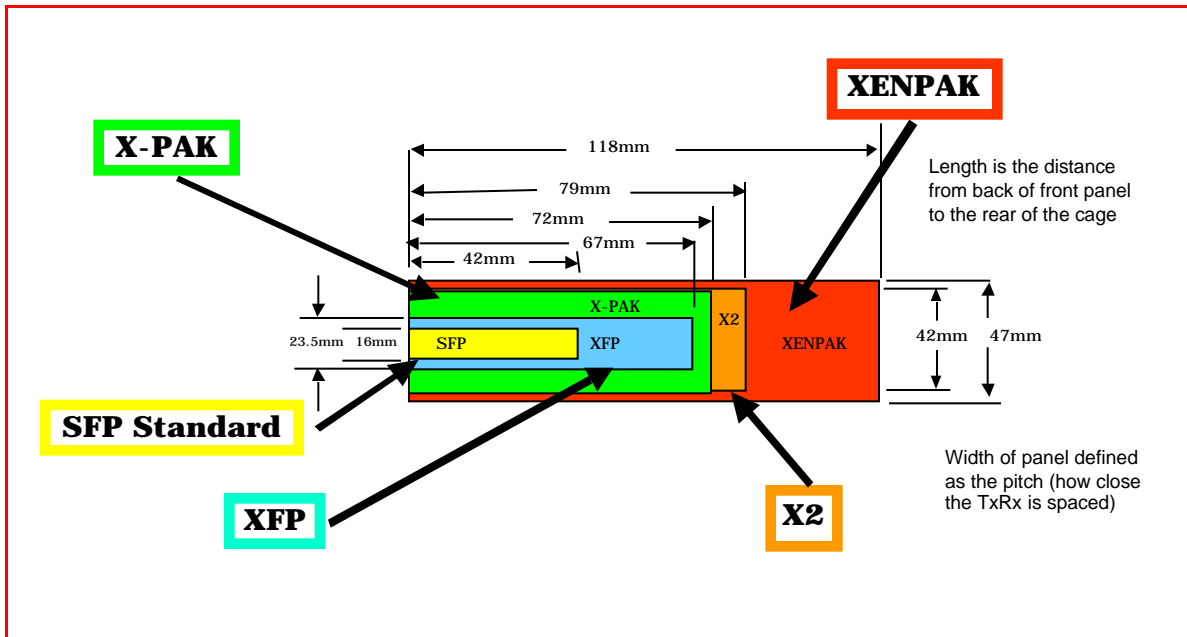


Figure 3 – Comparison of Module Footprints<sup>i</sup>

Figure 4 demonstrates the impact of the serial line rate on the number of electrical pairs that would be needed at the switch card as the optical capacity of sixteen line cards feeding into the switch card is varied from 20 Gbps to 320 Gbps. It is clear that the I/O capacities enabled by the reduction in packaging size of the XFP module is providing a catalyst to the industry to upgrade the entire underlying infrastructure used to develop current systems..

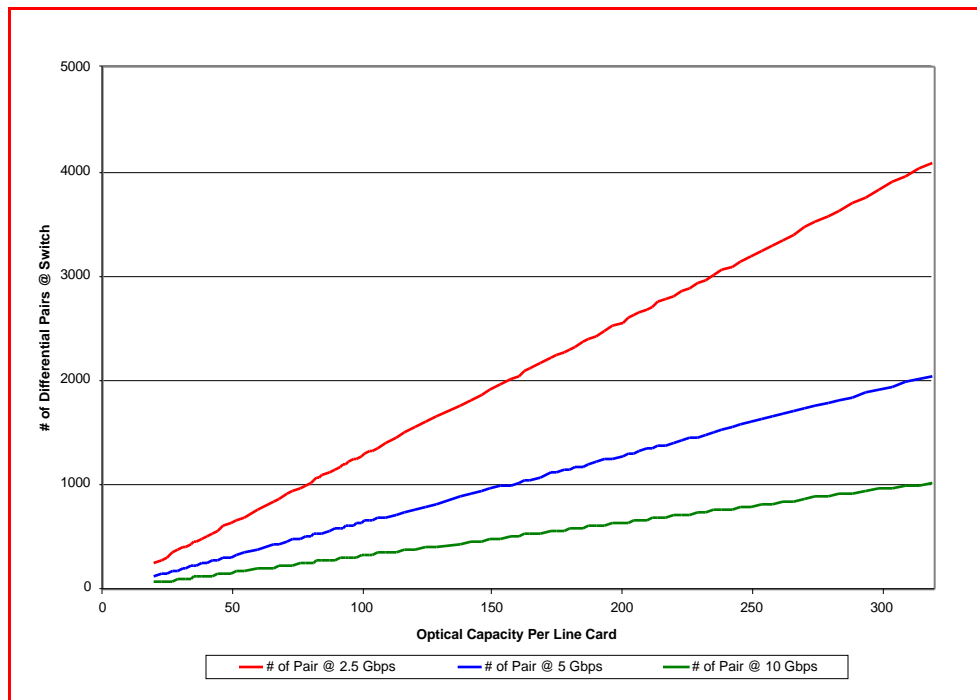


Figure 4 – Impact of Increased Capacity

## **Introducing the CEI Project**

Recognizing the industry's need for the entire component level infrastructure to be upgraded to support higher system capacity, the OIF authorized the PLL Working Group to begin a new project, referred to as the Common Electrical I/O (CEI). The goal of the project is to define the electrical specifications for 4.976 to 6+ Gigabit and 9.95 to 11+ Gigabit serial signaling. Each of these rates will be defined to support both short reach ("SR": 0 to 200 mm or 8 inches of printed circuit board trace with up to one connector) and long reach ("LR": 0 to 1 meter or 39 inches of printed circuit board trace with up to two connectors) applications.

CEI short reach signaling will provide the basis for the next generations of SFI and SPI interfaces, while CEI LR buffers will power backplane communications and next generation TFI interfaces. Four separate clauses will define these four specifications; namely, 6G+ SR, 6G+ LR, 11G+ SR, and 11G+ LR, respectively. The SR and LR specs will endeavor to use common specifications at 6G+ and common specifications at 11G+ as much as possible.

CEI buffers will be based on high speed, low voltage logic with a nominal differential impedance of 100  $\Omega$ . Connections are point-to-point balanced differential pairs and signaling is unidirectional. The CEI implementation agreement (IA) specifically excludes any requirements on pin-out, management interface, power-supply specification, or higher-level activity such as addressing or error control. Signaling is DC balanced non-return-to-zero (NRZ) with appropriate sync or framing bits provided by respective protocols. A related OIF implementation agreement in development, called the Data Protocol Project, will describe the protocols to be used over CEI. The compliant bit error rate will be at least  $10^{-12}$ , with an objective of  $10^{-15}$ . The IA will support AC-coupling and will optionally support hot plug capabilities.

### ***CEI SR I/O***

The new CEI signaling interfaces will enable the reduction in bus widths to support higher capacity line cards by reducing board real estate requirements and reducing power requirements to further simplify line card design. Furthermore, the development of the 10 Gigabit Serial Electrical Interface (XFI) by the XFP MSA group has demonstrated that serial 10Gbps transmission over 8" of FR4 with one connector is feasible.

It can easily be seen how chip-to-chip applications, such as SFI and SPI, could be taken to new levels of performance by CEI SR buffers similar to XFI, but it will be critical that the following technical issues are resolved by the CEI SR specification:

- *Data coding requirements:*  
Different encoding techniques can affect the jitter introduced by the channel and the Phase Locked Loop filter characteristics. The CEI specification must analyze the impact of the different coding schemes to maintain support of the broadest range of standard interfaces. The correct determination of the coding effects on electrical and jitter characteristics will be vital for guaranteeing interoperability.

- *Signal levels*  
Signal levels must be minimized to reduce power and emissions. However, the levels must still allow for sufficient signal to noise ratio to make the channel operate at a low Bit error rate. The ability to DC couple also needs to be considered for direct chip to chip connections.
- *Bit error rate requirements*  
The industry desires lower bit error rates than the normal optical bit error rates of  $10^{-12}$  for the underlying infrastructure in order to maintain the  $10^{-12}$  bit error rate for the overall system.
- *ESD*  
ESD protection must be provided up to the maximum level while avoiding the degradation of the signal integrity.
- *Channel characteristics*  
The correct definition and modeling of the channel characteristics will allow vendors to avoid “over-designing” the interface to accommodate for unknown variances in impedance, return loss etc.
- *Jitter requirements*  
The jitter requirements of even this relatively short distance link need to be carefully specified in order to avoid impacting the optical jitter requirements and avoid over-designing of either the transmit or receive interface.
- *Constraints on optical channel specifications*  
The solution selected should not have an impact on the optical channel requirements. This will allow the widest use of the interface specification.

### **CEI LR I/O**

CEI LR buffers will power backplane communications and next generation TFI interfaces. System vendors will use these buffers to not only create new systems, but to also extend the life of existing systems by expanding the backplane capacity of these systems. These “legacy” backplanes pose a particularly challenging problem, since there is a limited ability to improve system performance because of a fixed electrical channel. The CEI LR buffers themselves must enable the backplane to achieve higher capacities. In a backplane environment the capability of every high-speed pair on every signal layer needs to be considered, especially when considering the various layers within the backplane. Figure 5 demonstrates how the different layer extremes in a backplane will have significantly different performance capabilities. This variation grows as the backplane thickness grows, and poses a significant hurdle for chip vendors.

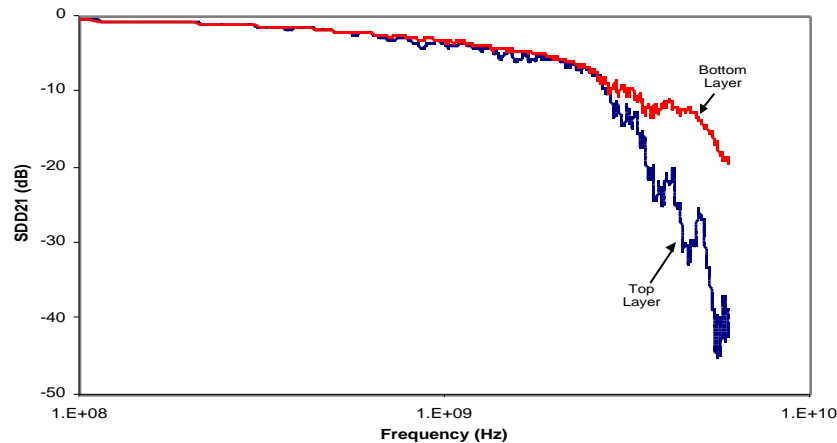


Figure 5 – Impact of Layer Connection on Channel Throughput

For TFI-5 and XAUI the bit rate ranges from 2.488 Gbps to 3.125 Gbps. At these speeds shaping the signal at the transmitter can typically compensate for the loss of the channel. This technique is known as pre-emphasis, or alternatively de-emphasis, and is an example of pre-equalization.. Figure 5 demonstrates the low-pass filter nature of a channel. It can be seen that as the frequency of operation increases, so does the amount of channel loss. At the 6+ and 11+ Gbps speeds, transmit pre-emphasis by itself does not sufficiently compensate for the loss of the channel. To compensate for the additional loss, equalization will be employed at the receiver. There are various flavors of receive or post-equalization techniques, such as linear filter equalizers, decision feedback equalizers (DFE), and feed forward equalizers (FFE). Thus, an optimum combination of pre and post-equalizations will work the best to counter the interconnect losses associated with these higher speeds of operation.

CEI LR 11+ I/O face the same problems illustrated in Figure 5. "Greenfield" backplanes, which refers to new backplane designs that are in progress will leverage off of new developments in PWB board materials, connector design, design knowledge, and understanding of channels, will help to enable these speeds. Electrical signaling at a serial line rate at 11+Gps will require the appropriate synergistic performance between the passive components of the channel and the techniques employed in the semiconductor devices that interact with the channel. However, the OIF must also consider the associated cost of these "Greenfield" techniques in determining how much the active and passive components of the system can contribute to the overall resolution of the challenge. The OIF understands that system vendors area facing increasing competitive pressures to minimize cost. Furthermore, the OIF understands the need for developing a specification around a channel that is manufacturable in high volume production.

## Summary

The CEI project defines the electrical characteristics for 4.976 to 6+ Gigabit and 9.95 to 11+ Gigabit signaling for chip-to-chip and board-to-board applications. By defining these characteristics, the OIF is enabling the development of the next generation SFI, SPI, and TFI interfaces. With the CEI project underway, the OIF has begun the Data Transport Protocol Project, which will define the protocol for these next generation interfaces. These two projects will enable higher capacity systems by reducing the overall size and cost of all of the internal electrical interfaces that are used to build them.

This article is the collaborative effort of the following members of the OIF:

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<sup>i</sup> Provided by Ignis Optics