

OIF CEI Overview

The OIF pushes forward on electrical interfaces

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Luxtera

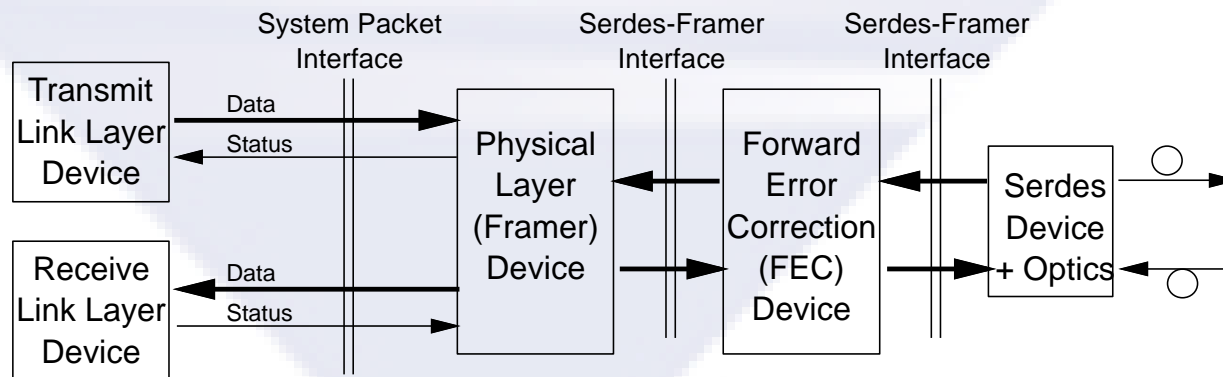
OIF Physical & Link Layer Interop Chair

March 8, 2010



OIF Reference Model

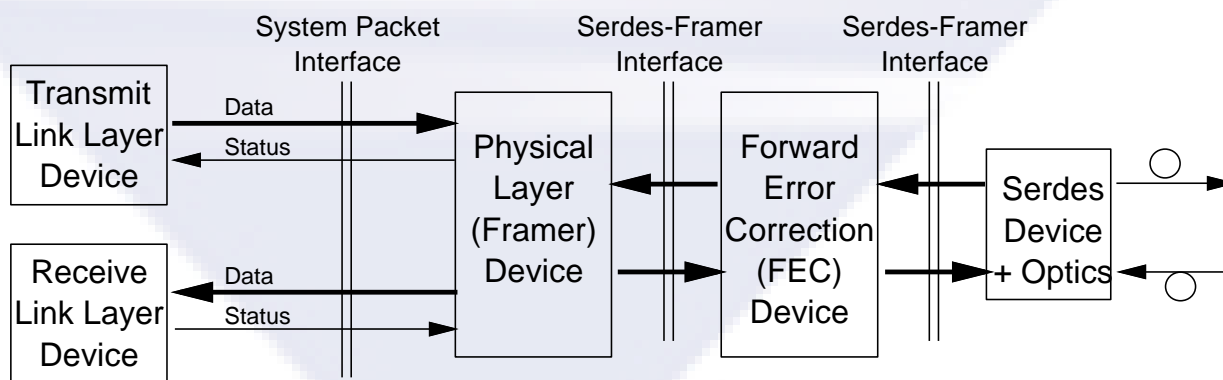
- ◆ The OIF Reference Model forms the basis of most OIF projects over the past 10+ years.
- ◆ The Reference Model recognizes two electrical interface applications:
 - ◆ Serdes-Framer Interfaces
 - ◆ System Packet Interfaces



OIF Reference Model

OIF Reference Model - SFI

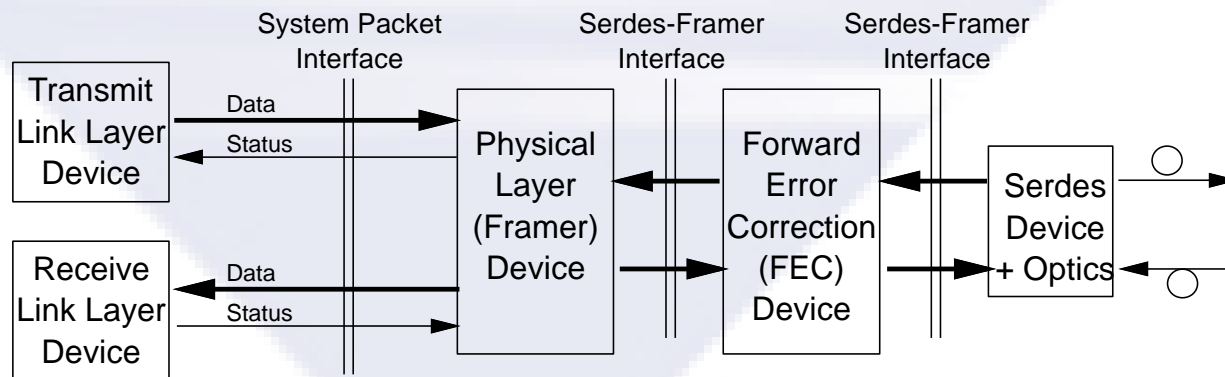
- ◆ Serdes-Framer Interfaces connect Framer devices, FEC devices, and optics devices.
- ◆ Chip-to-chip or chip-to-optics – generally less than 8” and no more than one connector.
- ◆ Retimed in optics module.
- ◆ Optics module may have separate chips for Mux, Demux functions – therefore backchannel cannot be assumed.



OIF Reference Model

OIF Reference Model - SPI

- ◆ **System Packet Interfaces connect Framer devices and Network Processor Elements which process the Link Layer.**
- ◆ **Chip-to-chip or backplane – up to 1 meter in some configurations and up to 2 connectors.**
- ◆ **Tx/Rx data paths may connect to separate NPEs – therefore backchannel cannot be assumed.**



OIF Reference Model

Generalized Application Space

Increasing Insertion Loss on Electrical Channel



Chip-to-Optics, No or Partial Retiming in Optics Module



Chip-to-Optics, Full Retiming in Optics (SFI)



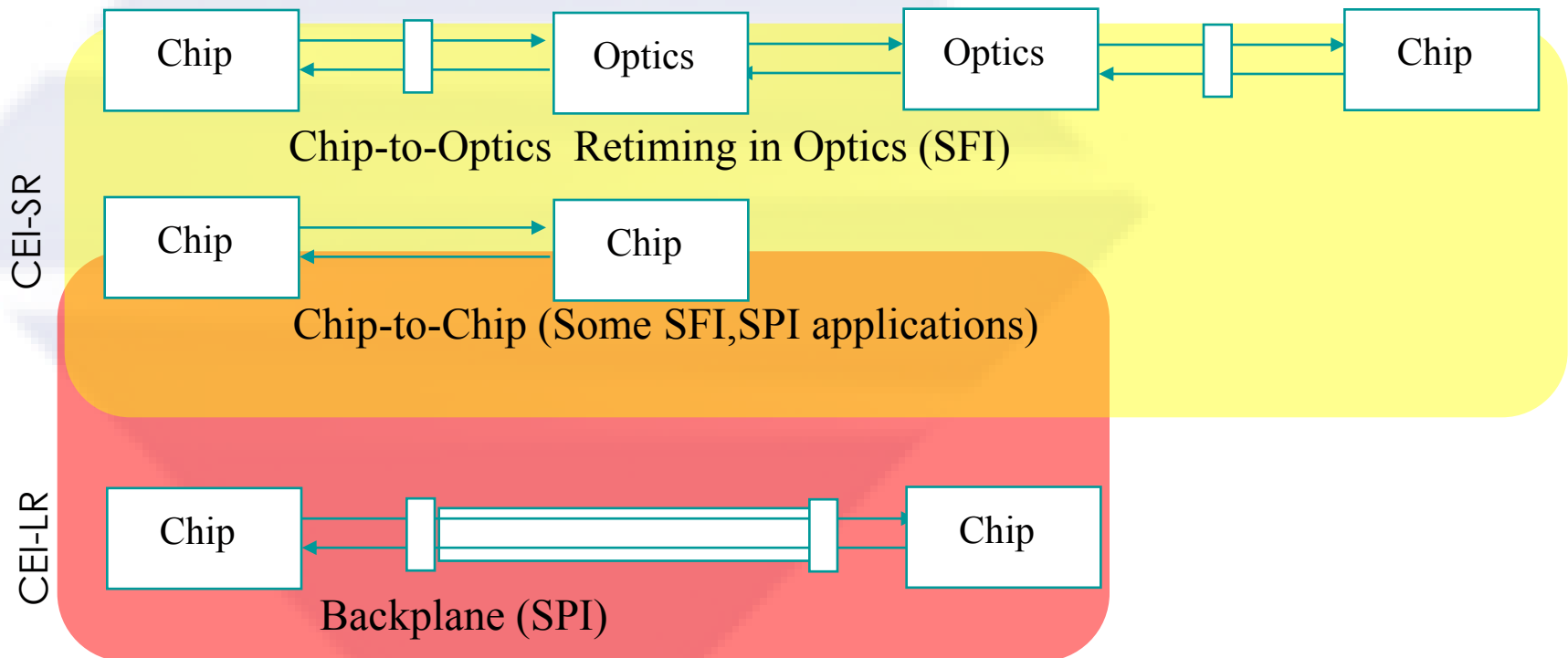
Chip-to-Chip (Some SFI, SPI applications)



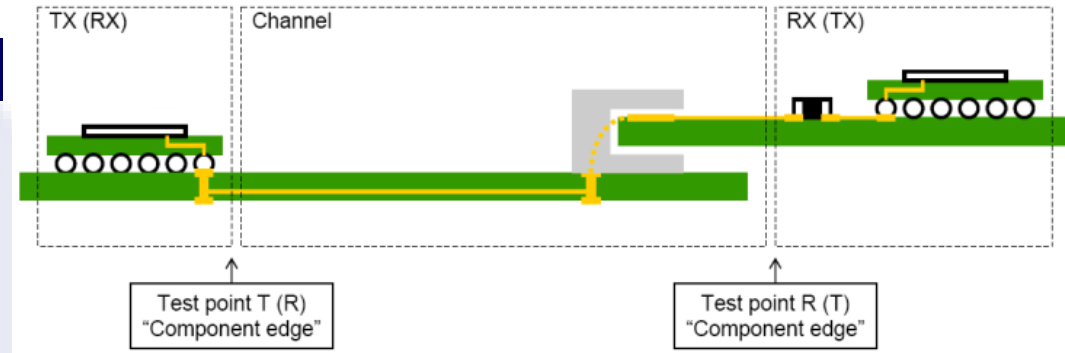
Backplane (SPI)

- ◆ **Application Space** ranges from short low-loss interfaces to high-loss backplane channels.
- ◆ **The higher the loss of the channel, the more signal processing required in the Serdes device.**
- ◆ **More signal processing means more power.**

Legacy CEI Application Space

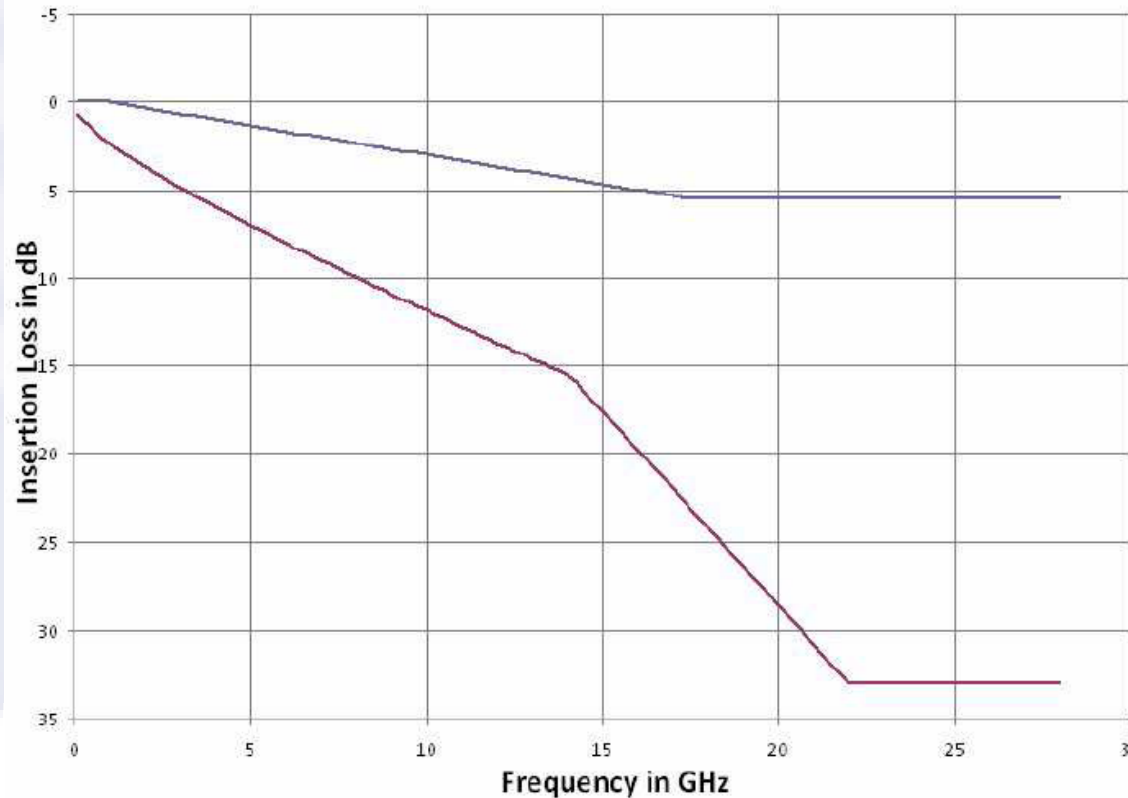


CEI-28G-SR channel



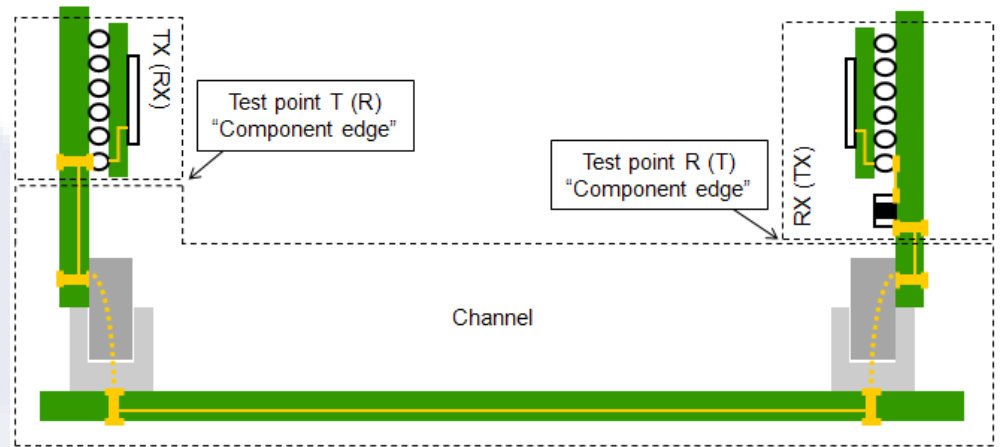
- ◆ Intended to support 4 lanes (100G)
- ◆ Budget allows for 12 inch reach with 1 connector
- ◆ Channel specified with insertion loss of 15.4dB at 14.0 GHz
- ◆ Specifies insertion loss deviation and crosstalk

CEI-28G-SR 300mm Channel Loss Definition



CEI-25G LR channel

- ◆ Intended to support 4 lanes (100G)
- ◆ Budget allows for 27 inch reach with 2 connectors
- ◆ Channel specified with insertion loss of 25.5dB at 12.9GHz
- ◆ Specifies insertion loss deviation and crosstalk



CEI-28G Adds VSR application Space

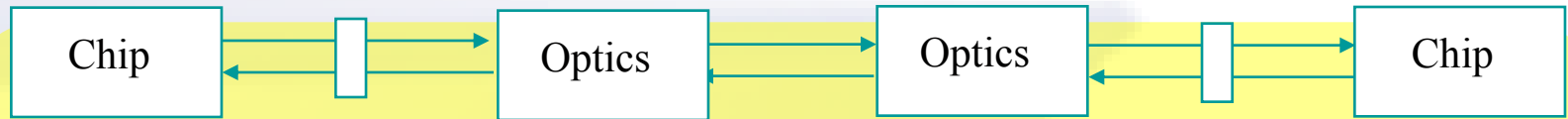
CEI-28G-VSR



Chip-to-Optics, Retiming in Optics Module (SFI)

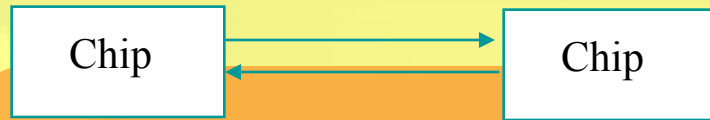
- ◆ VSR was started in response to industry feedback at the OIF CEI Workshop in Cupertino
- ◆ Focus is on low power

CEI-SR



Chip-to-Optics Retiming in Optics (SFI)

CEI-LR



Chip-to-Chip (Some SFI,SPI applications)



Backplane (SPI)

CEI-28G-VSR Scope & Objectives

- ◆ Address low cost chip-to-optics applications.
- ◆ Define data lane(s) to support bit rates up to 28 Gbps.
 - ◆ **Must achieve BER = 1E-15 or better.**
- ◆ Define channel model based on a chip-to-module application.
 - ◆ **Channel must be at least 3 dB better than SR to differentiate the solution.**
 - ◆ **Document constraints used to derive channel model specifications.**
- ◆ Define a compliance test methodology for a chip-to-module interface including a single connector.
 - ◆ **The compliance test methodology includes compliance test boards.**



OIF

OPTICAL
INTERNETWORKING
FORUM

CEI Project Status

◆ CEI-25-LR and CEI-28G-SR:

- ◆ Several Straw Ballots have been conducted.
- ◆ Relevant discussion needs to occur as to loss budget for CEI-28G-SR.

◆ CEI-28G-VSR

- ◆ Project started at Feb. 2010 meeting.
- ◆ Progressing along an 18 month project timeline

CEI Workshops

- ◆ **Present Needs of the Industry:**
 - ◆ **Presentations representing various application spaces.**
- ◆ **State of Technology:**
 - ◆ **Experts from various disciplines present on the available technologies and trade-offs.**
- ◆ **Discussion:**
 - ◆ **Where is the common ground between various standards?**
 - ◆ **What are the appropriate boundaries for the application space?**