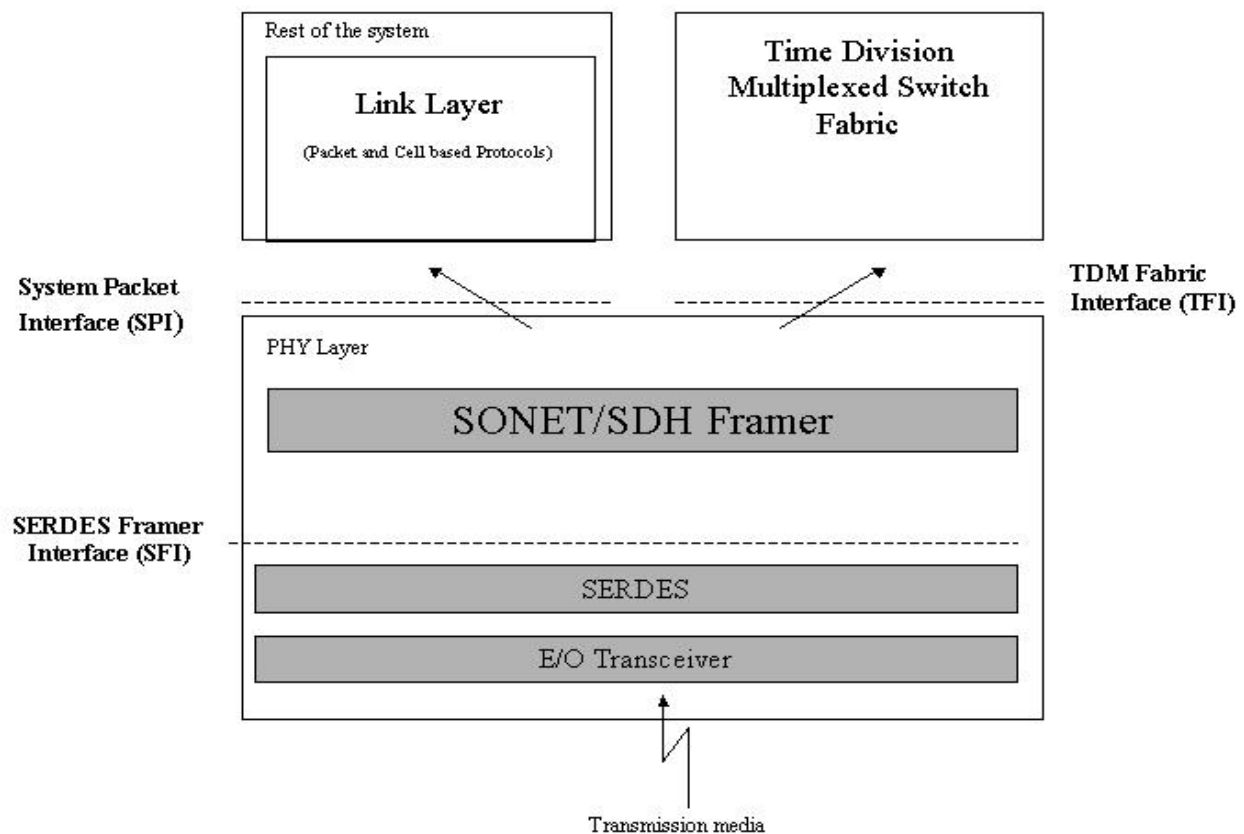


OIF OC-48, OC-192 & OC-768 Electrical Interfaces

The mission of the Optical Internetworking Forum (OIF) is to foster the development and deployment of interoperable data switching and routing products and services that use optical networking technologies.

To promote multi-vendor interoperability at the chip-to-chip and module-to-module level, the Physical and Link Layer (PLL) Working Group within the OIF has defined electrical interfaces at two different points within a Synchronous Optical NETWORK/ Synchronous Digital Hierarchy (SONET/SDH) based communication system.

These interfaces, the System Packet Interface (SPI) and the SERDES Framer Interface (SFI), are depicted in the following reference model:



The System Packet Interface (SPI) is between the Physical Layer (PHY) device(s) and the rest of the SONET/SDH System (i.e. between the SONET/SDH Framer and the Link Layer). This interface separates the synchronous PHY layer from the asynchronous packet-based processing performed by the higher layers. As such, the SPI supports

transmit and receive data transfers at clock rates independent of the actual line bit rate. It is designed for the efficient transfer of both variable-sized packet and fixed-sized cell data.

The SERDES Framer Interface (SFI) defines an electrical interface between a SONET/SDH Framer and the high speed Parallel-to-Serial/ Serial-to-Parallel (SERDES) logic. This permits the SERDES and Framer to be implemented in different speed technologies, allowing a cost-effective multiple chip solution for the SONET/SDH PHY.

The TDM Fabric Interface (TFI) defines the backplane interface between a SONET based Time division Multiplexed (TDM) framer and switch fabric. Traffic between the framer and the fabric is modeled after a SONET/SDH frame, and operates at the STS-48/STM-16 equivalent bit rate.

To keep up with evolving transmission speeds and technology enhancements, the OIF has defined several different versions of these electrical interfaces. Each version is tailored for a specific application environment and timeframe. The OIF has adopted the following naming convention to identify the various PLL interfaces and the application environment they are designed for:

SPI-3	OC-48/STM-16 and below	(2.48832 Gbps range)
SPI-4/SFI-4	OC-192/STM-64	(10 Gbps range)
SPI-5/SFI-5	OC-768/STM-256	(40 Gbps range)
TFI-5	OC-48/STM-16 to OC-768/STM-256 (2.5 –40 Gbps range)	
SxI/CEI	Common Electrical Interfaces	

OC = Optical Carrier (SONET terminology)

STM = Synchronous Transport Module (SDH terminology)

Implementation Agreements

The OIF has published 7 electrical interface Implementation Agreements for the OC-48 through OC-192 environments.

By the time the OIF was formed, the OC-48 market was well established, so only an SPI-3 interface was deemed necessary. For the OC-192/SDH-64 market, two different SPI-4 interfaces were defined, as well as two SFI-4 interfaces. The SPI-4.2 and SFI-4.2 interfaces use less pins and operate at higher frequencies in order to take advantage of advances in semiconductor technologies.

Work on the SPI-5 and SFI-5 Interfaces for the OC-768 (40 to 50 Gbps) environment has also been completed. These interfaces utilize a clockless data path that eliminates the difficult clock to data timing requirements.

Work on the TFI-5 Interface is completed pending the balloting process. This interface supports OC-48, OC-192 and OC-768. TFI is intended to be used over a backplane interconnect.

Interface Overviews

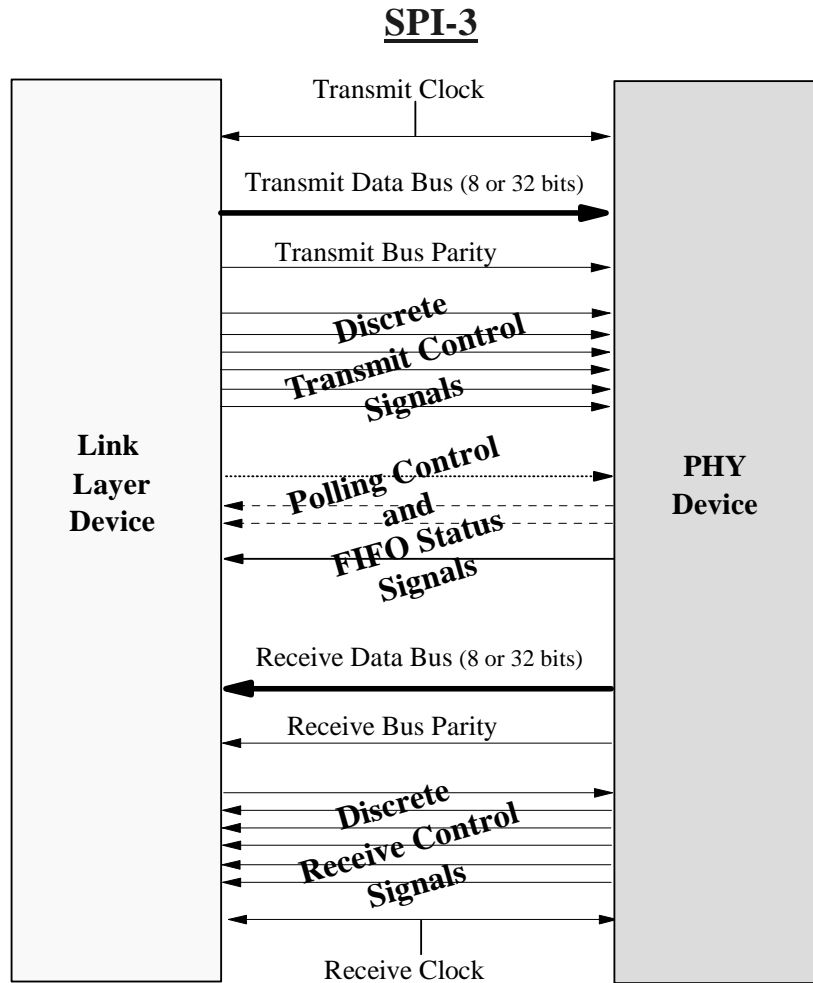
The following are brief overviews of each of the published OIF Electrical Interfaces. Each specification defines:

- the physical implementation of the bus
- the signaling protocol used to communicate data
- the data structures used to transmit data over the interface.

Each interface is graphically shown, and key attributes are described.

SPI-3 OC-48 Interface

SPI-3 was the first electrical interface defined by the OIF. It was designed to support Packet over SONET/SDH (POS) in the OC-48 (2.488 Gbps) and below environment. It defines an interface for efficient packet transfer between a physical layer (PHY) device and a link layer device. Since the SPI-3 supports data transfers at clock rates independent of the actual line bit rate, FIFOs are specified to allow the rate decoupling. Each physical layer device is required to support a minimum FIFO size of 256-bytes.



SPI-3 Interface Attributes

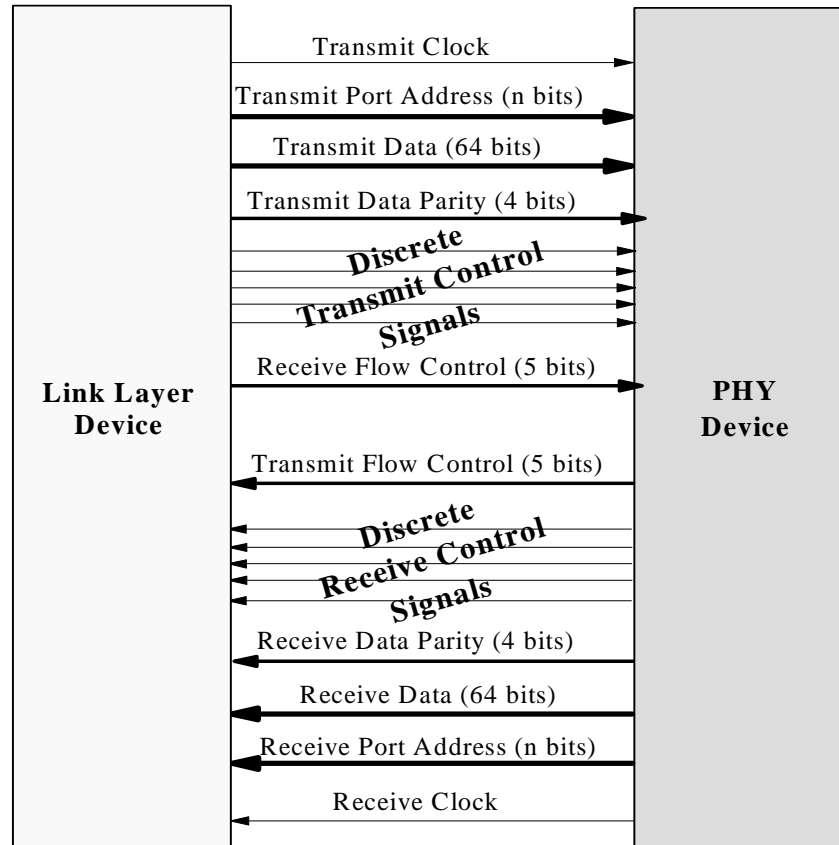
- Point-to-point connection (i.e., between single PHY and single Link Layer device)
- Variable length packets
- Defines both byte-level and packet-level transfer modes
- Transmit / Receive Data Path:
 - 8 or 32 bits wide
 - Parity on the Data bus
 - Maximum clock rate of 104 MHz
- In-band PHY port selection
 - PHY port address is inserted in-band with the packet data being transferred on the data bus
 - 256 ports supported (8-bit address)
- Discrete transmit/receive control signals for Start of Packet (SOP), End of Packet (EOP), Start of Transfer, Error indications, etc.
- Transmit FIFO Status
 - Transmit Flow Control provided using either a polling or a direct status indication scheme
 - Discrete address polling control and FIFO status signals used
- FIFO buffer 256-bytes deep

SPI-4 Phase 1 OC-192 Interface

The SPI-4 Phase 1 interface is a packet and cell transfer interface that supports transfers at a nominal rate of 10 Gbps (OC-192-based) and a maximum rate of 12.8 Gbps. Transfers may be between Physical and Link layer devices, or between peer entities.

SPI-4 Phase 1 is a wide and relatively low rate interface. This approach in phase 1 of the SPI-4 interfaces minimized the risk and improved the time to market of early OC-192 products.

SPI-4 Phase 1



Unlike SPI-3, flow control information is passed back to the sending device on a continuous basis. The flow control information specifies whether the receiving device is full or not.

SPI-4 Phase 1 Interface Attributes

- Point-to-point connection (i.e., between single PHY and single Link Layer device)
- Variable-length packets and fixed-sized cells
- Transmit / Receive Data Path:
 - 64 bits wide
 - Optional 16 bit wide data path
 - Source-synchronous clocking at 200 MHz
 - Parity on the Data bus
 - Single-ended HSTL Class 1 I/O (JEDEC JESD8-6)
- Out-of-band port address
- Discrete address bus
- Maximum number of port address bits is not specified

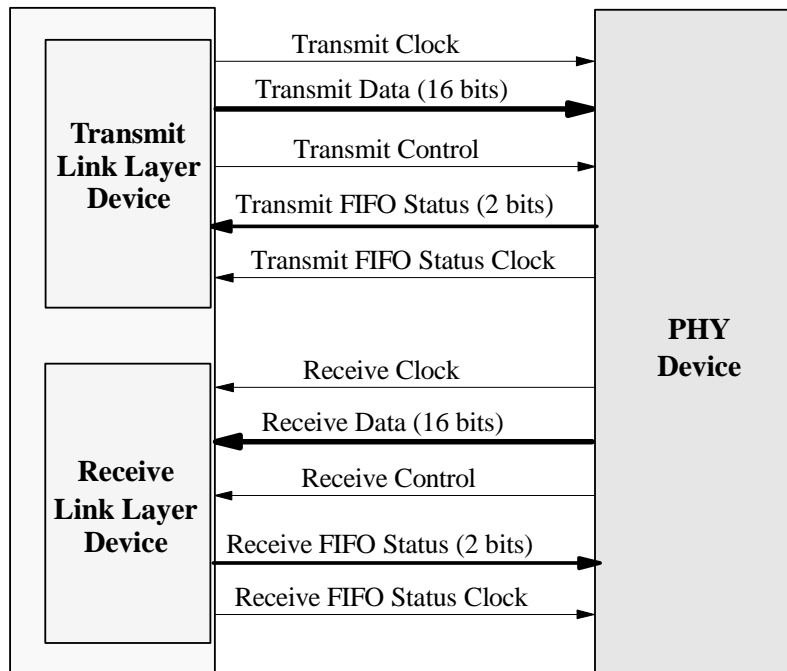
- Discrete transmit/receive control signals for Start of Packet (SOP), End of Packet (EOP), Error indications, etc.
- Transmit/Receive FIFO Status interface:
 - 4-bit parallel FIFO status bus
 - Out-of-band Start-of-FIFO-Status signal
 - Flow control information is passed back to the sending device on a continuous basis. The flow control information specifies whether the receiving device FIFO is full or not.
 - No polling
 - Transmit status bus synchronized with Receive Clock, Receive status bus synchronized with Receive Clock
 - Same clock rate as the data bus

SPI-4 Phase 2 OC-192 Interface

SPI-4 is an interface for packet and cell transfer between a Physical Layer (PHY) device and a Link Layer device. It runs at a minimum of 10 Gbps and supports the aggregate bandwidths required of ATM and Packet over SONET/SDH (POS) applications.

SPI-4 specifies a higher-speed and narrower interface than defined in SPI-4 Phase 1 and its transmit and receive interfaces are completely separate and independent. This allows more flexibility in the design of higher layer devices. SPI-4 is well positioned as a versatile general-purpose interface for exchanging packets any where with in a communications system.

SPI-4 Phase 2



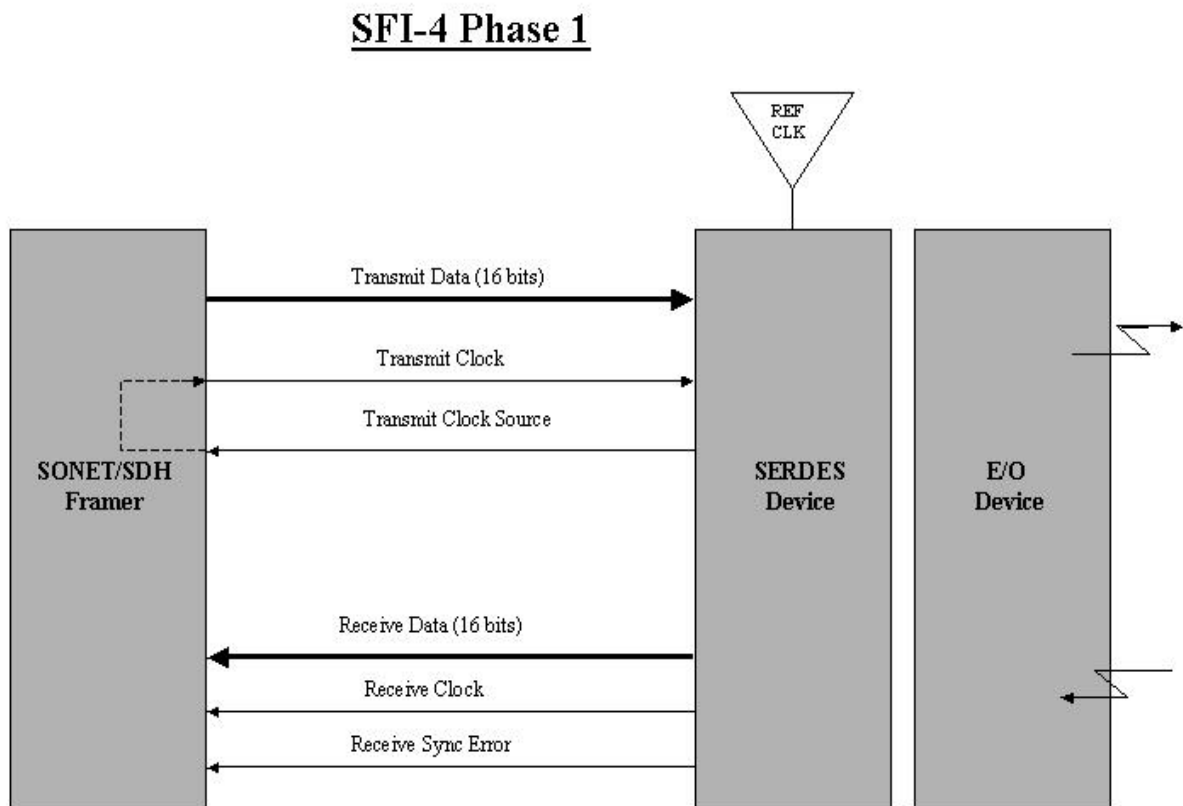
SPI-4 Phase 2 Interface Attributes

- Point-to-point connection (i.e., between single PHY and single Link Layer device)
- Variable-length packets and fixed-sized cells
- Transmit / Receive Data Path:
 - 16 bits wide
 - Source-synchronous double-edge clocking with a 311 MHz minimum
 - 622 Mbps minimum data rate per line
 - LVDS I/O (IEEE 1596.3 – 1996, ANSI/TIA/EIA-644-1995)
 - Control word extension supported
- In-band PHY port addressing
- Support for 256 ports (suitable for STS-1 granularity in SONET/SDH applications (192 ports) and Fast Ethernet granularity in Ethernet applications (100 ports))
- Extended addressing supported for highly channelized applications
- In-band start/end-of-packet indication, error-control code
- Transmit/Receive FIFO Status interface:
 - 2-bit parallel FIFO status bus
 - In-band Start-of-FIFO-Status signal
 - Source-synchronous clocking

- Flow control information is passed back to the sending device on a continuous basis. The flow control information specifies whether the receiving device FIFO is full or not.
- No polling
- Uses either CMOS LVTTTL I/O (3.3V) or LVDS I/O (IEEE 1596.3 – 1996, ANSI/TIA/EIA-644-1995)
- Run at a maximum of ¼ data path clock rate for LVTTTL I/O or at full data path clock rate for LVDS I/O
- Segmentation of data is in multiples of 16 bytes with the exception of transfers that terminate with an End-of-Packet indication.

SFI-4 Phase 1 OC-192 Interface

The SFI-4 phase 1 interface supports transmit and receive data transfers at clock rates locked to the actual line bit rate. It is optimized for the pure transfer of data. There is no protocol or framing overhead. Information passed over the interface is serialized by the SERDES and transmitted on the external link.



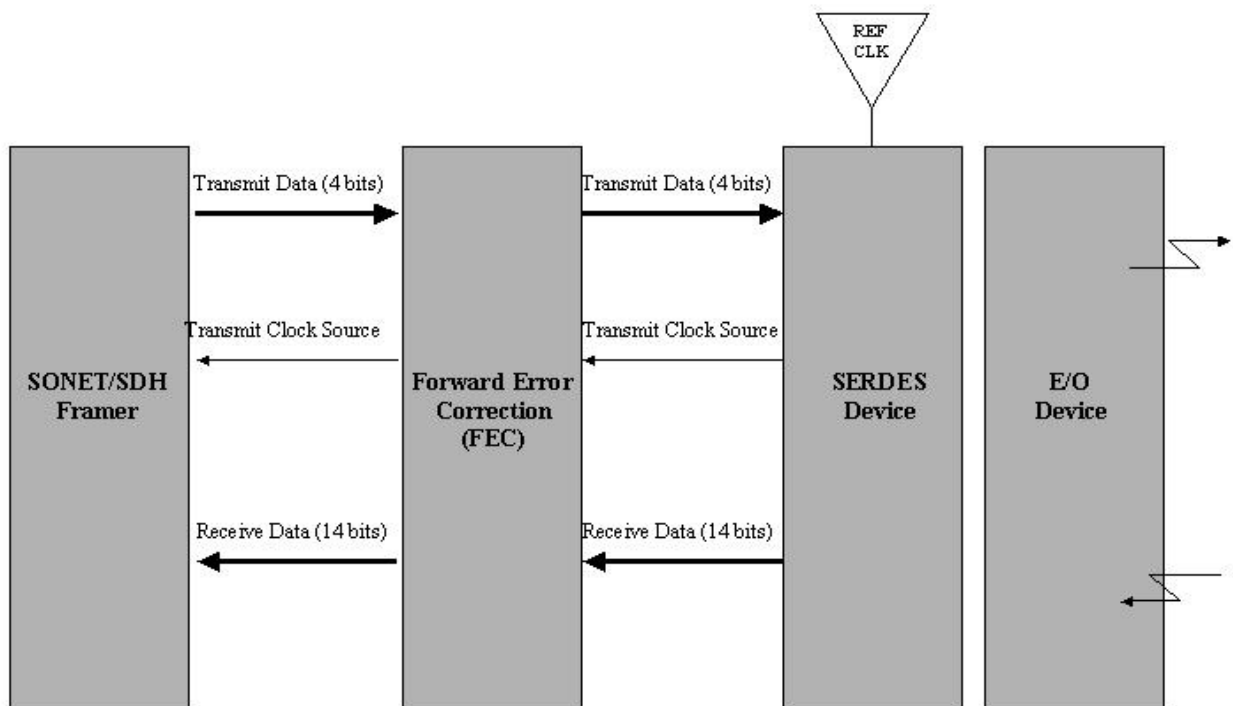
SFI-4 Phase 1 Interface Attributes

- Point-to-point connection (i.e., between single Framer and single SERDES device)
- Transmit / Receive Data Path:
 - 16 bits wide
 - Source-synchronous clocking at 622.08 MHz (311.04 MHz with Double Data Rate sample optional)
 - 622 Mbps minimum data rate per line
 - An aggregate of 9953.28 Mbps is transferred in each direction
 - Timing specifications allow operation up to 10.66 Gbps
 - LVDS I/O (IEEE Std 1596.3-1996)
- The 622.08 MHz Framer Transmit Clock sourced from the SERDES
- Uses a 622.08 MHz LV-PECL reference clock input
- A low-speed (LVTTTL) Receive Loss of Synchronization Error is signaled when the Receive Clock and Receive Data are not derived from the received optical signal

SFI-4 phase 2 OC-192 Interface

The SFI-4 phase 2 interface supports a narrower 4 bit transmit and receive data path. In addition to the Framer to SERDES interface, SFI-4.2 can be used to transmit higher rate Forward error correction transfers between the FEC and SERDES. The interface uses 64B66B coding to perform byte and lane alignment functions and encode the clock. The interface is protocol agnostic, supporting 10G Ethernet, 10G Fibre Channel, OC-192/STM-64, G.709, proprietary FEC coding and other proprietary data streams.

SFI-4 Phase 2



SFI-4 Phase 2 Interface Attributes

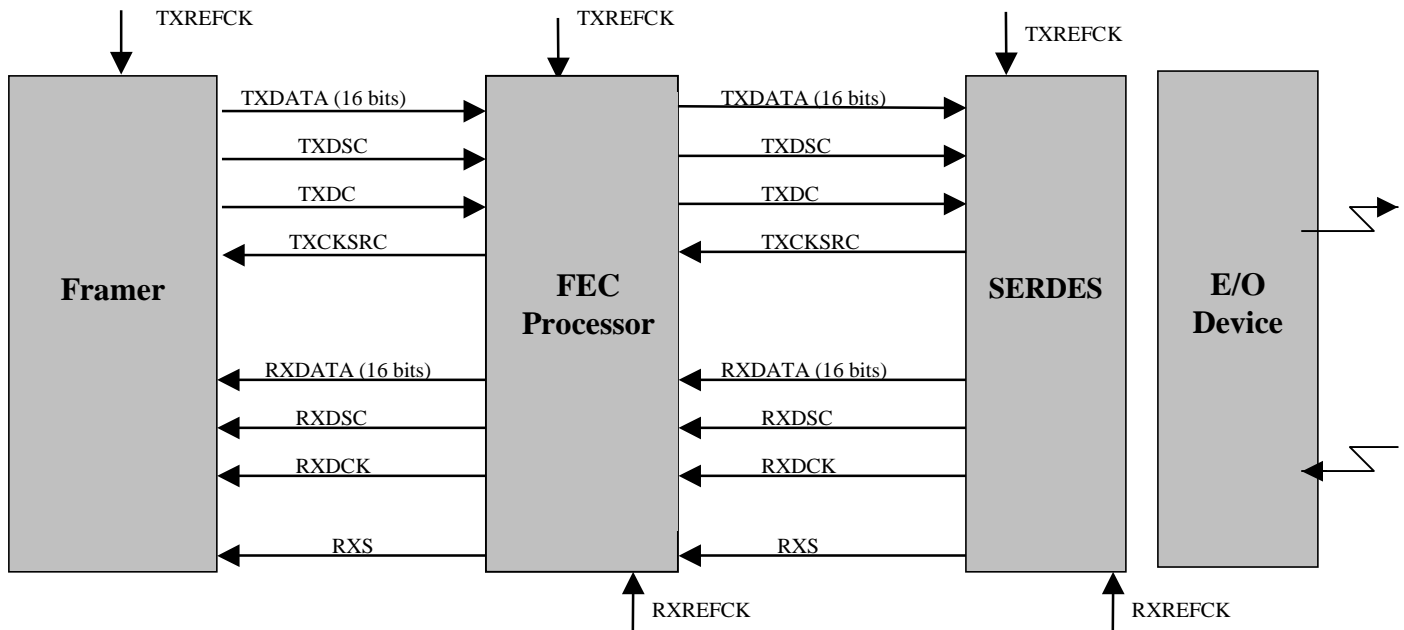
- Point-to-point connection (i.e., between single Framer to FEC, Framer to SERDES or FEC to SERDES device)
- Transmit / Receive Data Path:
 - 4 bits wide
 - Clockless interface (clock is embedded in the data path)
 - 2.488 Gbps minimum data rate per line
 - An aggregate of 9953.28 Mbps is transferred in each direction
 - Timing specifications allow operation up to 12.5 Gbps
 - CML I/O (electrical and jitter specifications per SxI-5 common electrical specification)
- A 622.08 MHz Framer Transmit Clock is sourced from the SERDES
- A low-speed (LVTTL) Receive Loss of Synchronization Error is signaled when the Receive Clock and Receive Data are not derived from the received optical signal

SFI-5 OC-768 Interface

The SFI-5 interface supports a 16 bit transmit and receive data path. In addition to the Framer to SERDES interface, SFI-5 can be used to transmit higher rate Forward error

correction transfers between the FEC and SERDES. The interface assumes scrambled data maintain DC balance. Clock and lane deskew are accomplished using additional signals. The interface supports OC-768/STM-256 and FEC coded OC-768 data.

SFI-5



SFI-5 Interface Attributes

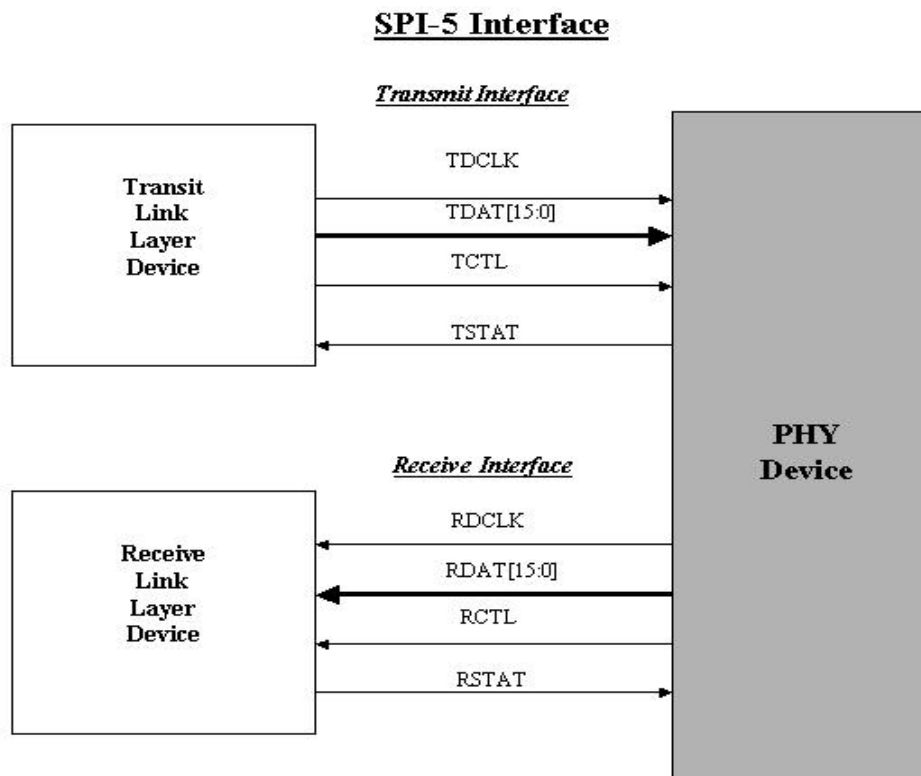
- Point-to-point connection (i.e., between single Framer to FEC, Framer to SERDES or FEC to SERDES device)
- Transmit / Receive Data Path:
 - 16 bits wide
 - 622 MHz clock
 - 2.488 Gbps minimum data rate per line
 - An aggregate of 39.8 Gbps is transferred in each direction
 - Timing specifications allow operation up to 50 Gbps
- CML I/O (Electrical and jitter characteristics per SxI-5 common electrical specification)
- A 622.08 MHz Framer Transmit Clock is sourced from the SERDES
- A deskew channel included in both RX and TX directions is used to deskew the 16 lane data path.

- A low-speed (LVCMOS) Receive Loss of Synchronization Error is signaled when the Receive Clock and Receive Data are not derived from the received optical signal

SPI-5 OC-768 Interface

SPI-5 is an interface for packet and cell transfer between a Physical Layer (PHY) device and a Link Layer device. It runs at a minimum of 40 Gbps and supports the aggregate bandwidths required of ATM and Packet over SONET/SDH (POS) applications.

SPI-5 specifies a 16-lane interface with transmit and receive interfaces completely separate and independent. Each direction of the SPI-5 bus has its own Pool Status Channel that is sent separately from the corresponding data path. This makes it possible to decouple the Transmit and Receive interfaces making SPI-5 suitable for both bi-directional and unidirectional link layer devices.



SPI-5 Interface Attributes

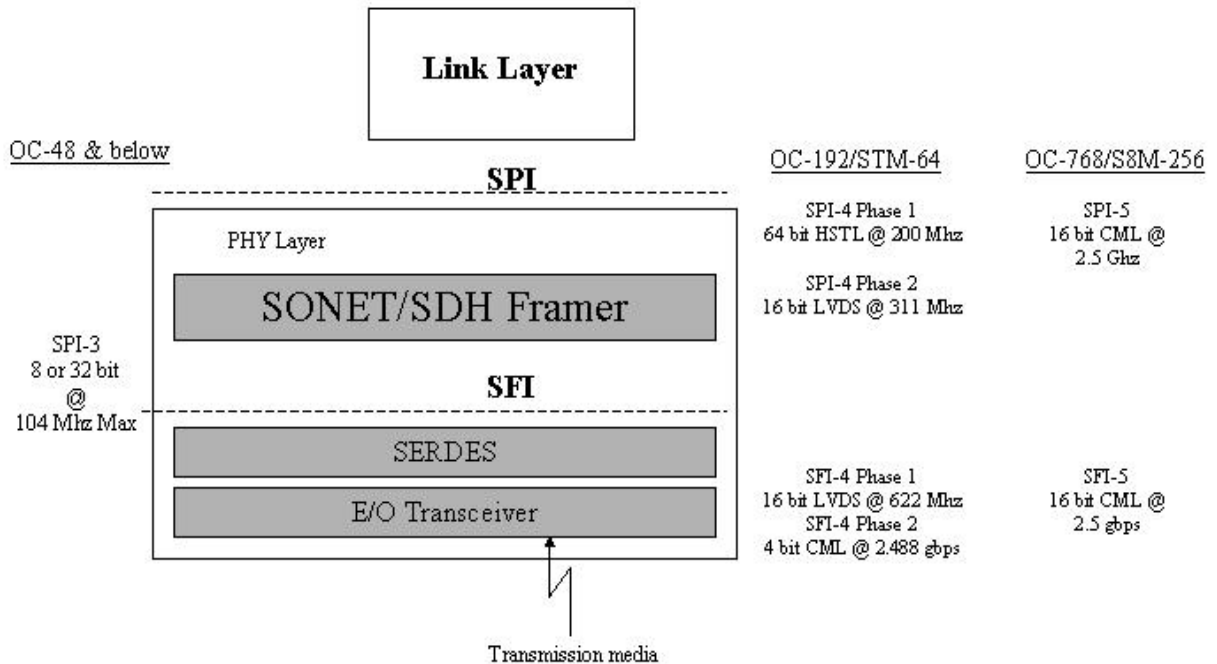
- Point-to-point connection (i.e., between single PHY and single Link Layer device)
- Variable-length packets and fixed-sized cells
- Transmit / Receive Data Path:
 - 16 bits wide
 - Source-synchronous clock at one quarter the data rate

- 3.125 Gbps maximum, 2.488 min. data rate per line
- CML I/O per the SxI-5 common electrical specification
- In-band PHY port addressing
- Support for 256 ports
- Extended addressing (up to 2^{144} ports) supported for highly channelized applications
- Control words carry In-band port address, start/end-of-packet indication and error-control code
- Transmit/Receive Pool Status channel:
 - Operates at the same clock rate as the data path
 - Bit Pool status indication
 - In-band Pool Status framing
 - Electrical, training and scrambling functions common with data path
 - In-band training
- Segmentation of data is in multiples of 16 words (32 bytes) for nominal burst transfer. EOP packets can be shorter (allowing data burst lengths to be sized appropriate to the application).

Summary

The OIF has published 7 Implementation Agreements for the SPI and SFI interfaces depicted in the following figure. (TFI will be published shortly)

OIF Interface



For more information, the following OIF Implementation Agreements can be downloaded from the OIF Web site at www.oiforum.com

SPI-3 (OC-48 System Packet Interface)

OIF-SPI3-01.0 - SPI-3 Packet Interface for Physical and Link Layers for OC-48

SFI-4 Phase 1 (OC-192 SERDES-Framer Interface)

OIF-SFI4-01.0 – A Common Electrical Interface Between SONET Framers and Serializer/Deserializer Parts for OC-192 interfaces

SFI-4 Phase 2 (OC-192 SERDES-Framer Interface)

OIF-SFI4-02.0 – A Common Electrical Interface Between SONET Framers and Serializer/Deserializer Parts for OC-192 interfaces

SPI-4 Phase 1 (OC-192 System Packet Interface)

OIF-SPI4-01.0 - System Physical Interface Level 4 (SPI-4) Phase 1: A System Interface or Interconnection Between Physical and Link Layer, or Peer-to-Peer Entities Operating at an OC-192 Rate (10 Gbps)

SPI-4 Phase 2 (OC-192 System Packet Interface)

OIF-SPI4-02.0 - System Packet Interface Level 4 (SPI-4) Phase 2: OC-192 System Interface for Physical and Link Layer Devices

SPI-5 (OC-768 System Packet Interface)

OIF-SPI5-01.0 - System Physical Interface Level 5 (SPI-5) Phase 1: A System Interface or Interconnection Between Physical and Link Layer, or Peer-to-Peer Entities Operating at an OC-768 Rate (40 Gbps)

SFI-5 (OC-768 SERDES-Framer Interface)

OIF-SFI5-01.0 – A Common Electrical Interface Between SONET Framers and Serializer/Deserializer Parts for OC-768 interfaces

TFI-5 (OC-48/192/768 TDM-Fabric Interface)

Publication pending completion of balloting process

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