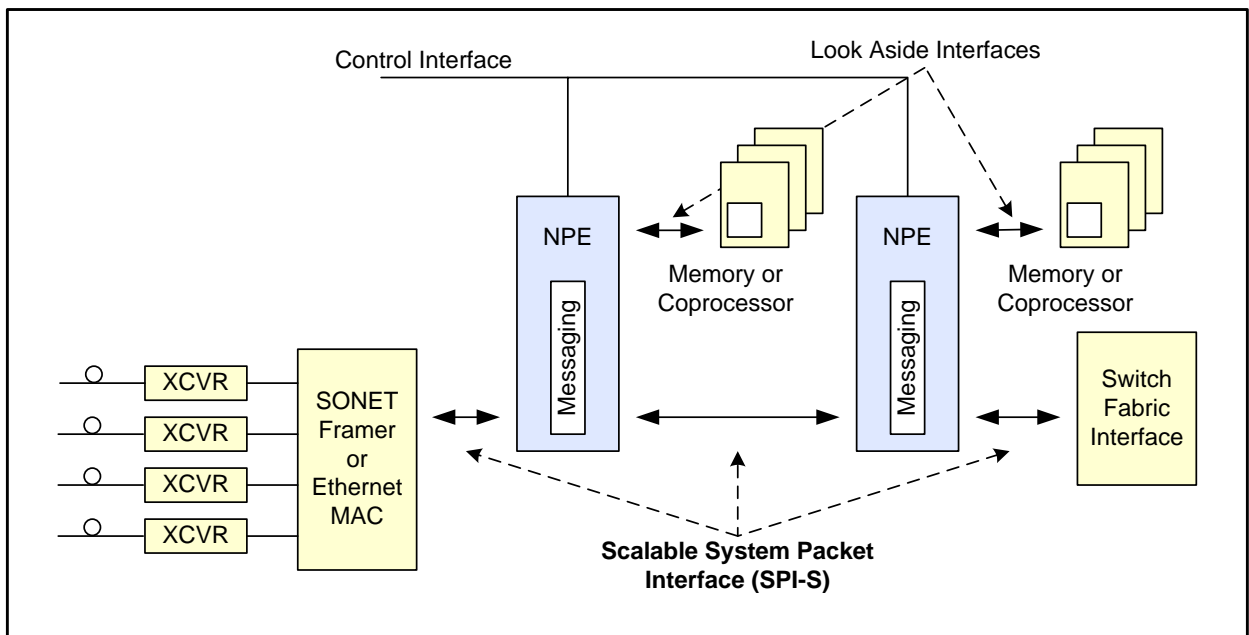


## OIF Introduces System Packet Interface - Scalable (SPI-S)

*By Christopher Ebeling and Harmeet Bhugra, OIF members*

As the overall bandwidth throughput increases, selecting the right chip-to-chip interface becomes critical for systems (such as switches, routers, etc.). So far, Optical Internetworking Forum's (OIF) System Packet Interface (SPI) 4.2 is the most widely deployed chip-to-chip interconnect for high-speed data paths. The System Packet Interface - Scalable (SPI-S) is the next-generation interface developed by the OIF to take advantage of serialization of physical interconnects.



**Figure 1: System Block Diagram showing SPI-S**

The SPI-S effort was jointly started by the Network Processor Forum (NPF) and OIF in summer 2004. Since then, NPF and OIF have merged and the OIF Physical Link Layer (PLL) group took over the development of the SPI-S interface. The OIF is an industry group comprising of over 100 system vendors, carriers and silicon vendors. The OIF recently approved the SPI-S implementation agreement for publishing after almost two years of development.

Early on the members of the NPF and OIF recognized that the number of pins on application-specific standard products and network processors was experiencing rapid

growth. The wider parallel interfaces were causing problems on the board (i.e. routing and lane to lane skew). Traditional high-speed interconnects used to transfer chip-to-chip data have transitioned to serial interconnects. As a result, the OIF and NPF partnered to define a SPI-like interface, providing a significant performance boost with considerable technology reuse based on an industry standard Serial I/O Block. After taking an exhaustive look at the physical I/O available at that time, the group decided to base the interface on OIF's CEI (Common Electrical Interface) physical I/Os. This resulted in a significant reduction in pin-count. For example, pin count for a 10G interface configuration could be reduced from 80 pins for SPI 4.2 to eight pins using CEI 6.25G, and four pins using CEI 11G links. Refer figure 2 for a comparison.

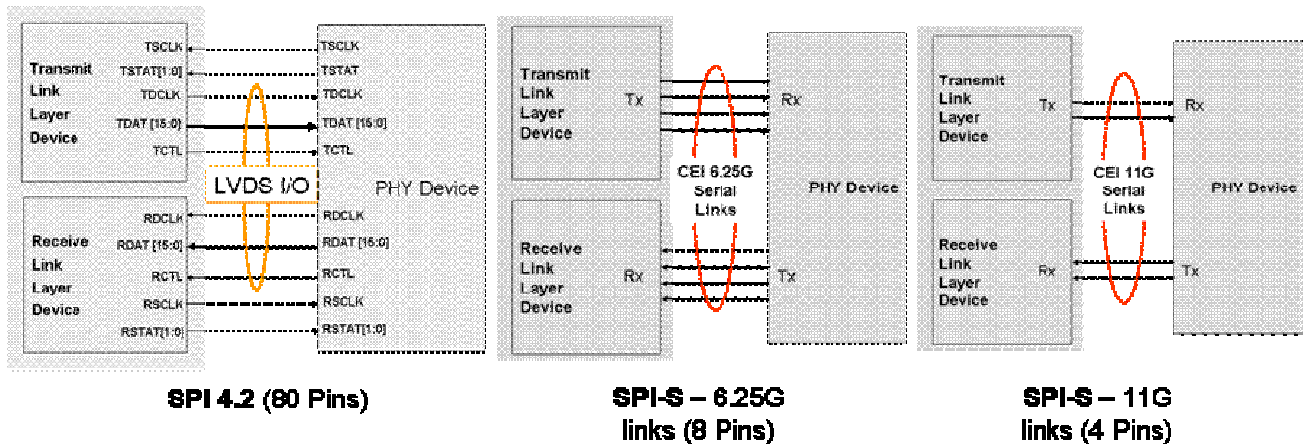


Figure 2: Pin comparison for 10 Gbps link

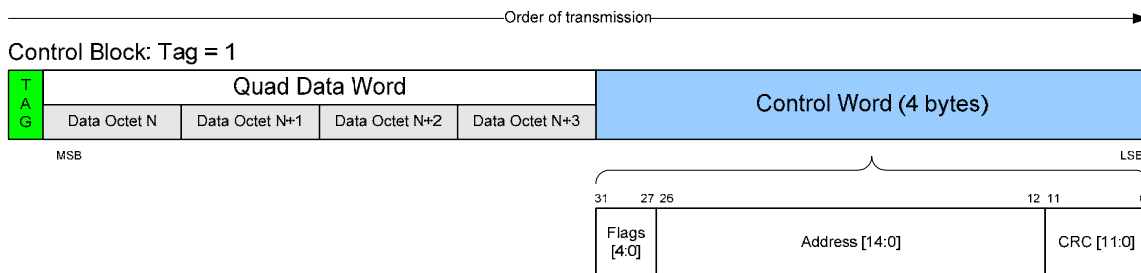
The objective for SPI-S was to define an evolutionary, high speed, scalable SPI that could efficiently transfer common packet formats, such as Ethernet packets ( $\geq 64$  bytes), ATM cells (48 or 52 bytes), IP packets ( $\geq 40$  bytes) and Control packets (6 to 10 bytes for NPF Messaging).

## SPI-S (Highlights/Features)

SPI-S leverages many of the features of the existing SPI standards. In addition to moving to high-speed serial interface(s), the specification is designed to be scalable (SPI-Scalable) in both the signaling frequency and the number of physical links. As system requirements evolve the physical interface can be modified to meet the new demands either by increasing the number of physical lanes used or increasing the signaling frequency (or both). SPI-S can support up to 127 lanes. Obviously, both ends of a particular SPI-S implementation will have to use the same number of links and support operation at a common link signaling rate. The scalable nature of the protocol ensures that future bandwidth requirements can be supported without needing to modify or abandon the SPI-S standard.

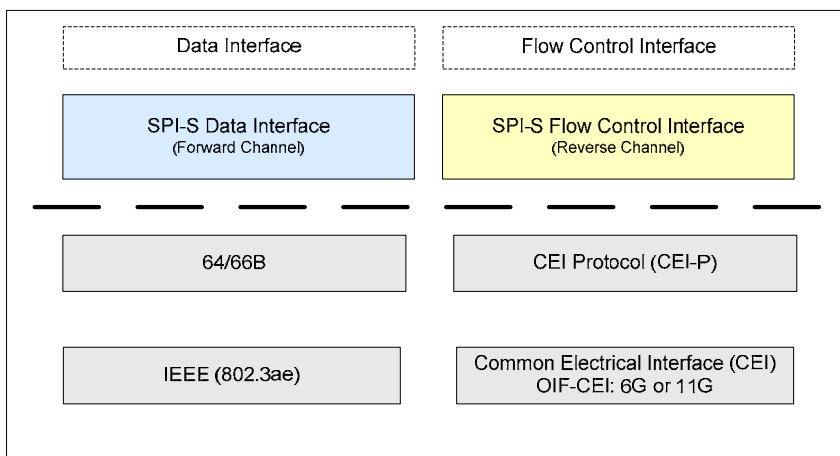
SPI-S utilizes eight byte blocks as the base granularity for data transfer. There are two block types: a Data Block and a Control Block. Block type is determined by the Block's tag bits, which is either the two sync bits for links using 64/66B encoding or a single bit if CEI is used as the transport mechanism. A Data Block contains only data with the data

context determined by the current link state. Conversely, as shown in figure 3, a Control Block is composed of a 32-bit (4 byte) data field and a 32-bit control field (Control Word). The ability of Control Blocks to also carry data limits the bandwidth overhead of control signaling. The control field performs the same functions as prior versions of the SPI specification, packet delineation (start and end of packet, as well pause) and context switching for the link. SPI-S has a 15-bit address field, so 32K is the maximum number of channels. The specification also allows the use of some address bits to support service classes. Important applications that SPI-S can support are 4K VLANs with eight Classes of Service, as well as STS-1 and Fast Ethernet granularity at all rates of interest. The twelve bit CRC (Cyclic Redundancy Check) field within the Control Word provides burst error detection covering all the preceding data and the Control Word itself.



**Figure 3: Control Block Bit Ordering**

The SPI-S specification supports the same per-channel, flow-control mechanism present in SPI-4.2 with starving, hungry and satisfied states. This information is carried in band on the reverse channel link (if present). Flow-control signaling is transferred as data, which allows many channels to be updated with low-bandwidth overhead. The flow-control signaling is initiated with a Control Word that provides a pointer to the first accessed channel. Consequently, the concept of a calendar for flow-control signaling is no longer required.



**Figure 4: SPI-S Reference Model**

Additional higher-level (and precedence), flow-control mechanisms have been introduced that can either augment the per-channel flow control or in some cases make them superfluous. Control Words in a reverse channel can use Payload Data Ready signaling to throttle all data transfers on a link with very low latency either at burst boundaries or immediately via SUSPEND Control Words. The SUSPEND mechanism allows an active data transfer to be paused on non-burst boundaries provided no new data transfers are initiated prior to resumption and completion of the suspended data transfer. A token bucket mechanism has also been defined that allows a transmit link to be self-throttling. This feature is particularly useful in supporting uni-directional (no reverse channel) links.

Transfer of non-payload signaling information is formally supported within the specification using [NPF messaging](#). Including this in the SPI-S specification will prevent potential inter-operability issues arising from ad-hoc methods supported through loosely defined mechanisms.

SPI-S can tolerate large-burst errors on its interface without locking up as the other SPI interfaces do through the use of “soft-state” algorithms. Additionally, SPI-S will restore without requiring a reset after a total disruption of its interface due to an event, such as a failover of one of the cards communicating by way of the interface. In both the burst-error and failover cases, packets will be lost, but SPI-S will restore on its own without requiring a reset or user intervention.

## Summary

SPI-S delivers a channelized, streaming-packet interface scaleable to hundreds of Gb/s for chip-to-chip and backplane applications. It is the next generation of the highly successful SPI series of interfaces from the OIF which utilizes OIF CEI interconnects with either 64B66B or CEI-P framing. By leveraging existing FPGA and ASIC SERDES technology SPI-S will not require new development for its physical interface. We expect SPI-S to be widely adopted in the industry. This is due to the broad participation from the OIF members in developing the implementation agreements and the motivation to get to a best technical solution.

## Reference:

[SPI-S Implementation Agreement](#)

## About the Authors:

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