



**Serdes Frammer Interface Level 5 (SFI-5):
Implementation Agreement for 40Gb/s
Interface for Physical Layer Devices.**

OIF-SFI5-01.02

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4 Document Revision History

OIF2001.082.2 Jan 25th 2001 PMC-Sierra proposal for SFI-5 presented at the February 2001 OIF meeting in Tampa: SFI-5: Common electrical interface between framers and serializer/deserializer parts for STS-768/STM-192 interfaces.

OIF2001.145.0 SFI-5 Implementation Agreement Draft 1.0, 27th Feb 2001

OIF2001.145.1 SFI-5 Implementation Agreement Draft 2.0, 20th April 2001. Document revised to remove preskew in Transmit direction and to remove parity function on reference lane. Pin naming convention and graphics brought in line with SFI-4. Interface testing clause added.

OIF2001.145.2 SFI-5 Implementation Agreement Draft 2.1, 16th May 2001. Document revised to reflect changes from May 2001 OIF meeting in Paris: Data clocks and Reference clocks changed to $\frac{1}{4}$ data rate.

OIF2001.145.3 SFI-5 Implementation Agreement Draft 3.0, 3rd July 2001. Document revised to reflect changes from June 2001 OIF PLL Group Interim meeting in Boston: Changes to Data clock, ref clock descriptions. Update skew magnitude. Include Appendix A: Quad OC192 mode.

OIF2001.145.4 SFI-5 Implementation Agreement Draft 3.1, 20th July 2001. Editorial corrections.

OIF2001.145.5 SFI-5 Implementation Agreement Draft 3.2, 3rd August 2001. Document revised to reflect changes from July/August 2001 OIF Plenary meeting in Vancouver: Remove Appendix 1 – Quad OC192 mode, clarify TXDCK.

OIF2001.145.6 SFI-5 Implementation Agreement Draft 4.0, 14th September 2001. Document revised to reflect changes from Sep 5/6 2001 OIF Interim meeting in Minneapolis: Update reference model to include TXCKSRC. Update signal descriptions. Remove skew parameters. Clarify RXS and TXDATA description. Clarify RXOOA, TXOOA as internal signals.

OIF2001.145.7 SFI-5 Implementation Agreement Draft 5.0, 6th November 2001. Document revised to reflect changes from Nov 6-8 2001 OIF Plenary meeting in Dallas: changes from Straw ballot #17 comment resolution.

OIF2001.145.8 SFI-5 Implementation Agreement Draft 5.1, 7th November 2001. Document revised to include the re-instated Quad OC192 mode as Appendix B.

OIF2001.145.9 SFI-5 Implementation Agreement Draft 5.1, 7th November 2001. Minor editorial change.

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OIF2001.145.10 SFI-5 Implementation Agreement Draft 5.3, 29th January 2002. Document revised to reflect changes from Straw ballot #20 comment resolution.

5 Introduction

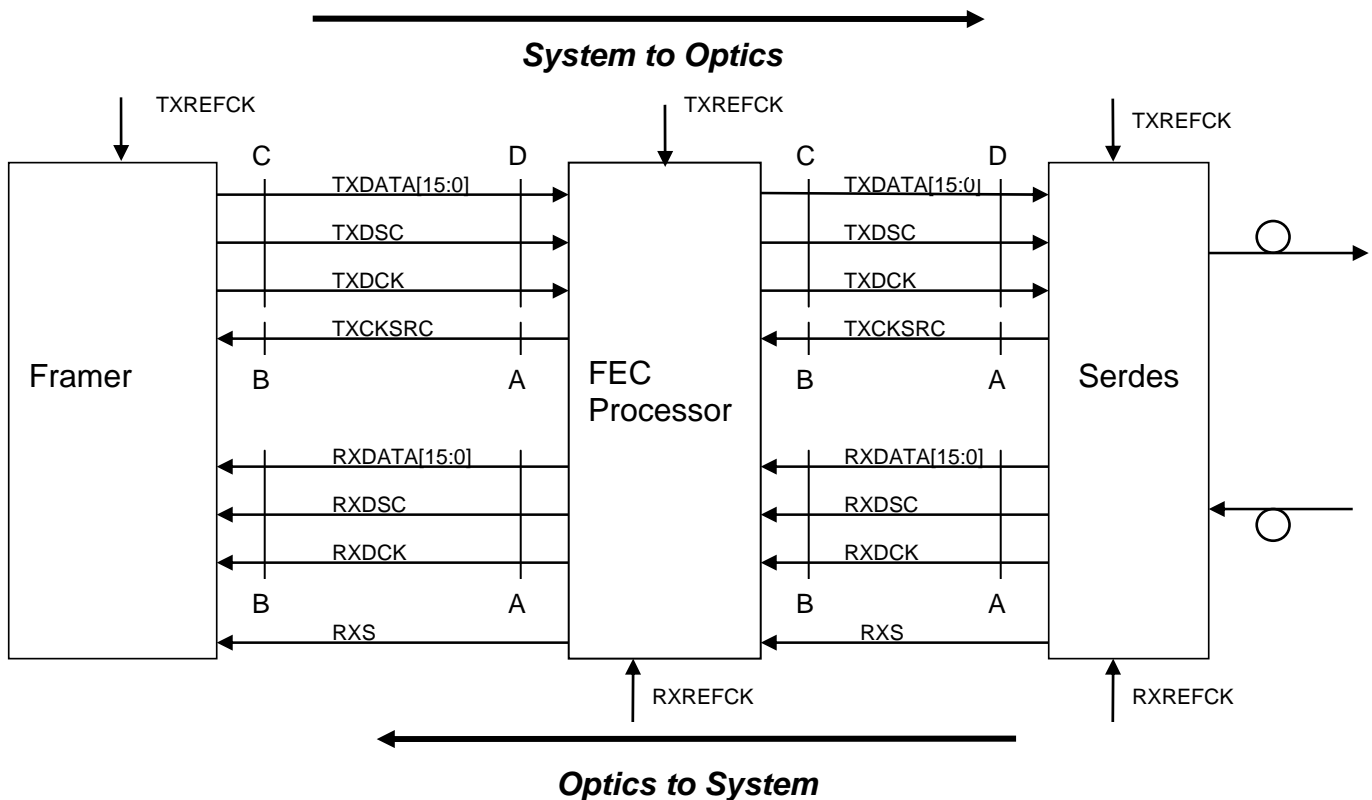
The typical line interface of a communications system with 40Gb/s optical links is expected to consist of three separate devices; an optical module containing a Serdes component, a forward error correction (FEC) processor and a Framer. The interconnection between these devices will be electrical where the maximum data rate per signal is less than the optical data rate. Thus, a multi-bit bus is required. It is desirable for the protocol of this bus to comply with the following objectives and requirements:

1. Support up to 50Gb/s bi-directional Aggregate data throughput such as SONET OC-768 [2], SDH STM-256 [3], OTN OTU-3 [4] and other systems operating at the payload data rate in the 40Gb/s range, and including up to 25% FEC overhead.
2. The interface can be used for point to point connection between Framer and FEC processor, Framer and Serdes, FEC processor and Serdes. Requirements for electrical parameters and control are the same between the different components.
3. The interface is intended to handle any format of data, which has been randomised, eg by a scrambler.
4. Capable of driving at least 8" of FR4 interconnect with one connector
5. Interface should be capable of operating indefinitely, without losing sync.
6. Support both in-band and out-of-band Forward Error Correction (FEC). A flexible clocking arrangement accounts for the additional FEC overhead.
7. The interface is independent of the type of optics – serial, CWDM or parallel, SMF or MMF.
8. Support of skew compensation over the signals comprising the interface bus. The Deskew algorithm used should minimize the complexity of the Serdes component.
9. Support of simple and robust clock and data recovery of the signals comprising the interface bus.
10. The interface includes independent status monitoring and supports received loss of signal detection.
11. The receive timing reference operates continuously, independent of link status.

12. The receive side of the interface will tolerate being driven while powered down without damage.
13. The interface includes data path link verification for component qualification and system integration test purposes.

The following is a general synopsis of the SFI Level 5 interface. For reference, a general block diagram is shown in Figure 5.1. SFI Level 5 is the interface between the Serdes component, the forward-error-correction (FEC) processor, and the Framer. It is designed to meet requirements of this particular application, although it may also be used in other applications. “Receive” and “Transmit” refer to data flow and associated control/status information from the optics-to-system direction, and from the system-to-optics direction, respectively. Note that the two instantiations of the SFI-5 bus in Figure 5.1 are independent and may operate at different frequencies.

Figure 5.1: System Reference Model



The points A, B, C and D are the reference points as defined in the common electrical specification (OIF2001.149)

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On both the receive and transmit interfaces, control and status information is sent separately from the corresponding data path. To accommodate the expected minute frequency offsets between the data stream in the two directions, the Receive and Transmit interfaces operate independently.

The SFI-5 bus has the following general characteristics:

1. Point-to-point connections applicable for connection of the Serdes component to the FEC processor, the FEC processor to the SONET/SDH framer or the Serdes component directly to the SONET/SDH framer.
2. 16-bit wide data bus with each channel operating at up to 3.125 Gb/s.
3. Electrical parameters are defined in the common electrical specification oif.2001.149 [1]. Parameters specific to SFI-5 are included in this document.
4. Maximum bus bandwidth of the 50 Gb/s is sufficient to support SONET OC-768 [2], SDH STM-256 [3], OTN OTU-3 [4] and other systems operating at the payload data rate in the 40Gb/s range, with up to 25% FEC overhead.
5. Deskew Channel included in both RX and TX directions contains out-of-band data sample to enable Deskew algorithm. Deskew Channel is 17th data channel, running continuously at full data rate. Deskew algorithm will be operating continuously to monitor skew tracking.
6. Minimize power consumption and the number of I/O signals to simplify PC board manufacture.
7. Maximize commonality of the receive and transmit directions and of instantiations in different applications of the bus.

6 Signal definition

6.1 Receive signals

The Receive signals are related to the transport of data from the optics towards the system. They are applicable to conducting data from the Serdes component to the FEC processor, from the FEC processor to the Framer, or from the Serdes Component directly to the Framer. All Receive signals, unless otherwise specified below, are differential CML as defined in the Common Electrical Implementation agreement oif2001.149.

Table 6.1: SFI-5 Receive Signal Summary

Signal Name	Direction	Function
RXDATA[15:0]	Optics to System	<p>The Receive Data (RXDATA[15:0]) signals carry the data in the optics to system direction. Serial optical data is striped onto RXDATA[15:0] in a round-robin fashion. RXDATA[15] contains the first bit received while RXDATA[0] the last bit received. When RXDATA[15:0] is generated by a Serdes component, the 16-bit word on RXDATA[15:0] has arbitrary alignment to the octets on the receive optical data stream. When RXDATA[15:0] is generated by an FEC processor and the 16-bit words are octet aligned, RXDATA[15] contains the first bit of the first byte received while RXDATA[0] contains the last bit of the second byte received.</p> <p>Each RXDATA[X] signal is a 2.488 Gb/s to 3.125 Gb/s stream. It contains every 16th bit of the data stream.</p> <p>RXDATA is frequency locked to RXDCK with unspecified static phase offset.</p>

Signal Name	Direction	Function
RXDSC	Optics to System	<p>The Receive Deskew Channel (RXDSC) signal provides reference data to enable skew measurements of the Receive data bus (RXDATA[15:0]).</p> <p>RXDSC contains reference frames consisting of 4 framing bytes, 4 bytes of expansion header, and 16 sets of 8-byte samples of each signal on the Receive data bus (RXDATA[15:0]). Samples are taken from the Receive data bus in a round-robin fashion, starting with RXDATA[15] and ending with RXDATA[0]. RXDSC is a 2.488 Gb/s to 3.125 Gb/s stream.</p> <p>RXDSC is frequency locked to RXDCK with unspecified static phase offset.</p>
RXDCK	Optics to System	<p>The Receive Data Clock (RXDCK) signal provides timing reference for the Receive data path signals (RXDATA, RXDSC). RXDCK is nominally a 50% duty cycle clock with a frequency that is one-quarter of the data bit rate of RXDATA and RXDSC. RXDCK is frequency locked to these signals. Static phase offset between RXDCK and RXDATA, RXDSC is unspecified.</p> <p>It is mandatory for the source device of the receive interface to generate RXDCK. It is optional for the sink device in the receive interface to use RXDCK.</p>

Signal Name	Direction	Function
RXREFCK	Optics to System	<p>The Receive Reference Clock (RXREFCK) signal provides reference timing to the Receive interface.</p> <p>RXREFCK is nominally a 50% duty cycle clock with a frequency that is one quarter of the data bit rate of RXDATA and RXDSC. In the SERDES component, RXREFCK is nominally the same frequency as RXDCK. In the FEC processor, RXREFCK is the frequency reference to the source of RXDATA, RXDCK, RXDSC. Jitter characteristics of RXREFCK do not directly concern interoperability and are beyond the scope of this implementation agreement.</p> <p>Implementation of RXREFCK is mandatory for a Serdes and FEC component, and not necessary for a Framer component. In some implementations, RXREFCK could share a common pin with TXREFCK.</p>
RXS	Optics to System	<p>The Receive Status (RXS) signal carries status from the Serdes component to the FEC processor, from the FEC processor to the SONET/SDH framer, or from the Serdes component directly to the SONET/SDH framer. The encoding of RXS is:</p> <p>RXS = 'b0 : Idle, RXS = 'b1 : Receive alarm,</p> <p>Receive alarm shall indicate the RXDCK and RXDATA are not derived from the optical receive signal. The electrical I/O type shall be LVCMOS. It is mandatory for the source device of the receive interface to generate RXS. It is optional for the sink device in the receive interface to use RXS. RXS is an asynchronous signal.</p>

6.2 Transmit Signals

The Transmit signals are related to the transport of data from the system towards the optics. They are applicable to conducting data from the Framer to the FEC processor, from the FEC processor to the Serdes Component, or from the Framer directly to the Serdes component. All Transmit signals, unless otherwise specified below, are differential CML as defined in the Common Electrical Implementation Agreement oif2001.149.

Table 6.2: SFI-5 Transmit Signal Summary

Signal Name	Direction	Function
TXDATA[15:0]	System to Optics	<p>The Transmit Data (TXDATA[15:0]) signals carry data in the system to optics direction. Data on TXDATA[15:0] are placed on the transmit optical stream in a round-robin fashion. TXDATA[15] contains the first bit transmitted while TXDATA[0] the last bit transmitted. When TXDATA[15:0] is octet aligned, TXDATA[15] contains the first bit of the first byte transmitted while TXDATA[0] contains the last bit of the second byte transmitted.</p> <p>Each TXDATA[X] signal is a 2.488 Gb/s to 3.125 Gb/s stream. It contains every 16th bit of the transmitted data stream.</p> <p>TXDATA[15:0] is frequency locked to TXDCK with unspecified static phase offset.</p>
TXDSC	System to Optics	<p>The Transmit Deskew Channel (TXDSC) provides reference data to enable skew measurements of the Transmit data bus (TXDATA[15:0]). TXDSC is a 2.488 Gb/s to 3.125 Gb/s stream.</p> <p>TXDSC contains reference frames consisting of 4 framing bytes, 4 bytes of expansion header and 16 sets of 8-byte samples of each signal recovered from the Transmit data bus (TXDATA[15:0]). Samples are taken from the Transmit data bus in a round-robin fashion, starting with TXDATA[15] and ending with TXDATA[0]. TXDSC is a 2.488 Gb/s to 3.125 Gb/s stream.</p> <p>TXDSC is frequency locked to TXDCK with unspecified static phase offset.</p>

Signal Name	Direction	Function
TXDCK	System to Optics	<p>The Transmit Data Clock (TXDCK) signal provides timing reference for the Transmit data path signals (TXDATA, TXDSC). TXDCK is nominally a 50% duty cycle clock with a frequency that is one-quarter of the data bit rate of TXDATA and TXDSC. TXDCK is frequency locked to TXREFCK, TXDSC, and TXDATA. Static phase offset between TXDCK and TXDATA, TXDSC is unspecified.</p> <p>It is mandatory for the source device of the Transmit interface to generate TXDCK. It is optional for the sink device in the Transmit interface to use TXDCK.</p>
TXCKSRC	Optics to System	<p>The Transmit Clock Source(TXCKSRC) signal provides timing reference for the Transmit data path signals (TXDATA, TXDSC, TXDCK).</p> <p>TXCKSRC is nominally a 50% duty cycle clock with a frequency that is one-quarter of the data bit rate of TXDATA and TXDSC. TXCKSRC is derived from TXREFCK in the sink device.</p> <p>It is mandatory for the source device in the transmit interface to be able to receive TXCKSRC into the TXREFCK and to use this input as a frequency reference for TXDCK, TXDSC, and TXDATA. It is optional for a sink device in the transmit interface to generate a TXCKSRC output. If the sink device does not drive the TXCKSRC output, then the source device uses an external clock source connected to TXREFCK as the frequency reference for TXDCK, TXDSC, and TXDATA, and the sink device must accept data at the resulting frequency.</p> <p>Note: Although defined as separate functions by the reference model, this signal description allows an implementation to use a single device pin on the source device as a common TXCKSRC or TXREFCK input.</p>

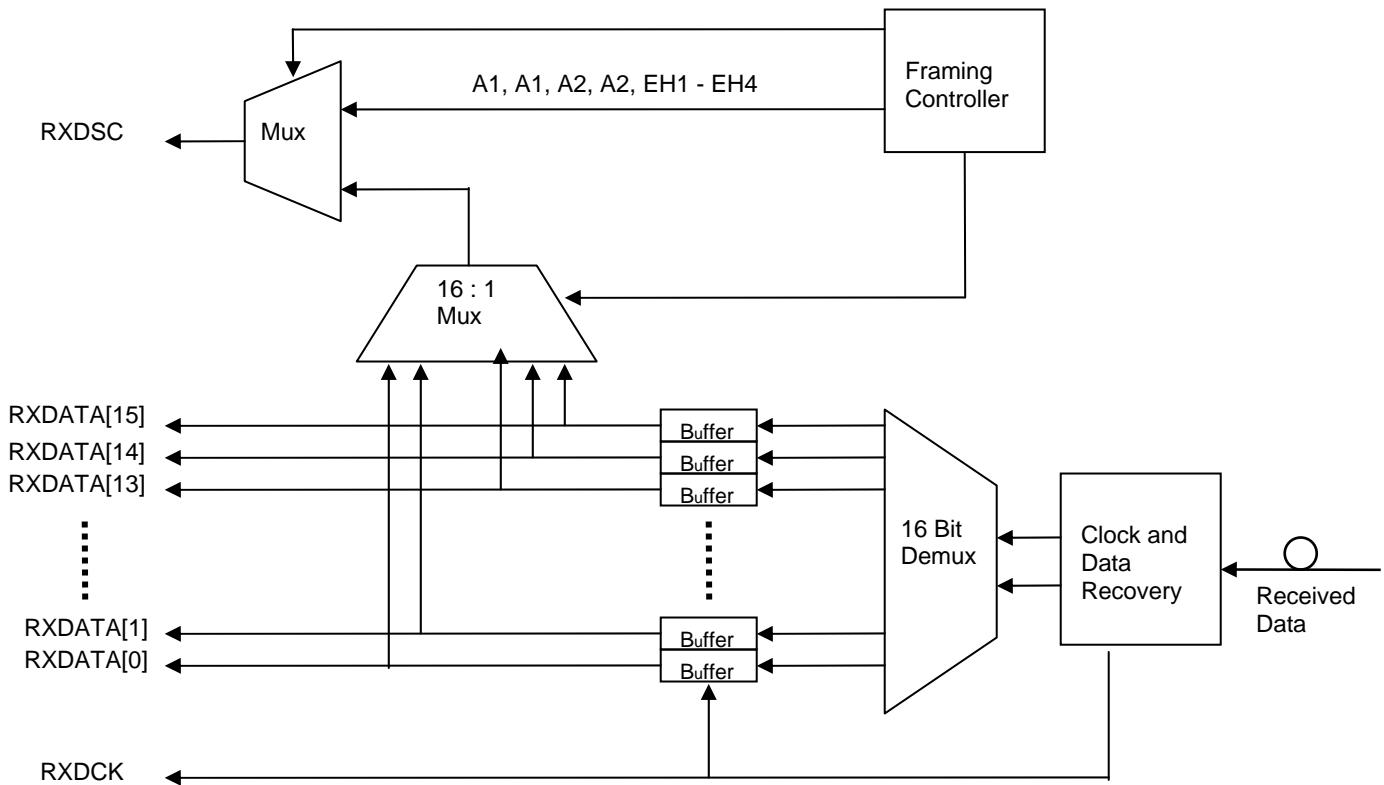
Signal Name	Direction	Function
TXREFCK	System to Optics	<p>The Transmit Frequency Reference (TXREFCK) signal provides the frequency reference for the Transmit data path devices (Framer, FEC, and Serdes). TXREFCK is nominally a 50% duty cycle clock with a frequency that is one-quarter of the data bit rate of TXDATA and TXDSC. TXDATA, and TXDSC shall be frequency locked to TXREFCK. Static phase offset between TXDCK, TXDSC and TXDATA is unspecified.</p> <p>It is mandatory for one device in the Transmit chain to have an external clock source connected to TXREFCK.</p>

7 Logical Reference Models

7.1 Serdes component Receive interface

Figure 7.1 below shows a logical model of the Receive interface in a Serdes component. The intent is to show the source of data in the Receive Deskew Channel (RXDSC). No limit is placed on device implementation, and this model is not intended to represent an actual design.

Figure 7.1: Model of Serdes component - Receive I/F Source



Data in the optical stream is striped across the 16 bit lanes of the Receive Data bus (RXDATA[15:0]) in a round-robin fashion. The first bit received is written into the re-timing buffer associated with RXDATA[15] and the last into that associated with RXDATA[0]. The re-timing buffers act as a set of FIFOs to bridge between the optical timing domain and the Receive interface timing domain. Wander between the bit lanes is absorbed by the re-timing buffers.

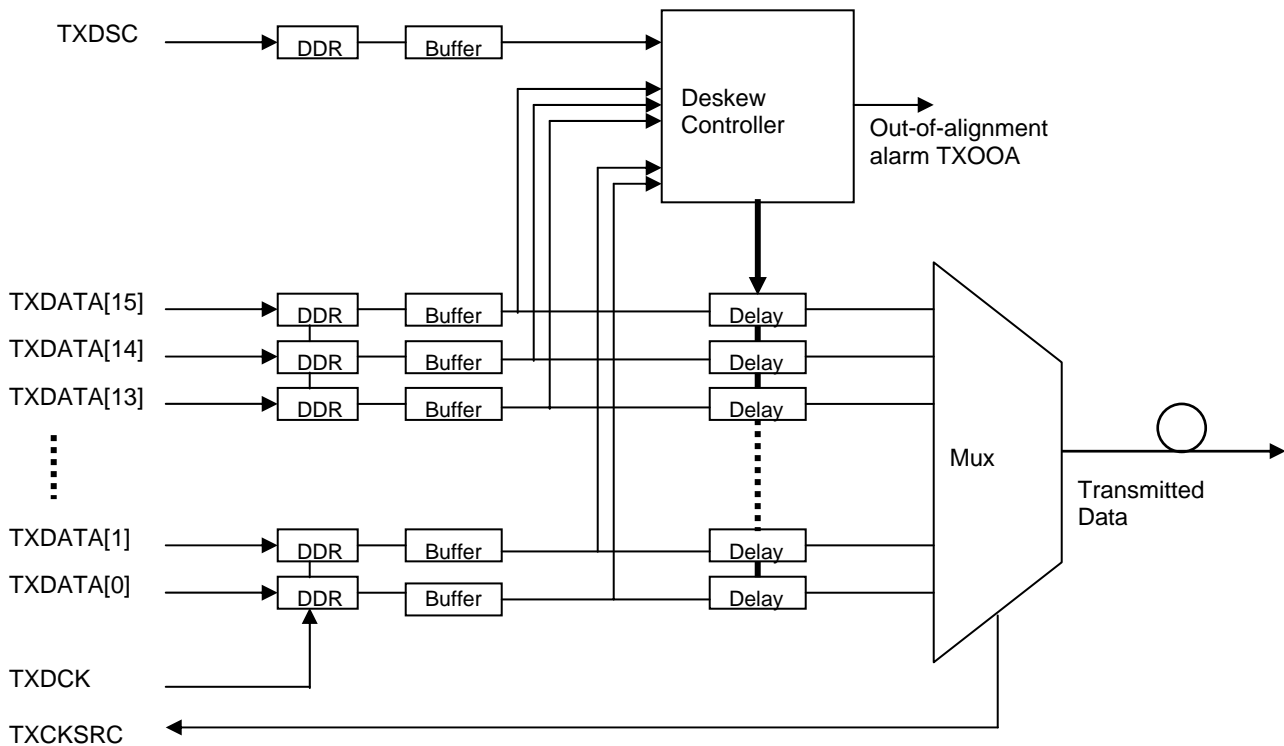
RXDSC replicates the data sent on each signal of the Receive Data bus RXDATA[15:0] cyclically. The framing pattern generator is chosen first to insert the framing pattern of two A1 (F6 Hex) and two A2 (28 hex) bytes and 4 bytes of expansion header (EH1 to EH4 are each currently set to 1010

1010 pattern when unused). Then, each RXDATA[X] signal is sampled, in turn, for 64 bit times (8 bytes). Reporting begins with RXDATA[15] and ends with RXDATA[0]. After all the data lanes have been sent, a new reference frame is initiated on RXDSC and then continuously generated.

7.2 Serdes Component Transmit interface

Figure 7.2 below shows a logical model of the Transmit interface in a Serdes Component. The intent is to show operation of the Deskew algorithm, controlled by the Deskew Channel (TXDSC). No limit is placed on device implementation, and this model is not intended to represent an actual design.

Figure 7.2: Model of Serdes component - Transmit I/F Sink



Data on the Transmit Data bus (TXDATA[15:0]) and TXDSC is conditioned by the data recovery units (DDR) which tracks the center of the “eye” at each bit period. Data from each bit lane is written into an associated re-timing buffer. Data from the re-timing buffer associated with TXDATA[15] is transmitted first while data in that associated with TXDATA[0] is transmitted last. The re-timing buffers act as a set of FIFOs to bridge between the Transmit interface timing domain and the optical stream timing domain. Wander between the bit lanes is absorbed by the re-timing buffers.

The function of the Deskew Controller block is to recognise the framing bytes and header bytes in the Deskew Channel TXDSC, to identify the start of the reference data that is replicated from each of TXDATA[X]. Each of the TXDATA[X] channels is then compared with the sampled data in the Deskew Channel in turn. The Deskew Controller performs a pattern match between the replicated data in TXDSC with the original data in the corresponding TXDATA[X] signal. Where there is a match, the relative delay of TXDATA[x], in relation to TXDSC, is found. It is possible to measure how many bit periods of skew there are on each channel. This information is used to compensate for the skew by adjusting the delay elements specific to each channel.

A delay chain is associated with each interface signal that allows the Deskew Controller to use the set of 16 relative delays to compensate for the skew in the SFI-5 interface and to reconstruct the original alignment of the Transmit data TXDATA[15:0].

The loss of frame sync alarm TXLOF is an internal signal communicated over a management interface, and is not an SFI-5 signal pin. TXLOF is set if the framing bytes of the deskew channel have not been recognised and locked. When the deskew controller has locked onto the framing bytes, then TXLOF is cleared.

The out-of-alignment alarm TXOOA is an internal signal communicated over a management interface, and is not an SFI-5 signal pin. TXOOA is set if a match has not been found on any of the 16 data channels. When a data match has been found on all 16 data channels, and stable skew data derived, then the Deskew algorithm is considered as locked, and the TXOOA is cleared. Skew measurements are monitored continuously, and the TXOOA alarm remains cleared as long as consistent skew data is generated.

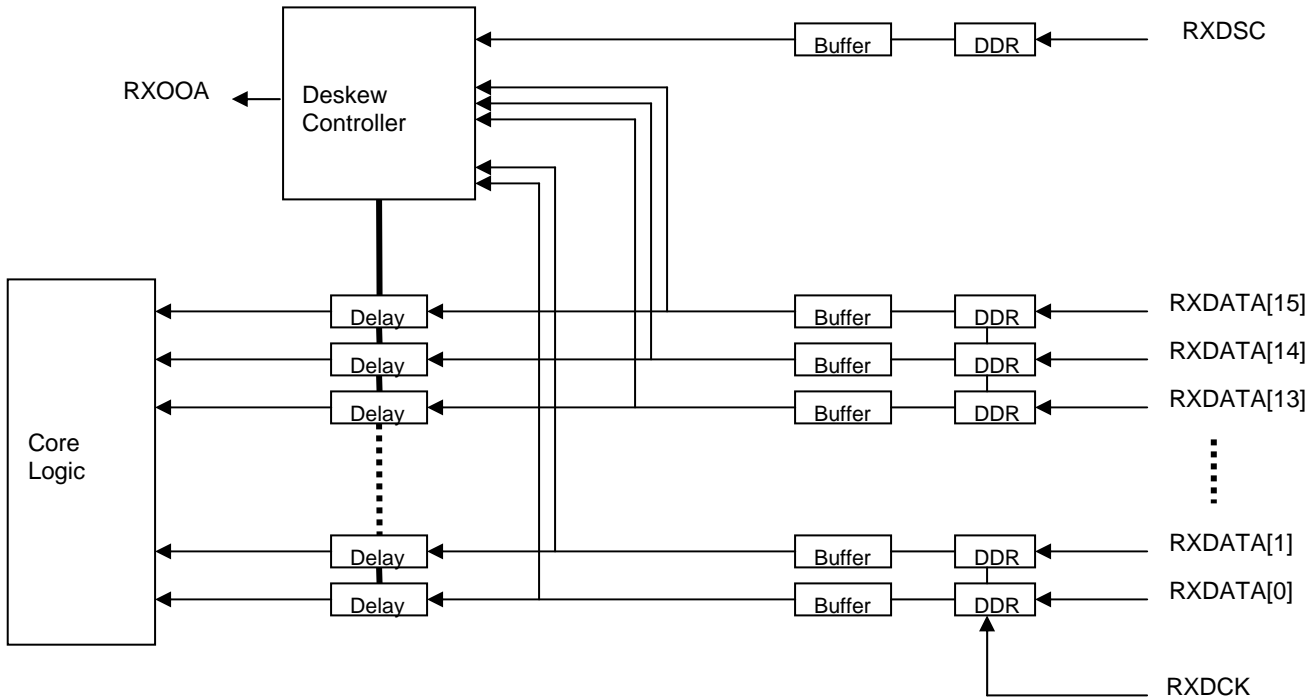
The function of the Deskew Controller is to continuously compare data on the Deskew Channel TXDSC with the respective Data Channels TXDATA[15:0]. Any mis-match errors can be detected, which would represent errors generated over the SFI-5 interface. These errors should be reported as part of the minimum test requirements for the interface. These test requirements are described in section 10.

7.3 Receive Interface of FEC Processor / Framer

Figure 7.3 below shows a model of the Receive interface in the FEC processor or in the Framer. The intent is to show operation of the Deskew algorithm, controlled by the Receive Deskew Channel RXDSC. No limit is

placed on device implementation, and this model is not intended to represent an actual design.

Figure 7.3: Model of FEC Processor / SONET Framer – Receive I/F Sink



The DDR blocks track the center of the “eye” of the Receive Data bus (RXDATA[15:0]) and the Receive Deskew Channel (RXDSC) signal. The re-timing buffers bridge between the Receive interface timing domain and the system timing domain. Wander between the bit lanes is absorbed by the re-timing buffers.

The function of the Deskw Controller block is to recognise the framing bytes and header bytes in the Receive Deskew Channel RXDSC. These identify the start of the reference data that is replicated from each of RXDATA[X]. Each of the RXDATA[X] channels is then compared with the sampled data in the Deskw Channel in turn. The Deskw Controller performs a pattern match between the replicated data in RXDSC with the original data in the corresponding RXDATA[X] signal. Where there is a match, the relative delay of RXDATA[X], in relation to RXDSC, is found. It is possible to measure how many bit periods of skew there are on each channel. This information is used to compensate for the skew by adjusting the delay elements specific to each channel.

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A delay chain is associated with each interface signal that allows the Deskew Controller to perform a pattern match between the replicated data in RXDSC with the original data in the corresponding RXDATA[X] signal. Where there is a match, the relative delay of RXDATA[X], in relation to RXDSC, is found. The Deskew Controller uses the set of 16 relative delays to construct the compensated Receive data (RXDATA[15:0]) that recovers the original alignment, prior to timing distortions.

The loss of frame sync alarm RXLOF is an internal signal communicated over a management interface, and is not an SFI-5 signal pin. RXLOF is set if the framing bytes of the deskew channel have not been recognised and locked. When the deskew controller has locked onto the framing bytes, then RXLOF is cleared.

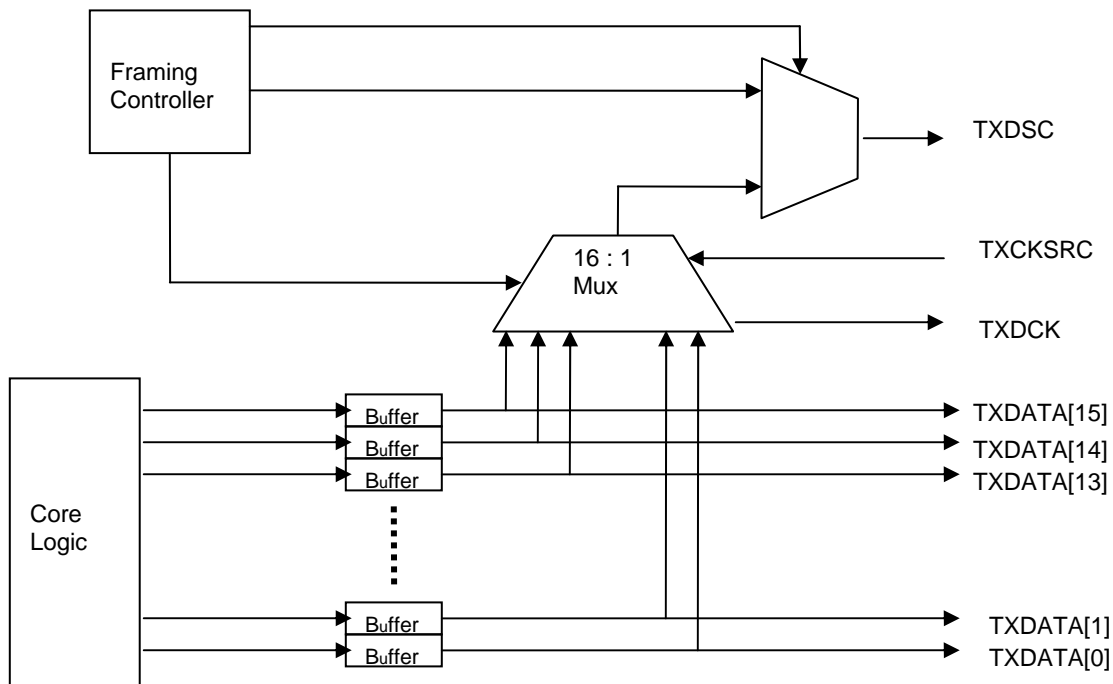
The out-of-alignment alarm RXOOA is an internal signal communicated over a management interface, and is not an SFI-5 signal pin. RXOOA is set if a match has not been found on any of the 16 data channels. When a data match has been found on all 16 data channels, and stable skew data derived, then the Deskew algorithm is considered as locked, and the RXOOA is cleared. Skew measurements are monitored continuously, and the RXOOA alarm remains cleared as long as consistent skew data is generated.

The function of the Deskew Controller is to continuously compare data on the Deskew Channel RXDSC with the respective Data Channels RXDATA[15:0]. Any mis-match errors can be detected, which would represent errors generated over the SFI-5 interface. These errors should be reported as part of the minimum test requirements for the interface. These test requirements are described in section 10.

7.4 Transmit interface in FEC Processor / Framer

Figure 7.4 below shows a model of the Transmit interface in the FEC processor or in the SONET/SDH framer. The intent is to show the source of data in the Transmit Deskew Channel. No limit is placed on device implementation, and this model is not intended to define an actual design.

Figure 7.4: Model of FEC Processor / SONET Framer – Transmit I/F Source



Data from the core logic of the FEC Processor or Framer is striped across the 16 bit lanes of the Transmit Data bus (TXDATA[15:0]) in a round-robin fashion. The first bit received is written into the re-timing buffer associated with TXDATA[15] and the last into that associated with TXDATA[0]. The re-timing buffers act as a set of FIFOs to bridge between the core logic timing domain and the Transmit interface timing domain.

TXDSC replicates the data sent on each signal of the Transmit Data bus TXDATA[15:0] cyclically. The framing pattern generator is chosen first to insert the framing pattern of two A1 (F6 Hex) and two A2 (28 hex) bytes and 4 bytes of expansion header (EH1 to EH4 are each currently set to 1010 1010 pattern when unused). Then, each TXDATA[X] signal is sampled, in turn, for 64 bit times (8 bytes). Reporting begins with TXDATA[15] and ends with TXDATA[0]. After all the data lanes have been sent, a new reference frame is initiated on TXDSC and then continuously generated.

8 Bit-lane Deskew

The Data signals may encounter different delays in transit from the SFI-5 source device to the sink device. The maximum relative skew introduced by the connection system is specified in the Common Electrical Implementation Agreement. The earliest arriving signal may lead the latest arriving by n bits. Relative to the earliest, each of the remaining signals is coincident, or is up to n unit intervals late. The search space for determining the relative delays of all 17 signals on SFI-5 is $(n+1)^{17}$ combinations. To make the problem tractable, a reference signal is used in SFI-5, known as the Deskew Channel, to allow each bit-lane to independently measure its own delay relative to the reference signal. Having de-coupled the measurement to individual signals, the search space becomes trivially small.

The bit-lane Deskew function is shared between the SFI-5 source and sink devices at either end of the Receive and Transmit interfaces. In the source device, data is sampled from each of the 16 data channels sequentially, and copied onto the Deskew Channel. The Deskew Channel is then sent with the 16 data channels to the sink device over the SFI-5 interface.

Data input to the sink device, will be skewed by the different delays in each of the data channels. It is the function of the Deskew algorithm operating in the sink device to measure the amount of skew on each data channel, and then to use this skew information to compensate for the amount of skew. The bit lane Deskew algorithm will make an initial skew measurement on initial power up or connection. Subsequent to skew measurement, external conditions may vary causing the skews to change. It is a requirement that devices that are compliant to this implementation agreement be able to track skew changes of the minimum value to the maximum value without introducing errors. The Deskew algorithm will operate continuously during normal operation of the SFI-5 interface, and continuously track skew.

Table 8.1 below shows a reference frame on the Receive Deskew Channel (RXDSC) or the Transmit Deskew Channel (TXDSC). Each reference frame is delimited by 4 framing bytes consisting of two A1 bytes (F6 hex) and two A2 bytes (28 hex). The use of the expansion header bytes is for further study. The 16 sets of data sample bytes are copied from the Receive Data bus (RXDATA[15:0]) or the Transmit Data bus (TXDATA[15:0]) starting with bit 15 (RXDATA[15]/TXDATA[15]) and ending with bit 0 (RXDATA[0]/TXDATA[0]). In Table 8.1, transmission is from left to right and top to bottom.

Table 8.1: Reference Frame on RXDSC or TXDSC

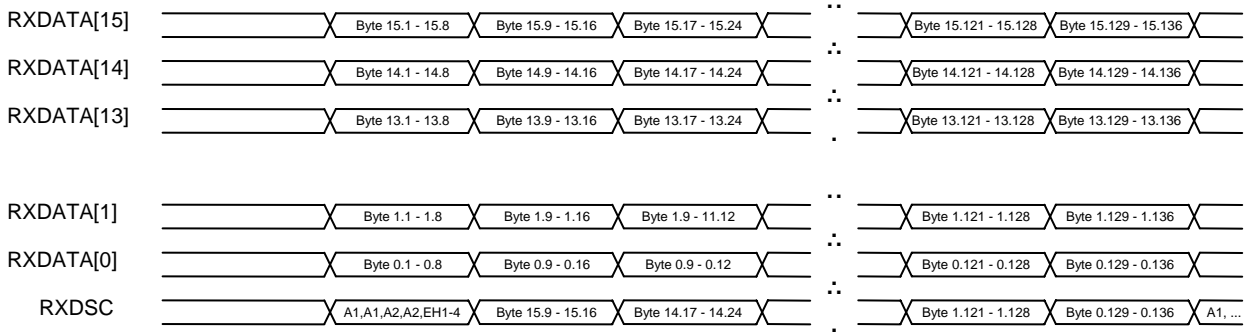
Bit time	Value	Value	Value	Value	Comments
1 - 32	A1 1111 0110	A1 1111 0110	A2 0010 1000	A2 0010 1000	Framing bytes
33 - 64	EH1 1010 1010	EH2 1010 1010	EH3 1010 1010	EH4 1010 1010	Expansion Header bytes For future use
65 - 96	R/TXDATA[15] Bits 1 - 8	R/TXDATA[15] Bits 9 - 16	R/TXDATA[15] Bits 17 - 24	R/TXDATA[15] Bits 25 - 32	64 consecutive bits from RXDATA[15] or TXDATA[15]
97 - 128	R/TXDATA[15] Bits 33 - 40	R/TXDATA[15] Bits 41 - 48	R/TXDATA[15] Bits 49 - 56	R/TXDATA[15] Bits 57 - 64	
129 - 160	R/TXDATA[14] Bits 1 - 8	R/TXDATA[14] Bits 9 - 16	R/TXDATA[14] Bits 17 - 24	R/TXDATA[14] Bits 25 - 32	64 consecutive bits from RXDATA[14] or TXDATA[14]
161 - 192	R/TXDATA[14] Bits 33 - 40	R/TXDATA[14] Bits 41 - 48	R/TXDATA[14] Bits 49 - 56	R/TXDATA[14] Bits 57 - 64	
193 - 1024					64 consecutive bits from each of RXDATA[13] to RXDATA[1] or TXDATA[13] to TXDATA[1]
1025 - 1056	R/TXDATA[0] Bits 1 - 8	R/TXDATA[0] Bits 9 - 16	R/TXDATA[0] Bits 17 - 24	R/TXDATA[0] Bits 25 - 32	64 consecutive bits from RXDATA[0] or TXDATA[0]
1057 - 1088	R/TXDATA[0] Bits 33 - 40	R/TXDATA[0] Bits 41 - 48	R/TXDATA[0] Bits 49 - 56	R/TXDATA[0] Bits 57 - 64	

Note: The expansion header bytes EH1-4 must not be allowed to contain the A1/A2 framing bytes.

8.1 Deskew of Receive interface

At the receive interface, a reference frame is generated in the source device, consisting of 4 framing bytes, 4 bytes of expansion header and 128 bytes of data samples. The framing pattern is two A1 bytes (F6 hex) followed by two A2 bytes (28 hex). The data samples are taken from the Receive data bus (RXDATA[15:0]) in 8-byte sets, starting with RXDATA[15] and ending with RXDATA[0]. Figure 8.1 below shows the functional timing diagram of the Receive Deskew Channel. Reference frames are sent continuously over the receive interface to enable the Deskew algorithm in the sink device and continuous monitoring of skew.

Figure 8.1: Receive Deskew Channel (RXDSC) Functional Timing



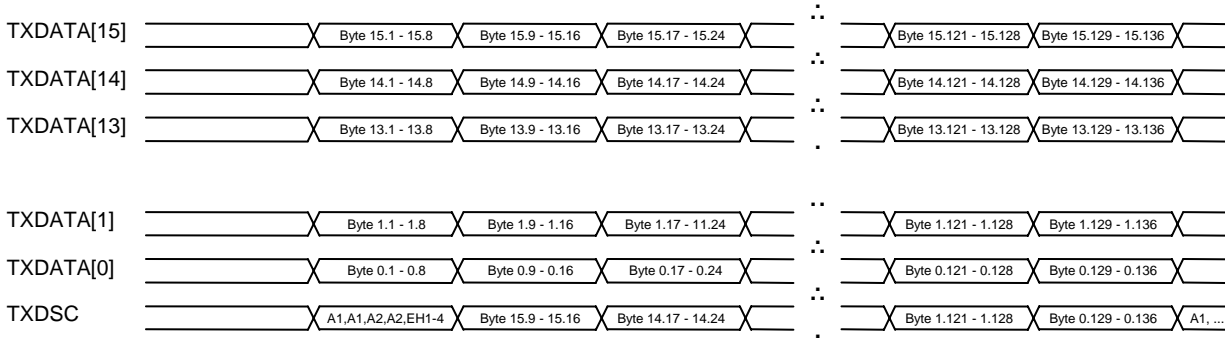
Until the Deskew Algorithm finds lock on all 16 data channels, the Receive interface is in an out-of-alignment state, and the RXOOA alarm is set.

The sink device monitors the Receive Deskew Channel (RXDSC) for the reference data. It shall adjust the delay of each RXDATA[15:0] signal, on a unit interval by unit interval basis, such that the delay from source device to the output of the delay chain at the sink device is identical for all 16 signals. When the skew of all 16 data channels is compensated and locked, the RXOOA alarm is cleared. The Deskew algorithm will continue to operate after the RXOOA is removed. Under normal circumstances, the interface will operate continuously with skew being monitored, and the RXOOA alarm remains off. If failure of the Deskew algorithm occurs, and any of the 16 channels fall out of lock, then the RXOOA alarm will be set.

8.2 Deskew of Transmit interface

At the Transmit interface, a reference frame is generated in the source device, consisting of 4 framing bytes, 4 bytes of expansion header and 128 bytes of data samples. The framing pattern is two A1 bytes (F6 hex) followed by two A2 bytes (28 hex). The data samples are taken from the Transmit data bus (TXDATA[15:0]) in 8-byte sets, starting with TXDATA[15] and ending with TXDATA[0]. Figure 8.2 below shows the functional timing diagram of the Transmit Deskew Channel. Reference frames are sent continuously over the Transmit interface to enable the Deskew algorithm in the sink device and continuous monitoring of skew.

Figure 8.2: Transmit Deskew Channel (TXDSC) Functional Timing



Until the Deskew Algorithm finds lock on all 16 data channels, the Transmit interface is in an out-of-alignment state, and the TXOOA alarm is set.

The sink device monitors the Transmit Deskew Channel (TXDSC) for the reference data. It shall adjust the delay of each TXDATA[15:0] signal, on a unit interval by unit interval basis, such that the delay from source device to the output of the delay chain at the sink device is identical for all 16 signals. When the skew of all 16 data channels is compensated and locked, the TXOOA alarm is removed. The Deskew algorithm will continue to operate after the TXOOA is removed. Under normal circumstances, the interface will operate continuously with skew being monitored, and the TXOOA alarm remains off. If failure of the Deskew algorithm occurs, and any of the 16 channels fall out of lock, then the TXOOA alarm will be enabled.

9 Component Functionality

9.1 Serdes component Receive Functionality

The Serdes component performs clock and data recovery (CDR) on the received optical data stream. A simple round-robin serial to parallel conversion is performed on the recovered data to construct 16-bit words. No heed is paid to the underlying octet alignments within the optical data stream. The first bit received is placed in the most significant bit of the word while the last bit received is placed in the least significant bit.

The Serdes component includes functionality to ensure that a continuous Receive data clock (RXDCK) is sent to the FEC processor or framer device. The lock range of the optical receiver shall exceed 100ppm over temperature and supply range. The clock recovered from the received optical signal is compared with a clock derived from a reference frequency. If the recovered clock deviates from the reference frequency by more than 1000ppm, then RXDCK shall be sourced from the reference clock (RXREFCK). Somewhere between 100ppm and 1000ppm, an out-of lock condition will be declared, and RXDCK shall switch from being sourced from the recovered clock to being sourced from the reference.

If loss of received data (LOS) is detected, then the RXDCK shall be sourced from the reference clock (RXREFCK).

Under conditions above when the RXDCK is not sourced from the received data, then the receive status alarm (RXS) shall be set high.

Switching the receive data clock (RXDCK) shall be done such that the minimum pulse width and minimum period of RXDCK are not violated.

The Serdes component continuously generates reference frames on the Deskew Channel (RXDSC). The reference frame consists of a framing pattern and copies data taken from the Receive data bus (RXDATA[15:0]), one signal at a time.

9.2 Serdes component Transmit Functionality

The Serdes component performs data recovery (DR) on the Transmit Data (TXDATA[15:0]) signals. The signals are frequency locked but not phase locked to each other and can have un-correlated jitter characteristics. Thus, the DR process must be performed independently on each signal. Data recovered at each signal is written into one of 17 re-timing buffers and is read out in parallel every 16 bit times of the transmit optical data stream. The purpose of the re-timing buffers is to compensate for relative jitter and arrival times on TXDATA signals as well as transient clock differences between

TXDATA and the transmit stream. A simple round-robin parallel to serial conversion process stripes transmitted data from the re-timing buffer servicing TXDATA[15] first and data from that servicing TXDATA[0] last.

The Serdes component uses reference frames from the Deskew Channel (TXDSC) to enable the Deskew algorithm, to compensate for timing skew in the SFI-5 interface. A transmit out-of-alignment alarm (TXOOA) will be raised until the skew compensation on all 16 channels is locked. The Deskew algorithm operates continuously, and under normal operation, the out-of-alignment alarm is cleared.

9.3 FEC Processor Receive Functionality

The FEC processor performs data recovery (DR) on the Receive Data (RXDATA[15:0]) and on the Receive Deskew Channel (RXDSC). The signals are frequency locked but not phase locked and can have un-correlated jitter characteristics. Thus, the DR process must be performed independently. The recovered data is written into one of 17 re-timing buffers and is read out using RXDCK. The purpose of the re-timing buffer is to compensate for relative jitter and arrival times on RXDATA as well as transient clock differences between RXDATA and RXDCK.

The FEC processor compares the replicated data on Deskew Channel (RXDSC) against the data on the RXDATA signals to determine the relative skew between the signals. It then adjusts the delay through the re-timing buffers to compensate. The Receive out-of-alignment alarm RXOOA is set until all 16 channels are locked.

As a result of the Deskewing process, the order of arrival of the bits at the output of the re-timing buffers is known. I.e., output of re-timing buffer #15 is the first bit received while output of re-timing buffer #0 is the last bit received. The FEC processor will search the data stream constructed from the output of the re-timing buffers for the framing pattern associated with the FEC frame.

9.4 FEC Processor Transmit Functionality

The Transmit side of the FEC processor generates data for transmission by the Serdes component. It also continuously generates reference frames on the Deskew Channel (TXDSC) to enable the Deskew algorithm in the downstream Serdes component, to compensate for timing skew in the SFI-5 Transmit interface. The reference frame consists of a framing pattern and data taken from the Transmit data bus (TXDATA[15:0]), one signal at a time.

Implementation Agreement OIF-SFI5-01.0

9.5 Framers Receive Functionality

The functionality of the Receive side of the SONET/SDH framer is identical to that of the FEC processor.

9.6 Framers Transmit Functionality

The functionality of the Transmit side of the SONET/SDH framer is identical to that of the FEC processor.

10 Interface test requirements

It is a requirement of the SFI-5 interface that it will operate indefinitely without inducing errors. A minimum set of test requirements is defined to indicate that the interface is set up correctly and that it monitors itself for continuous reliable operation. The following functions are necessary to provide a minimum set of test functions:

1. Confirm that each of the 16 data channels are connected correctly in both Receive and Transmit directions. This function can be implemented by the Deskew Controller in each direction. The Deskew Channel (RXDSC and TXDSC) is required to match with each of the data channels in turn. If persistent mis-match occurs with any of the 16 channels, then the RXOOA or TXOOA alarm is raised relating to the respective Receive or Transmit directions. The minimum requirement is to monitor each alarm. It would be possible to include functionality to indicate which Channel is faulty – this would be within the scope of individual implementations and not mandatory in this implementation agreement.
2. Verify that the Deskew function correctly compensates for Skew over the SFI-5 interface. It is the function of the Deskew Algorithm to measure the level of skew on each data channel in both Receive and Transmit directions and to control the delay compensation on each channel. When a stable skew measurement is made on each channel, the interface is considered in lock, and the RXOOA and TXOOA alarms are cleared. These alarms should indicate that the Deskew compensation is working correctly after initial power up and during continuous operation.
3. Error checking during continuous operation. It is possible to use the Deskew Channel in both Receive and Transmit directions to detect gross errors over the interface. The function of the Deskew Controller in the sink side of each interface is to compare the replicated data on the Deskew Channel with the respective data on each data channel. Mismatch errors can then be detected in the data sample. It is a requirement of the interface to continuously monitor for these potential errors. The procedure for reporting errors is not part of the SFI-5 implementation agreement, but should be included as part of the management function.

11 AC Characteristics

The majority of the AC characteristic of SFI-5 is detailed in the common electrical parameters in contribution OIF2001.149. Only those that differ are listed below.

Table 11.1: Data Path Interface Timing

Symbol	Description	Min	Max	Units
f_D	RXDATA[15:0], RXDSC, TXDATA[15:0], TXDSC data rate	2.488	3.125	Gb/s
f_R	RXREFCK, TXREFCK, RXDCK, TXDCK, TXCKSRC frequency	$f_D(\text{MIN})/4$	$f_D(\text{MAX})/4$	MHz

12 References

- [1] Optical Internetworking Forum OIF2001.149, "Sxl-5: Electrical Characteristics of Common I/Os for SFI-5 and SPI-5".
- [2] ANSI - T1.105-1995, "Synchronous Optical Network (SONET) – Basic Description including Multiplex Structure, Rates, and Formats", 1995.
- [3] ITU, Recommendation G.707 - "Network Node Interface For The Synchronous Digital Hierarchy", 07/09/2000.
- [4] ITU, Recommendation G.709 – " Network Node Interface for the Optical Transport Network (OTN)", Feb 2001.
- [5] Optical Internetworking Forum, OIF2001.011, "SFI-5 Proposal for a 40Gb/s Interface", January, 2001.
- [6] Optical Internetworking Forum, OIF2001.008, "SFI-5 Reference Bit for Lane Deskew", January, 2001.

Appendix A Sample System Configurations

1 Abstract

This appendix is informative and describes some examples of different system configurations where the SFI-5 interface will be implemented.

2 Introduction

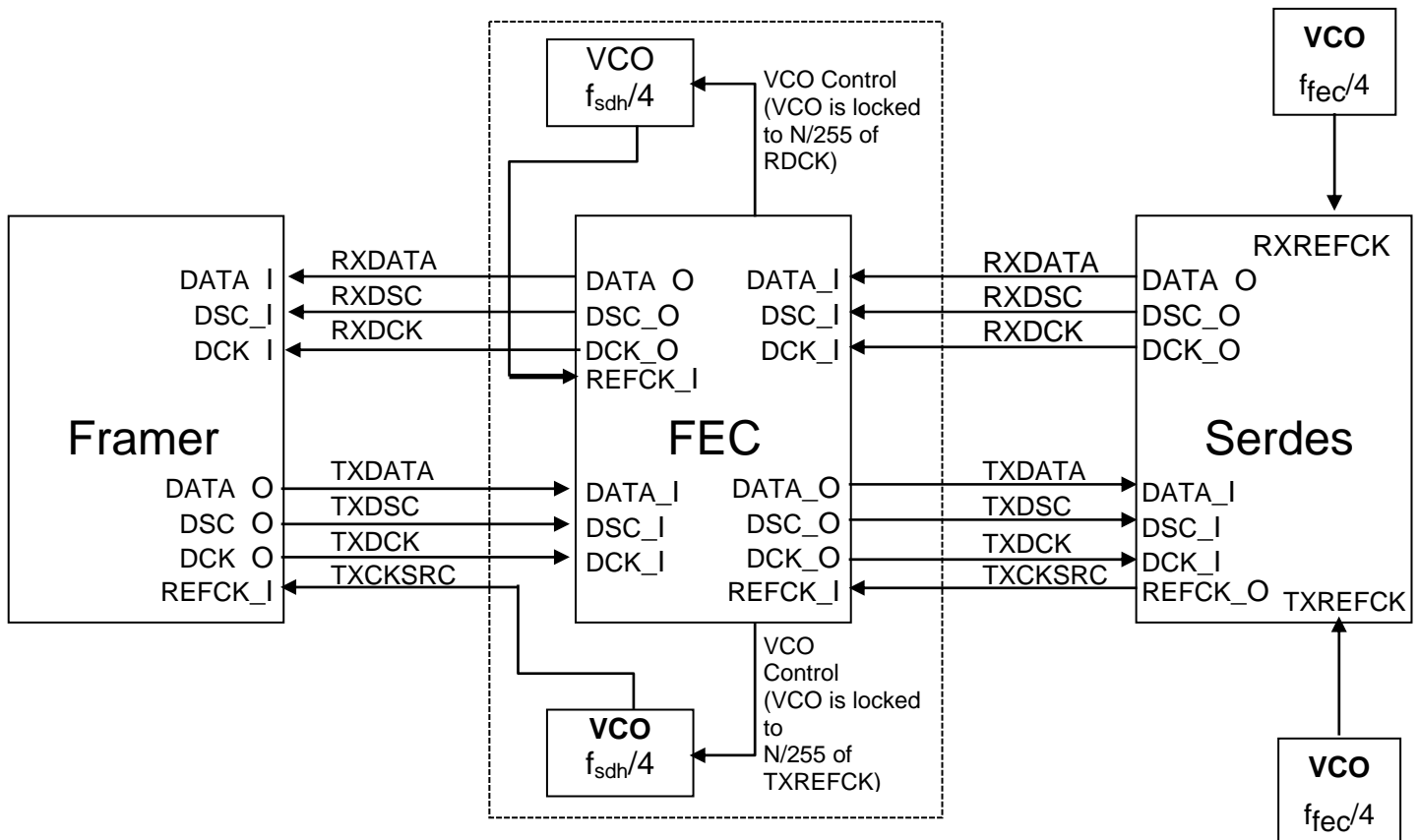
There are multiple ways to connect two sides of the SFI-5 interface together, specifically the clocking architecture. The SFI-5 interface reference model is meant to provide a guideline for this without restricting different configurations. This appendix provides example system configurations in which the reference model has been applied to show the implementation flexibility. This appendix does not restrict or dictate any specific configuration and is to be used solely as a reference.

3 Sample System Configurations

3.1 Reverse Clock Example

In this model the system sources all clocks from the Serdes. The system reference is fed into the Serdes and in the case of the receive (RX) path the reference clock is passed in the same direction as the data, where in the transmit path the reference clock is passed in the opposite direction as the data.

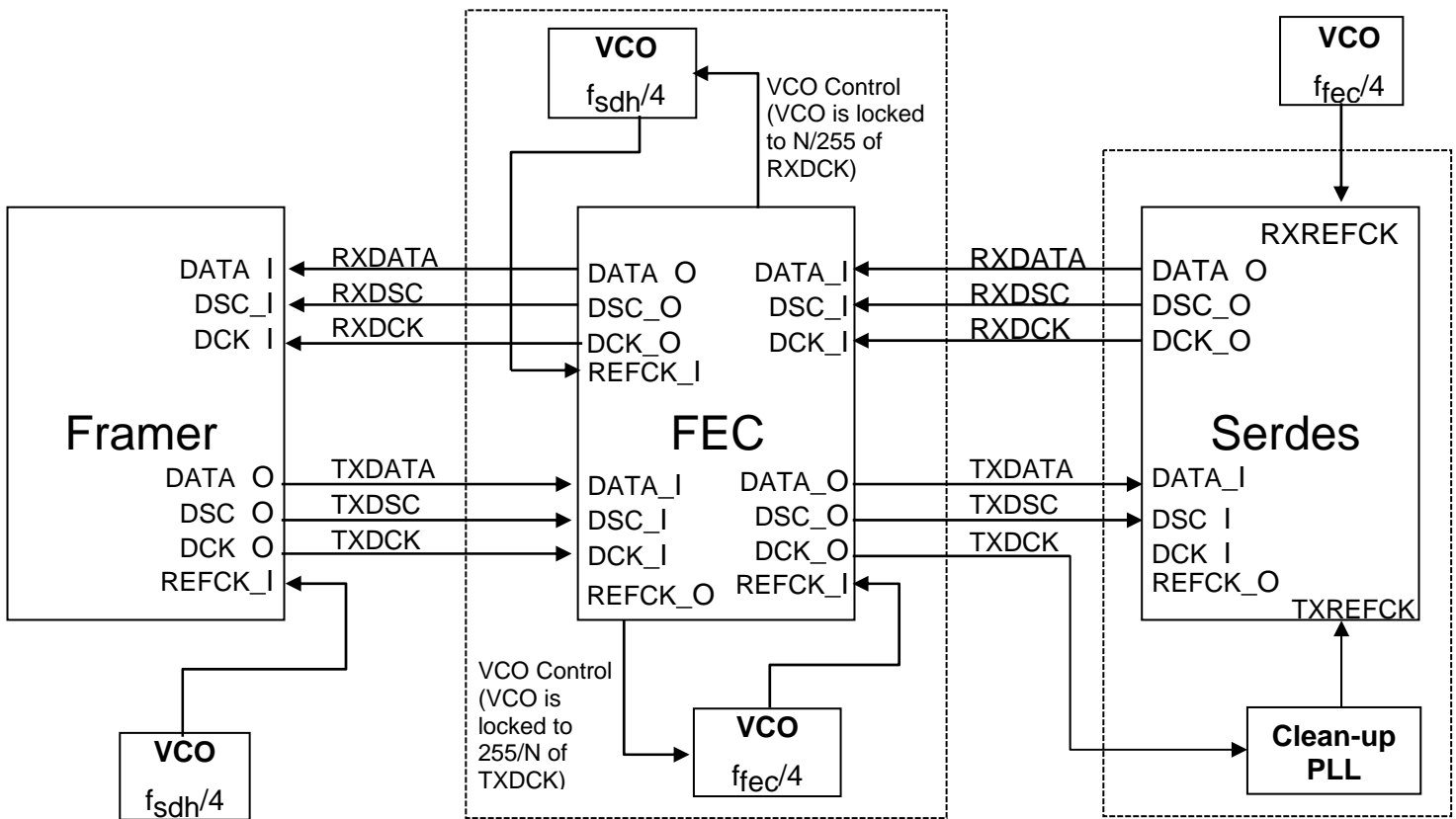
Figure A.1: Reverse Clock Reference Model



3.2 Forward Clock Example

In this model the system sources all clocks from the source of the data. This indicates that the reference clock is passed in the same direction as the data. In the case of the receive (RX) path the system reference is fed into the Serdes and is passed downstream to the FEC/Framer, where in the transmit (TX) path the reference clock is fed into the FEC/Framer and passed downstream to the Serdes.

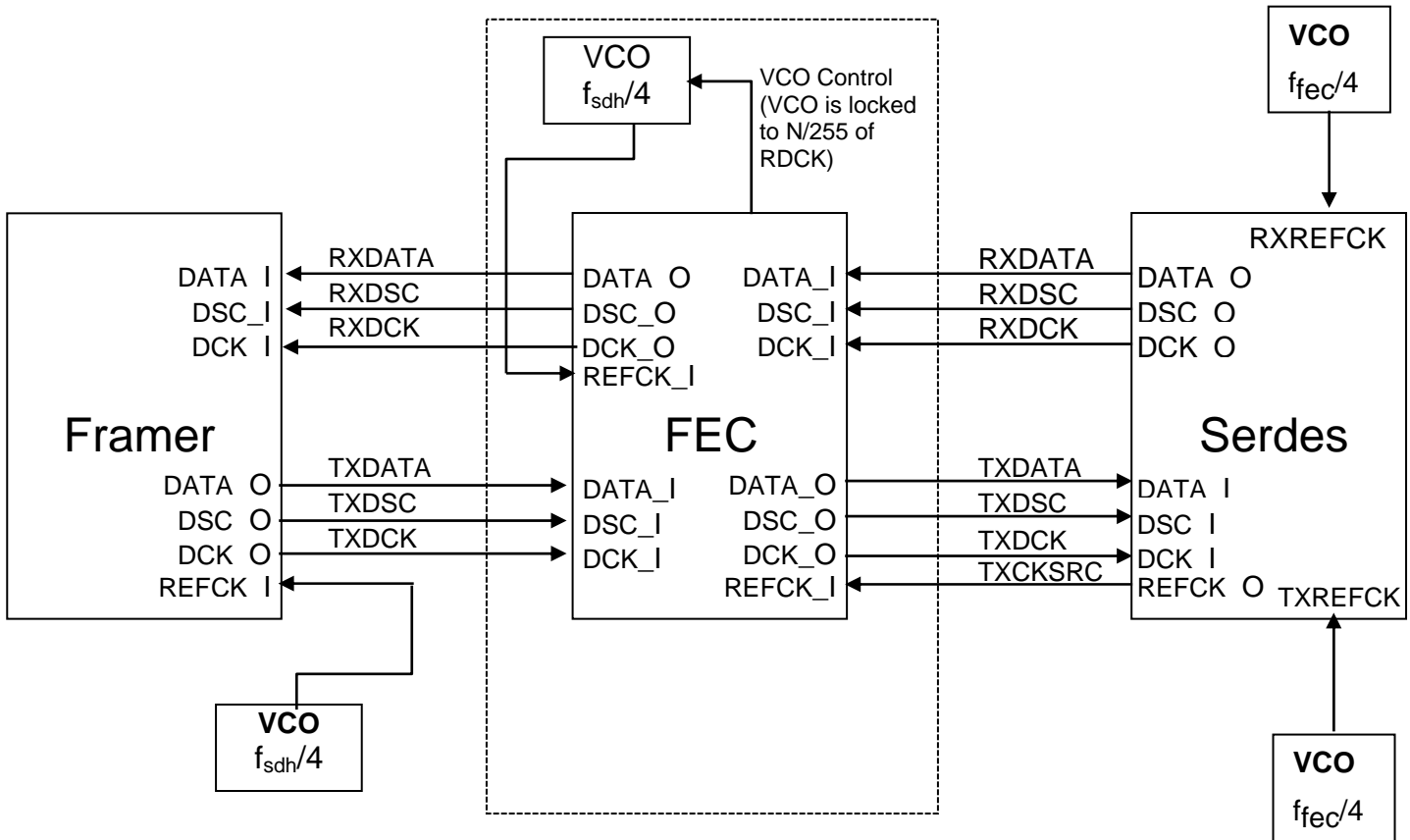
Figure A.2: Forward Clock Reference Model



3.3 Independent Reference Example

The transmit path have independent reference clocks at different frequencies to both the Framer and the Serdes. The FEC is responsible for byte stuffing to accommodate for any differences in the two reference clocks. In this case the SFI-5 interface is treated independently on either side of the FEC device. The receive path has the reference clock passed in the same direction as the data as described in the previous two examples.

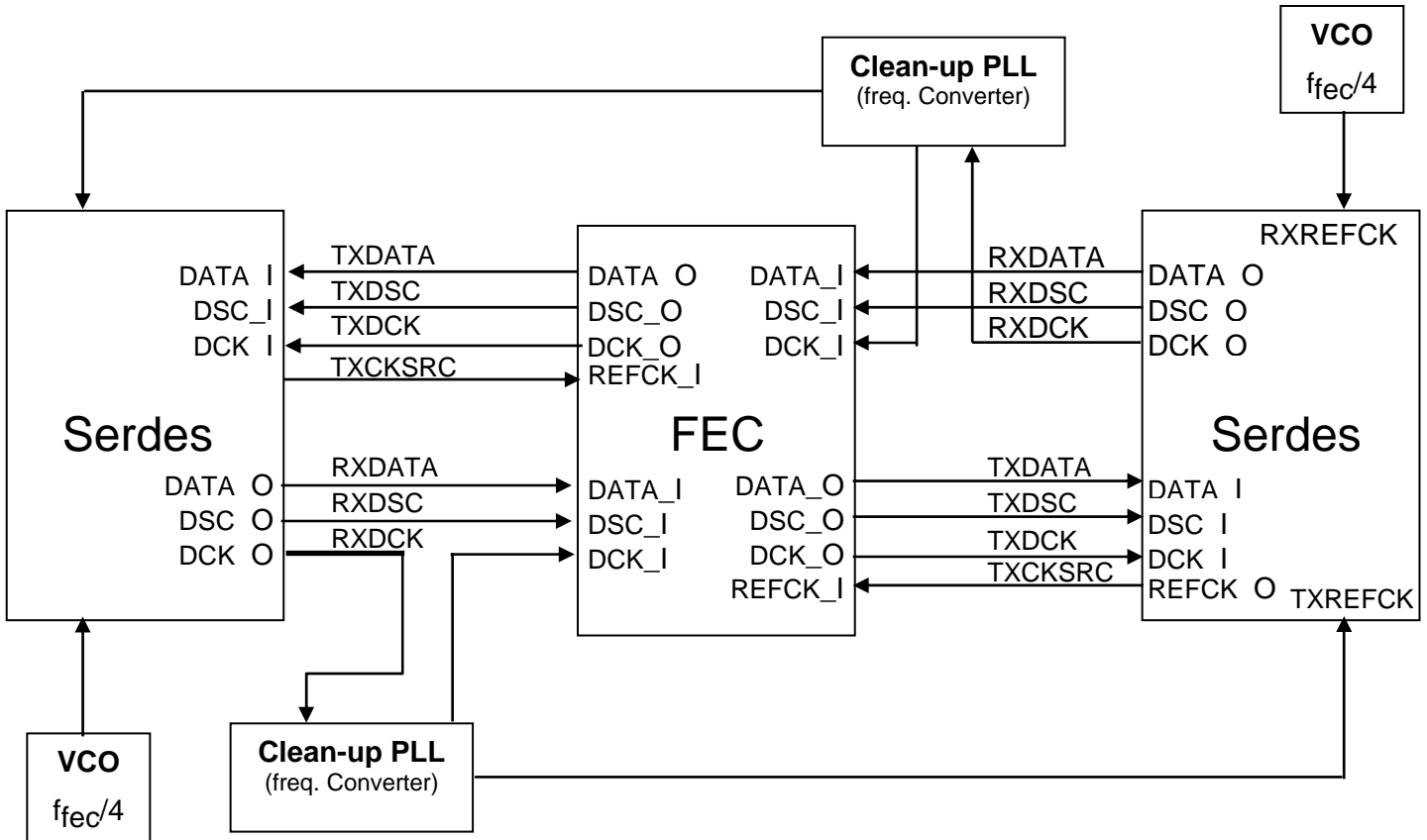
Figure A.3: Independent Reference Model



3.4 Regenerator Example

The reference clock in this configuration must be derived from the receive data. A "Clean-up PLL" is used to provide a clean reference clock to the output Serdes to achieve high quality transmission. The Clean-up PLL can be of unity gain or include a frequency converter depending on whether data is being encoded or decoded by the FEC device.

Figure A.4: Regenerator Reference Model



Appendix B "SFI-5s" Quad OC-192 Optional Mode

1 Abstract

This appendix describes an optional implementation to scalable SFI-5 as Quad OC-192 interface and referred to as "SFI-5s". The SFI-5s just like SFI-5 has an aggregate data bandwidth of OC-768, but it also allows the use of the interface for Quad OC-192.

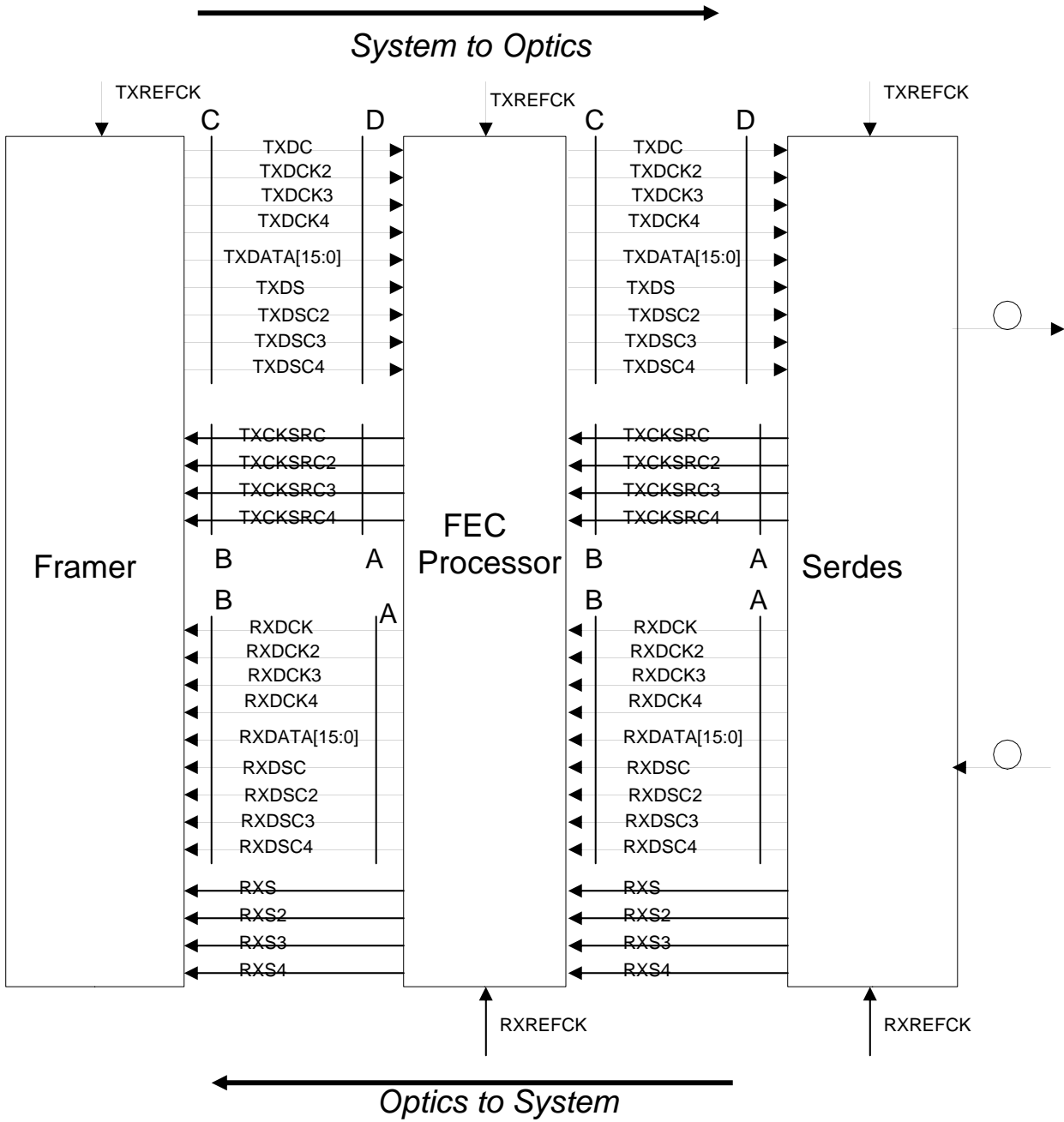
2 Introduction

SFI-5 has defined a 16 bit full duplex interface to support OC-768 with an aggregate data rate of 40-50 Gb/s. The electrical interface as defined in SFI-5 defines a 16 bit bus carrying OC-768 data traffic. The optional implementation SFI-5s redefines the 16 bit interface with granularity of 4 bits to allow support of Quad OC-192 as well OC-768 across the same interface. Quad OC-192 operation mode is achieved by breaking 16 bits SFI interface into 4 individual links each one 4 bits wide. The optional SFI-5s require 3 additional TXDSC, TXDCK, RXDSC, RXDCK. SFI-5s objective and requirements in addition to the SFI-5 are:

- 1.Supports up to 50Gb/s bi-directional point to point interface including SONET OC-768, SDH STM-256, OTN-3, or other system Operating at data rate of 40 Gb/s with up to 25% FEC overhead.
- 2.The Interface operates as a OC-768 or as Quad OC-192.
- 3.The data bytes are striped over each set of 4 wires to transfer an OC-192 frame when operating in SFI-5s mode. When the interface operates in SFI-5 mode the standard stripping as specified in SFI-5 implemented.
- 4.The SFI-5s if operated in the SFI-5 mode only a single clock and deskew channel are required.

The following is a general synopsis of the SFI Level 5s interface. For reference, a general block diagram is shown in Figure B.1. SFI Level 5s is the interface between the Serdes component, the forward-error-correction (FEC) processor, and the Framer supporting OC-768 as well as Quad OC-192 mode. Note that the two instantiations of the SFI-5s bus in Figure B.1 are independent and may operate at different frequencies.

Figure B.1: SFI-5s System Reference Model



The points A, B, C and D are the reference points as defined in the common electrical specification (OIF2001.149).

System to Optic operation of SFI-5s:

When the SFI-5s interface is operating in the 4xOC-192 mode the data may originate from a single or four framers/FEC Processors supporting 4xOC-192. The four transmit interfaces may operate from a single clock or from four independent clocks. Transmit data are designated TXDATA[15:0] carry 4xOC-192 data as the following:

Table B.1: SFI-5s Framer to Optics Data Format

Channel	Data	Clock	De-skew
1 st OC-192	TXDATA[3:0]	TXDCK	TXDSC
2 nd OC-192	TXDATA[7:4]	TXDCK2	TXDSC2
3 rd OC-192	TXDATA[11:8]	TXDCK3	TXDSC3
4 th OC192	TXDATA[15:12]	TXDCK4	TXDSC4

An SFI-5s enabled device operating in the SFI-5 mode, only uses TXDSC to transfer deskew data from system to optics.

Optics to System Interface:

When the SFI-5s interface is operating in the 4xOC-192 the data may originate from four independent optical signals. The 4 receive signals may originate from independent bit streams with slightly different frequency, within specified tolerance. The SerDes, FEC Processor, and framer may be implemented as one device supporting both OC-768 as well as 4xOC192 or as four separate devices only supporting 4xOC192. The receive data are designated RXDATA[15:0] when carrying 4xOC-192 data the format is as the following:

Table B.2 : SFI-5s Optics to Framer Data Format

Channel	Data	Clock	De-skew
1 st OC-192	RXDATA[3:0]	RXDCK	RXDSC
2 nd OC-192	RXDATA[7:4]	RXDCK2	RXDSC2
3 rd OC-192	RXDATA[11:8]	RXDCK3	RXDSC3
4 th OC-192	RXDATA[15:12]	RXDCK4	RXDSC4

An SFI-5s enabled device operating in SFI-5 mode, only uses RXDSC to transfer deskew data from optics to system.

On both the receive and transmit interfaces, control and status information is sent separately from the corresponding data path. To accommodate the expected minute frequency offsets between the data stream in the two directions, the Receive and Transmit interfaces operate independently.

3 Signal definition

3.1 Receive signals

The Receive signals are related to the transport of data from the optics towards the system. They are applicable to conducting data from the Serdes component to the FEC processor, from the FEC processor to the Framer, or from the Serdes Component directly to the Framer. All Receive signals, unless otherwise specified below, are differential CML as defined in the Common Electrical Implementation Agreement oif2001.149.

Table B.3: SFI-5s Receive Signal Summary

Signal Name	Direction	Function
RXDCK	Optics to System	The Receive Data Clock (RXDCK) is the clock associated with the first OC-192 carried on RXDATA[3:0]. If an SFI-5s interface is operating in the OC-768 mode, then RXDCK is the only clock mandatory from Optics to Framer.
RXDCK2	Optics to System	The Receive Data Clock (RXDCK2), receive clock from the second OC-192 carried on RXDATA[7:4].
RXDCK3	Optics to System	The Receive Data Clock (RXDCK3), receive clock from the second OC-192 carried on RXDATA[11:8].
RXDCK4	Optics to System	The Receive Data Clock (RXDCK4), receive clock from the forth OC-192 carried on RXDATA[15:12].
RXDATA[3:0] RXDATA[7:4] RXDATA[11:8] RXDATA[15:12]	Optics to System	For the OC-768 mode of operation please see SFI-5 section. In the SFI-5s: Serial optical data from the first channel or fiber is striped onto RXDATA[3:0] in a round-robin fashion, 8 bits at a time. Serial optical data from the second channel or fiber is striped onto RXDATA[7:4] in a round-robin fashion, 8 bits at a time. Serial optical data from the third channel or fiber is striped onto RXDATA[11:8] in a round-robin fashion, 8 bits at a time. Serial optical data from the forth channel or fiber is striped onto RXDATA[15:12] in a round-robin fashion, 8 bits at a time. RXDATA[3] contains the first 8 bits received from the

Signal Name	Direction	Function
		<p>first channel. RXDATA[2] contains the 9th to 16th bits received. RXDATA[1] contains the 17th to 24th bit received. RXDATA[0] contains the last 8 (25th to 32nd) bits received. Data from the second, third and fourth channels are similarly byte striped onto RXDATA[7:4], RXDATA[11:8] and RXDATA[15:12], respectively. Within the 8 bits of each RXDATA[x], the bits are arranged in the order they are received.</p> <p>When RXDATA's are generated by an Serdes component, the 8 bits placed on each RXDATA[x] signal are arbitrarily aligned to the octets on the receive optical data stream. When RXDATA's are generated by an FEC processor, and the data is octet aligned, the first byte is placed in RXDATA[3,7,11,or15]. The fourth byte is placed in RXDATA[0,4,8,or 12].</p> <p>Each RXDATA[X] signal is a 2.488 Gb/s to 3.125 Gb/s stream. It contains every 4th byte of the data stream.</p> <p>RXDATA is frequency locked to RXDCK with unspecified static phase offset.</p>
<p>RXDSC RXDSC2 RXDSC3 RXDSC4</p>	<p>Optics to System</p>	<p>The Receive Deskew Channel (RXDSC) signal provides reference data to enable skew measurements and to identify the 8-bit boundaries of the striping structure of the Receive data bus (RXDATA[x]), please see table B.2 for associated data bus. In OC-768 mode only RXDSC is required to operate.</p> <p>RXDSC[x] contains reference frames consisting of 4 framing bytes, 4 bytes of expansion header, and 4 sets of 8-byte samples of each signal on the Receive data bus (RXDATA[15:0]). The 64-bit samples for each channel are aligned to the 8-bit structure in the striping scheme. I.e., the first bit of the sample is the first bit of received, the 9th bit of the sample is the 33rd bit received, etc, from the associated fiber or channel.</p> <p>Samples on RXDSC is taken from the Receive data bus in a round-robin fashion, starting with RXDATA[3] and ending with RXDATA[0].</p> <p>Samples on RXDSC2 is taken from the Receive</p>

Signal Name	Direction	Function
		<p>data bus in a round-robin fashion, starting with RXDATA[7] and ending with RXDATA[4].</p> <p>Samples on RXDSC3 is taken from the Receive data bus in a round-robin fashion, starting with RXDATA[11] and ending with RXDATA[8].</p> <p>Samples on RXDSC4 is taken from the Receive data bus in a round-robin fashion, starting with RXDATA[15] and ending with RXDATA[12].</p> <p>RXDSC is a 2.488 Gb/s to 3.125 Gb/s stream.</p> <p>RXDSC is frequency locked to RXDCK with unspecified static phase offset.</p>
RXS	Optics to System	<p>The channel 1 Receive Status (RXS) signal carries status from the Serdes component to the FEC processor, from the FEC processor to the SONET/SDH framer, or from the Serdes component directly to the SONET/SDH framer for fiber or channel 1. The encoding of RXS is:</p> <p>RXS = 'b0 : Idle, RXS = 'b1 : Receive alarm,</p> <p>Receive alarm shall indicate the RXDCK and RXDATA are not derived from the optical receive signal. The electrical I/O type shall be LVCMOS. Output is required to be driven by the source; input is not required to be used.</p> <p>RXS is an asynchronous signal</p>
RXS2	Optics to System	<p>The channel 2 Receive Status (RXS2) signal carries status from the Serdes component to the FEC processor, from the FEC processor to the SONET/SDH framer, or from the Serdes component directly to the SONET/SDH framer for fiber or channel 2.</p>
RXS3	Optics to System	<p>The channel 3 Receive Status (RXS3) signal carries status from the Serdes component to the FEC processor, from the FEC processor to the SONET/SDH framer, or from the Serdes component directly to the SONET/SDH framer for fiber or channel 3.</p>

Signal Name	Direction	Function
RXS4	Optics to System	The channel 4 Receive Status (RXS4) signal carries status from the Serdes component to the FEC processor, from the FEC processor to the SONET/SDH framer, or from the Serdes component directly to the SONET/SDH framer for fiber or channel 4.
RXREFCK	Optics to System	<p>The Receive Reference Clock (RXREFCK) signal provides reference timing to the Receive interface. RXREFCK is nominally a 50% duty cycle clock with a frequency that is one quarter of the data bit rate of RXDATA and RXDSC. In the SERDES component, RXREFCK is nominally the same frequency as RXDCK. In the FEC processor, RXREFCK is the frequency reference to the source of RXDATA, RXDCK, RXDSC. Jitter characteristics of RXREFCK do not directly concern interoperability and are beyond the scope of this implementation agreement.</p> <p>Implementation of RXREFCK is mandatory for a Serdes and FEC component, and not necessary for a Framer component. In some implementations, RXREFCK could share a common pin with TXREFCK.</p>

3.2 Transmit signals

The Transmit signals are related to the transport of data from the system towards the optics. They are applicable to conducting data from the Framer to the FEC processor, from the FEC processor to the Serdes Component, or from the Framer directly to the Serdes component. All Transmit signals, unless otherwise specified below, are differential CML as defined in the Common Electrical Implementation Agreement oif2001.149.

Table B.4 : SFI-5s Transmit Signal Summary

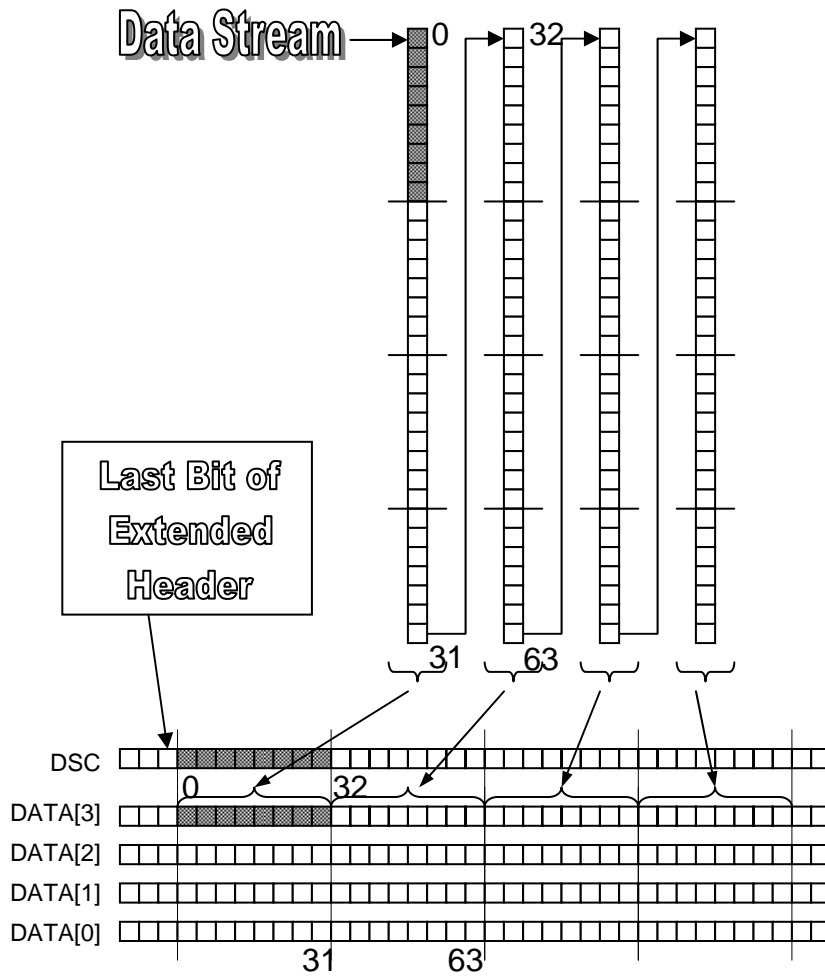
Signal Name	Direction	Function
TXDCK	Optics to System	<p>The Transmit Data Clock (TXDCK) is the clock associated with the first OC-192 carried on TXDATA[3:0]. If an SFI-5s interface is operating in the OC-768 mode, then TXDCK is the only clock from Framer to Optics.</p> <p>It is mandatory for the source device of the Transmit interface to generate TXDCK. It is optional for the sink device in the Transmit interface to use TXDCK. Generation of this clock shall have the capability to be disabled.</p>
TXDCK2	Optics to System	The Transmit Data Clock (TXDCK2), receive clock from the second OC-192 carried on TXDATA[7:4].
TXDCK3	Optics to System	The Transmit Data Clock (TXDCK3), receive clock from the second OC-192 carried on TXDATA[11:8].
TXDCK4	Optics to System	The Transmit Data Clock (TXDCK4), receive clock from the forth OC-192 carried on TXDATA[15:12].
TXCKSRC	Optics to System	<p>The Transmit Clock Source(TXCKSRC) signal provides timing reference for the Transmit data path signals (TXDATA[3:0], TXDSC, TXDCK).</p> <p>TXCKSRC is nominally a 50% duty cycle clock with a frequency that is one-quarter of the data bit rate of TXDATA and TXDSC. TXCKSRC is derived from TXREFCK in the sink device.</p> <p>It is mandatory for the source device in the transmit interface to be able to receive TXCKSRC into the TXREFCK and to use this input as a frequency reference for TXDCK, TXDSC, and TXDATA. It is optional for a sink device in the transmit interface to generate a TXCKSRC output. If the sink device does not drive the TXCKSRC output, then the source device uses an external clock source TXREFCK as the frequency reference for TXDCK, TXDSC, and TXDATA, and the sink device must</p>

Signal Name	Direction	Function
		accept data at the resulting frequency. Note: Although defined as separate functions by the reference model, this signal description allows an implementation to use a single device pin on the source device as a common TXCKSRC or TXREFCK input.
TXCKSRC2	Optics to System	The Transmit Clock Source (TXCKSRC2) signal provides timing reference for the Transmit data path signals (TXDATA[7:4], TXDSC2, TXDCK2). The function and characteristics of TXCKSRC2 is identical to that of TXCKSRC but is associated with fiber or channel 2.
TXCKSRC3	Optics to System	The Transmit Clock Source (TXCKSRC3) signal provides timing reference for the Transmit data path signals (TXDATA[11:8], TXDSC3, TXDCK3). The function and characteristics of TXCKSRC3 is identical to that of TXCKSRC but is associated with fiber or channel 3.
TXCKSRC4	Optics to System	The Transmit Clock Source (TXCKSRC4) signal provides timing reference for the Transmit data path signals (TXDATA[15:12], TXDSC4, TXDCK4). The function and characteristics of TXCKSRC4 is identical to that of TXCKSRC but is associated with fiber or channel 4.
TXDATA[15:0]	System to Optical	For the OC-768 mode of please see SFI-5 section. In the SFI-5s: Serial data TXDATA[3:0] from Framer or FEC is striped onto first channel or fiber in a round-robin fashion, 8 bits at a time. Serial data TXDATA[7:4] from Framer or FEC is striped onto second channel or fiber in a round-robin fashion, 8 bits at a time. Serial data TXDATA[11:8] from Framer or FEC is striped onto third channel or fiber in a round-robin fashion, 8 bits at a time. Serial data TXDATA[15:12] from Framer or FEC is striped onto forth channel or fiber in a round-robin fashion, 8 bits at a time. TXDATA[3,7,11,15] contains the byte and transmitted first while TXDATA[0,4,8,12] are the fourth byte and gets transmitted last. Within the 8 bits of each TXDATA[x], the bits are arranged in the

Signal Name	Direction	Function
		<p>order they are transmitted.</p> <p>Each TXDATA[X] signal is a 2.488 Gb/s to 3.125 Gb/s stream. It contains every 4th byte of the data stream.</p> <p>TXDATA's are frequency locked to TXDCK's with unspecified static phase offset as specified in table 5.1.</p>
<p>TXDSC TXDSC2 TXDSC3 TXDSC4</p>	<p>System to Optics</p>	<p>The Transmit Deskew Channel (TXDSC) signals provide reference data to enable skew measurements and to identify the 8-bit boundaries of the striping structure of the Transmit data bus (TXDATA[x]), please see table B.1 for associated data bus. In OC-768 mode only TXDSC is required to operate.</p> <p>TXDSC[x] contains reference frames consisting of 4 framing bytes, 4 bytes of expansion header, and 4 sets of 8-byte samples of each signal on the Transmit data bus (TXDATA[15:0]). The 64-bit samples for each channel are aligned to the 8-bit structure in the striping scheme. I.e., the first bit of the sample is the first bit transmitted, the 9th bit of the sample is the 33rd bit transmitted, etc, on the associated fiber or channel.</p> <p>Samples on TXDSC is taken from the Transmit data bus in a round-robin fashion, starting with TXDATA[3] and ending with TXDATA[0].</p> <p>Samples on TXDSC2 is taken from the Transmit data bus in a round-robin fashion, starting with TXDATA[7] and ending with TXDATA[4].</p> <p>Samples on TXDSC3 is taken from the Transmit data bus in a round-robin fashion, starting with TXDATA[11] and ending with TXDATA[8].</p> <p>Samples on TXDSC4 is taken from the Transmit data bus in a round-robin fashion, starting with TXDATA[15] and ending with TXDATA[12].</p> <p>TXDSC is a 2.488 Gb/s to 3.125 Gb/s stream.</p> <p>TXDSC is frequency locked to TXDCK with unspecified static phase offset. Please see Table 5.2.</p>

Signal Name	Direction	Function
TXREFCK	System to Optics	<p>The Transmit Reference Clock (TXREFCK) signal provides reference timing to the clock synthesis unit that drives the Transmit interface.</p> <p>TXREFCK is nominally a 50% duty cycle clock with a frequency that is one quarter of the data bit rate of TXDATA and TXDSC. It is the same frequency as TXDCK. Jitter characteristics of TXREFCK do not directly concern interoperability and are beyond the scope of this implementation agreement.</p>

Figure B.2: Alignment of byte striping with DSC samples to allow proper reconstruction.

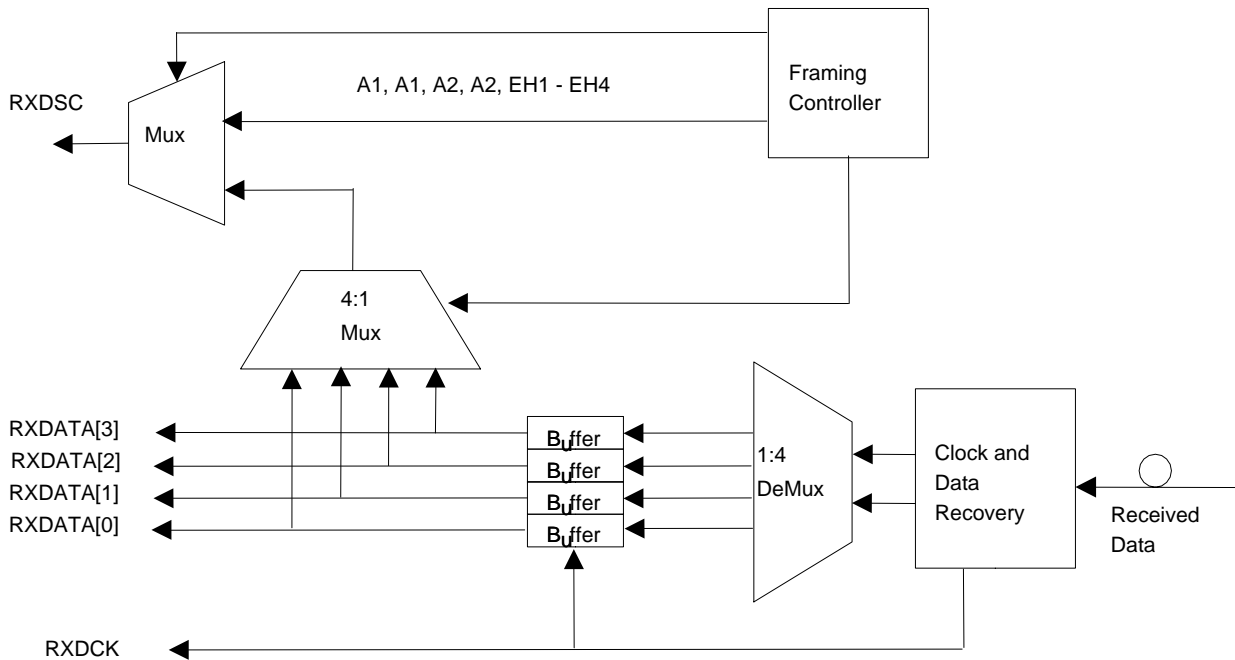


4 Logical Reference Models

4.1 Serdes component Receive interface

Figure B.3 below shows a logical model of the Receive data interface for the first channel or fiber in an Serdes component. Please see Table B.2 for data propagation of channel 2, 3, and 4. The intent is to show the source of data in the Receive Deskew Channel (RXDSC). No limit is placed on device implementation, and this model is not intended to represent an actual design.

Figure B.3: Model of Serdes component - Receive I/F Source



The data in the optical stream from each fiber is striped across the 4 bit lanes of the Receive Data bus (RXDATA[x]) in a round-robin fashion. The first bit received from fiber ONE is written into the re-timing buffer associated with RXDATA[15] and the last bit into that associated with RXDATA[12]. Similarly other three channel written per Table A.2. The re-timing buffers act as a set of FIFOs to bridge between the optical timing domain and the Receive interface timing domain. Wander between the bit lanes is absorbed by the re-timing buffers.

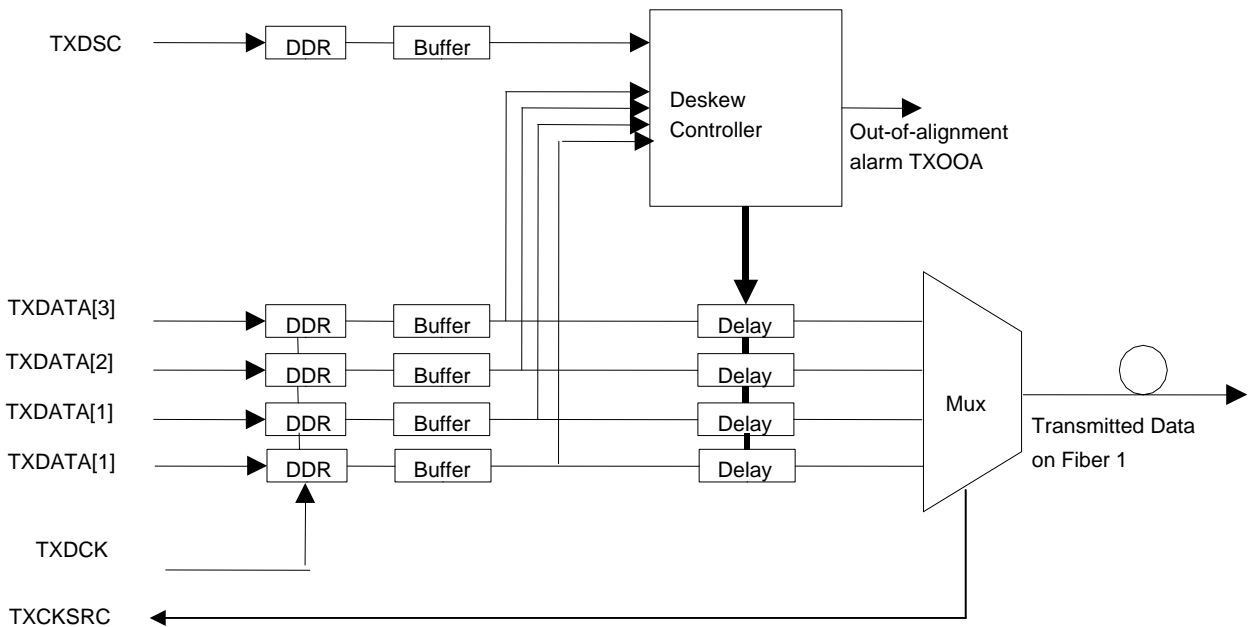
RXDCS replicates the data sent on each signal of the Receive Data bus RXDATA[15:0] cyclically. The framing pattern generator is chosen first to insert the framing pattern of two A1 (F6 Hex) and two A2 (28 hex) bytes and 4

bytes of expansion header (EH1 to EH4 are each currently set to 1010 1010 pattern when unused). Then, each RXDATA[X] signal is sampled, in turn, for 64 bit times (8 bytes). Reporting begins with RXDATA[3] and ends with RXDATA[0]. Similarly RXDCS2 reporting begins with RXDATA[7] ends with RXDATA[4], RXDCS3 reporting begins with RXDATA[11] ends with RXDATA[8], RXDCS4 reporting begins with RXDATA[15] ends with RXDATA[12]. After all the data lanes have been sent, a new reference frame is initiated on all RXDSC's and then continuously generated.

4.2 Serdes Component Transmit interface

Figure B.4 below shows a logical model of the Transmit interface for one out of 4 fiber in an Serdes Component, please see Table B.1. The intent is to show operation of the Deskew algorithm, controlled by the Deskew Channel (TXDSC). No limit is placed on device implementation, and this model is not intended to represent an actual design.

Figure B.4 : Model of Serdes component - Transmit I/F Sink



Data

on each of the 4 Transmit Data bus TXDATA's and TXDSC's are conditioned by the data recovery units (DDR) which tracks the center of the "eye" at each bit period. Data from each bit lane is written into an associated re-timing buffer. Data from the re-timing buffer associated with TXDATA[3,7,11, and 15] are transmitted respectively on fiber one, two,

three, and four. The re-timing buffers act as a set of FIFOs to bridge between the Transmit interface timing domain and the optical stream timing domain. Wander between the bit lanes is absorbed by the re-timing buffers.

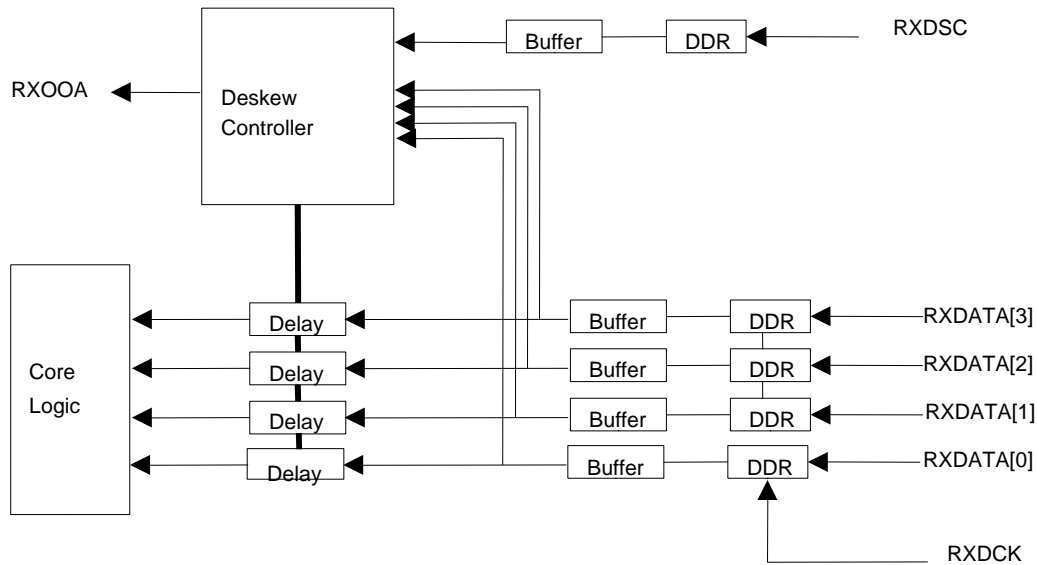
The function of the Deskew Controller block is to recognize the framing bytes and header bytes in each of the Deskew Channel TXDSC's, to identify the start of the reference data which is replicated from each of TXDATA[X]. Each of the TXDATA[X] channels is then compared with the sampled data in the Deskew Channel in turn. The Deskew Controller performs a pattern match between the replicated data in a TXDSC's with the original data in the corresponding TXDATA[X] signal. Where there is a match, the relative delay of TXDATA[x], in relation to TXDSC's, is found. It is possible to measure how many bit periods of skew there are on each channel. This information is used to compensate for the skew by adjusting the delay elements specific to each channel.

The out-of-alignment alarm TXOOA1 is set if a any of the 4 channel data does not match associated TXDSC's. When a data match has been found on set of 4 channel each 4 bit wide, then the Deskew algorithm is considered as locked, and the TXOOA is cleared. Skew measurements are monitored continuously, and the TXOOA alarm remains cleared as long as consistent skew data is generated. It is possible to operate SFI-5s even if one, two, or three channel are non operating assuming optical transceiver functions.

The function of the Deskew Controller is to continuously compare data on the Deskew Channel TXDSC's with the respective Data Channels TXDATA's. Any mis-match errors can be detected, which would represent errors generated over the SFI-5 interface. These errors should be reported as part of the minimum test requirements for the interface.

4.3 Receive Interface of FEC Processor / Framer

Figure B.5 below shows a model of the Receive interface in the FEC processor or in the Framer. The intent is to show operation of the Deskew algorithm for channel 1, controlled by the Receive Deskew Channel RXDSC. For operation of channel 2, 3, and 4 please see Table B.2. No limit is placed on device implementation, and this model is not intended to represent an actual design.

Figure B.5 : Model of FEC Processor / SONET Framer - Receive I/F Sink

The DDR blocks track the center of the "eye" of the Receive Data bus RXDATA's and the Receive Deskew Channel RXDSC's signal. The re-timing buffers bridge between the Receive interface timing domain and the system timing domain. Wander between the bit lanes is absorbed by the re-timing buffers.

The function of the Deskew Controller block is to recognize the framing bytes and header bytes in the for each of the Receive Deskew Channel RXDSC's. These identify the start of the reference data which is replicated from each of RXDATA's. Each 4 bit RXDATA's channels is then compared with the sampled data in the Deskew Channel in turn according to table A.1.

The Out-of-alignment alarm (RXOOA) is set if a match has not been found on any of the 4 data channels. When a data match has been found on all 4 data channels and stable skew data derived, then the De-skew algorithm is considered as locked and RXOOA is cleared. Skew measurements are monitored continuously, RXOOA alarm remains cleared as consistent skew data is generated. Channel 2, 3, and 4 each have their associated out-of-alignment alarm respectively RXOOA2, RXOOA3, and RXOOA4.

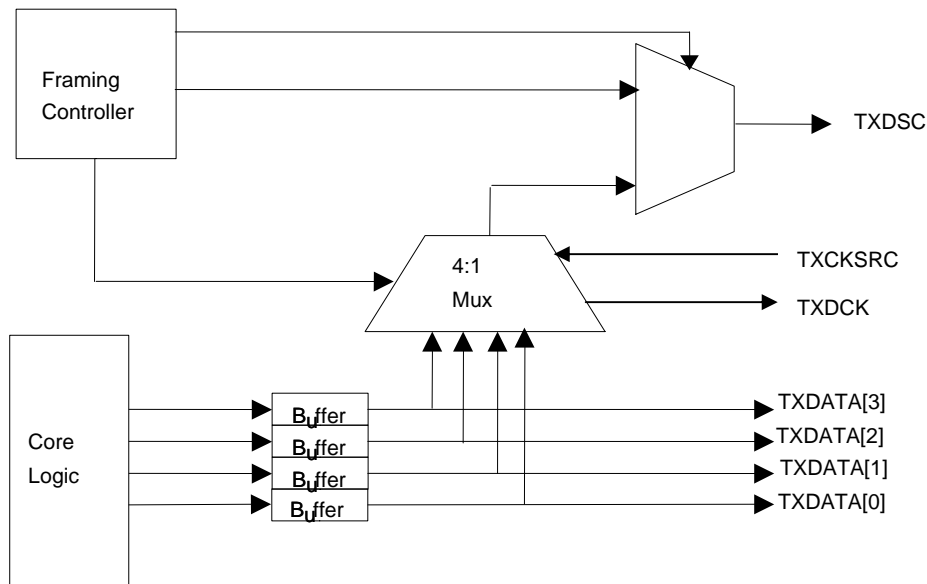
The function of the Deskew Controller is to continuously compare data on the Deskew Channel RXDSC with the respective Data Channels RXDATA[3:0] and similarly for RXDSC2, RXDSC3, and RXDSC4 according to Table A.2. Any mis-match errors can be detected, which would represent errors

generated over the SFI-5s interface. These errors should be reported as part of the minimum test requirements for the interface.

4.4 Transmit interface in FEC Processor / Framer

Figure B.6 below shows a model of the Transmit interface showing first channel in the FEC processor or in the SONET/SDH framer. The intent is to show the source of data in the Transmit Deskew Channel. No limit is placed on device implementation, and this model is not intended to define an actual design.

Figure B.6 : Model of FEC Processor / SONET Framer - Transmit I/F Source



Data from the core logic of the FEC Processor or Framer is striped across the 4 bit lanes of the first Transmit Data bus TXDATA[3:0] channel in a round-robin fashion. For channel 2, 3, and 4 operation please see table 1. The first bit received is written into the re-timing buffer associated with TXDATA[3] and the last into that associated with TXDATA[0]. The re-timing buffers act as a set of FIFOs to bridge between the core logic timing domain and the Transmit interface timing domain.

TXDCS replicates the data sent on each signal of the Transmit Data bus TXDATA[3:0] cyclically. For operation of TXDCS2, TXDCS3, and TXDCS 4 please see Table A.1. The framing pattern generator is chosen first to insert the framing pattern of two A1 (F6 Hex) and two A2 (28 hex) bytes and 4 bytes of expansion header (EH1 to EH4 are each currently set to 1010 1010 pattern

when unused). Then, each TXDATA[3,2,1,0] signal is sampled, in turn, for 64 bit times (8 bytes). Reporting begins with TXDATA[3] and ends with TXDATA[0]. After all the data lanes have been sent, a new reference frame is initiated on RXDSC and then continuously generated. Similarly data from channel two, three, and four are sampled and sent respectively on RXDSC2, RXDSC3, and RXDSC4.

5 SFI-5s Bit-lane Deskew

The Data signals may encounter different delays in transit from the SFI-5s source device to the sink device. The maximum differential skew introduced by the connection system is specified in the Common Electrical Implementation Agreement. The earliest arriving signal may lead the latest arriving by n bits. Relative to the earliest, each of the remaining signals is coincident, or is up to n unit intervals late. The search space for determining the relative delays of 5 signals on SFI-5s is $(n+1)^5$ combinations. To make the problem tractable, a reference signal is used in SFI-5, known as the Deskew Channel, to allow each bit-lane to independently measure its own delay relative to the reference signal. Having de-coupling the measurement to individual signals, the search space becomes trivially small.

The bit-lane Deskew function is shared between the SFI-5s source and sink devices at either end of the Receive and Transmit interfaces. In the source device, data is sampled from each of the 4 data channels sequentially, and copied onto the Deskew Channel. The Deskew Channel is then sent with the 4 data channels to the sink device over the SFI-5s interface.

Data input to the sink device, will be skewed by the different delays in each of the data channels. It is the function of the Deskew algorithm operating in the sink device to measure the amount of skew on each data channel, and then to use this skew information to compensate for the amount of skew. The bit lane Deskew algorithm will make an initial skew measurement on initial power up or connection. Subsequent to skew measurement, external conditions may vary causing the skews to change. It is a requirement that devices that are compliant to this implementation agreement be able to track skew changes of the minimum value to the maximum value without introducing errors. The Deskew algorithm will operate continuously during normal operation of the SFI-5s interface, and continuously track skew.

Table B.5 shows a reference frame on the Receive Deskew Channel (RXDSC) or the Transmit Deskew Channel (TXDSC) for channel 1. Similarly channel 1, 2, and 3 operates respectively with RXDSC2/TXDSC2, RXDSC3/RXDSC3, and RXDSC4/TXDSC4. Each reference frame is delimited by 4 framing bytes consisting of two A1 bytes (F6 hex) and two A2 bytes (28 hex). The use of the expansion header bytes is for further study. The 4 sets of data sample bytes are copied from each Receive Data bus RXDATA's or the Transmit Data bus TXDATA's starting with bit

TXDATA/RXDATA[3, 7, 11, and 15] and ending with bit RXDATA/TXDATA[0,4,8,and 12]. In Table B.5, transmission is from left to right and top to bottom.

Table B.5 : Reference Frame on RXDSC or TXDSC

Bit time	Value	Value	Value	Value	Comments
1 – 32	A1 1111 0110	A1 1111 0110	A2 0010 1000	A2 0010 1000	Framing bytes
33 – 64	EH1 1010 1010	EH2 1010 1010	EH3 1010 1010	EH4 1010 1010	Expansion Header bytes For future use
65 – 96	R/TXDATA[3] Bits 1 - 8	R/TXDATA[3] Bits 9 - 16	R/TXDATA[3] Bits 17 - 24	R/TXDATA[3] Bits 25 - 32	64 consecutive bits from RXDATA[3] or TXDATA[3]
97 - 128	R/TXDATA[3] Bits 33 - 48	R/TXDATA[3] Bits 41 - 48	R/TXDATA[3] Bits 49 - 56	R/TXDATA[3] Bits 57 - 64	
129 - 160	R/TXDATA[2] Bits 1 - 8	R/TXDATA[2] Bits 9 - 16	R/TXDATA[2] Bits 17 - 24	R/TXDATA[2] Bits 25 - 32	64 consecutive bits from RXDATA[2] or TXDATA[2]
161 - 192	R/TXDATA[2] Bits 33 - 48	R/TXDATA[2] Bits 41 - 48	R/TXDATA[2] Bits 49 - 56	R/TXDATA[2] Bits 57 - 64	
193 - 256					64 consecutive bits from RXDATA[1] or TXDATA[1]
257 - 288	R/TXDATA[0] Bits 1 - 8	R/TXDATA[0] Bits 9 - 16	R/TXDATA[0] Bits 17 - 24	R/TXDATA[0] Bits 25 - 32	64 consecutive bits from RXDATA[0] or TXDATA[0]
289 - 320	R/TXDATA[0] Bits 33 - 48	R/TXDATA[0] Bits 41 - 48	R/TXDATA[0] Bits 49 - 56	R/TXDATA[0] Bits 57 - 64	

Note: The expansion header bytes EH1-4 must not be allowed to contain the A1/A2 framing bytes.

5.1 Deskew of Receive interface

At the receive interface, a reference frame is generated in the source device, consisting of 4 framing bytes, 4 bytes of expansion header and 32 bytes of data samples. The framing pattern is two A1 bytes (F6 hex) followed by two A2 bytes (28 hex). The data samples are taken from the each of the Receive data bus RXDATA's in 8-byte sets as defined in Table B.5, starting with RXDATA[3,7,11,15] and ending with RXDATA[0,4,8,12] per Table B.5 configuration. Reference frames are sent continuously over the receive interface to enable the Deskew algorithm in the sink device and continuous monitoring of skew.

RXOOA alarm monitor de-skew out-of-alignment of the first channel, similarly RXOOA2, RXOOA3, and RXOO4 respectively reports on channel 2, 3, and 4.

The sink device monitors the Receive Deskew Channel (RXDSC, RXDSC2, RXDSC3, and RXDSC4) for the reference data. It shall adjust the delay of each RXDATA's on a unit interval by unit interval basis, such that the delay from source device to the output of the re-timing buffers at the sink device is identical for all data signals. When the skew of all data channels is compensated and locked, the RXOOA's alarms are cleared. The Deskew algorithm will continue to operate after the RXOOA's are removed. Under normal circumstances, the interface will operate continuously with skew being monitored, and the RXOOA's alarm remains off. If failure of the Deskew algorithm occurs, and any of the data channels fall out of lock, then one or more RXOOA's alarm will be set.

5.2 Deskew of Transmit interface

At the Transmit interface, a reference frame is generated in the source device, consisting of 4 framing bytes, 4 bytes of expansion header and 32 bytes of data samples. The framing pattern is two A1 bytes (F6 hex) followed by two A2 bytes (28 hex). The data samples are taken from the Transmit data bus TXDATA, TXDATA2, TXDATA3, TXDATA4 in 8-byte sets, respectively starting with TXDATA[3], TXDATA[7], TXDATA[11], TXDATA[15] and ending with TXDATA[0], TXDATA[4], TXDATA[8], and TXDATA[12].

TXOOA alarm monitor de-skew out-of-alignment of the first channel, similarly TXOOA2, TXOOA3, and TXOO4 respectively reports on channel 2, 3, and 4.

The sink device monitors the Transmit Deskew Channel (TXDSC, TXDSC2, TXDSC3, and TXDSC4) for the reference data. It shall adjust the delay of each TXDATA's on a unit interval by unit interval basis, such that the delay from source device to the output of the re-timing buffers at the sink device is identical for all data signals. When the skew of all data channels is compensated and locked, the TXOOA's alarms are cleared. The Deskew algorithm will continue to operate after the TXOOA's are removed. Under normal circumstances, the interface will operate continuously with skew being monitored, and the TXOOA's alarm remains off. If failure of the Deskew algorithm occurs, and any of the data channels fall out of lock, then one or more TXOOA's alarm will be set.

Appendix C: OIF Companies at Time of Ballot Period:

Accelerant Networks	LSI Logic
Accelight Networks	Lucent
Acorn Networks	Lumentis
Actel	LuxN
Acterna	LYNX - Photonic Networks
ADC Telecommunications	Mahi Networks
Aeluros	Maple Optical Systems
Aerie Networks	Marconi Communications
Agilent Technologies	MathStar
Agility Communications	Maxim Integrated Products
Alcatel	Memlink
Alidian Networks	Meriton
All Optical Networks, Inc.	Metro-OptiX
Allegro Networks	MindTree Consulting Pvt. Ltd
Alphion	Mintera
Altamar Networks	Mitsubishi Electric Corporation

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Altera	Movaz Networks, Inc.
Alvesta Corporation	Multilink Technology Corporation
AMCC	Multiplex
America Online	MultiWave Networks
Ample Communications	Myrica Networks
ANDO Corporation	Mysticom
Anritsu	National Semiconductor
Appian Communications	Nayna Networks
Applied Innovation	NEC
Applied Optoelectronics	Net Brahma Technologies
Aralight	Network Associates
AT&T	Network Elements
Atoga Systems	Network Photonics
Atrica Inc.	New Focus
Avici Systems	NIST
Axiowave Networks	Nokia
Bandwidth9	Nortel Networks
Bay Microsystems	NTT Corporation
BellSouth Telecommunications	NurLogic Design
Big Bear Networks	Octillion Communications
Bit Blitz Communications	OKI Electric Industry
Bitmath	ONI Systems
Blaze Network Products	OpNext
Blue Sky Research	Ophos
Bookham Technology	Optical Datacom
BrightLink Networks	Optical Switch
Broadcom	Optillion
BT	Optium

Implementation Agreement OIF-SFI5-01.0

C Speed Corp.	Optivera
Cable & Wireless	Optix Networks
Calient Networks	Optobahn
Calix Networks	OptronX
Caspian Networks	PacketLight Networks
Catamaran Communications	Paracer
Celion Networks	Parama Networks
Cenix	Paxonet Communications
Centellax	Peregrine Semiconductor
Centerpoint Broadband Technologies	Perihelion Associates
Centillium Communications	Peta Switch Solutions
Ceyba	Philips Semiconductors
Chiaro Networks	Photonami, Inc.
Chunghwa Telecom Labs	PhotonEx
Cielo Communications	Photuris, Inc.
Ciena Communications	Phyworks
CIR	Picarro
Cisco Systems	PicoLight
CIVCOM	Pine Photonics Communications
Clearwater Networks	Pluris
Coherent Telecom	PMC Sierra
Computer & Communications Research Labs	Polaris Networks, Inc.
Conexant	Power X Networks
Continuum Networks	Princeton Optronics
CoreOptics	Procket Networks
Coriolis Networks	QOptics
Corning Incorporated	Quake Technologies
Corona Optical Systems	Qwest Communications

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Cortina Systems	Radiant Photonics, Inc.
Corvis Corporation	Raza Foundries
CPlane	Redback Networks
Crescent Networks	RedClover Networks
CyOptics	RF Micro Devices
Cypress Semiconductor	RHK
Data Connection	Riverstone Networks
Department of Defense	Sandia National Laboratories
Derivelt	Santec Corporation
Dorsal Networks	Santel Networks
Dowslake Microsystems	Santur
E2O Communications	Siemens
Efficient Channel Coding	Sierra Monolithics
Elisa Communications	Silicon Access Networks
Emcore	Silicon Bridge
Emperative	Silicon Labs
Entridia	Silicon Logic Engineering
Equant Telecommunications SA	SiPackets, Inc.
Ericsson	Solidum
ETRI	Sorrento Networks
Extreme Networks	Sparkolor
EZChip Technologies	Spirent Communications
Fiberhome Telecommunications	Sprint
Fiberspace	StrataLight Communications
Finisar Corporation	Stratos Lightwave
FirstWave Intelligent Optical Networks	Sumitomo Electric Industries
Flextronics Semiconductor	Sun Microsystems
Force 10 Networks	Sycamore Networks

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Foundry Networks	Syntera Communications
France Telecom	Tality
Free Electron Technology	TDK Semiconductor
Fujikura	Tektronix
Fujitsu	Telcordia Technologies
Furukawa Electric Technologies	Tellabs
Galazar Networks	Tellium
Gazillion Bits	TelOptica
GDA Technologies	Tenor Networks
Gemfire	TeraBeam Networks
General Dynamics	TeraBurst Networks
Gennum Corporation	TeraConnect
Genoa	Teradiant Networks, Inc.
Geyser Networks	Terago Communications
GigaTera	Texas Instruments
Glimmerglass Networks	TILAB S.p.A.
Global Crossing North American Networks	T-Networks, Inc.
Greenfield Networks	Toshiba Corporation
Gtran	Transparent Networks
GWS Photonics	Transpectrum
Harris Corporation	Transwitch Corporation
Harting Electro-Optics GmbH	Trellis Photonics
Helic S.A.	TriCN Associates, LLC
Helix AG	TriQuint Semiconductor
Hi/fn	Tropic Networks Inc.
Hitachi	TSRI
Honeywell	T-Systems Nova
Huawei Technologies	Turin Networks

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Hyperchip	TyCom
IBM Corporation	US Conec
Ignis Optics	Valiant Networks
Infineon Technologies	Velio Communications
Infinera	Velocium (TRW)
Innovance Networks	Verizon
Inphi	VIPswitch
Integrated Device Technology	Vitesse Semiconductor
Intel	Vivace Networks
Internet Machines	VSK Photonics
Internet Photonics	W.L. Gore & Associates
Interoute Telecom	Wavium AB
Intune Technologies, Ltd.	West Bay Semiconductor
Iolon	White Rock Networks
Japan Telecom	Williams Communications
JDS Uniphase	WorldCom
Jedai Broadband Networks	Xanoptix
Jennic	Xelerated
Juniper Networks	Xignal Technologies
KDDI R&D Laboratories	Xilinx
KereniX	Xindium
Kestrel Solutions	Xlight Photonics
Kirana Networks	Yotta Networks
Kodeos Communications	Zagros Networks
KPNQwest	Zarlink Semiconductor
KT Corp.	ZettaCom
Lambda Crossing	
Laurel Networks	

Implementation Agreement OIF-SFI5-01.0

Lightbit Corporation	
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