System Physical Interface Level 4 (SPI-4) Phase 1: A System Interface for Interconnection Between Physical and Link Layer, or Peer-to-Peer Entities Operating at an OC-192 Rate (10 Gb/s)

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4 Document Revision History

Rev. 0.1	Adopted OIF99.50/56 as the basis of the draft specification
Jan 2000	OIF2000.054.0 approved to Straw Ballot
May/Aug 2000	OIF2000.054.1/OIF2000.184.0 incorporates comments from Straw Ballot
Aug 2000	OIF2000.184.0 approved to Principal Member Ballot as OIF2000.184.1
Oct 2000	Updated header and status to Approved Implementation Agreement following approval by Principal Member Ballot, and added Approval Date and Implementation Agreement Document Number. Added list of companies (Appendix C).
Apr 2001	Updated header to incorporate new document number of **OIF-SPI4-01.0** (replacing former number OIF-PLL-03.0)

5 Introduction

This specification describes a data path interface between the physical and link layers to support physical line data rates up to 10 Gb/s. This interface specification will be known as SPI-4.

The specification outlines the system architecture, I/O and design considerations for implementing the interface. An optional 4x16 interface mode is also described, which allows up to four separate 16-bit interfaces to support four independent Link Layer devices connected to a single Physical Layer device, or four independent Physical Layer devices connected to a single Link Layer device.

6 Interface Description

6.1 Overview

The SPI-4 interface has the following attributes:

- 64-bit single ended HSTL Class 1 I/O at 200 MHz supporting transfer rates of 12.8 Gb/s.
- Source synchronous clocking to simplify board design at high frequencies.
- Multi-PHY capability with a simple flow control mechanism that supports channelized or non-channelized operation.
- Out-of-band signaling to simplify the interface design eliminating the need for complex state machines required in the in-band signaling.

Owing to the high frequency operation of the interface, only a point-to-point configuration is supported. In the multi-PHY configuration, the number of ports or channels supported depends on the number of address bits in the interface. The standard does not put any restrictions on the number of address bits in the interface. The interface relies on the system to provide transmit data at a sustained rate so as to keep up with the rate at which the Physical Layer device is capable of operating. If the system cannot keep up with this rate, the Physical Layer device should automatically insert filler bytes in the stream. Similarly, the system should be able to keep up with the receive data rate in order to prevent a FIFO overflow in the Physical Layer device. In the multi-PHY configuration, the data transfer may be switched to any port or channel at any clock cycle.

6.2 I/O Drivers

In the SPI-4 interface, HSTL Class 1 drivers are specified. The use of HSTL drivers provides the required I/O drive capability between the Physical Layer and the Link Layer devices at considerably low power dissipation.

6.3 Source Synchronous Clocking

SPI-4 specifies a source synchronous clocking mechanism for the interface in which the clock and data are synchronous to each other. At frequencies greater than 200 MHz, the delays through the traces on the board become significant and without the source synchronous clocking, meeting the setup and hold times at the endpoints becomes quite challenging. The advantage of using the source synchronous clocking mechanism is that far end data recovery is much more easily achieved. There is no need to account for chip I/O delays or use expensive PLL techniques to ensure clock/data alignment.

With this source synchronous clocking mechanism, all the signals from the Link Layer to the Physical Layer use the Tx clock from the Link Layer as the reference clock and all the signals from the Physical Layer to the Link Layer use the Rx clock from the Physical Layer as the reference clock. As a consequence of this rule, the receive control signals that originate from the Link Layer must first be re-synchronized to the transmit clock before they are used internally by the Physical Layer. Similarly, the transmit control signals that originate from Physical Layer must be re-synchronized to the receive clock. This mechanism is illustrated in Figure 1 below.

6.4 Re-synchronization Latency

Owing to the re-synchronization delays of the control signals between the clock domains, there is a certain amount of latency before any change in values of the control signals is detected. The Link Layer and the Physical Layer devices must provide for this latency. As an example, during transmit, when the Physical Layer device fills up, it must signal the Link Layer to stop transmitting until it is ready to accept more transfers. Since the Link layer will encounter a certain amount of latency in detecting the full condition, the Physical Layer device must be capable of sustaining a few more transfers before the Link Layer responds to this condition and stops the transmission.

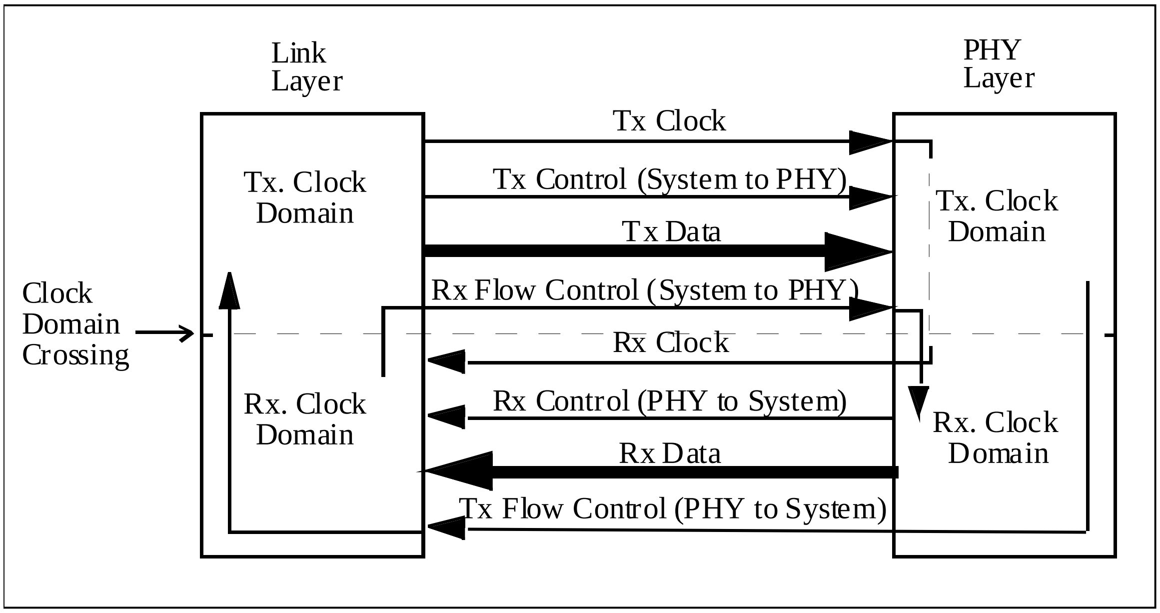


Figure 1. System Reference Model with Source Synchronous Interface

6.5 Multi-PHY Support

The proposed interface contains address bits to accommodate multi-ported or multi-channel PHY devices. There is no limitation on the number of address bits in the interface and it is dependent on the application.

6.5.1 Multi-PHY Flow Control

The flow control mechanism in this interface works consistently in a single-PHY environment as well as in the multi-PHY environment. This method does not require the Link layer to query the Physical Layer for the status. Instead, flow control information is passed back to the sending device on a continuous basis. The flow control information specifies whether the receiving device is full or not. When the sending device observes this signal, it takes an appropriate action. For example, if the receiver is full, the sender stops the data transfer, if not, it continues with the data transfer. Since, the latencies due to the length of the board traces and logic for observing the flow control information may be large, the receiver should be capable of accepting a reasonable amount of data even after signaling a full condition. In this standard, this latency is specified in number of 64-byte chunks rather than the number of clock cycles since the granularity of the clock is very small (on the order of 5 ns at 200 MHz).

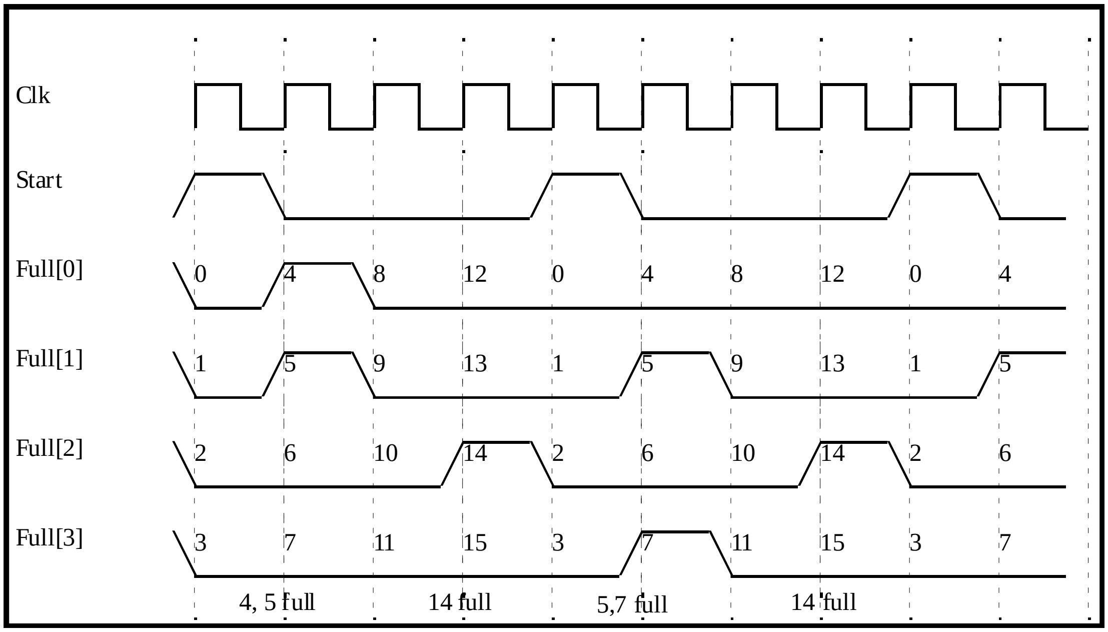


Figure 2. Multi-PHY flow control for up to 16-ported or 16-channel devices.

In order to minimize the number of pins required to provide the status information from each channel or a port, especially in a device with large number of ports or channels, a round robin scheme is used, in which the status indication is provided in a round robin fashion in groups of four per clock cycle. A start signal is asserted each time the status information for the first group of four is provided. This signal is again asserted when the status information wraps around to the first group of four. Figure 2 illustrates this mechanism for a device with 16 ports or channels.

6.6 Single-PHY Support

In single PHY applications the status information is continuously provided on the Full[0] pin and the round robin scheme is disabled. This mode of operation may be extended to applications up to four PHY ports or channels. Direct status may be provided continuously from each of the four ports or channels on four Full[3:0] lines. Note that in this application, the Start signal is continuously asserted (held high). Direct status operation is shown in Figure 3.

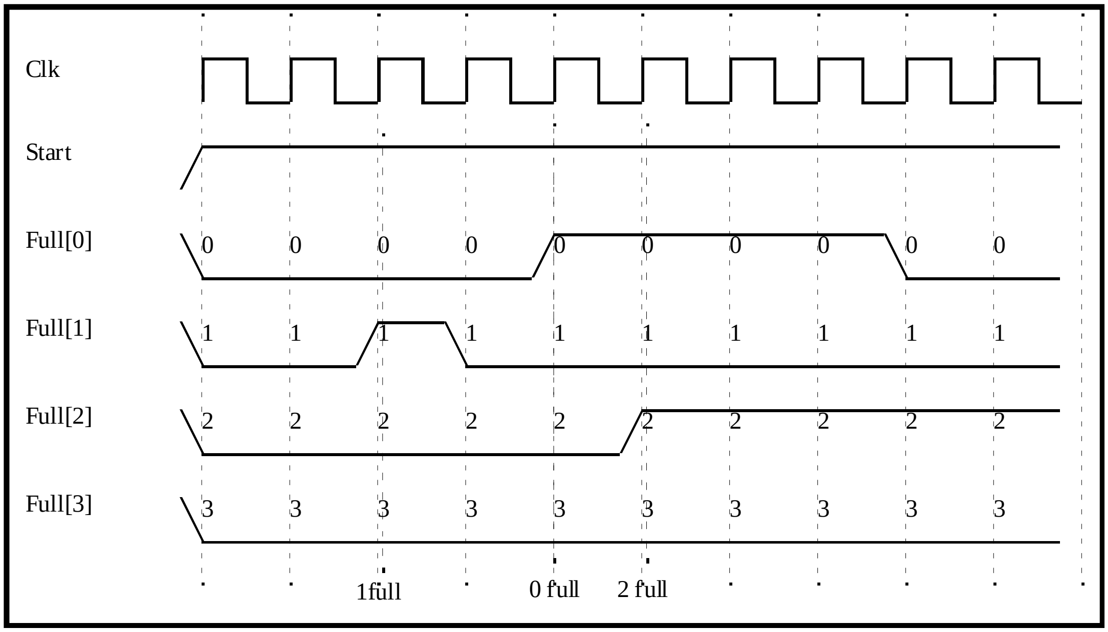


Figure 3. Direct Status Indication for up to 4-ported or 4-channel PHY devices

6.7 Physical Topology

The physical topology of the interface is assumed to be a point-to-point connection between the Link layer (sometimes referred to as “System” in this document) and the Physical layer. This means that a Link layer device is only electrically connected to a single Physical Layer device. The Physical Layer device can contain one or more PHY ports or channels in a multi-PHY configuration connected via a single electrical interface. In addition, the physical topology also may optionally support 4 independent 16-bit paths for connecting a single Link layer device with four Physical Layer devices and vice versa. The possible connection topologies are shown in Figure 4.

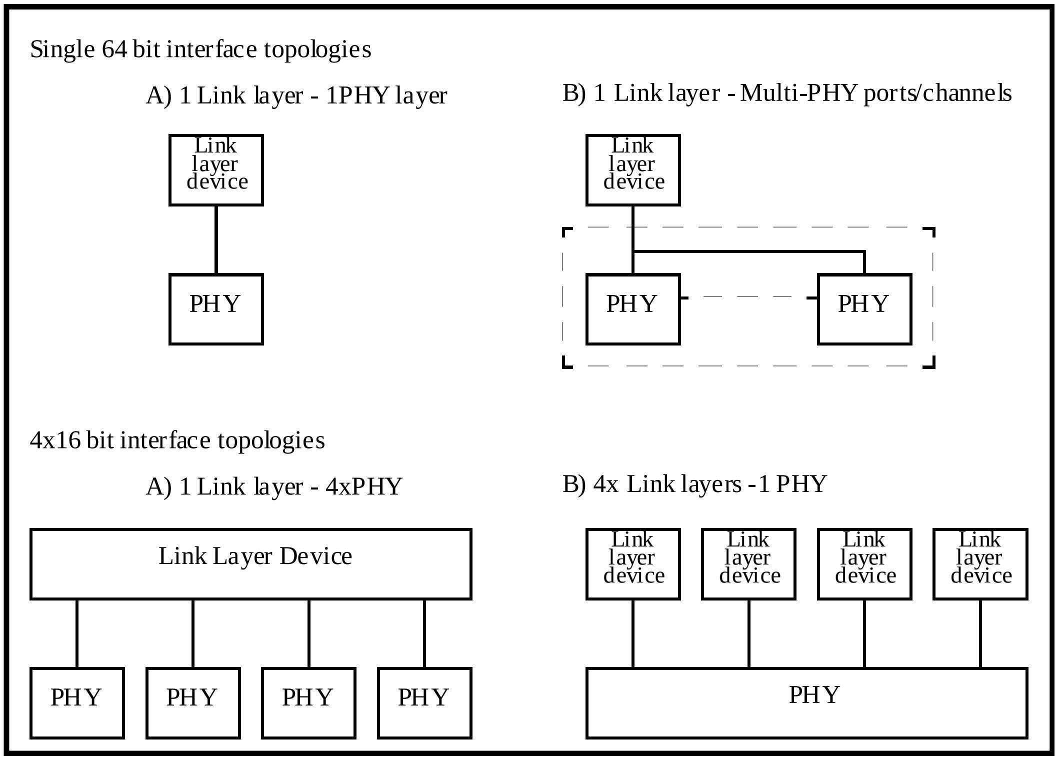


Figure 4. Reference Configurations

6.8 4x16 Mode

An optional 4x16 mode may also be supported, in which the interface can be configured to operate as four independent 16-bit interfaces to provide a total aggregate bandwidth of 12.8 Gb/s. Each 16-bit interface operates at 200 MHz to provide 3.2 Gb/s bandwidth. Figure 4 shows two configurations for the 4x16 mode. In the first configuration, a single Link layer device connects to four PHY Layer devices with each PHY Layer device operating at line rate of 2.5 Gb/s. In the second configuration, four Link Layer devices may be connected to a single PHY Layer device. The single PHY Layer device will treat each stream of data from the Link Layer as a separate channel and will multiplex these channels on a single physical interface. The motivation for this is driven by the fact that it is more difficult to create a single Link Layer devices that operate at higher speeds, especially at 10 Gb/s, than at lower rates, whereas it is easier to design the PHY Layer devices to operate at these rates. In the 4x16 mode, only a single PHY mode of operation is supported. The signals for the 4x16 mode are shown in Figure 7.

6.9 Parity Calculation

The interface uses parity to detect problems with the interconnect between the Link layer and PHY devices. There are four parity bits that protect the data bits. The parity bit must always contain valid parity even though the TxValid or RxValid signals are de-asserted. Four parity bits are provided with each bit providing an odd parity value for the data signals in groups of 16-bits. An example of the parity calculation for transmit data is shown in the following.

TxPrty[0] = NOT (TxData[0] ^ TxData[1] ^ TxData[2] ^ TxData[3]

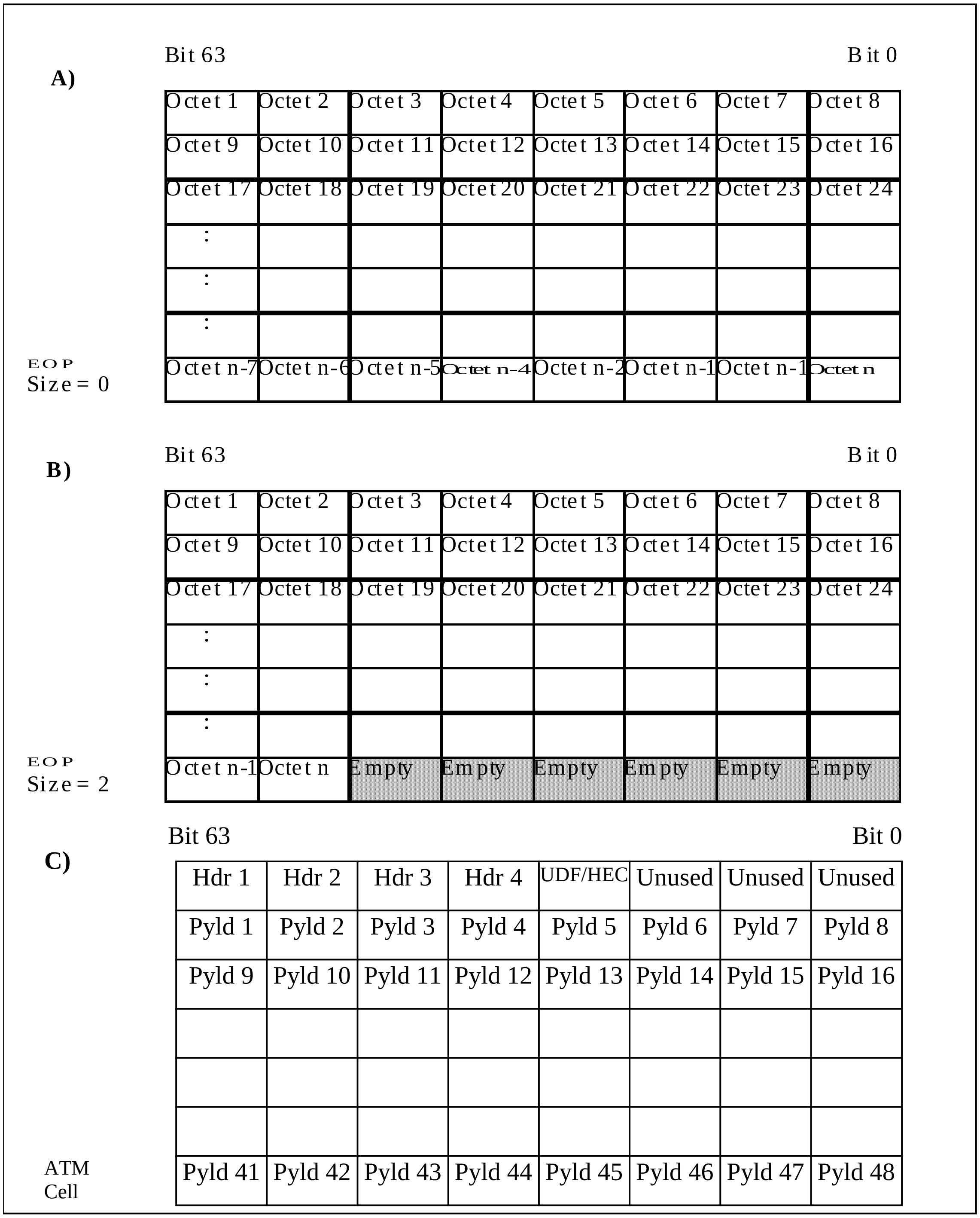
^ TxData[4] ^ TxData[5] ^ TxData[6] ^ TxData[7]

^ TxData[8] ^ TxData[9] ^ TxData[10] ^ TxData[11]

^ TxData[12] ^ TxData[13] ^ TxData[14] ^ TxData[15])

6.10 Octet Organization

The interface supports variable length packets. Since the interface is *eight* octets wide, a count of empty octets is provided during the transfer of the last word of a packet. This allows packets of any arbitrary length to be transferred across the interface. The interface will support packets as small as one octet as well as packets of unlimited length. The length of a packet may be limited by mechanisms beyond the scope of the interface. The organization of packet octets is shown in Figure 5.



A)

Bit 63 … Bit 0

	Octet 1	Octet 2	Octet 3	Octet 4	Octet 5	Octet 6	Octet 7	Octet 8
	Octet 9	Octet 10	Octet 11	Octet 12	Octet 13	Octet 14	Octet 15	Octet 16
	Octet 17	Octet 18	Octet 19	Octet 20	Octet 21	Octet 22	Octet 23	Octet 24
	:							
	:							
	:							
EOP Size = 0	Octet n-7	Octet n-6	Octet n-5	Octet n-4	Octet n-2	Octet n-1	Octet n-1	Octet n

B)

Bit 63 … Bit 0

	Octet 1	Octet 2	Octet 3	Octet 4	Octet 5	Octet 6	Octet 7	Octet 8
	Octet 9	Octet 10	Octet 11	Octet 12	Octet 13	Octet 14	Octet 15	Octet 16
	Octet 17	Octet 18	Octet 19	Octet 20	Octet 21	Octet 22	Octet 23	Octet 24
	:							
	:							
	:							
EOP Size = 2	Octet n-1	Octet n	Empty	Empty	Empty	Empty	Empty	Empty

C)

Bit 63 … Bit 0

	Hdr 1	Hdr 2	Hdr 3	Hdr 4	UDF/HEC	Unused	Unused	Unused
	Pyld 1	Pyld 2	Pyld 3	Pyld 4	Pyld 5	Pyld 6	Pyld 7	Pyld 8
	Pyld 9	Pyld 10	Pyld 11	Pyld 12	Pyld 13	Pyld 14	Pyld 15	Pyld 16
ATM Cell	Pyld 41	Pyld 42	Pyld 43	Pyld 44	Pyld 45	Pyld 46	Pyld 47	Pyld 48

Figure 5. Octet Organization

7 Interface Signals

The single 64-bit interface signals are shown in Figure 6.

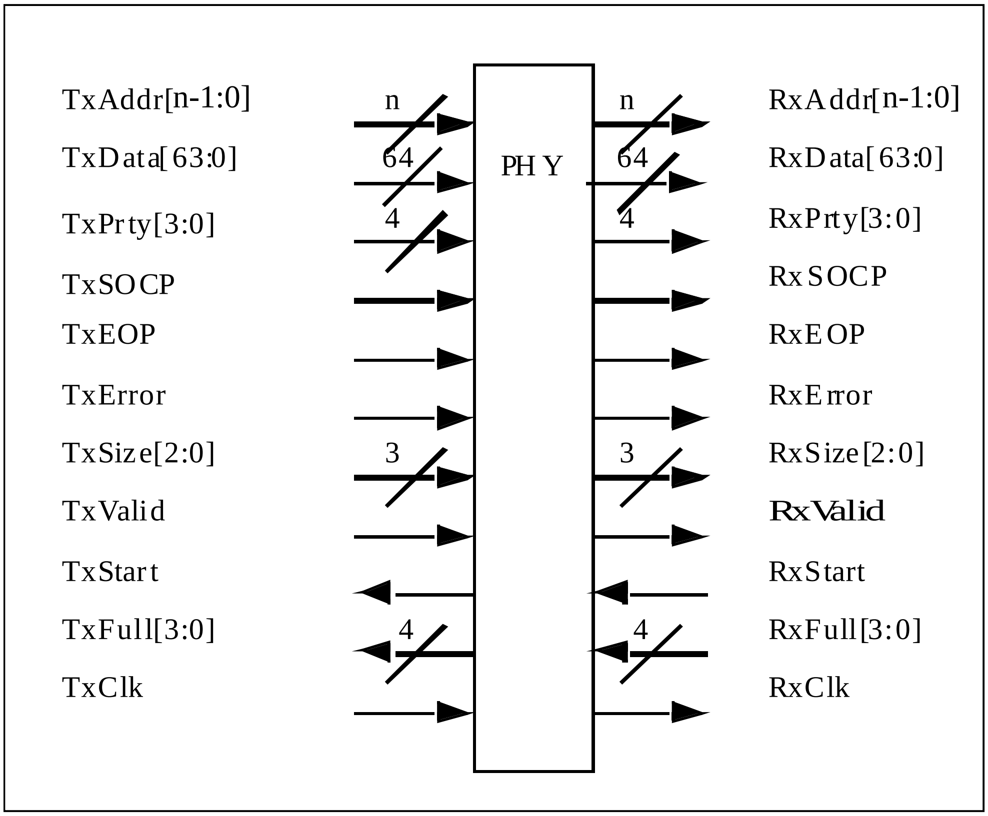


Figure 6. Interface Signals

8 Signal Description

Table 1. Signal Descriptions

Signal	Direction	Function
Transmit Interface Signals:		
TxAddr[n-1:0]	System to PHY	Transmit PHY port or channel address. n bits of address supports up to 2^n ports or channels. These signals are only sampled when TxValid is asserted, and are ignored when TxValid is deasserted. These signals determine the port or channel associated with the TxData, TxSOCP, TxEOP, TxError, TxSize, and TxValid signals.
TxData[63:0]	System to PHY	Transmit data. These signals are only sampled when TxValid is asserted, and are ignored when TxValid is de-asserted. The byte ordering of data is from most significant (bits 63:56) to least significant (bits 7:0).
TxPrty[3:0]	System to PHY	Transmit data parity. These signals must always have correct parity. TxPrty[0] provides parity over TxData[15:0] TxPrty[1] provides parity over TxData[31:16] TxPrty[2] provides parity over TxData[47:32] TxPrty[3] provides parity over TxData[63:48]
TxSOCP	System to PHY	Transmit start of cell or packet. This signal is only sampled when TxValid is asserted, and is ignored when TxValid is de-asserted.
TxEOP	System to PHY	Transmit end of packet. This signal is only sampled when TxValid is asserted, and is ignored when TxValid is de-asserted.
TxError	System to PHY	Transmit data error. This signal is only required to be sampled when both TxValid and TxEOP are asserted, and is ignored when TxValid is de-asserted.
TxSize[2:0]	System to PHY	Transmit octet count. A value of zero indicates that all 8 octets are valid, and values of 1-7 indicate 1 to 7 octets valid, from most-significant to least-significant octet. These signals are only sampled when TxEOP and TxValid are both asserted and are ignored at other times.
TxValid	System to PHY	Transmit data valid. When this signals is deasserted the following signals are ignored: TxAddr, TxData, TxSOCP, TxEOP, TxSize
TxStart	PHY to System	Transmit flow control frame start from the PHY layer to the link layer. Note that due to the source synchronous nature of this interface, this signal is synchronous to RxClk
TxFull[3:0]	PHY to System	Transmit flow control full indication from the PHY layer to the link layer. With cells this signal indicates that there is no room for more cells in the PHY. With packets this signal indicates that there is no room for more words in the PHY. The full status of channels is time multiplexed onto these four signals. Note that owing to the source synchronous nature of this interface, this signal is synchronous to RxClk. After assertion of TxFull (which may incur an internal 4-clock delay when multi-PHY flow-control is used), the PHY layer shall be able to accept a minimum of 12 clocks' of additional data from the link layer.
TxClk	System to PHY	Transmit clock. The PHY device will use this clock to sample all the Tx signals. The system device will drive all the Tx signals coincident with the rising edge of this clock.

Receive Interface Signals:		
RxAddr[n-1:0]	PHY to System	Receive PHY port or channel address. n bits of address supports up to 2^n ports or channels. These signals are only defined when RxValid is asserted. These signals determine the channel associated with the RxData, RxSOCP, RxEOP, RxError, RxSize, and RxValid signals.
RxData[63:0]	PHY to System	Receive data. These signals are only defined when RxValid is asserted. The byte ordering of data is from most significant (bits 63:56) to least significant (bits 7:0).
RxPrty[3:0]	PHY to System	Receive data parity. These signals must always have the correct parity. RxPrty[0] provides parity over RxData[15:0] RxPrty[1] provides parity over RxData[31:16] RxPrty[2] provides parity over RxData[47:32] RxPrty[3] provides parity over RxData[63:48]
RxSOCP	PHY to System	Receive start of cell or packet. This signal is only defined when RxValid is asserted.
RxEOP	PHY to System	Receive end of packet This signal is only defined when RxValid is asserted.
RxError	PHY to System	Receive data error. This signal should be asserted only when both RxValid and RxEOP are asserted.
RxSize[2:0]	PHY to System	Receive octet count. A value of zero indicates that all 8 octets are valid, and values of 1-7 indicate 1 to 7 octets valid, from most-significant to least-significant octet. These signals are only defined when RxEOP and RxValid are both asserted.
RxValid	PHY to System	Receive data valid. When this signal is deasserted the following signals are undefined: RxAddr, RxData, RxSOCP, RxEOP, RxError, RxSize.
RxStart	System to PHY	Transmit flow control frame start from the link layer to the PHY layer. Note that due to the source synchronous nature of this interface, this signal is synchronous to TxClk.
RxFull[3:0]	System to PHY	Receive flow control full indication from the link layer to the PHY layer. With cells this signal indicates that there is no room for more cells in the system. With packets this signal indicates that there is no room for more words in the system. The full status of the channels is time multiplexed onto these four signals. Note that owing to the source synchronous nature of this interface, this signal is synchronous to the TxClk. After assertion at an RxFull input, the PHY layer shall transmit a maximum of 12 clocks' of additional data to the link layer.
RxClk	PHY to System	Receive clock. This clock is used by the system device to sample all of the Rx signals. The PHY will drive the Rx signals coincident to the rising edge of this clock.

9 The 4x16 bit interface

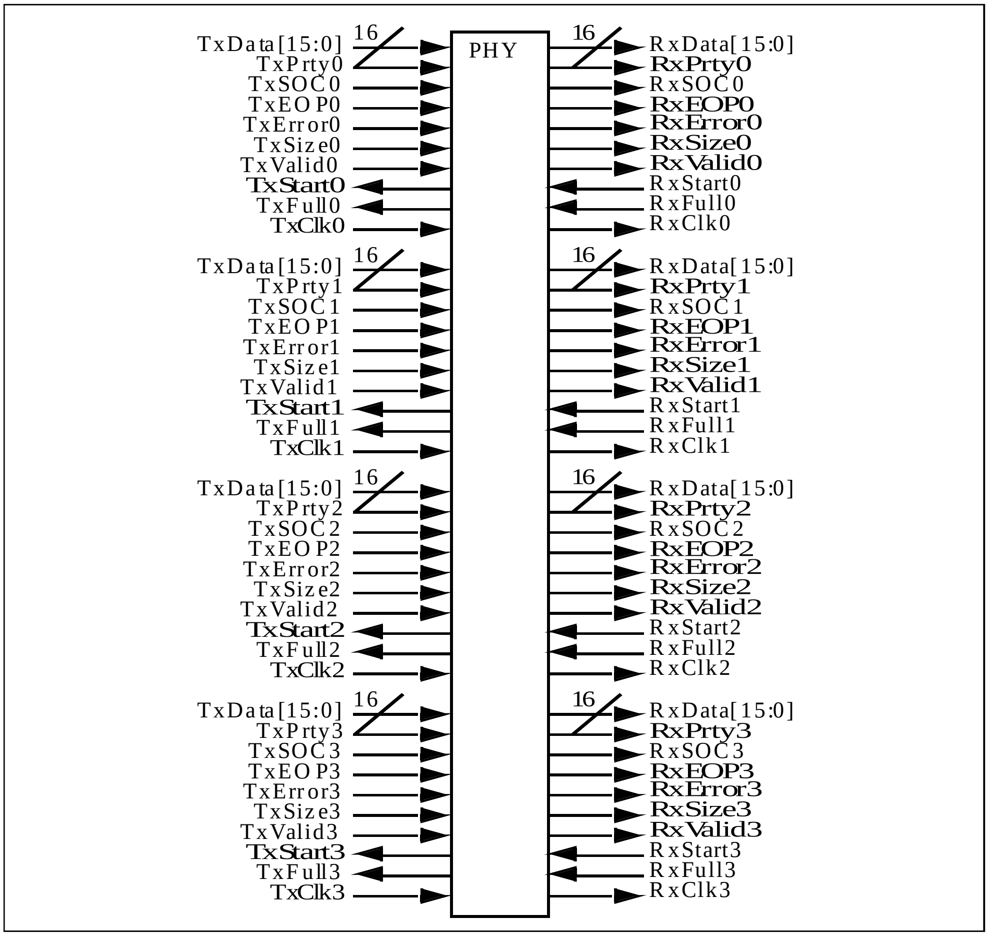


Figure 7. 4x16 Interface Signals

10 Interface Timing

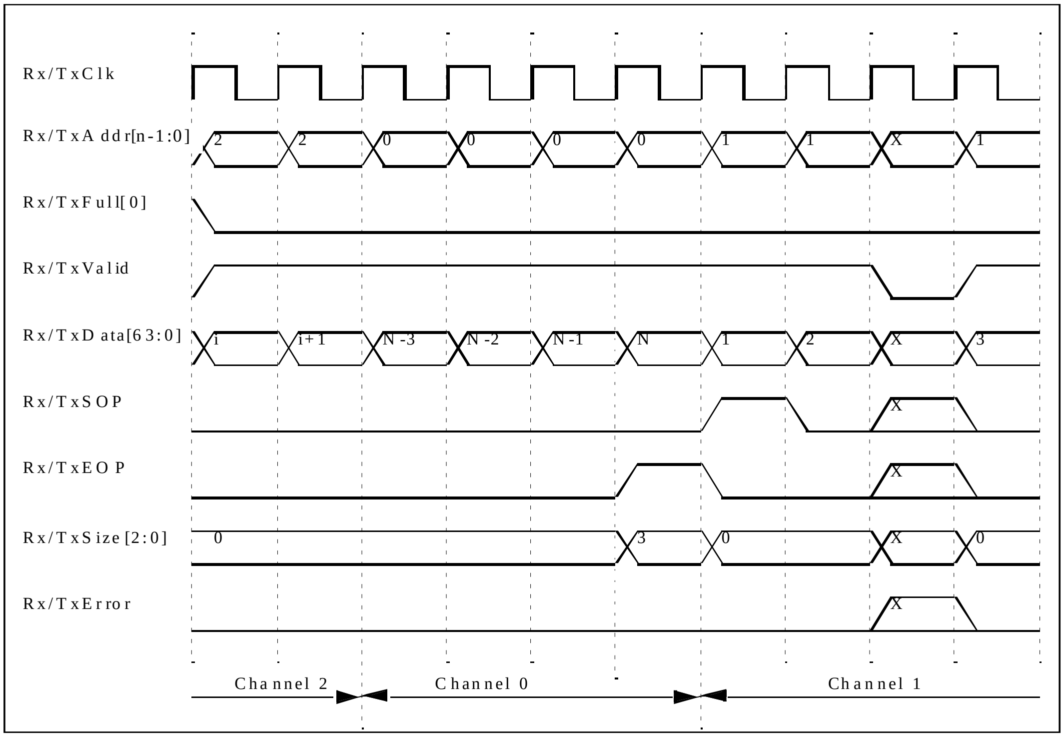


Figure 8. Interface Functional Timing

11 AC Specifications

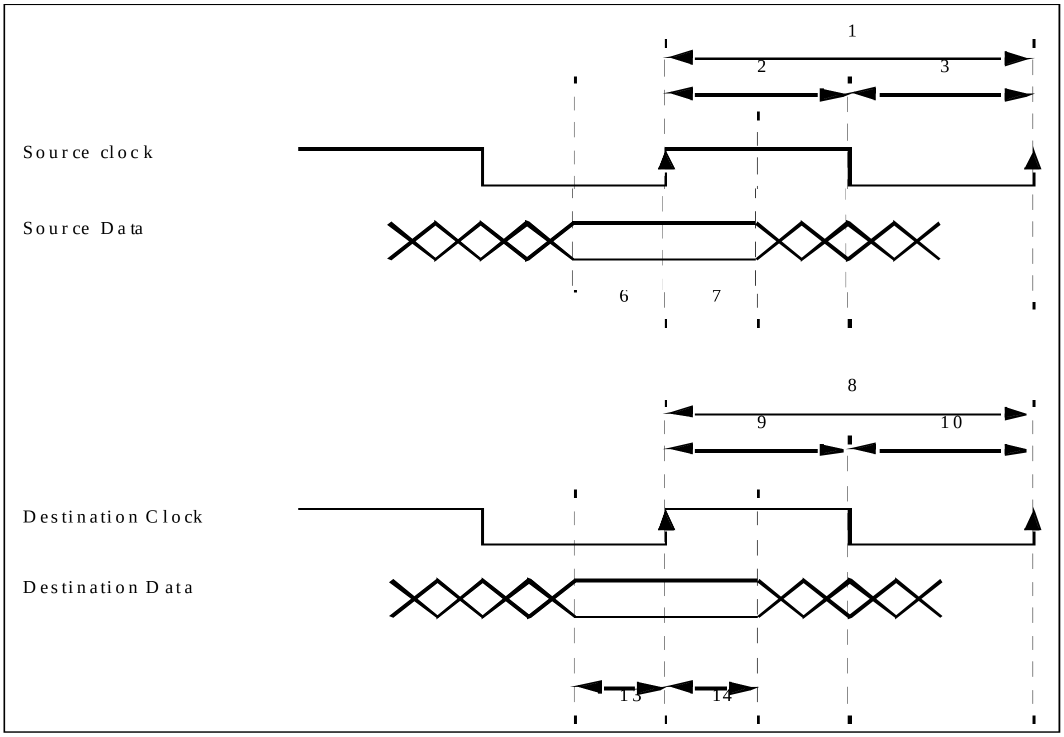


Figure 9. AC Specifications

Table 2. AC Specifications

Num	Characteristic	Min	Max	Units
1	Source Clock Period	5		ns
2	Source Clock High Pulse Width	2	3	ns
3	Source Clock Low Pulse Width	2	3	ns
4	Source Clock Rise Time		1	ns
5	Source Clock Fall Time		1	ns
6	Source Data Valid Before Rising Source Clock	1.2		ns
7	Source Data Hold From Rising Source Clock	1.2		ns
8	Destination Clock Period	5		ns
9	Destination Clock High Pulse Width	2	3	ns
10	Destination Clock Low Pulse Width	2	3	ns
11	Destination Clock Rise Time		1.5	ns
12	Destination Clock Fall Time		1.5	ns
13	Destination Data Valid Before Rising Destination Clock	0.8		ns
14	Destination Data Hold From Rising Destination Clock	0.8		ns

12 DC Specifications

The data interface will be implemented with HSTL Class 1 drivers. The voltage specifications are given in following table. All HSTL specifications are provided relative to V_{ddq}, so as to be applicable to 1.5V supply voltages referenced in the EIA/JEDEC standard, as well as to commonly available HSTL I/O drivers from many 1.8V ASIC and FPGA families.

Table 3. DC Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_{ddq}	Output Supply Voltage	V_{ddq} – 0.1	V_{ddq}	V_{ddq} + 0.1	V	V_{ddq} = 1.5V or 1.8V
V_{TT}	Termination Voltage	$V_{ddq(min)}$/2	$V_{ddq(nom)}$/2	$V_{ddq(max)}$/2	V	V_{ddq} / 2
V_{REF}	Differential Input Reference Voltage	$V_{ddq(min)}$/2	$V_{ddq(nom)}$/2	$V_{ddq(max)}$/2	V	V_{ddq} / 2
V_{oh}	Output High Voltage	V_{ddq} – 0.4			V	I_{oh} = 8 mA @ 1.0 V
V_{ol}	Output Low Voltage			0.4	V	I_{ol} = 8 mA @ 0.4 V
V_{ih}	Input High Voltage	V_{REF} + 0.10		V_{ddq} + 0.3	V	
V_{il}	Input Low Voltage	–0.3		V_{REF} – 0.10	V	
I_{oz}	3-State Leakage Current	0		10	µA	Driver Hi-Z

13 Summary

The SPI-4 Phase 1 interface is a packet and cell transfer interface that supports transfers of a nominal rate of 10 Gb/s (OC-192-based) and a maximum rate of 12.8 Gb/s. Transfers may be between Physical and Link layer entities, or between peer entities. Data and control I/O is at 200 Mb/s using HSTL Class 1 drivers. Source-synchronous data transfer and flow control simplify board- and system-level design and layout.

14 References

14.1 Normative references

1. EIA/JESD8-6, *High Speed Transceiver Logic (HSTL): A 1.5V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits*, August 1995, Electronic Industries Association.

14.2 Informative references

None.

15 Appendix A: Glossary

ATM	Asynchronous Transfer Mode
EIA	Electronic Industries Association
HEC	Header Error Correction
HSTL	High Speed Transceiver Logic
I/O	Input/Output
LSB	Least Signficant Bit (or Byte)
MSB	Most Significant Bit (or Byte)
OC-192	Optical Carrier Level 192 (9.95328 Gb/s)
PHY	Physical Layer Entity
PLL	Phase Locked Loop
SPI-4	System Physical Interface Level 4
UDF	User Defined Field

16 Appendix B: Open Issues / Current work items

None

17 Appendix C: List of companies belonging to OIF when document was approved

Accelerant Networks
Acorn Networks
AdventNet
Aerie Networks
Agilent Technologies
Agility Communications
Alcatel
Algety Telecom
Alidian Networks
Altera
Alvesta Corporation
Amber Networks
AMCC
America Online
Analog Devices
ANDO Corporation
Appian Communications
Applied Innovation
Artel Video Systems
Astral Point Communications
AT&T
Atoga Systems
Avici Systems
Axiowave Networks
Axsun Technologies
Bay Microsystems
Blaze Network Products
Bravida Corp
BrightLink Networks
Broadcom
Cable & Wireless
Calient Networks
Calix Networks
Caspian Networks
Catamaran Communications
Centerpoint Broadband Technologies
Chiaro Networks
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Juniper Networks
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Kromos Technology
Lambda Crossing
LANCAST
Laurel Networks
Level 3 Communications
LightLogic
Lucent Technologies
Luminous Networks
Luxcore
LuxN
LYNX - Photonic Networks
Mahi Networks
Maple Networks
Marconi Communications
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Memlink
Metro-OptiX
MicroOptical Devices
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NEC
Net Insight
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NetPlane
Network Associates
Network Elements
Network Photonics
NewPort Communications
NIST
Nokia
Nortel Networks
NTT Corporation
Ocular Networks
OKI Electric Industry
ON Semiconductor
ONI Systems
Opthos
Optix Networks
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OptronX

Panstera
Photuris, Inc.
PicoLight
Pine Photonics Communications
Pluris
PMC Sierra
Procket Networks
Quake Technologies
Quantum Bridge
Redback Networks
Redfern Broadband Networks
Reversi Networks
RHK
Sandia National Laboratories
Santec Corporation
Scientific Atlanta
Siemens
SITA Equant
Solidum Systems Corporation
Solinet Systems
Sorrento Networks
SpectraSwitch
Sprint
Stratos Lightwave
Sumitomo Electric Industries
Sycamore Networks
TDK Semiconductor
Tektronix
Telcordia Technologies
TELE-WORX
Tellabs
Tellium
Tenor Networks
Terawave Communications
Texas Instruments
Toshiba Corporation
TranSwitch Corporation
Trellis Photonics
TriQuint Semiconductor
Turin Networks
TyCom
US Conec
Valiant Networks
Verizon
Versanetworks
Vitesse Semiconductor
Vivace Networks

White Rock Networks
Williams Network
WorldCom
Xanoptix
Xilinx
YAFO Networks
Zaffire