System Architectures using OIF CEI-56G interfaces

OIF CEI-56G - It’s Happening Now

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Abstract

- The networking industry is faced with many challenges.

- This panel focuses on the trend for increasing aggregate bandwidth and increasing per lane data rates.
  - Increasing per lane data rates brings in the issues of fundamental reach limitations due to physical losses.
  - Increasing aggregate data requirements drive alternative equipment architectures such as the use of mid-board optics and mid-planes due to density limitations.

- This panel discusses the feasibility and practicality of architecture changes that can be enabled by the OIF’s newest developments that are in process including CEI-56G-USR, CEI-56G-XSR, CEI-56G-VSR, CEI-56G-MR, and CEI-56G-LR.
CEI Application Space is Evolving

- Technical challenges of 56G serial I/O are forcing evolution in system architectures and the interface application space:
  - 2.5D and 3D applications are becoming increasingly relevant.
  - High function ASICs (such as switch chips) are driving requirements for higher I/O density and lower interface power.
  - Chip-to-chip and mid-plane interfaces are becoming more relevant than high loss backplanes (at least in the near-term).

- Emerging Themes:
  - Pin density is not increasing fast enough for high density ASICs.
  - Power reduction of 30% from one generation to next is not good enough.
  - Modulation choices are being driven by both channel signal integrity and by silicon transistor characteristics.
Panel Speakers

Today’s panel speakers represent interconnect, silicon, and system perspectives on emerging system architectures.

- **Nathan Tracy - OIF Technical Committee Chair - TE Connectivity**
  Nathan Tracy has over 30 years of experience in Technology Development, Marketing, and Business Development for TE Connectivity (formerly Tyco Electronics). The initial 16 years were with M/A-COM prior to being acquired by TE Connectivity. Currently, he is a Technologist on TE's system architecture team, driving new product development for the data communications market. He also serves the Optical Internetworking Forum (OIF) as the Technical Committee Chair. Nathan is involved in a number of other outside industry associations. Presently he is a regular attendee and contributor to the Ethernet Alliance, and IEEE 802.3 as well as the OIF.

- **Ed Frlan - OIF Physical & Link Layer Interoperability Work Group Chair - Semtech**
  Ed Frlan is a Senior System Architect within the Signal Integrity Product Group of Semtech Corp responsible for the definition of next generation datacom and video PHY products. He is also the OIF's PLL Interoperability Working Group chair and has contributed to the development of the CEI-28G-VSR Implementation Agreement. He joined Gennum/Semtech from his role as a Hardware Architect at Ciena where he was responsible for the system architecture and synchronization of various line cards including those for Carrier Ethernet, SONET, OTN and Broadcast Video applications. Ed holds a Ph.D. degree in Electrical Engineering from Carleton University.

- **Ed Priest - Distinguished Engineer - Juniper Networks**
  Ed is presently a Distinguished Engineer at Juniper Networks. He has been actively involved in the design of large servers and supercomputers (Cray, D.E.Shaw, Silicon Graphics, and Supercomputer Systems), large networking platforms (Juniper, Abriiz) and very high speed components (PMC-Sierra, Cortina). Areas of expertise are high speed signaling and circuits, signal and power integrity, packaging (both systems and components), and system hardware design.