Implementation Agreement for the High Bandwidth Coherent Driver Modulator (HB-CDM)

OIF-HB-CDM-02.0

July 15,2021

Implementation Agreement created and approved

OIF

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Working Group: **Physical and Link Layer (PLL) Working Group**

TITLE: **Implementation Agreement for High Bandwidth Coherent Driver Modulator (HB-CDM)**

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ABSTRACT: This Implementation Agreement specifies key aspects of High Bandwidth Coherent Driver Modulators operating at rates including 64GBd, 96GBd, and up to 128GBd.

Table of Contents

1 List of Figures

2 List of Tables

3 Document Revision History

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4 Introduction

This document details an Implementation Agreement (IA) for a High Bandwidth Coherent Driver Modulator (HB-CDM) targeting modulation and data-rate agnostic coherent applications having nominal symbol rates including 64Gbaud, 96Gbaud and up to 128Gbaud. The IA aims to identify and specify the common features and properties of coherent transmitters to enable them to broadly meet the needs of current and future coherent systems and is an extension to the orginal OIF Specification OIF-HB-CDM-01.0, which defined rates to 64Gbaud (also called Class 40) and is a superset of that IA.

This IA defines the following: (1) Required functionality; (2) High speed electrical interfaces; (3) Low speed electrical interfaces; (4) Electro-Optical Specifications and Operating Characteristics; (5) Mechanical requirements.

The original HB-CDM IA defined a single electro-mechanical form factor labeled as Type 1 having a surface mount configuration and nominally targeting Class 40 or 60 for 64GBd or 96GBd applications respectively. This revision additionally defines Type 2 and 3 form-factors which retain the package size, but modify the SMT RF pin pitch (for Type 2) and use Flexible Printed Circuit (FPC) interfaces for the RF and DC (for Type 3) . This IA also introduces Class 60 and Class 80 EO masks for nominally 96GBd and 128GBd operation respectively. It is noted that while Type and Class are independent it is expected higher Class devices are accomodated by the Type 2 and Type 3 definitions.

The IA defines an SPI bus to control the Driver in the HB-CDM, including frame format and electrical specifications. The document includes vendor specific options for analog control using the optional Vendor Specific – Analog pins defined in the pin list, but these have not been standardized in this document.

The IA does not define the technologies used to implement the IA, nor the expected optical transmission performance of coherent systems using transmit components conforming to the IA.

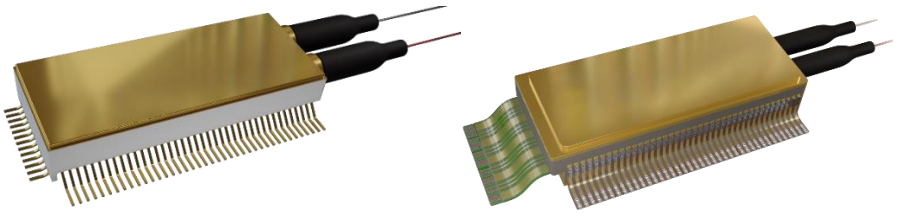


Figure 1 Type 1 and 2 modules (L), Type 3 modules (R)

5 Functionality

This Implementation Agreement specifies a single opto-electronic module with the functionality shown in Figure 2 and consisting of an integrated Coherent Driver and a Polarization Multiplexed Quadrature Modulator.

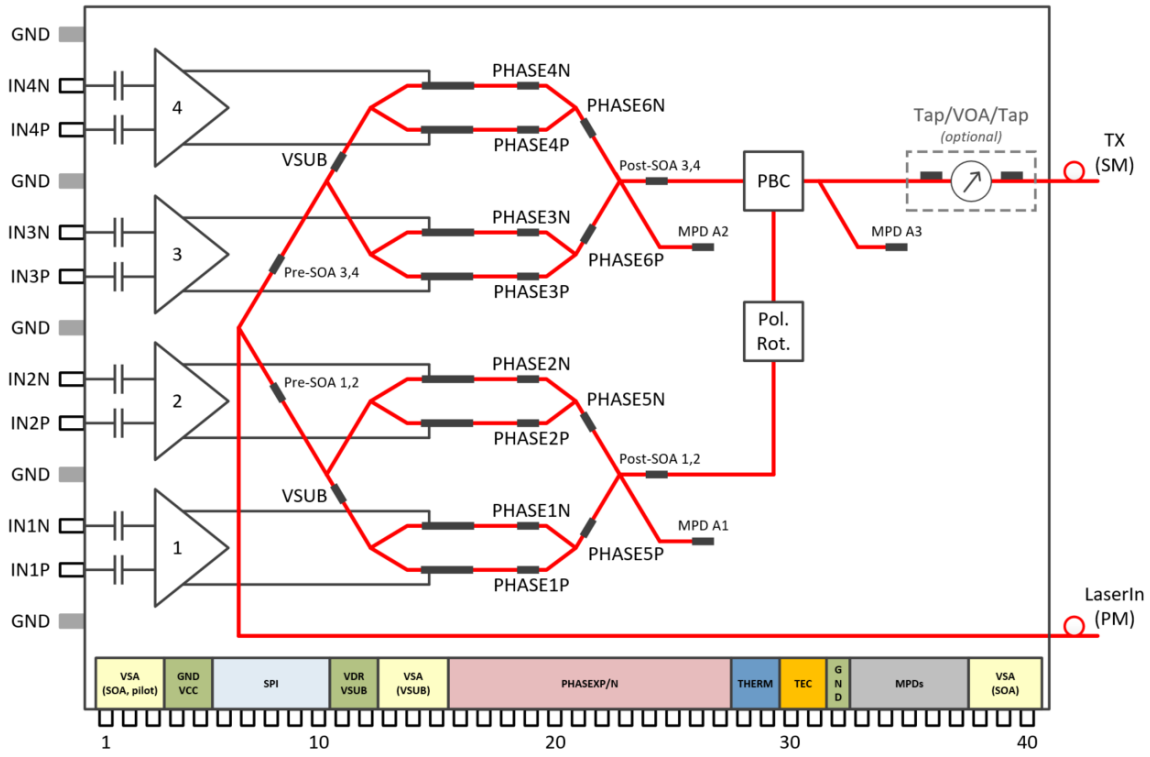


Figure 2 Functional schematic for the HB-CDM

Notes:

1. While one configuration for the position of the SM and PM fibers is shown here, the reverse orientation is equally acceptable for compliance.
2. An output shutter and VOA are optional
3. The MPDs are optional
4. The Vpilot tone modulation is optional
5. Pre and Post SOAs are optional
6. Per polarization PDs may be complementary or tap structures

The differential RF modulation inputs are fed to the Driver stage to amplify the electrical signals to match the modulator electrode requirements to induce sufficient optical phase change.

The PM fiber optical input is split and independently modulated by quadrature modulators, then recombined with their polarizations orthogonal to each other using a Polarization Rotator. The resulting optical signal is output through a Single Mode fiber.

6 Mechanical

6.1 Types 1, 2, and 3 Overview

The electro-mechanical form factors use a surface mount configuration (Types 1 and 2) or Flexible Printed Circuit (Type 3) with the low speed electrical interface signals applied from the left side of the package (viewed from top, optical south).

The outline mechanical size of the HB-CDM is shown in Table 1. These figures represent an informative specification with the key compliance of the module being compatible with the Landing Pad definitions in Section 7.

Form Factor	Width (mm)	Height (mm)	Length[1] (mm)	RF signal-signal (pitch)	RF channel (pitch)	DC (pitch)	Proposed Rates [2]
Type 1	≤12	≤5.5	≤30	SMT (0.8mm)	SMT (2.4mm)	SMT (0.7mm)	64, 96GBd
Type 2	≤12	≤5.5	≤30	SMT (0.65mm)	SMT (2.4mm)	SMT (0.7mm)	64, 96, 128GBd
Type 3	≤12	≤5.5	≤30	FPC (0.45mm)	FPC (2.4mm)	SMT or FPC (0.7mm)	96, 128GBd

Table 1 Outline mechanical size of the HB-CDM

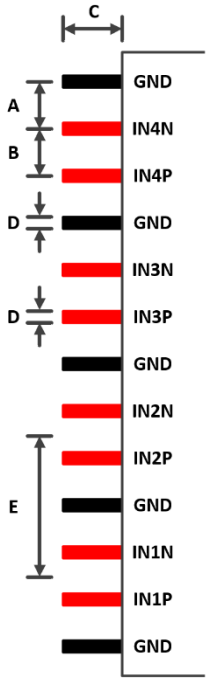
Notes:

1. Extensions to the Length parameter while keeping to the same pad frame are permitted and deemed compliant to the Implementation Agreement
2. These proposed rates are informative only to guide expected system usage

The top surface of the module is defined as the Hot Area (opposite side to the PCB).

7 High Speed Electrical Interface

The high speed electrical output interface uses surface mounted pins in a differential co-planar waveguide arrangement (GSSG), with shared ground pins. The pin definitions and pitches shall be as detailed in Table 2, Table 3, and Figure 3. It is noted that alternate channel configurations for the differential signals shown are acceptable.



Parameter	Value	
Interface type	Differential	
Channel number	4	
Channel configuration	G-S-S-G	
Signal line coupling	AC	
Signal line impedance	100 Ohm Differential	
Channel pin-out	1 2 3 4	
Differential pin-out	Signal Complimentary Signal	P N

Table 2 High speed electrical interface description

Figure 3 High speed electrical interface definition

Parameter	Symbol	Type 1 and 2 SMT Pin Dimensions (mm)			
		Min.	Typ.	Max.	Note
Signal/Ground lead pitch	A		0.8		Type 1 only
Signal/Signal lead pitch	B		0.8		Type 1 only
Signal/Ground lead pitch	A		0.875		Type 2 only
Signal/Signal lead pitch	B		0.65		Type 2 only
Signal & Ground lead length	C	1.75	2.0	2.25	
Signal & Ground lead width	D	0.15	0.2	0.25	
Channel pitch	E		2.4		

Table 3 Type 1 and Type 2 High speed electrical interface dimensions

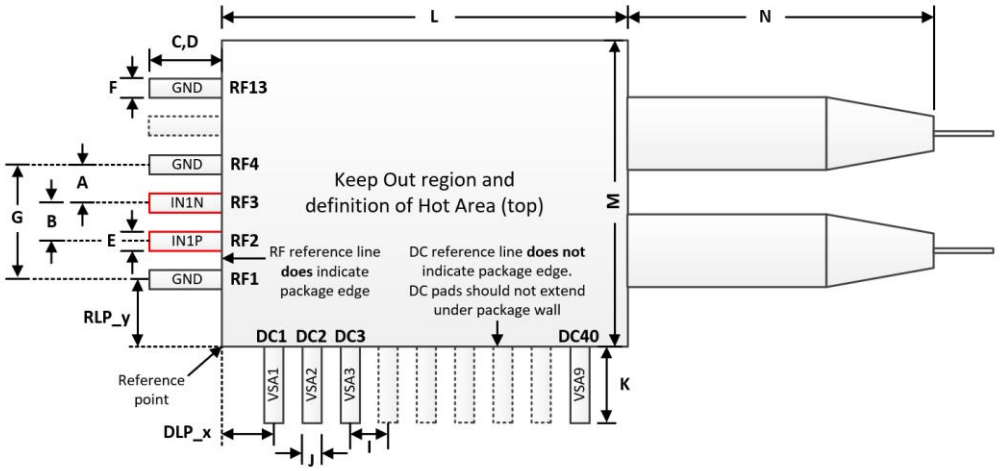


Figure 4 Type 1 and 2 RF and DC Landing Pads

Parameter	Symbol	Type 1 and 2 PCB Landing Dimensions (mm)			
		Min.	Typ.	Max.	Note
RF pad pitch (Sig-Gnd)	A		0.80		Fixed, Type 1
RF pad pitch (Sig-Sig)	B		0.80		Fixed, Type 1
RF pad pitch (Sig-Gnd)	A		0.875		Fixed, Type 2
RF pad pitch (Sig-Sig)	B		0.65		Fixed, Type 2
RF pad length (Sig)	C	2.55			
RF pad length (Gnd)	D	2.55			
RF pad width (Sig)	E	0.35			
RF pad width (Gnd)	F	0.35			
RF Channel pitch	G		2.4		Fixed
DC Channel pitch	I		0.70		Fixed
DC pad width	J	0.35			
DC pad length	K	3.10			
x_keep_out	L	Standard		30	
		Extended		55	
y_keep_out	M			13	
boot_keep_out	N			15	
RLP_y			1.20		Fixed
DLP_x			1.00		Fixed

Table 4 Type 1 and Type 2 Landing Pad Dimension Table

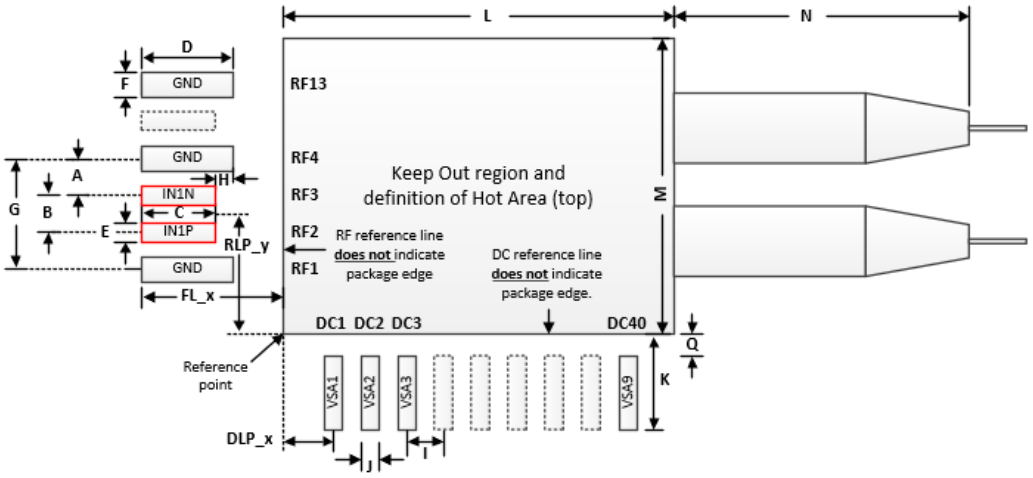


Figure 5 Type 3 RF and DC Landing Pads

Parameter	Symbol	Type 3 PCB Landing Dimensions (mm)			
		Min.	Typ.	Max.	Note
RF pad pitch (Sig-Gnd)	A		0.975		Fixed
RF pad pitch (Sig-Sig)	B		0.45		Fixed
RF pad length (Sig)	C	0.7	0.8		
RF pad length (Gnd)	D	0.9	1.0		
RF pad width (Sig)	E	0.1	0.2		
RF pad width (Gnd)	F	0.4	1.0		
RF Channel pitch	G		2.4		Fixed
RF pad length offset (Sig/Gnd)	H		0.2		
DC Channel pitch	I		0.70		Fixed
DC pad width	J	0.35			
DC pad extension from ref line	K	3.1			
x_keep_out	L	Standard		30	
		Extended		55	
y_keep_out	M			13	
boot_keep_out	N			15	
Reference line to DC pad start	Q	0		1.1	
RLP_y			2.4		Fixed
DLP_x			1.00		Fixed
FL_x (ref. line to far pad edge)			7.0		Fixed

Table 5 Type 3 Landing Pad Dimension Table

8 Low Speed Electrical Interface

The low speed electrical connections are provided through 40 signals with the orientation shown in Figure 6 and numbered as shown in Table 6. An HB-CDM vendor may choose to populate fewer signals, but the definitions of the populated signals should match those in the table. While Vendor-Specific-Analog (VSA) signals are optional, each has an assumed function as shown. If a vendor chooses to use VSA signals for alternative functions, the electrical specification should match the listed function to allow electrical compatibility so as not to damage module or host.

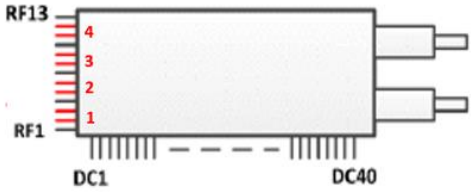


Figure 6 RF and DC signal orientation

For Table 6, refer to Figure 2 for reference numbers for PHASE#, MPD# and SOA#

Pin DC#	Signal Name	Description	Pin DC#	Signal Name	Description
1	VSA1	VSA / pre-SOA 3, 4 Anode (current)	21	PHASE3N	MZ Phase control or VSA
2	VSA2	VSA / pre-SOA 1, 2 Anode (current)	22	PHASE4P	MZ Phase control
3	VSA3	VSA / Pilot (voltage)	23	PHASE4N	MZ Phase control or VSA
4	GND	Ground	24	PHASE5P	MZ Phase control
5	VCC	3.3V supply	25	PHASE5N	MZ Phase control or VSA
6	SPI-RST	SPI Reset	26	PHASE6P	MZ Phase control
7	SPI-MISO	SPI MasterInSerialOut	27	PHASE6N	MZ Phase control or VSA
8	SPI-MOSI	SPI MasterOutSerialIn	28	THERMP	Thermistor +
9	SPI-CLK	SPI Clock	29	THERMN	Thermistor -
10	SPI-CS	SPI ChipSelect	30	TECN	TEC power -
11	VDR-BIAS	Driver far end bias	31	TECP	TEC power +
12	VSUB1	MZ substrate bias (voltage)	32	GND	Ground
13	VSA4	VSA / MZ substrate bias2	33	MPD-A3	Monitor PD Anode 3 or VSA
14	VSA5	VSA / MZ substrate bias3	34	MPD-C3	Monitor PD Cathode 3 or VSA
15	VSA6	VSA / MZ substrate bias4 (or GND)	35	MPD-A1	Monitor PD Anode 1 or VSA
16	PHASE1P	MZ Phase control	36	MPD-A2	Monitor PD Anode 2 or VSA
17	PHASE1N	MZ Phase control or VSA	37	MPD-C12	Monitor PD Cathode 1 and 2 or VSA
18	PHASE2P	MZ Phase control	38	VSA7	VSA / post SOA 1, 2 Anode (current)
19	PHASE2N	MZ Phase control or VSA	39	VSA8	VSA / post SOA 3 ,4 Anode (current)
20	PHASE3P	MZ Phase control	40	VSA9	VSA / post SOA Cathode (current)

Table 6 Low speed electrical interface definition

Notes:

1. VSA1 and VSA2 use common Cathode to GND for the pre-SOA
2. Thermistor function may be implemented with a single THERMP pin in which case THERMN becomes VSA (optionally connected to GND).
3. PHASE#N controls may be omitted for single-end bias adjust implementations and VSA used in place
4. VOA functionality may be included and controlled by VSA pins

9 Electro-Optical Specifications

Basic operating characteristics and specifications are listed in Table 7 at the End of Life over the operating temperature and frequency ranges.

Parameter		Unit	Min	Typ	Max	Remarks/Note
Operating frequency	C-band	THz	191.35		196.20	Note 1
	L-band		186.00		191.50	
Optical input power		dBm			18	Peak power
Insertion loss		dB			16	Per polarization
PDL		dB			1	
Optical return loss		dB		27		Input and output
Parent MZI ER		dB		22		
Child MZI ER		dB		25		
Polarization ER		dB		20		
Monitor PD bias voltage	Option 3.3	V	3.14	3.3	3.46	Note 2
	Option 5.0		4.75	5.0	5.25	
Monitor PD responsivity (combined, referred to output power)		mA/W	10		800	Note 3
Monitor PD Bandwidth (combined)		GHz	1			Note 3
Monitor PD Bandwidth (per pol)		GHz	0.1			Note 3
VOA control voltage (optional)		V	0		9	Note 4
Thermistor resistance		kOhm		10		At 25°C
Thermistor beta value		K		3930		
TEC voltage		V	-3.3		3.3	Note 6
TEC current		A	-1.8		1.8	Note 6
Driver Supply Voltage		V	3.14	3.3	3.46	
VDR-BIAS (Driver far end termination)		V			6.0	Class 40
VDR-BIAS (Driver far end termination)		V			7.0	Class 60 and 80
Maximum differential input swing		mVpp	600			Note 7
Minimum differential input swing		mVpp			300	Note 7
RF differential impedance		Ohm		100		
S21 E/O Bandwidth (3dB), referenced to 1GHz						+/- 1GHz span moving average See Figure 7, 9 and 11
S11 electrical return loss						See Figure 8, 10 and 12
I/Q skew (channels 1/2 or 3/4)		ps			50	
Total skew		ps			100	

I/Q skew variation (channels 1/2 or 3/4)		ps			1.5	
Total skew variation		ps			4	
Low frequency cut-off		MHz			1	
ESD (HBM)		V	250			
Operating humidity (non-condensing)		%RH	5		85	
Operating temperature	Standard	°C	-5		75	Note 5
	Preferred		-5		80	
Power dissipation	Class 40	W			4.5	Note 6
	Class 60				5.5	
	Class 80				6.5	

Table 7 Electro-Optical Specifications and Operating Characteristics

Notes:

1. Specifications should be maintained across at least one of the described ranges.
2. Vendor shall state which Bias Voltage Option or Options are allowed.
3. Monitor PDs are optional.
4. The VOA shall be of type “normally bright”.
5. The operating temperature is defined as the minimum/maximum of the HB-CDM case “hot zone” surface temperature.
6. Over the Standard Operating Temperature as defined in the table. Higher TEC voltage is preferred over higher TEC current for overall TEC efficiency and TEC driver/controller solution size.
7. Peak to peak differential. HB-CDM contains AC coupling capacitors. Normative input swing is 300 to 600mVppd.
8. THD is not defined in this IA and remains Application Specific and should be included in the HB-CDM Vendor Specification.

10 Power Sequencing Requirements

The following baseline power sequence is recommended but informative as HB-CDM vendors and customers have the flexibility to change with agreement between them:

Power On:

1. TEC enable
2. Enable substrate bias and set voltage VSUB to the maximum VDR-BIAS value
3. Enable driver VCC (3.3V supply)
4. Establish driver VDR-BIAS within 1s
5. Adjust substrate bias VSUB to final set point
6. Enable SOAs if present
7. Enable remaining pins

Power Off:

1. Disable SOAs if present
2. Disable VDR-BIAS
3. Disable VCC within 1s
4. Disable substrate bias VSUB
5. Disable remaining pins

11 RF Frequency Response

11.1 Measurement Methods

The HB-CDM electrical-to-optical S_{21} transfer function and S_{11} electrical return loss frequency responses shall be measured *differentially* to evaluate conformance to the RF masks in Section 11.2.

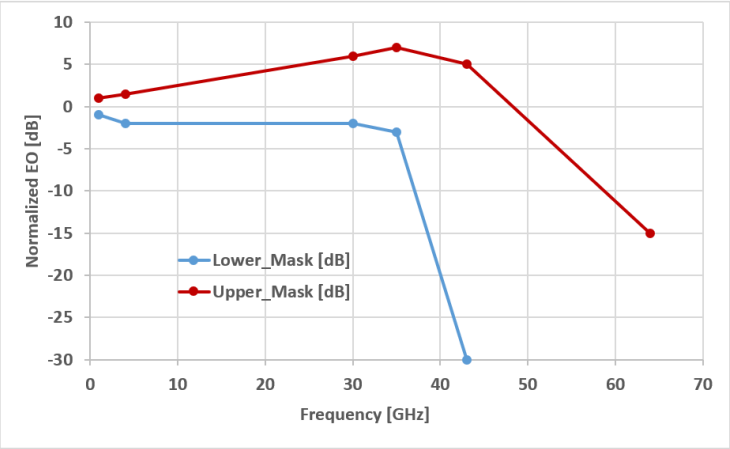
For these measurements, the HB-CDM shall be *soldered* to the measurement test fixture, and the collected data shall be de-embedded to the *RF reference point*. The *RF reference point* is defined as the point on the Host PCB RF traces that is 2.5mm beyond the maximum extent of the HB-CDM RF lead pad.

The masks of Figure 7 to Figure 12 show *target* ranges for the electrical-to-optical S_{21} transfer functions and S_{11} electrical return loss frequency responses, allowing for component to component variations. These masks may be revised in a future revision of the document as more component and system level performance data becomes available.

11.2 EO S_{21} Transfer Function Masks

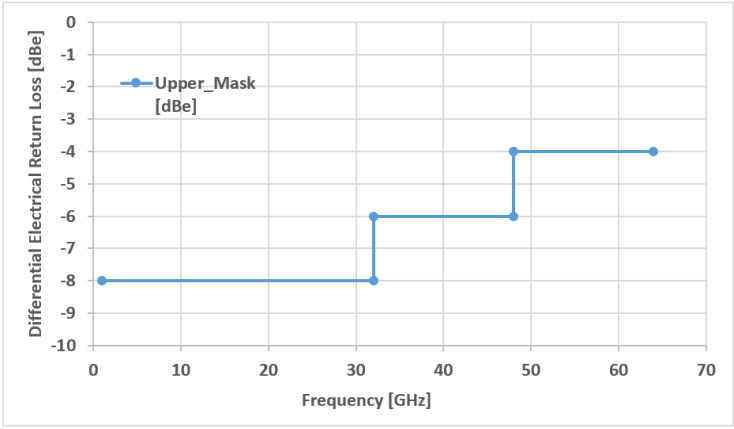
The ideal RF frequency response for the transmit chain of a coherent modem – consisting of the DAC at the output of the ASIC, the differential signal traces between the DSP and the HB-CDM – is a low pass response which is flat up to the targeted signal bandwidth and rolls off steeply beyond that. Given that the losses of the signal traces between the DSP ASIC and the HB-CDM increase gradually with frequency, it is generally preferred that the RF frequency response of the HB-CDM increases gradually with frequency up to the targeted signal bandwidth, and then rolls off steeply.

The S_{21} transfer functions shall be measured at a HB-CDM gain condition and temperature agreed with the customer. All S_{21} responses shall be normalized to the response at 1GHz. It is assumed that any Driver functionality that manipulates the S_{21} transfer function (i.e. bandwidth adjust functions) can be utilized to obtain compliance with the masks provided in this section.



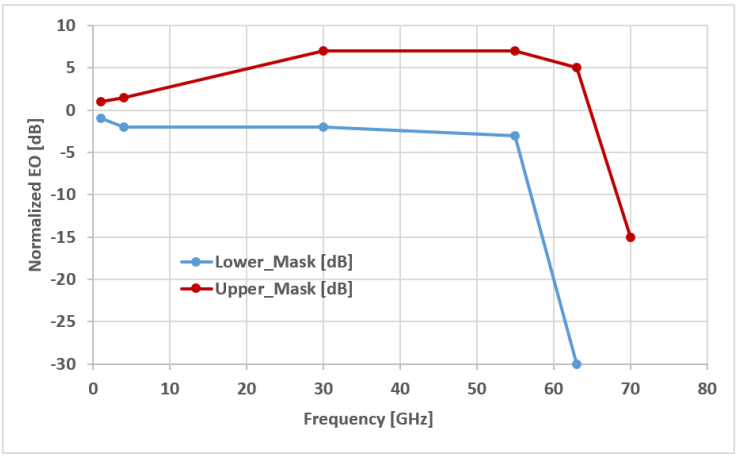
Frequency [GHz]	Lower_Mask [dB]	Upper_Mask [dB]
1	-1	1
4	-2	1.5
30	-2	6
35	-3	7
43	-30	5
64		-15

Figure 7 Normalized EO S_{21} transfer function mask for Class-40 HB-CDMs



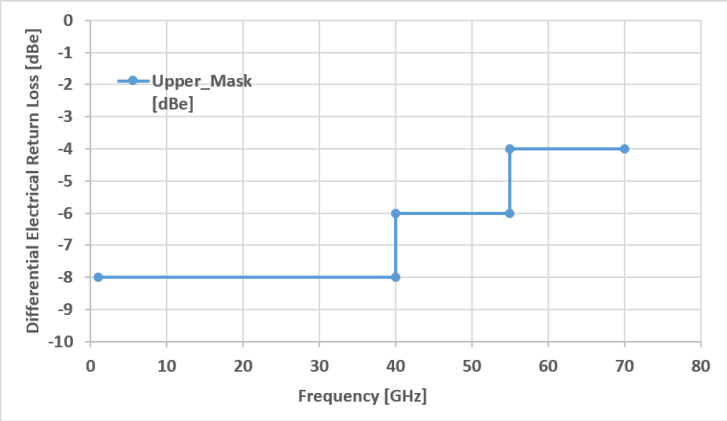
Frequency [GHz]	Upper_Mask [dBe]
1	-8
32	-8
32	-6
48	-6
48	-4
64	-4

Figure 8 Differential S_{11} electrical return loss mask for Class-40 HB-CDMs



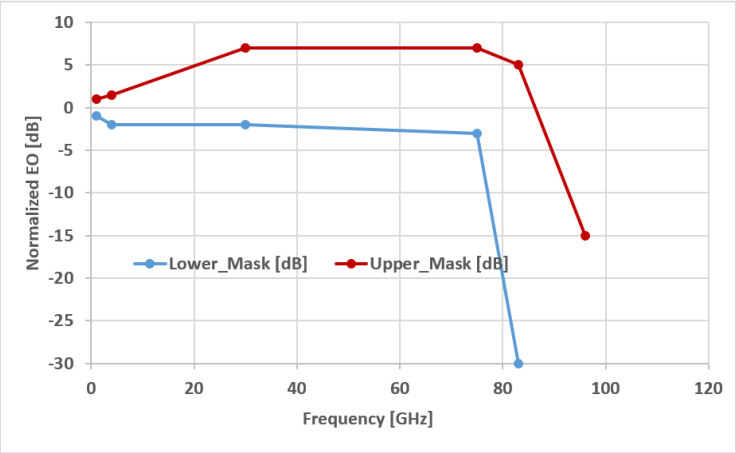
Frequency [GHz]	Lower_Mask [dB]	Upper_Mask [dB]
1	-1	1
4	-2	1.5
30	-2	7
55	-3	7
63	-30	5
70		-15

Figure 9 Normalized EO S_{21} transfer function mask for Class-60 HB-CDMs



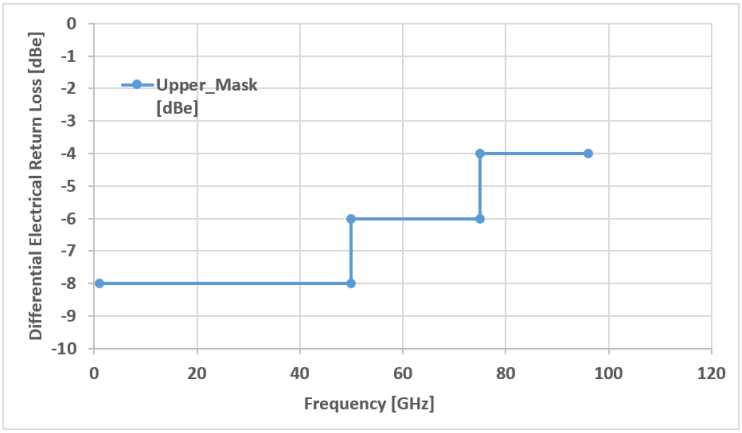
Frequency [GHz]	Upper_Mask [dBe]
1	-8
40	-8
40	-6
55	-6
55	-4
70	-4

Figure 10 Differential S_{11} electrical return loss mask for Class-60 HB-CDMs



Frequency [GHz]	Lower_Mask [dB]	Upper_Mask [dB]
1	-1	1
4	-2	1.5
30	-2	7
75	-3	7
83	-30	5
96		-15

Figure 11 Normalized EO S_{21} transfer function mask for Class-80 HB-CDMs



Frequency [GHz]	Upper_Mask [dBe]
1	-8
50	-8
50	-6
75	-6
75	-4
96	-4

Figure 12 Differential S_{11} electrical return loss mask for Class-80 HB-CDMs

12 Fiber Types

The input and output optical fiber types are defined in Table 8.

Parameter		Unit	Min	Typ	Max	Note
"Minimum bend radius" specification for PM fiber input		Mm			7.5	1, 2
"Minimum bend radius" specification for SM fiber output	Option 1	Mm			5.0	3
	Option 2				7.5	4
Fiber cladding diameter (SM and PM)		µm		125		
Fiber coating diameter (SM and PM)		µm		250		
PM fiber colour				Transparent		
SM fiber colour				Red		

Table 8 Input fiber characteristics

Notes:

1. The polarization state in the PM fiber shall be aligned to the slow axis of the PM fiber.
2. The slow axis of the PM fiber shall be aligned to the connector key.
3. The Option 1 SMF shall be compliant to ITU-T Recommendations G.657.B3 and G.652.D.
4. The Option 2 SMF shall be compliant to ITU-T Recommendations G.657.B2 and G.652.D.

13 SPI Based Low Speed Electrical Interface

The Low Speed control method for the Driver inside the HB-CDM is SPI and the following sections describe the Voltage Specifications, Read/Write Datagram, Operation Diagrams and Timing Specifications. Register definitions are not contained in this Implementation Agreement as these are deemed Vendor Specific and are not required to enable hardware compatibility between HB-CDM vendor units. The HB-CDM is defined as the *Client* or *Slave* in the SPI interface with the terms used interchangeably.

Hardware features controlled by the SPI interface may include, but are not required or limited to:

- Gain control
- Equalization/Peaking control
- Reading the output signal level
- Die temperature reading

Signal name	In/Out	Function
SCLK	In	SPI Clock
MISO	Out	Master In Serial Out
MOSI	In	Master Out Serial In
CS	In	Chip Select (active low)
RST	In	Reset (active low)

Table 9 SPI Control Signals

13.1 SPI Interface Voltage and Control Specifications

The SPI used is a full duplex synchronous serial interface originally defined by Motorola. The key voltage and control specifications are summarized in Table 10.

Parameter	Conditions	Unit	Value	
			Min	Max
Voltage threshold levels[2]	V_{IL}	V	-0.3	0.8
	V_{IH}	V	2.0	VCC + 0.3
	V_{OL}	V		0.4
	V_{OH}	V	VCC – 0.4	VCC
IO Standard[2]	LVCMOS	V	3	3.6
SCLK cycle time		ns	50	1000
SCLK frequency[1]		MHz	1	20
Time delay between asserting CS and toggling SCLK		ns	25	
Data register width	Address+Op-code	bit	16	
	Data block	bit	16	
Data register shift direction			MSB first	
Clock polarity			Idle state for CLK is low	
Clock phases			Data is latched on the leading edge of CLK, data changes on the trailing edge	
Client select state for data transmission			Chip select for read/write commands (active low)	
Client reset (via Reset pin)			Asynchronous Reset (active low)	

Table 10 SPI voltage and control specification

Notes:

1. SPI control can be operated by any specific frequency within the Min/Max range.
2. Type 2 and Type 3 optionally support a V_{IH} (min) of 1.5V to enable 1.8V logic compatibility

13.2 SPI Read / Write Datagram

Table 11 depicts the data structure of the SPI command datagram. The protocol is designed to work with OIF IA compliant HB-ICR receivers using SPI control, where the HB-ICR addressing will reside in memory addresses 0x0000 to 0x01fff and the HB-CDM will reside in memory addresses 0x0200 to 0x03fff.

	Opcode – 16b																Data Block – 16b															
	HB-CDM device select						Chan* Address		Register Address							RW	Data in via MOSI, or Data out via MISO															
Bit#	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0	R/W	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Value	0	0	0	0	0	1	00 = 1 01 = 2 10 = 3 11 = 4		Select register							0=W 1=R	Data															

* Chan Address references are defined in Figure 2-1.

Table 11 SPI data telegram structure

When an SPI controlled HB-ICR and a HB-CDM are connected in-system, they may share all the SPI signaling without duplication as shown in Figure 13 below as long as unique addressing and highZ MISO modes are available for both devices.

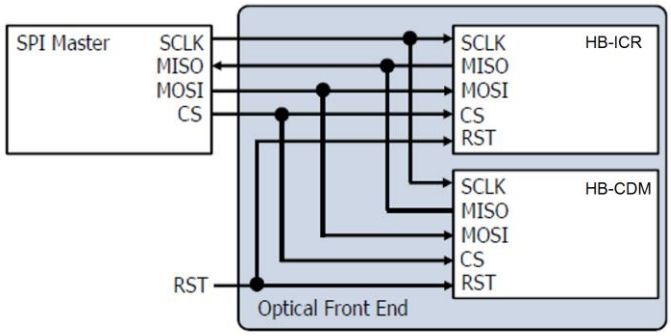


Figure 13 Connection example of SPI controlled HB-ICR and HB-CDM, when MISO sharing by address space is enabled on both devices

13.3 SPI Read / Write Operation Timing Diagrams

Figure 14 and Figure 15 show the SPI write operation timing and the SPI read timing operation.

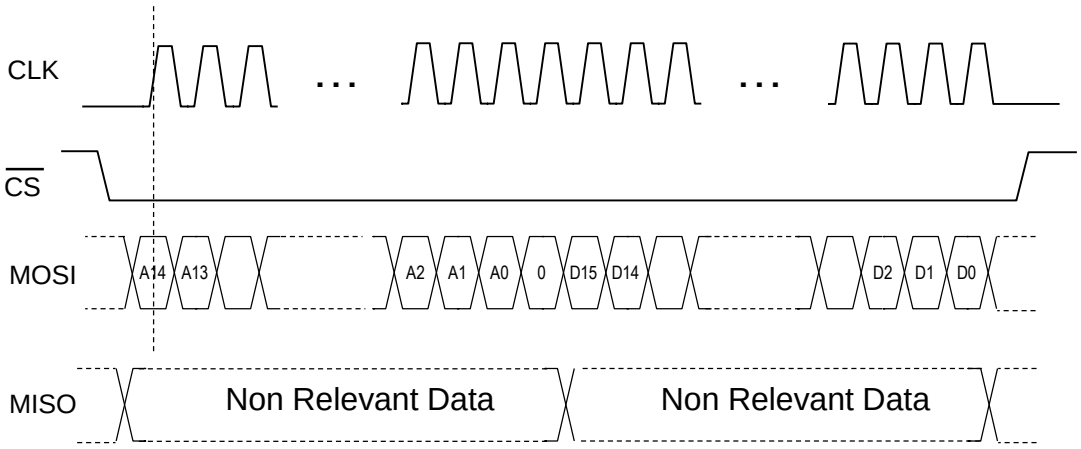


Figure 14 SPI write operation timing diagram

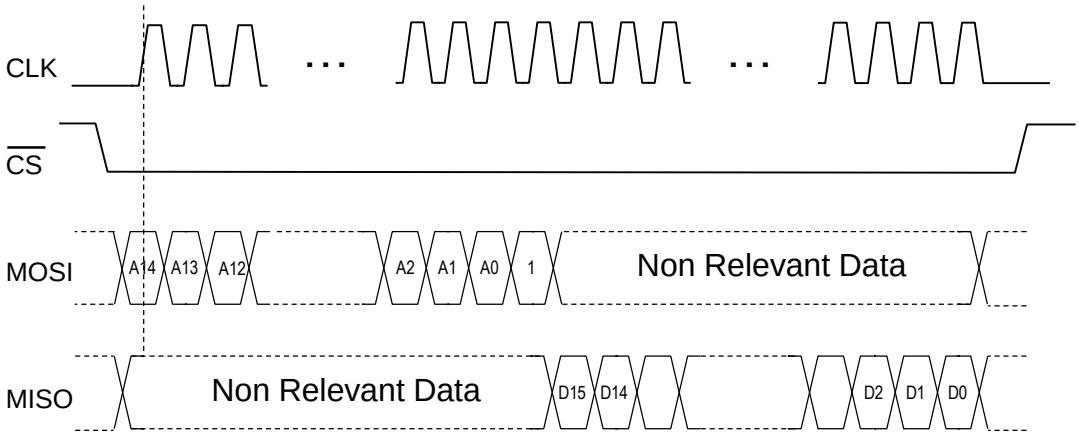


Figure 15 SPI read operation timing diagram

13.4 SPI Timing Specifications

The SPI timing specifications are summarized in Table 12 and illustrated in Figure 16 and Figure 17. The SPI client hardware reset is defined as asynchronous. After the reset, the Driver configuration should be returned to its defaults.

Description	Condition	Symbol	Unit	Value	
				min.	max.
CLK clock frequency			MHz	1	20
CLK clock period		t_{CK}	ns	50	1000
CLK peak-peak jitter			ps		500
CLK high time		t_{CKH}	ns	20	550
CLK low time		t_{CKL}	ns	20	550
CLK 10%-90% rise time	15 - 18 pF capacitive load	t_{CKR}	ns	0.5	5
CLK 10%-90% fall time		t_{CKF}	ns	0.5	5
CSN to SPI CLK↑ setup time		t_{CSCK}	ns	50	1000
CLK ↓ to SPI CSN hold time		t_{CKCS}	ns	50	1000
CLK ↓to SPI MISO valid time	15 - 18 pF capacitive load	t_{CKSO}	ns	2	11
MISO 10%-90% rise time	15 - 18 pF capacitive load	t_{SOR}	ns	0.5	5
MISO 10%-90% fall time		t_{SOF}	ns	0.5	5
MOSI to SPI CLK↑ edge setup time		t_{MOCK}	ns	8	
MOSI to SPI CLK↑ edge hold time		t_{CKMO}	ns	8	
MOSI 10%-90% rise time		t_{MOR}	ns	0.5	5
MOSI 10%-90% fall time		t_{MOF}	ns	0.5	5
Min. SPI access inactive time		t_{CSCS}	ns	$5*t_{CK}$	
RSN time		t_{RS}	ns	t_{CK}	
RSN10%-90% rise time	15 - 18 pF capacitive load	t_{RSR}	ns	0.5	5
RSN10%-90% fall time		t_{RSF}	ns	0.5	5

Table 12 SPI read / write timing specifications

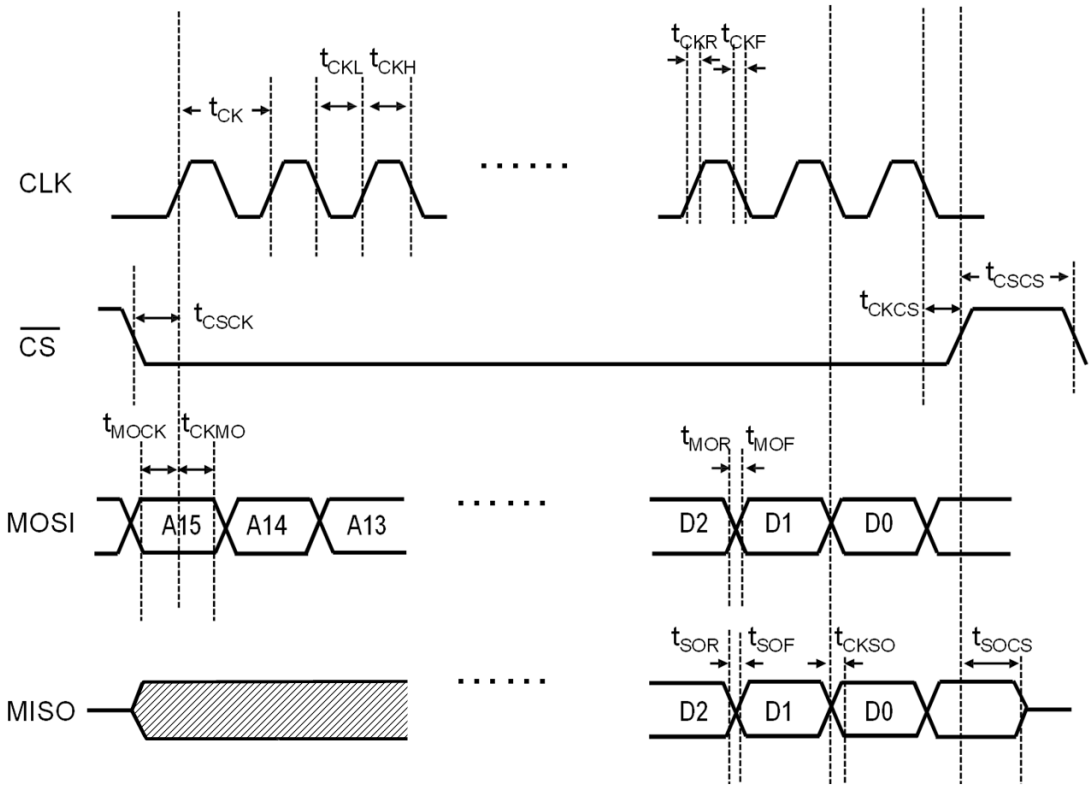


Figure 16 SPI client read/write timing

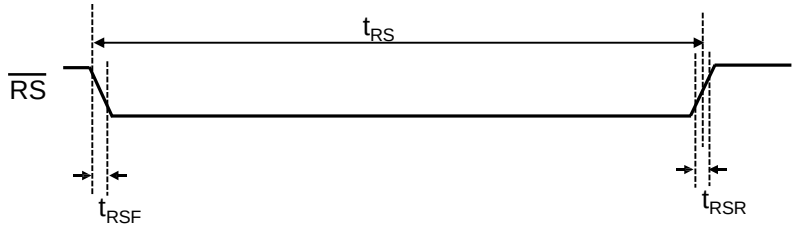


Figure 17 SPI client reset timing – asynchronous

13.5 SPI Registers Specification

Register maps are not defined as part of this Implementation Agreement except for Address 0x0200 which should be reserved for a 16bit Driver manufacturer vendor ID to allow device specific register maps and capabilities to be loaded.

The Vendor ID should follow the LSB 16bits of the 24bit Organizationally Unique Identifier (OUI) code system assigned to device manufacturers by the IEEE. If a manufacturer doesn't have an OUI, another unique identifier may be used as the Vendor ID.

Further information on OUI numbers is available from:

https://en.wikipedia.org/wiki/Organizationally_unique_identifier

Currently assigned OUI numbers are listed here:

http://standards-oui.ieee.org/oui.txt

Extra functions that could be provided as part of the SPI register map include:

- Gain control
- Equalization/Peaking control
- Peak detector reading
- Unique serial number tracking ability
- Temperature readout

For a HB-CDM module to be compliant to this Implementation Agreement, only the Address 0x0200 device manufacturer register is a strict requirement, all other functions are optional.

14 References

14.1 Informative references

- OIF-HB-CDM-01.0 – Implementation Agreement for the High Bandwidth Coherent Driver Modulator
- OIF-DPC-RX-01.2 – Implementation Agreement for Integrated Dual Polarization Intradyne Coherent Receivers (November 2013)
- OIF-CFP2-ACO-01.0 – Implementation Agreement for Analogue Coherent Optics Module (January 2016)
- OIF-HBPMQ-TX-01.0 – Implementation Agreement for the High Bandwidth Integrated Polarization Multiplexed Quadrature Modulators

15 Appendix A: Glossary

ADC	Analog to Digital Converter
AGC	Automatic Gain Control
BS	Beam Splitter
CMRR	Common Mode Rejection Ratio
DSP	Digital Signal Processor
FPC	Flexible Printed Circuit
Gbaud	10^9 Symbols per second
IA	Implementation Agreement
HB-ICR	High Bandwidth Intradyne Coherent Receiver
MPD	Monitor Photodiode
MSA	Multi-Source Agreement
OIF	Optical Internetworking Forum
PBS	Polarization Beam Splitter
PCB	Printed Circuit Board
SOA	Semiconductor Optical Amplifier
SPI	Serial Port Interface
THD	Total Harmonic Distortion
VOA	Variable Optical Attenuator
VSA	Vendor-Specific-Analog (signal type)

16 Appendix B: Open Issues / current work items

17 Appendix C: List of companies belonging to OIF when document was approved

Accton Technology Corporation	MACOM Technology Solutions
ADVA Optical Networking	Marvell Semiconductor, Inc.
Alibaba	Maxim Integrated Inc.
Alphawave IP Inc.	MaxLinear Inc.
Amphenol Corp.	MediaTek
AnalogX Inc.	Microchip Technology Incorporated
Applied Optoelectronics, Inc.	Microsoft Corporation
Ayar Labs	Molex
BitifEye Digital Test Solutions GmbH	Multilane Inc.
Broadcom Inc.	NEC Corporation
Cadence Design Systems	NeoPhotonics
CICT	Nitto Denko Corporation
China Telecom	Nokia
Ciena Corporation	NTT Corporation
Cisco Systems	Nubis Communications, Inc.
Commscope Connectivity Belgium BVBA	NVIDIA Corporation
Corning	O-Net Communications (Shenzhen) Limited
Credo Semiconductor (HK) LTD	Open Silicon Inc.
Dell, Inc.	Optomind Inc.
DustPhotonics	Orange
EFFECT Photonics B.V.	PETRA
Eoptolink Technology	Precise-ITC, Inc.
Epson Electronics America, Inc.	Quintessent Inc.
ETRI	Rambus Inc.
Facebook Inc.	Ranovus
Foxconn Interconnect Technology Ltd	Rockley Photonics
Fujikura	Rosenberger Hochfrequenztechnik GmbH & Co. KG
Fujitsu	Samsung Electronics Co. Ltd.
Furukawa Electric Japan	Samtec Inc.
Global Foundries	Semtech Canada Corporation
Google	Senko Advanced Components
Hewlett Packard Enterprise (HPE)	Sicoya GmbH

Hisense Broadband	SiFotonics Technologies Co., Ltd.
Huawei Technologies Co., Ltd.	Socionext Inc.
I-Pex	Source Photonics, Inc.
IBM Corporation	Spirent Communications
Idea Sistemas Electronicos S.A.	Sumitomo Electric Industries, Ltd.
II-VI Incorporated	Sumitomo Osaka Cement
Infinera	Synopsys, Inc.
InnoLight Technology Limited	TE Connectivity
Innovium	Telefonica S.A.
Integrated Device Technology	TELUS Communications, Inc.
Intel	US Conec
IPG Photonics Corporation	Viavi Solutions Deutschland GmbH
Juniper Networks	Wilder Technologies, LLC
Kandou Bus	Xelic
KDDI Research, Inc.	Xilinx
Keysight Technologies, Inc.	Yamaichi Electronics Ltd.
Lumentum	ZTE Corporation
Luxshare-ICT	