OIF's CEI 56G Interfaces – Key Building Blocks for Optics in the 400G Data Center

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Agenda

- Interconnect challenges facing next-generation 200G/400G data centers
- Overview of OIF's CEI-56G projects
- 56G VSR chip-to-module example
- Other OIF projects addressing the Data Center
- Summary

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Data Center (DC) Trends

- **2015 Data Center facts**
  - **DC traffic > 5 ZB in 2015, much of that being intra-DC**
  - **Inter-DC traffic growth to increase at a higher rate than intra-DC**
  - **DC SDN based networks**
- **Data center interconnect (DCI) becoming a significant portion of DC overall cost and power consumption**
- **Expect significant growth of DCI market addressing geographically dispersed sites**
- **10G/40G/100G in deployment now, 25G/50G/200G/400G on the horizon**

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Data Center Interconnect Challenges

- **Power efficiency (pJ/bit or mW/Gb/s)**
- **Port density (Gb/s/mm^2)**
- **Reach (km)**
- **Cost efficiency ($/Gb/s)**

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Technologies Enabling Future DC Client Interconnects

- **Electrical passive/active cabled interconnect (e.g. twin-ax)**
- **Multi-mode/single-mode VCSELs**
- **Single-mode Si Photonics**
- **Single-mode Coarse Wavelength Division Multiplexing (CWDM)**
- **PAM-4 modulation**
- **System Forward Error Correction (e.g. RS(528,514) FEC)**

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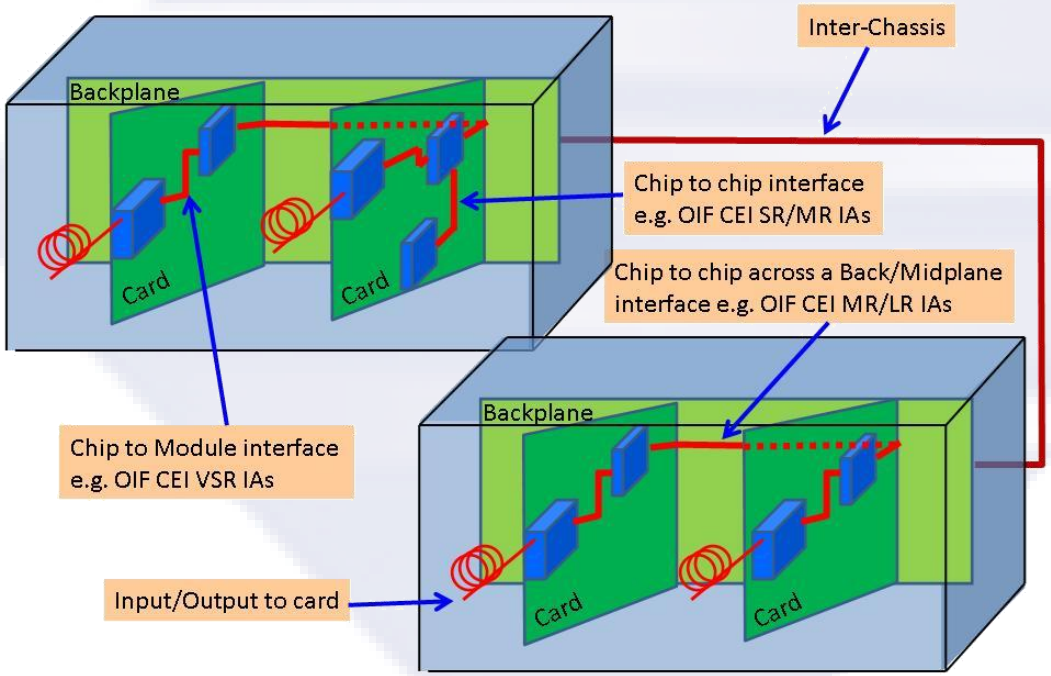
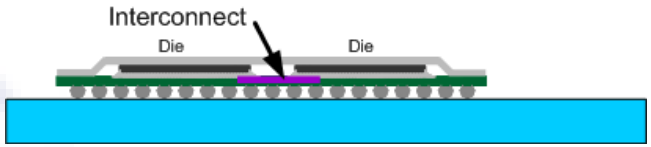
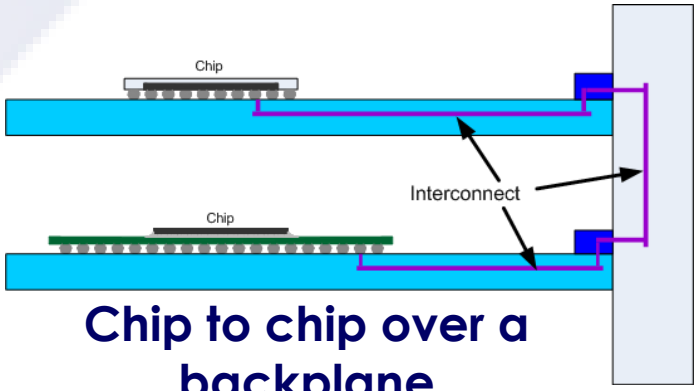
Next Generation Interconnect Framework

- **Identify the application spaces that might benefit from Implementation Agreements**





Die to Die



Chip to chip over a backplane

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OIF Physical and Link Layer Projects

- CEI – 56G – Ultra Short Reach (CEI-56G-USR)
- CEI – 56G – Extra Short Reach (CEI-56G-XSR)
- CEI – 56G – Very Short Reach (CEI-56G-VSR)
- CEI – 56G – Medium Reach (CEI-56G-MR)
- CEI – 56G – Long Reach (CEI-56G-LR)

- Flex Ethernet Project
- MLG (Multi-Link Gearbox) 3.0

- Intermediate Reach DWDM Framework
- Electro-Mechanical Footprint for Optical Engines in a Chip Scale Package
- CFP2 Analog Coherent Optics Module (CFP2-ACO)
- Integrated Polarization Multiplexed Quadrature Modulated Transmitters for Metro Applications
- High Bandwidth Polarization Multiplexed Quadrature Transmitter
- High Bandwidth Integrated Coherent Receiver

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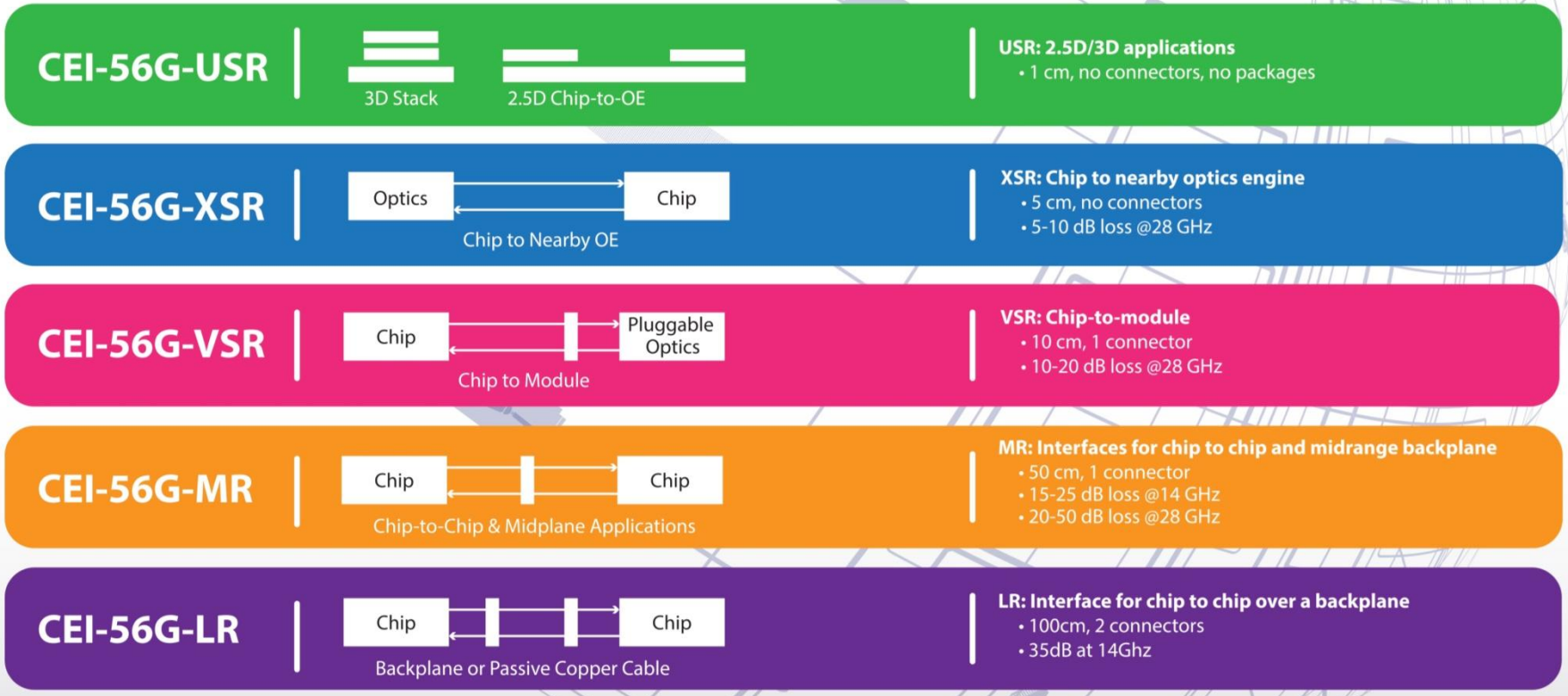
OIF CEI-56G Projects

- **CEI-56G is leading the drive to higher bandwidths**
- **Projects underway in five link reaches with multiple modulations**



CEI-56G Electrical Modulation Variants

- **OIF is pursuing multiple modulation variants for several reaches including NRZ, PAM-4 and ENRZ**

Interface	NRZ	PAM-4	ENRZ
CEI-56G-USR	•		
CEI-56G-XSR	•	•	
CEI-56G-VSR	•	•	
CEI-56G-MR	•	•	
CEI-56G-LR		•	•

- **What about CEI-112G? When will it come and what will enable it?**

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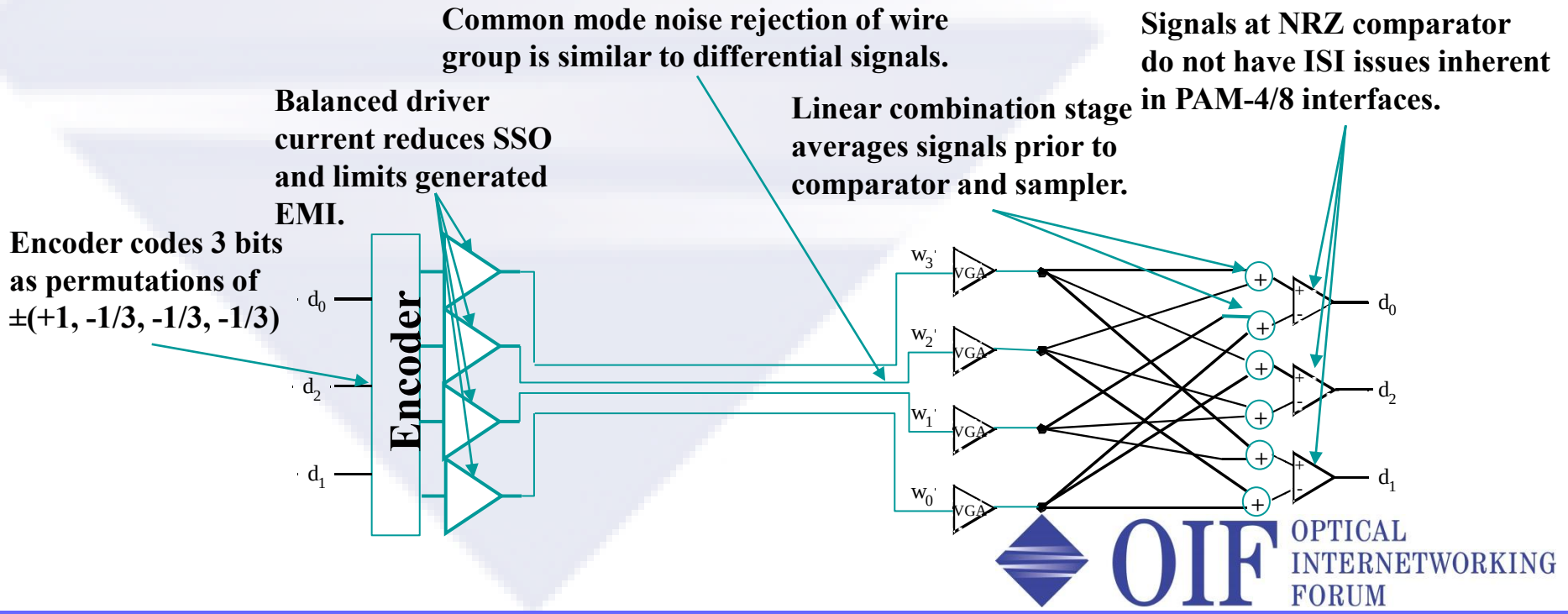
ENRZ Multiwire Code

- **ENRZ is a 3-bit over wire code that uses a channel composed of 4 correlated wires**
  - **Bandwidth per wire is higher than differential NRZ at similar baud rate**
  - **Inter-symbol Interference (ISI) is lower than PAM-4/8 interfaces**
  - **Noise rejection characteristics are similar to differential signals**
- **Because of signal integrity advantages, CEI-56G-LR-ENRZ does not require a FEC as is required for other LR variants**



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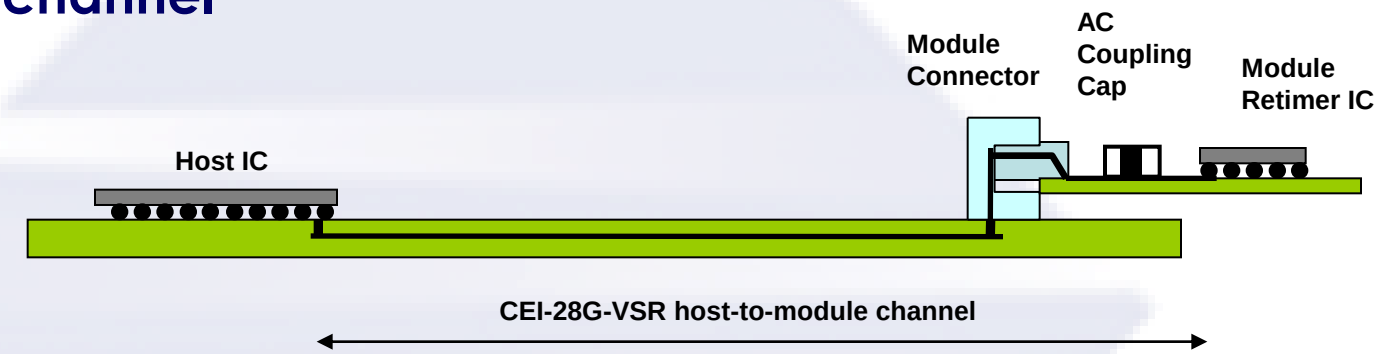
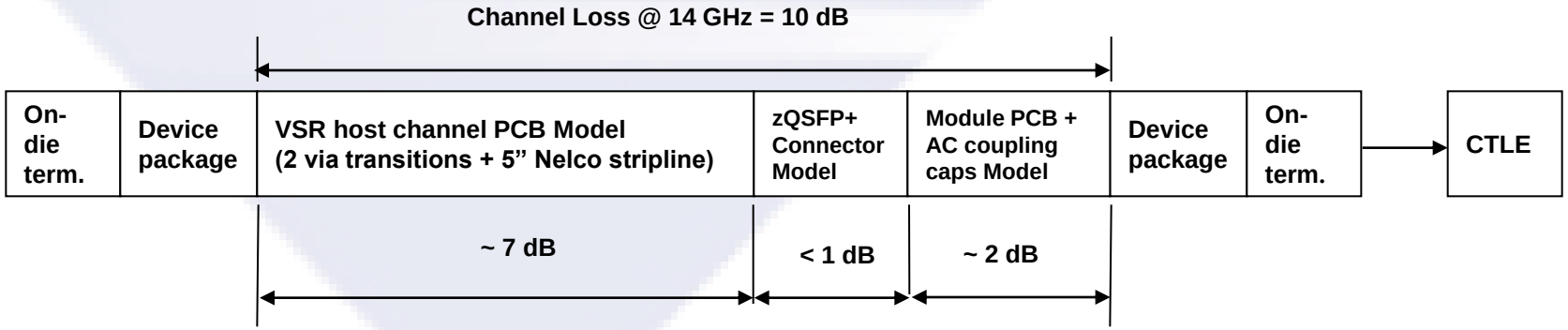
56G VSR/Chip-to-Module Channel

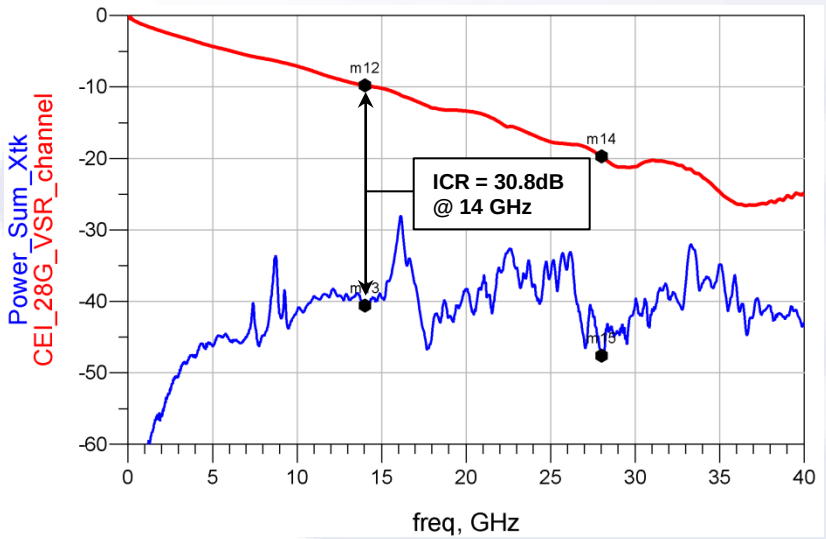
- **Potential 56G channel based upon present CEI-28G-VSR channel**





Challenges of serial 56 Gb/s electrical interconnects

Typical QSFP28 VSR Electrical Channel Loss and Crosstalk



- **Interconnect challenges:**
  - **Even premium PCB materials show significant losses for 56 Gb/s NRZ signals**
  - **Package and connector performance/crosstalk will also be an issue**
  - **Cost effective electronics with necessary performance can be an issue at 56 Gb/s**
- **More complex electrical modulation schemes should be considered**

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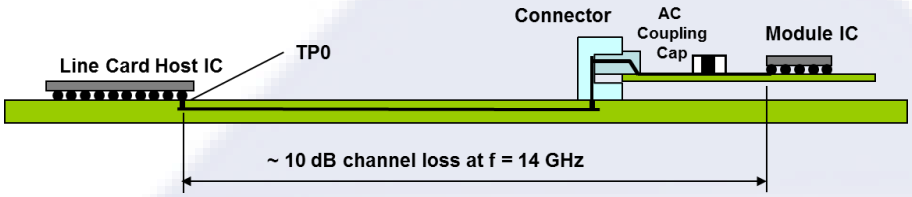
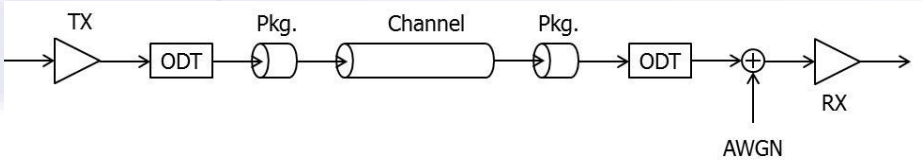
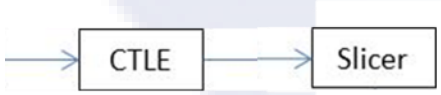
56G PAM-4 VSR Channel Simulation Parameters



Serial Link System:



CDR Input Block Diagram:



Simulation setup

- **Data pattern: PRBS23**
- **Signaling format: PAM-4**
- **Jitter**
  - **TX RJ: 0.18ps RMS**
  - **RX RJ: 0.22ps RMS**
  - **TX DJ: 1.5ps peak-to-peak**
- **Rx Noise**
  - **3.7e-8 V^2/GHz**
- **Baud rate: 28.0 Gbaud**
- **Target BER: 1e-6, 1e-15**
- **Equalization schemes**
  - **One-zero and two-pole CTLE with variable DC gain and up to 10dB AC gain at 14GHz**

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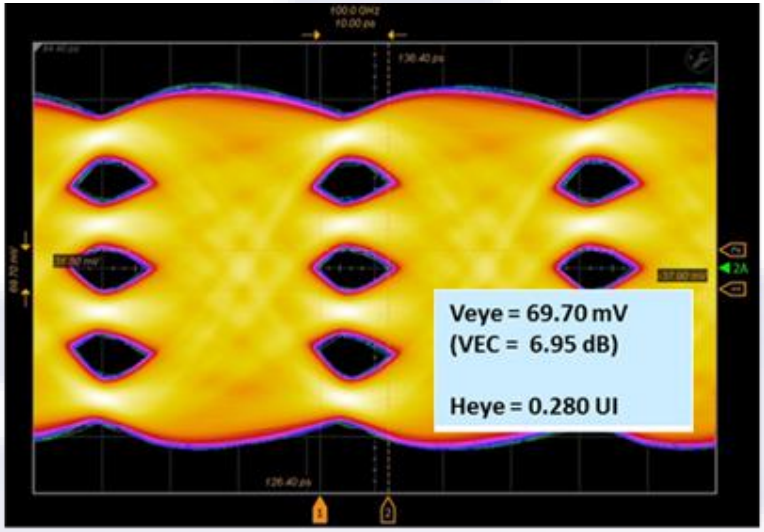
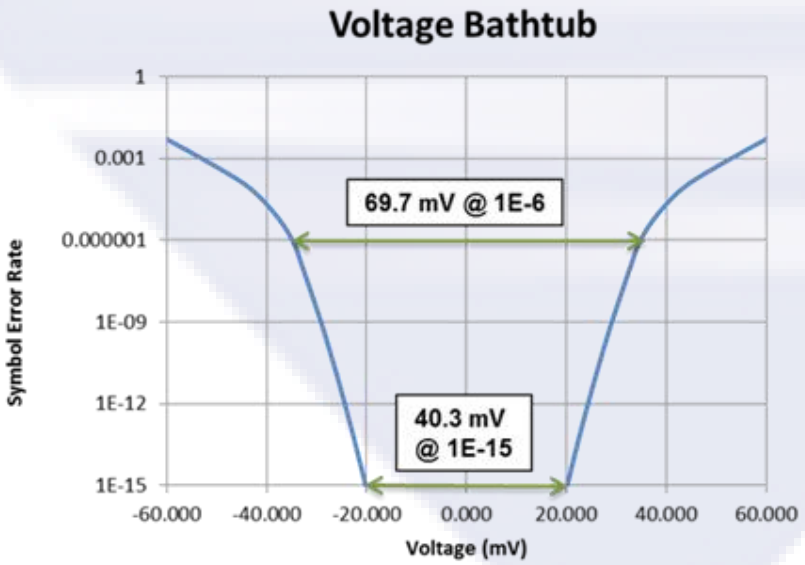
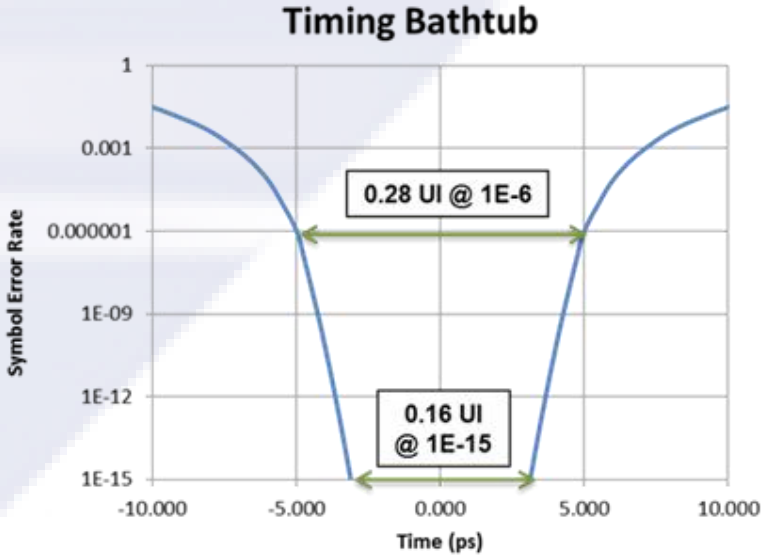
PAM4 VSR Analysis



- **1E-6 eye diagram at CDR slicer input**





- **Voltage, Timing Bathtub Curves**

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IEEE 400G 802.3bs electrical interfaces and optical PMD's

- **CDAUI-8 chip-to-module and chip-to-chip electrical interconnects selected as PAM-4 based upon OIF's CEI-56G-VSR-PAM4 and CEI-56G-MR-PAM4, respectively**
- **400G FR8/LR8 2km/10km SM PMD's based on 8x 50G PAM-4 modulation with host based FEC**
- **400G PSM4 or DR4 based on 4x 100G PAM-4**

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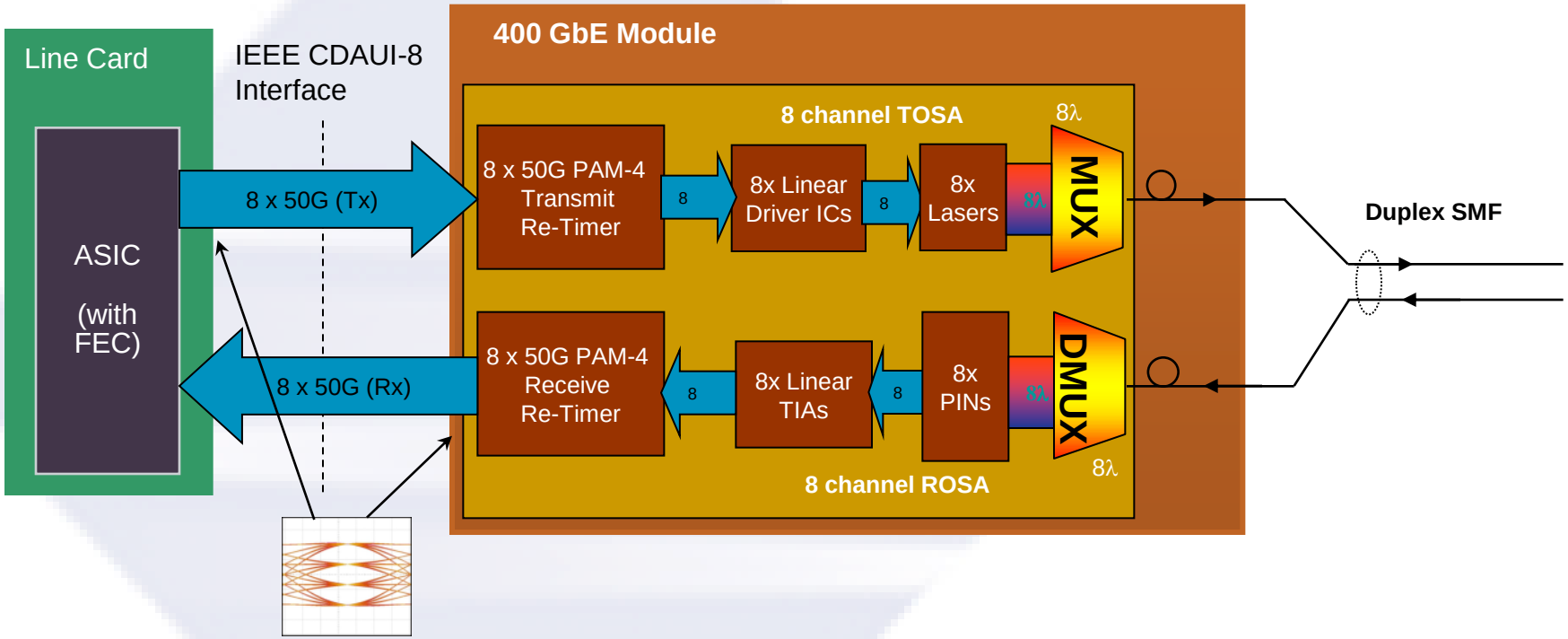
IEEE 802.3bs 400G FR8/LR8 Module (1/2)



- **CDAUI-8 c2m electrical interface based on CEI-56G-VSR-PAM4 interface**
- **c2c interface based on CEI-56G-MR-PAM4**
- **FR8/LR8 optical PMD also selected as PAM4**

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IEEE 802.3bs 400G FR8/LR8 Module (2/2)

- **400G FR8/LR8 module:**
  - **Initial 400G CDAUI-8 module could be based on a CFP2 form factor with other options to follow**
  - **This architecture can be largely implemented with present 25 Gb/s optics thus leveraging components developed for the high volume 100 GbE market**
  - **Having both PMA and PMD blocks based on PAM-4 is beneficial from several aspects**
  - **Required FEC in the host IC manages both the optical and electrical links**

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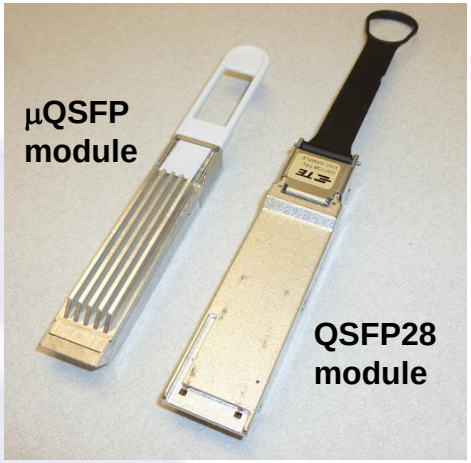
Possible future client pluggable modules based on 56G VSR host interfaces

- **50G SFP56**
  - 1x 56G client interface
- **100G QSFP56, μQSFP**
  - 2x 56G client interface
- **200G QSFP56, μQSFP**
  - 4x 56G client interface
- **400G "double" QSFP28 module**
  - 8x 56G client interface



- **At present QSFP28 is most desirable data center 100G client pluggable**
- **μQSFP targeting next generation 100G/200G data center client interconnects**

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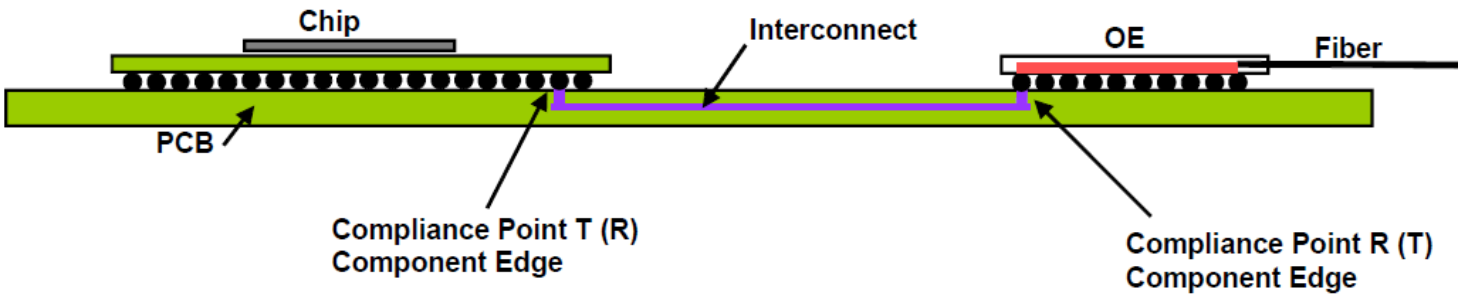
CEI-56G-XSR "Chip-to-OE" Introduction

- **56G-XSR goals:**
  - **Data rate of 39 – 56 Gb/s**
  - **BER < 1E-15**
  - **Short interconnect < 50 mm**
  - **Interface needs to be optimized for low power**

- **Related to OIF's "Electro-Mechanical Footprint for Optical Engines in a Chip Scale Package" project**



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Status of CEI-56G-XSR Specifications

- **XSR interface target BER < 1E-15 with no external FEC**
- **Interconnect is DC-coupled with 92.5 Ω diff impedance**
- **Interface timing based on a low-speed fbaud/64 common clock, traditional per lane CDR approach not explicitly mandated**
- **NRZ variant has Tx Vamp 250-400 mVpp, possibly with some Rx equalization**
- **PAM4 variant has Tx Vamp = 400-600mVpp, with Rx equalization being required**

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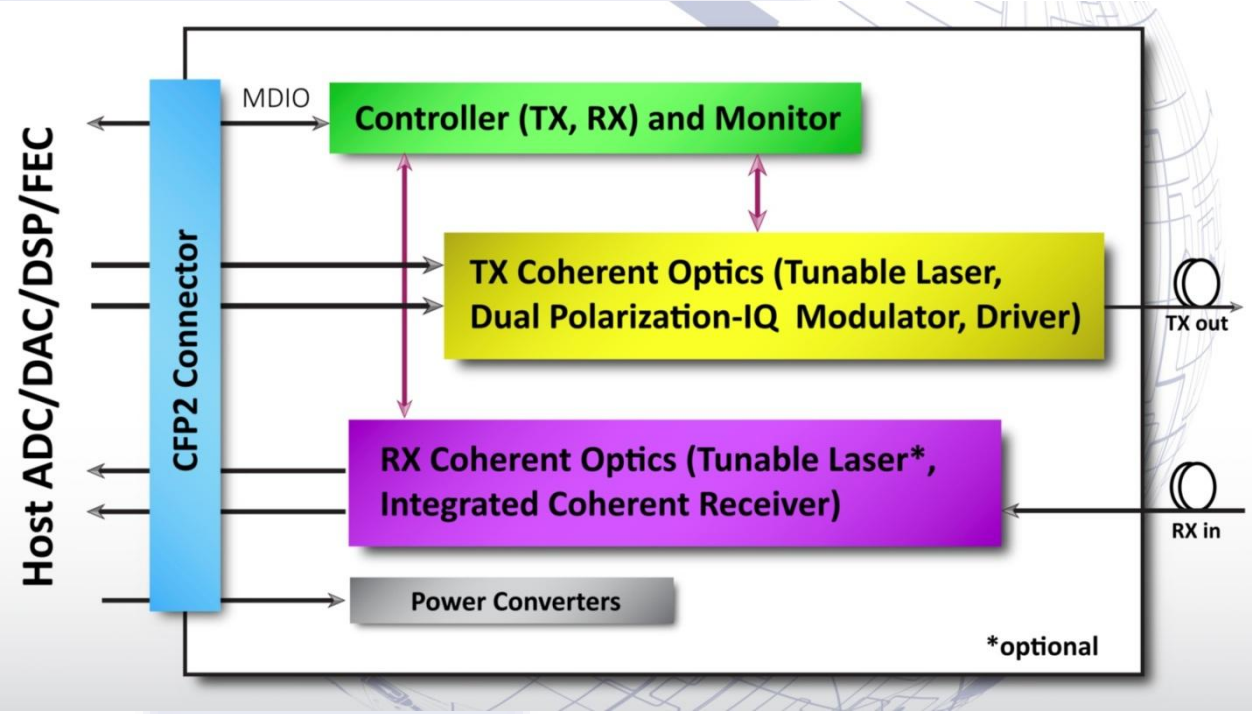
OIF 100G/200G CFP2-ACO Module Form Factor

- **CFP2-ACO pluggable modules are presently one option addressing the DCI Metro/Regional DWDM market**



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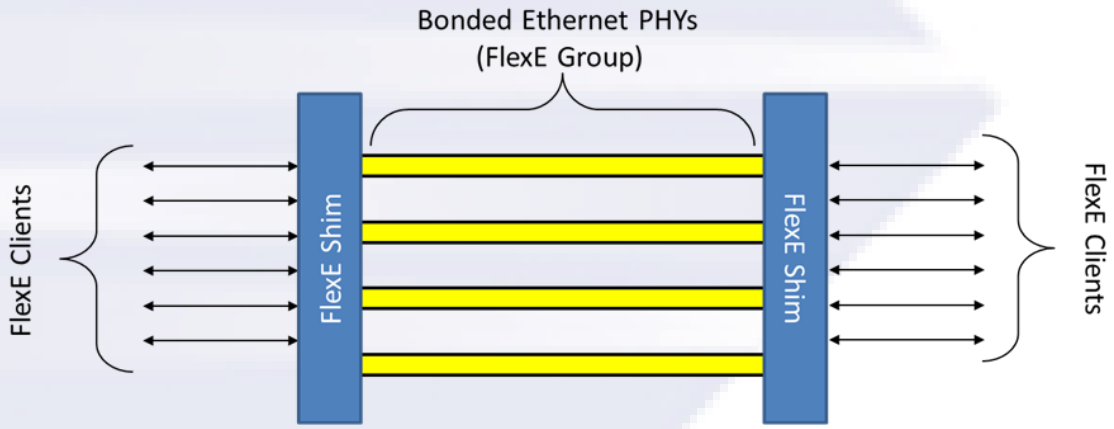
OIF Flex Ethernet Project

- **A mechanism to support a variety of Ethernet MAC rates not corresponding to an existing Ethernet PHY rate**
- **Can enable bonding of PHYs, sub-rate operation of PHY or channelization within a group of PHYs**



- **Enables applications such as "router-to-transport" connection and intra-DC "fat-pipe"**

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Summary

- CEI-56G interface specification work is well under way
- Several standards bodies are planning to leverage OIF's work on CEI-56G
- CEI PAM4 interfaces will be key in enabling a solid foundation for next generation 200G/400G client optics
- OIF has several projects under way addressing the future needs of the data center (CFP2-ACO, Flex Ethernet, etc)

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