OPTICAL INTERNETWORKING FORUM

White Paper:

CEI-25G-LR and CEI-28G-VSR Multi-Vendor Interoperability Testing at the 2012 ECOC Exhibition

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Executive Summary

The Optical Interworking Forum has been developing a set of Clauses focused on new electrical interfaces applicable to higher speed optical systems requiring interconnect baud rates of 19.90 Gbaud to 28.05 Gbaud using NRZ coding. The OIF membership, consisting of semiconductor, connector, optic suppliers, communications equipment OEMs, and service providers, allows a unique perspective for developing industry requirements, and a comprehensive understanding of the technology trade offs necessary to enable the development and support for these requirements.

A multi-vendor interoperability event to demonstrate the CEI-25G-LR and CEI-28G-VSR interfaces in action has been successfully carried out at the 2012 ECOC Exhibition by several members of the OIF Physical and Link Layer (PLL) Working Group. This new demonstration follows the successful OIF interoperability event that took place at the 2012 OFC Exposition. The ECOC PLL interoperability consisted of four individual demonstrations with nine participating vendors. Three demonstrations addressed the 19.60 - 28.05 Gbaud chip-to-module CEI-28G-VSR interface and one demonstration addressed the 19.90 - 25.80 Gbaud CEI-25G-LR interface for backplane applications. Interoperability participants included IC, connector, optical component, optical module and test equipment manufacturers.

CEI-25G-LR and CEI-25G-VSR Background Information and Applications

The communications and networking industries' data rates have increased along with the demands for higher levels of traffic aggregation. Additionally, the industry desires interoperable interfaces that support these next generation data rates. The OIF has been at the forefront of this demand, leading the industry with the development of common electrical interface (CEI) implementation agreements (IA) that support up to 25 Gb/s over backplane architectures, 28 Gb/s in chip-to-chip applications and 28 Gb/s in chip-to-module applications. This development work is unique and important in enabling the industry to re-use conventional chassis, linecard and cabling architectures as they develop equipment that is able to meet the evolving and challenging bandwidth demands of the communications industry.

CEI-25G-LR and CEI-28G-VSR are two recent OIF Clauses which address the needs of 25 Gb/s Long Reach backplane applications and 28 Gb/s Very Short Reach chip-to-module applications respectively. The CEI-25G-LR Clause was recently ratified along with CEI-28G-SR as part of the Common Electrical I/O (CEI) 3.0 Implementation Agreement. The CEI-28G-VSR Clause is under development and is expected to be ratified later this year.

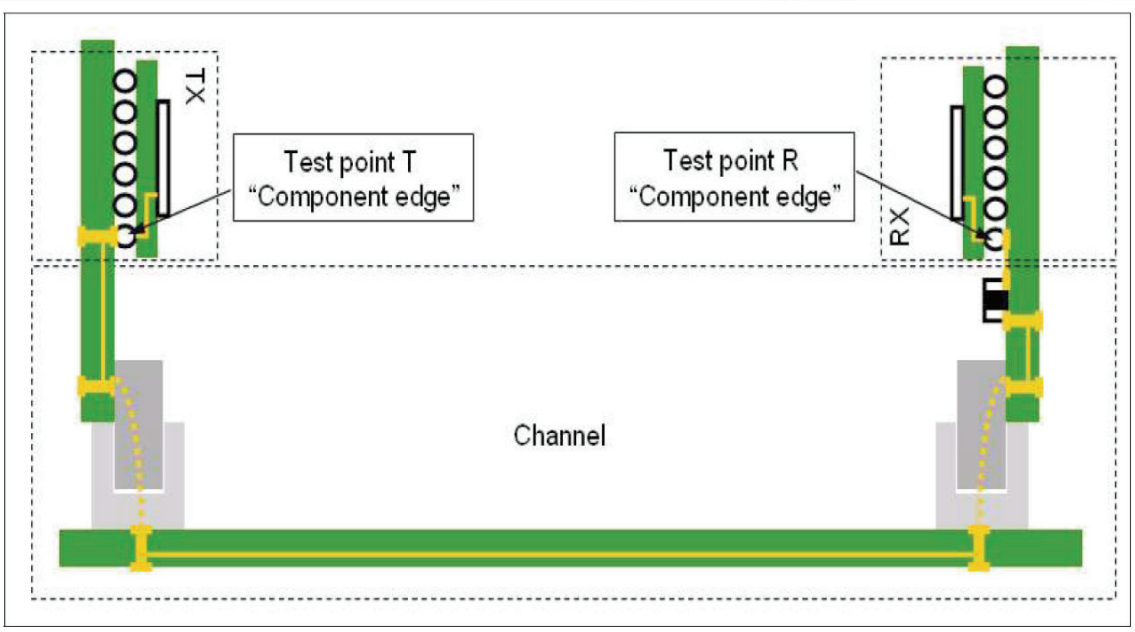


Fig. 1: CEI-25G-LR Reference Model

As shown in figure 1, backplane architectures are commonly used in communications equipment. Developing 25 Gb/s backplane channel specifications is important to enable the industry to continue use of this architecture in switches, routers, transport and data center equipment. The 25G-LR channel consists of 100Ω

differential PCB traces, vias and up to two connectors. As this IA is targeted to longer reach backplane applications total allowable channel loss can be up to 25 dB at Nyquist rate and the transmitter is able to generate a maximum swing of 1200 mVppd and is required to have an FIR equalizer. The receiver implementation is not mandated and can be vendor specific.

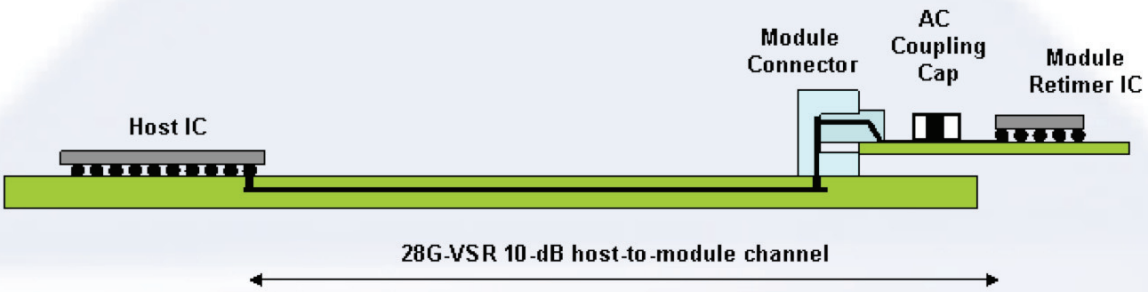


Fig. 2: CEI-28G-VSR Reference Model

The use of pluggable optical transceivers and direct attach copper cables is a common practice in equipment developed for the communications market. Developing interoperable pluggable IO (input/output) solutions that keeps up with the demanding bandwidth needs of industry is critical to enabling next generation equipment that supports the communications service providers. The 28G-VSR channel shown in figure 2 consists of 100Ω differential PCB traces, vias, one connector and AC coupling capacitors. The 28G-VSR IA is intended to be used for Very Short Reach channels with up to 10 dB loss at Nyquist rate and is being initially targeted for the next generation of optical modules having retimed interfaces operating at 25 – 28 Gb/s.

OIF PLL Multi-Vendor Interoperability Testing Objectives

Interoperability is one of the keys to the success of any standard. In order to promote the acceptance and demonstrate the viability of CEI, the OIF sponsored a private, closed door interoperability Plugfest in August of 2012. Proving that CEI is widely supported by various companies across the industry the participants included four semiconductor manufacturers (AppliedMicro, Avago Technologies, Inphi and Semtech), two connector vendors (Molex and TE Connectivity), one optical module vendor (Molex), one optical component vendor (Luxtera) and two test equipment manufacturers (Agilent Technologies and Tektronix). Cooperation between semiconductor, connector, optical module, optical component and test equipment suppliers is crucial to enable implementation and integration of high-speed signaling by system vendors. ECOC 2012 will showcase working demonstrations of the the CEI-25G-LR and CEI-28G-VSR Clauses, using test scenarios similar to the private interoperability tests.

OIF Interop Test Equipment

Test equipment supplied to the PLL Interop demonstration by Agilent Technologies included the following:

- 86100D DCA-X Oscilloscope: Modular platform that accommodates up to 4 measurement modules and 16 measurement channels.
- 86108B Wide Bandwidth Module: Has integrated dual receiver to 50 GHz, clock recovery to 32 Gb/s and precision timebase enabling typical intrinsic jitter of less than 50 fs
- 86116C Optical Module: Has optical bandwidth to 65 GHz and electrical bandwidth to 80 GHz. Filter response for wide range of data rates is enabled through use of System Impulse Response Correction.
- 86107A Precision Timebase Module: Operates to 40 GHz and has intrinsic jitter well under 200 fs
- 86100D Option 200: Performs jitter decomposition for an extensive selection of jitter parameters
- N1012A OIF CEI 3.0 Compliance Application: Measures the nearly 120 parameters for CEI 3.0 and the draft VSR implementation agreements
- U8031A Power Supply: High capacity, triple output in a compact form factor

Test equipment supplied to the PLL Interop by Tektronix included the following:

- DSA8300 Series Sampling Scope: A modular oscilloscope platform that provides a low native instrument jitter floor (200 fs RMS) for accurate acquisition of up to 6 test channels and 4x faster acquisition throughput.
- 80E10 Electrical Sampling Module: 50GHz Bandwidth for Electrical Conformance Testing of 25.781 Gb/s (100GBASE-ER4 and 100GBASE-LR4), 27.739 Gb/s (100GBASE-ER4 FEC and 100GBASE-LR4 FEC) standards in a single module with remote heads for signal integrity placed right at the DUT.
- CR286A Clock Recovery Module: 28.6Gb/sec clock recovery for golden PLL and precision timebase.
- 82A04 Phase Reference Module: 200 femtosecond jitter capability for accurate timebase, low intrinsic jitter
- 80C10C Optical Sampling Module: Provides 80GHz Optical bandwidth and support for Optical Conformance Testing of 25.781 Gb/s (100GBASE-ER4 and 100GBASE-LR4), 27.739 Gb/s (100GBASE-ER4 FEC and 100GBASE-LR4 FEC) standards in a single module.
- 80SJARB Software: Jitter measurement application providing IEEE 802.3ba requirements for J2 and J9 jitter measurements along with eye diagram analysis.
- PWS400 Series Power Supply: With voltage accuracy of 0.03% and less than 5 mVp-p noise for reliable output
- DMM4020: With 5.5 digit resolution, this digital multimeter enables measurement of volts, ohms and amps with a basic V DC accuracy of 0.015%.

Demonstration No. 1
Inphi-Semtech-Molex CEI-28G-VSR Application

Component Overview

The Inphi INx12510 is a single-chip, low-power CMOS PHY enabling 10:4 gearbox applications for 100G Ethernet and OTU4 line cards and CFP optical modules. Optimized for low-latency operation, it delivers high system performance for demanding applications. It is designed to exceed CEI-28G-VSR requirements and allows real-time monitoring of link margin with dynamic high-resolution eye scan diagnostics.

The zQSFP+ system from Molex supports next-generation CEI-28-VSR, 100 Gbps Ethernet and 100 Gbps InfiniBand* Enhanced Data Rate (EDR) applications with excellent cooling, unparalleled signal integrity (SI), superior electro magnetic interference (EMI) protection and the lowest power consumption in the optical industry.

Leveraging a generation of innovation in 10G module CDRs, Semtech's GN2425 and GN2426 are low-power retimers optimized for reference-free 25-28Gbps operation in next-generation optical modules and active cables. By resetting the jitter budgets within the module in both directions, Semtech's CDRs are perfect for challenging new applications such as 100GBASE-LR4/ER4 and OTU4 CFP2 optical modules. The GN2425 and GN2426 feature best-in-class receive sensitivity, input jitter tolerance and output jitter, allowing for reliable signal recovery and clean, wide-open transmit eyes.

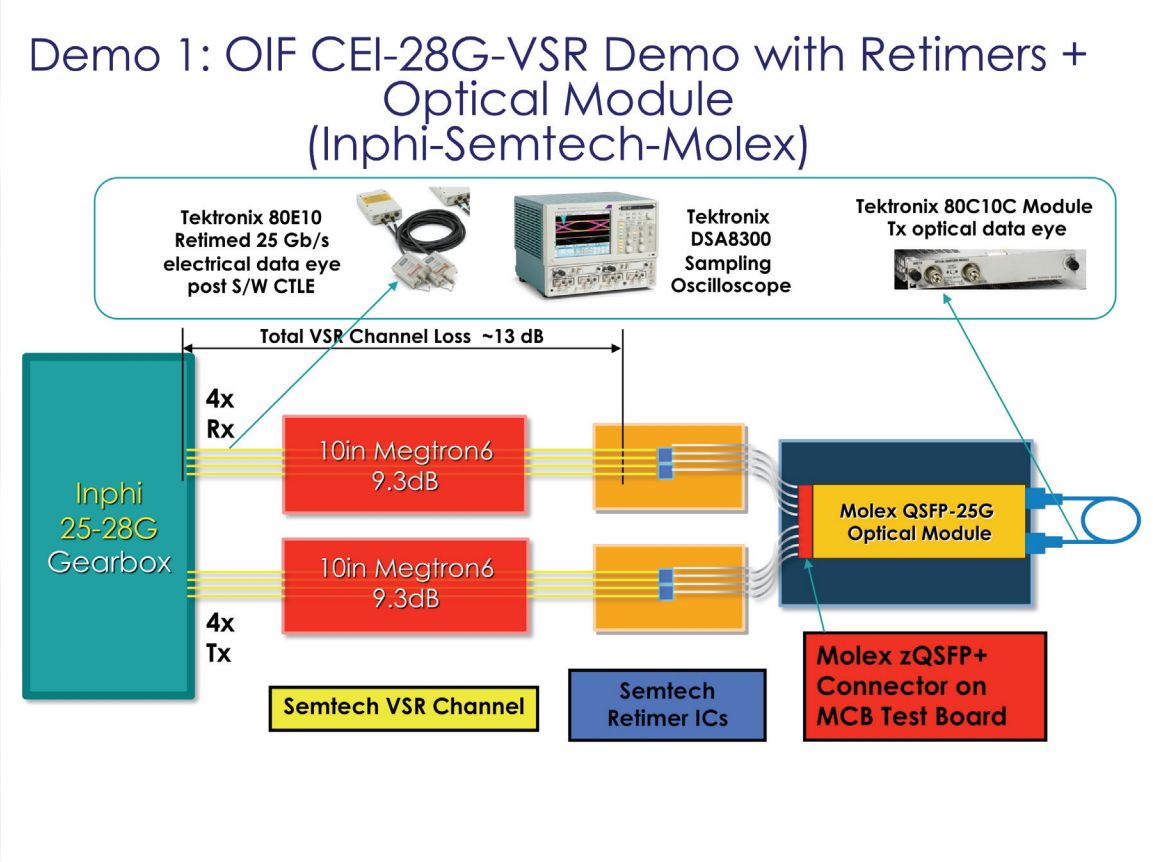
The Molex Active Optical Cable (AOC) can transmit up to 4KM 100G links. Molex use of Luxtera's Silicon Photonics technology allows customers to transmit much greater distances than traditional VCSEL based solutions using less power than long range optics. The use of advanced photonics technologies enables ease of implementation through an industry standard zQSFP+ port.

Demo 1 description

This demonstration system consists of the following blocks: an Inphi 100G gearbox, a Semtech VSR host channel, Semtech retimer ICs, a Molex zQSFP+ connector, and a Molex QSFP-25G Active Optical Cable (AOC). The system generates PRBS31 data at 25.78 Gb/s rate within the Inphi Gearbox which is transmitted over a Semtech VSR host channel trace PCB (contributing approximately 9dB of insertion loss) to the Semtech CDR ICs. Total channel loss for this case is approximately 13dB. The CDR receiver inputs have sufficient CTLE equalization to enable error free operation of the host VSR link in the optical transmit direction. The retimed outputs of the CDRs are transmitted across the Molex zQSFP+ connector to the Molex QSFP-25G AOC which loops the optical data back to its receiver. In the receive direction the data flow is in the reverse order through the cascaded blocks terminating at the PRBS31 error checkers within the Inphi Gearbox in order to verify that the entire transmit and

receive data path through the system is operating error free. Two channels in the system are broken out to a Tektronix DSA8300 Digital Sampling Oscilloscope. One of the QSFP-25G Tx optical channel data eyes is shown on the DSA8300 using a Tektronix 80C10C module. As well, one of the optical receiver channels at the output of the retimer and host VSR channel is shown on a Tektronix 80E10 electrical module. As this electrical data eye is located in the system at the output of the CDR after a host VSR channel a S/W CTLE function is required to be enabled within the oscilloscope in order to display a realistic data eye.

Fig. 3: Demo No. 1 Block Diagram



Demonstration No. 2
AppliedMicro-Inphi-Molex-Luxtera CEI-28G-VSR Application

Component Overview

This interoperability demonstration pairs AppliedMicro with a Gearbox as host, electrical retimers from Inphi, Molex zQSFP+ connector and an Active Optical Cable from Molex, featuring a Luxtera silicon photonics integrated optical transceiver chip. Simulated traffic at 103Gbps is produced at the host, transferred across a CEI-28G-VSR compliant channel, retimed to improve signal quality and converted to the optical domain for transmission. The optical signal is recovered by the optical module, retimed and returned to the host for integrity testing.

The single-chip, CMOS S28010 Gearbox from AppliedMicro is compliant with IEEE802.3 Standard for 100GBASE-LR4/ER4 and CAUI interface. It can be used in OTU4 applications to convert between OTL4.10 and OTL4.4. The high-speed interface operates from 25.7 to 28Gbps and is compatible with the OIF-28G-VSR interface. Both the CAUI and 28Gbps interface provides best-in-class performance with self-calibrating CTLE receiver and three-tap FIR driver.

Inphi's CMOS 100G Ethernet and OTU4 Quad 25-28G Retimer targets next-generation ultra low power optical modules with new levels of integration and advanced metrics and analysis on-die. Containing transmit and adaptive receive equalization, this device is designed to exceed 28G-VSR requirements for optical module attachment with lowest power in the industry.

The zQSFP+ system from Molex supports next-generation CEI-28-VSR, 100 Gbps Ethernet and 100 Gbps InfiniBand* Enhanced Data Rate (EDR) applications with excellent cooling, unparalleled signal integrity (SI), superior electro magnetic interference (EMI) protection and the lowest power consumption in the optical industry.

Luxtera's single chip Silicon Photonics optical transceiver includes four integrated 28 Gbps transmit and receive channels. The transmit optical modulators are powered from a single laser source delivering superior optical performance when mated with standard single mode ribbon fiber cables. Luxtera's Silicon Photonics technology coupled with single mode fiber permits greater reach compared to multimode fiber solutions. The built-in optical receivers retrieve the optical signal and produce 28 Gbps electrical signaling for downstream processing. Luxtera's optical transceiver is compatible with CEI-28G-VSR applications as illustrated in the demo. The device is targeted for 100 Gbps Ethernet, OTN and InfiniBand applications as well as high performance systems implementing OIF Common Electrical Interface standards. Utilizing Silicon Photonics technology, the Luxtera optical transceiver IC enables low latency, low bit error rate, long reach, high reliability and small footprint.

Demo 2 description

AppliedMicro provided the S28010 Gearbox configured as the host for this demonstration. In this mode, the Gearbox uses built-in pattern generators on each of the high-speed outputs to simulate a 100Gbps Ethernet payload. The 3-tap FIR driver is configured to equalize signal distortion created by a 12dB, CEI-28G-VSR compliant channel.

The 12dB channel includes de-coupling capacitors, 50mm of PCB trace on Rogers 3003 and an RF connector. Up to 300mm of RF cable connects to an additional 8.5dB Megtron 6 channel supplied by Inphi. The output of the VSR channel connects to Inphi's IN012525 retimer CDR through 2.5dB of microstrip via an MXP connector.

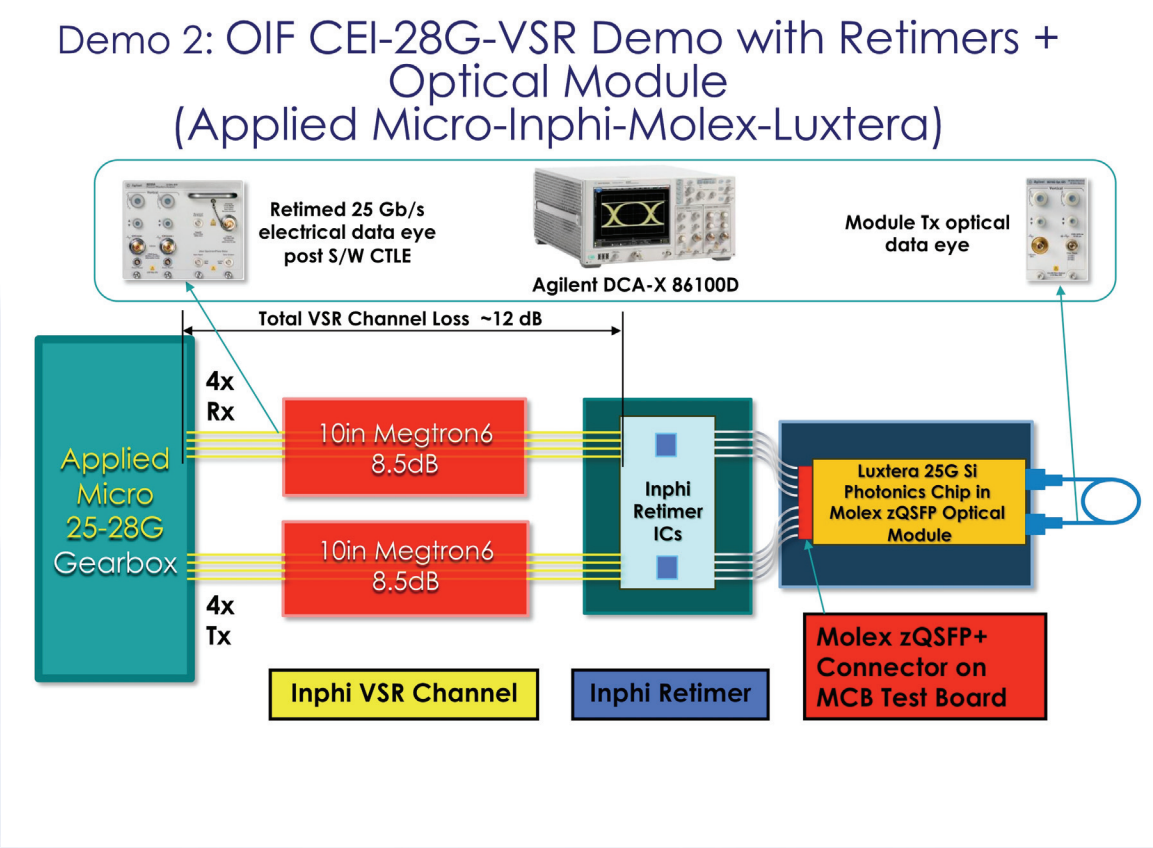
The Inphi retimer verifies the pattern and calculates BER as the stream passes - including non-destructive high resolution eyes. The retimer output feeds the Molex optical module with Luxtera silicon photonics for 1490nm optical transport.

Continuing down the transmit path, the CEI-28G-VSR signaling is passed into the Luxtera optical transceiver where each electrical lane is converted to optical signaling. The optical output is looped back to the optical receiver through single mode ribbon fiber cable. The receiver translates the optical signaling back to CEI-28G-VSR compatible electrical signaling where it is passed back down the receive path to the second Inphi retimer, which drives data back through the VSR channel, returning to the AppliedMicro Gearbox for pattern verification and margin analysis.

At the output of the VSR compliant channel the AppliedMicro Gearbox uses a CTLE receiver to compensate for channel distortion and recover the data. The built-in pattern checker is used to monitor bit errors.

A pair of Agilent DCA-X oscilloscopes monitor two channels in the system. The first uses an Agilent 86116C module for an optical output eye from the Luxtera optics, while the second captures an electrical eye after the VSR channel using an Agilent 86108B module. As this electrical data eye is located in the system at the output of the CDR after a host VSR channel, a S/W CTLE function is required to be enabled within the oscilloscope in order to display a realistic data eye.

Fig. 4: Demo No. 2 Block Diagram



Demonstration No. 3
Avago Technologies, TE Connectivity, Semtech CEI-28G-VSR Application

Silicon Overview

Avago Technologies' 28nm CMOS SerDes cores represent Avago's eighth generation of high performance, multi-Gbps transceiver ASIC IP. The SerDes are suitable for links with optical transceivers, active and passive copper cables, and backplane applications, and Avago's unique decision feedback equalization results in overall power and area savings to equalize channels characterized by high loss and reflections. Avago has shipped over 250M SerDes channels in the networking, storage and server markets.

Leveraging a generation of innovation in 10G module CDRs, Semtech's GN2425 and GN2426 are low-power retimers optimized for reference-free 25-28Gbps operation in next-generation optical modules and active cables. By resetting the jitter budgets within the module in both directions, Semtech's CDRs are perfect for challenging new applications such as 100GBASE-LR4/ER4 and OTU4 CFP2 optical modules. The GN2425 and GN2426 feature best-in-class receive sensitivity, input jitter tolerance and output jitter, allowing for reliable signal recovery and clean, wide-open transmit eyes.

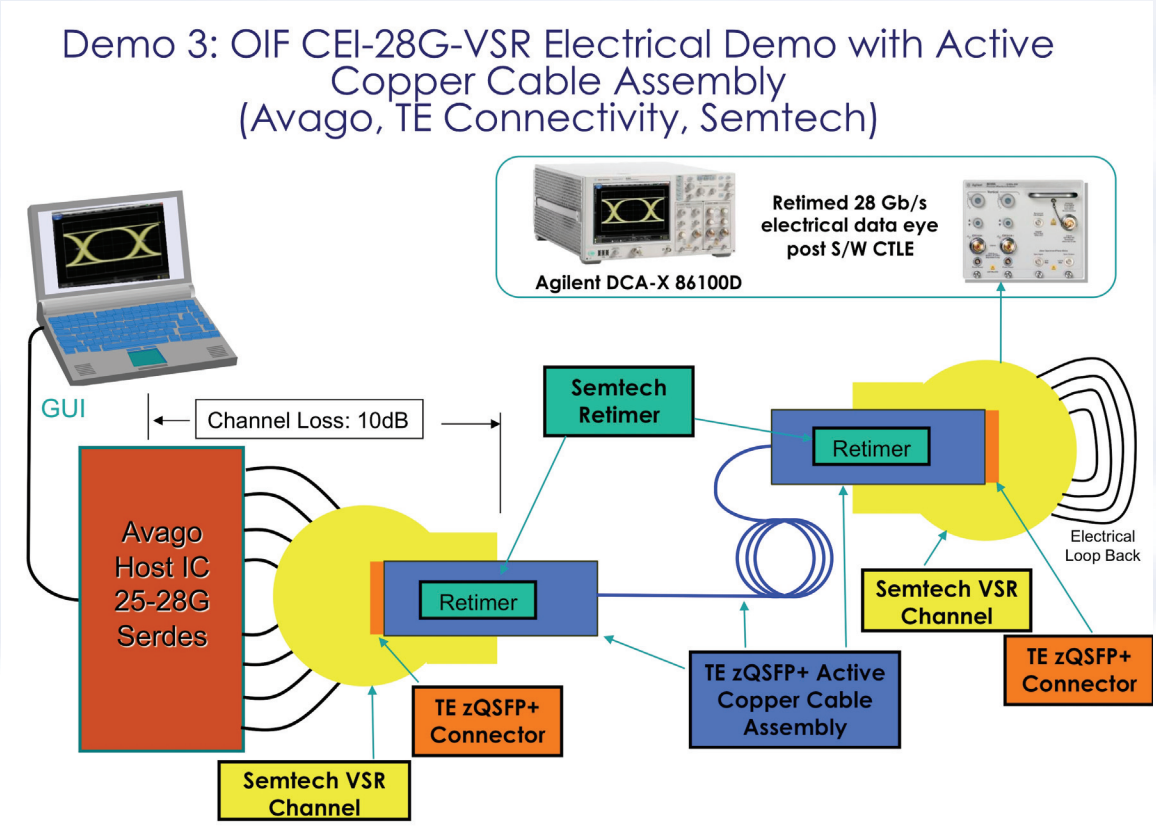
TE Connectivity's zQSFP+ connector is a new high speed, high density interconnect that supports data rates from 28 Gbps per lane over the connector's 4 channels, providing an aggregate bandwidth of 100Gbps. The connector interface is fully backwards compatible to the existing QSFP+ modules and cable assemblies. Through a coupled, narrow-edged, blanked- and formed- contact geometry and insert molding design, the zQSFP+ interconnect exhibits robust industry compliant signal integrity, mechanical and electrical performance. The zQSFP+ cage offers excellent thermal performance and enhanced EMI protection.

The active copper cable assembly supplied by TE Connectivity leverages TE's Madison Cable brand Infinitwist cable to provide a four channel, 5.8 mm diameter cable assembly with reduced diameter for improved airflow and improved flexibility for ease of cable management. The cable assembly's QSFP-28G end points house the Semtech clock and data recovery (CDR) chips mentioned above, enabling the use of the 34 AWG differential pairs in the Infinitwist cable.

Demo 3 description

This demonstration system consists of the following blocks: an Avago 25-28G SerDes, a Semtech VSR host channel, a TE zQSFP+ connector and cage, mated with Semtech 25-28G Retimer ICs packaged within a TE Connectivity QSFP-28G Active Copper Cable (ACC) Assembly. The system generates PRBS31 data at 25.78 Gb/s rate within the Avago SerDes which is transmitted over the 10dB Semtech VSR channel through the TE zQSFP+ connector to the inputs of the Semtech CDR ICs in the TE QSFP-28G ACC modules. The retimed outputs of the CDRs are transmitted across a 34 AWG 8-pair cable. The electrical outputs at the far-end of the QSFP-28G ACC assembly are looped back to their inputs through another Semtech channel and then eventually terminated at the PRBS31 error checkers within the receiver of the Avago SerDes in order to verify that the entire transmit and receive data path through the system is operating error free. An electrical data eye is shown on an Agilent DCA-X 86100D Digital Sampling Oscilloscope at one of the Semtech CDR outputs using the built-in CTLE S/W function within the oscilloscope to display an equalized electrical data eye.

Fig. 5: Demo No. 3 Block Diagram



Demonstration No. 4
Avago Technologies and TE Connectivity CEI-25G-LR Application

Silicon Overview

Avago Technologies' 28nm CMOS SerDes cores represent Avago's eighth generation of high performance, multi-Gbps transceiver ASIC IP. The SerDes are suitable for links with optical transceivers, active and passive copper cables, and backplane applications, and Avago's unique decision feedback equalization results in overall power and area savings to equalize channels characterized by high loss and reflections. Avago has shipped over 250M SerDes channels in the networking, storage and server markets.

Connector Overview

TE's STRADA Whisper backplane connector is designed to support data rates per differential pair up to 40Gbps. The connector's individually shielded pairs results in noise performance that is less than 1% @ 20 ps signal edge rates and insertion loss of less than 1db and flat past 15GHz. The in-row "horizontal" pair orientation results in zero skew. Since PCB interfaces are a critical element of over-all connector performance, the STRADA Whisper connector footprint has been engineered to optimize the technical tradeoffs of impedance, cross talk and routability.

Backplane Overview

The TE supplied reference backplane channel consists of two daughter cards, a backplane, and two STRADA Whisper connectors. The STRADA Whisper connector is made up of a vertical header and a right-angle receptacle. The Avago SerDes connects to the TE daughter cards through 2.4mm connectors.

The daughter cards are 110mils thick using Megtron 6 material encompassing 14 layers each.[1] All of the differential traces routed from the 2.4mm test points to the skew-less STRADA Whisper connector footprint are 5 inches in length in a 6-9-6 mil trace width configuration. The traces and other copper in the boards utilize Megtron 6 VLP foil finishes. The signal vias in both the STRADA Whisper connector and 2.4mm test points are counter-bored to within 10 mils of the signal layer. The daughter card contains the STRADA Whisper receptacle.

The backplane, which contains the STRADA Whisper header, is 200mils thick using Megtron 6 material encompassing 20 layers. All of the differential traces routed on the backplane are in a 7-9-7 mil trace width configuration. The traces and other copper in the board utilize a Megtron 6 H-VLP foil finish. The signal vias in the STRADA Whisper connector footprint are counter-bored to within 10mils of the signal layer. The backplane demonstrates lengths of 4, 8, 17, and 30". When combined with a daughter card on each end the total trace length demonstrated in the channel is extended to 14, 18, 27, and 40 inches.

[1] Megtron is a registered trademark of Panasonic.

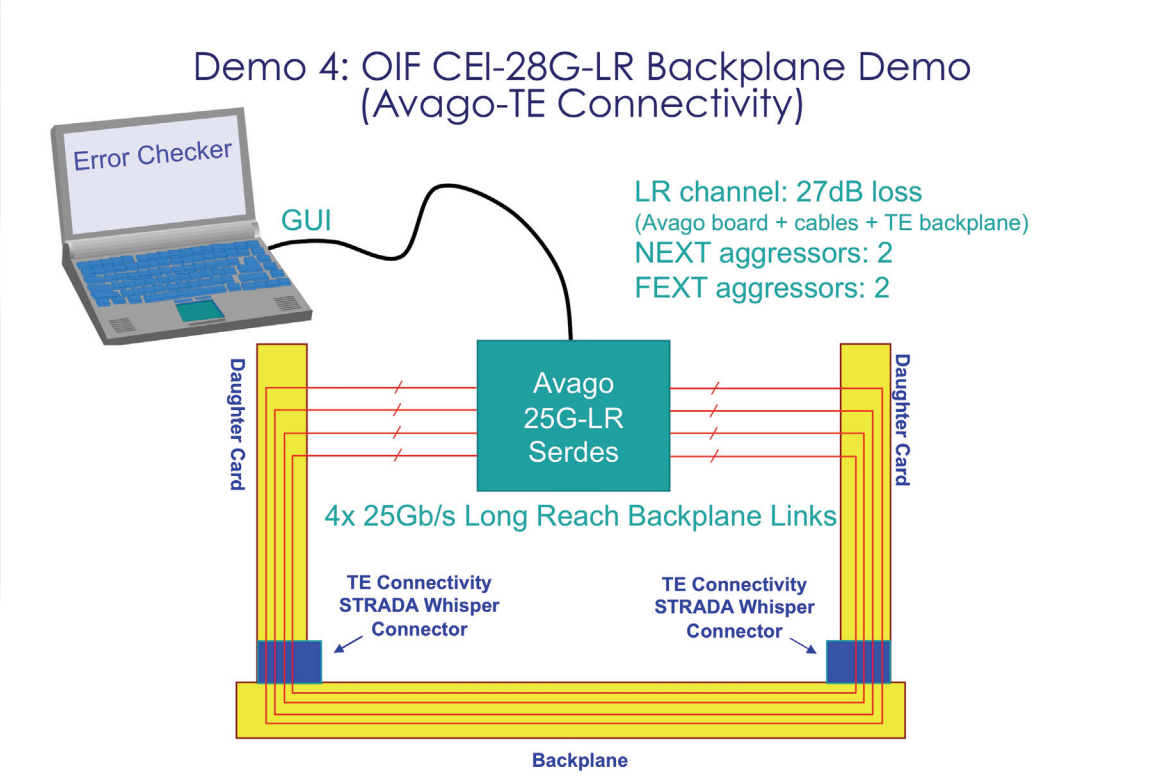
Demo 4 description

The goal of the demonstration is to exhibit the OIF CEI 25G LR Implementation Agreement (IA) with 4-lane 100G operation across a backplane link with end-to-end loss of 27dB at 12.9GHz. Each lane carries a PRBS-31 pattern running at a 25.78125Gb/s data rate. PRBS generation and checking is performed on-chip.

The demonstration contains an Avago 28nm 28G test chip operating over a TE Connectivity-supplied reference backplane. It is built with Megtron6 material and implements TE's STRADA Whisper backplane connector product.

The 8 inch backplane channel and two 5 inch line cards, which are used in this demonstration, contains approximately 15.5 dB of loss from the 2.4mm connector on one daughter card to the 2.4mm connector on the other daughter card. An additional 11.5 dB of loss is on the Avago chip test board for a total channel loss of 27dB. The demonstration runs 5 lanes at 25Gbps with 2 NEXT (near end cross talk) lanes, in row and in column, and 2 FEXT (far end cross talk) lanes, in row and in column acting on victim pair in order to increase the amount of crosstalk.

Fig. 6: Demo No. 4 Block Diagram



Conclusions

This interoperability demonstration successfully brought semiconductor, connector, optical module and test equipment vendors together to show that the CEI-25G-LR and CEI-28G-VSR Clauses have evolved from concept to reality and that a viable ecosystem is now in place to enable the commercial success of the next generation of optical module electrical interfaces in the 25 – 28 Gbaud speed range along with the backplane architectures operating with 25 Gbaud channels.