OPTICAL INTERNETWORKING FORUM

White Paper
CEI-25G-LR and CEI-28G-VSR Multi-Vendor Interoperability Testing

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Executive Summary

The Optical Interworking Forum has been developing a set of Clauses focused on specifying a set of new electrical interfaces applicable to higher speed optical systems requiring interconnect baud rates of 19.90 Gbaud to 28.05 Gbaud using NRZ coding. The OIF membership, consisting of semiconductor, connector, optic suppliers, communications equipment OEMs, and service providers, allows a unique perspective of developing industry requirements, and a comprehensive understanding of the technology trade offs necessary to enable the developments necessary to support these requirements.

A multi-vendor interoperability event to demonstrate the CEI-25G-LR and CEI-28G-VSR interfaces in action has been successfully carried out at the 2012 OFC/NFOEC by several members of the OIF Physical Link Layer (PLL) Working Group. The PLL interoperability consisted of five individual demonstrations with ten participating vendors. Three demonstrations addressed the 19.60-28.05 Gbaud chip-to-module CEI-28G-VSR interface and two demonstrations addressed the 19.90-25.80 Gbaud CEI-25G-LR interface for backplane applications. Interoperability participants included IC, connector, optical component, optical module and test equipment manufacturers.

CEI-25G-LR and CEI-25G-VSR Background Information and Applications

As the demands on industry data rates have increased along with the demands for higher levels of traffic aggregation, the communications and networking industries have need of interoperable interfaces that support these next generation data rates. The OIF has been at the forefront of this demand by leading the industry with the development of common electrical interface (CEI) implementation agreements (IA) that support 25 Gb/s over backplane architectures, 28 Gb/s in chip-to-chip applications and 28 Gb/s in chip-to-module applications. This development work is important in enabling the industry to re-use conventional chassis, linecard and cabling architectures as they develop equipment that is able to meet the evolving and challenging bandwidth demands of the communications industry.

CEI-25G-LR and CEI-28G-VSR are two recent OIF Clauses which address the needs of 25 Gb/s Long Reach backplane applications and 28 Gb/s Very Short Reach chip-to-module applications respectively. The CEI-25G-LR Clause was recently ratified along with CEI-28G-SR as part of the Common Electrical I/O (CEI) 3.0 Implementation Agreement. The CEI-28G-VSR Clause is under development and is expected to be ratified later this year.

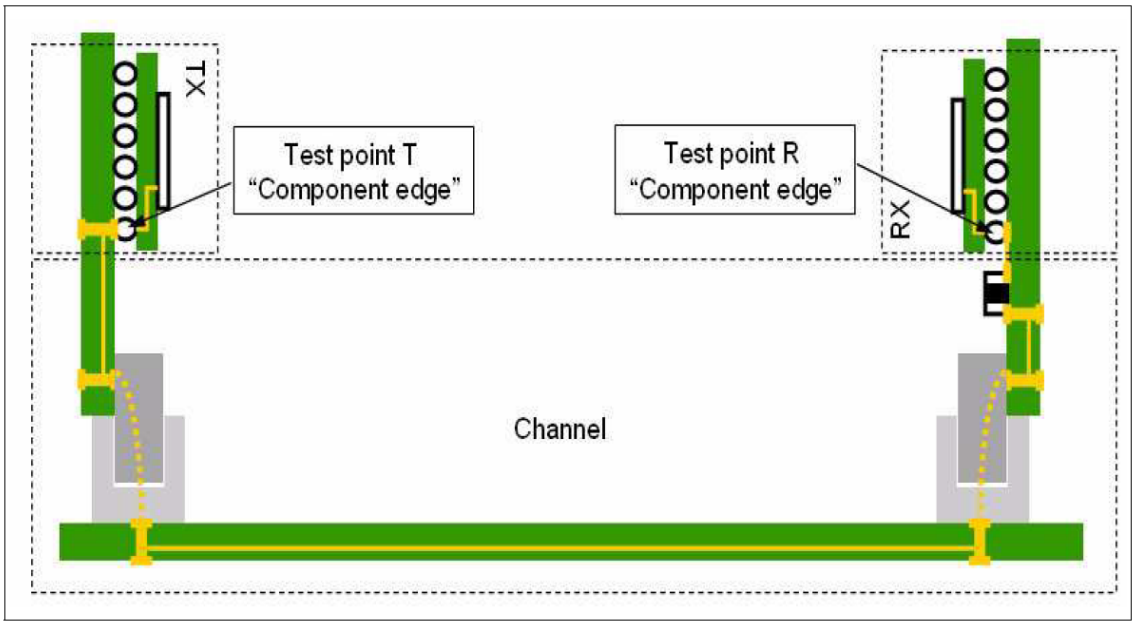

Fig. 1: CEI-25G-LR Reference Model

As shown in figure 1, backplane architectures are commonly used in commuications equipment. Developing 25 Gb/s backplane channel specifications is important to enable the industry to continue use of this architecture in switches, routers, transport and data center equipment. The 25G-LR channel consists of 100Ω differential PCB traces, vias and up to two connectors. As this IA is targeted to

longer reach backplane applications total allowable channel loss can be up to 25 dB at Nyquist rate and the transmitter is able to generate a maximum swing of 1200 mVppd and is required to have an FIR equalizer. The receiver implementation is not mandated and can be vendor specific.

Fig. 2: CEI-28G-VSR Reference Model

The use of pluggable optical transceivers is a common practice in equipment developed for the communications market. Developing interoperable pluggable IO (input/output) solutions that keeps up with the demanding bandwidth needs of industry is critical to enabling next generation equipment that supports the communications service providers. The 28G-VSR channel shown in figure 2 consists of 100Ω differential PCB traces, vias, one connector and AC coupling capacitors. The 28G-VSR IA is intended to be used for Very Short Reach channels with up to 10 dB loss at Nyquist rate and is being initially targeted for the next generation of optical modules having retimed interfaces operating at 25 – 28 Gb/s.

OIF PLL Multi-Vendor Interoperability Testing Objectives

Interoperability is one of the keys to the success of any standard. In order to promote the acceptance and demonstrate the viability of CEI, the OIF sponsored a private, closed door interoperability Plugfest in January of 2012. Proving that CEI is widely supported by various companies across the industry the participants included five semiconductor manufacturers (Altera, Gennum, IBM, Inphi and Xilinx), three connector vendors (Amphenol, Molex and TE Connectivity), two optical module vendors (Fujitsu Optical Components and Molex), one optical component vendor (Luxtera) and one test equipment manufacturer (Tektronix). Cooperation between semiconductor, connector, optical module, optical component and test equipment suppliers is crucial to enable implementation and integration of high-speed signaling by system vendors. OFC 2012 will showcase working demonstrations of the the 25G-LR and 28G-VSR Clauses, using test scenarios similar to the private interoperability tests.

OIF Interop Test Equipment

Test equipment supplied to the PLL Interop by Tektronix included the following:

DSA8300 Series Sampling Scope: The Tektronix DSA8300 is a modular oscilloscope platform that provides a low native instrument jitter floor (425 fs RMS) for accurate acquisition of up to 8 test channels.

Analysis of eye diagrams and jitter using 80SJARB jitter measurement application software address IEEE 802.3ba requirements for J2 and J9 jitter measurements.

Equipped with the 80C10B Optical Module; the DSA8300 provides support for Conformance Testing of 25.781 Gb/s (100GBASE-ER4 and 100GBASE-LR4), 27.739 Gb/s (100GBASE-ER4 FEC and 100GBASE-LR4 FEC) standards in a single module.

AWG7000: The Tektronix AWG7000 Series Arbitrary Waveform Generators provide up to 24 GSamples/sec and 10 Bit vertical resolution for signal stimulus of high speed patterns and clock reference sources.

Demonstration No. 1
Altera-Gennum-Molex CEI-28G-VSR Application

Component Overview

Altera's Stratix V FPGAs deliver the highest system bandwidth at the lowest power consumption, under 200mW per transceiver at 28 Gbps. Stratix V FPGAs support backplane, chip-to-optical module, and chip-to-chip applications through 28 Gbps transceivers, and up to 66 full-duplex 14.1 Gbps transceivers. The transceivers in Stratix V FPGAs provide the industry's highest system reliability and performance with the lowest jitter.

The zQSFP+ system from Molex supports next-generation 100 Gbps Ethernet and 100 Gbps InfiniBand* Enhanced Data Rate (EDR) applications with excellent thermal cooling, signal integrity (SI), electro magnetic interference (EMI) protection and the lowest power consumption in the industry.

Leveraging a generation of innovation in 10G module CDRs, Gennum's GN2425 and GN2426 are low-power retimers optimized for reference-free 25-28Gbps operation in next-generation optical modules and active cables. By resetting the jitter budgets within the module in both directions, Gennum's CDRs are perfect for challenging new applications such as 100GBASE-LR4/ER4 and OTU4 CFP2 optical modules. The GN2425 and GN2426 feature best-in-class receive sensitivity, input jitter tolerance and output jitter, allowing for reliable signal recovery and clean, wide-open transmit eyes.

The Molex optical module is a demonstration platform for 25Gbps silicon photonics transceiver technology. The optoelectronic transceiver consists of four 28G transmitters and four 28G receivers integrated onto a single silicon photonics chip. A DFB laser is shared across the four externally modulated transmitter channels enabling an aggregate un-encoded data rate of up to 112Gbps (4x28).

Molex will design and bring to market products based on this technology. These products will address a variety of different standards, including 100Gbps Ethernet and InfiniBand EDR optical interconnect applications, and will be compliant with the emerging OIF Short Reach (SR) and Very Short Reach (VSR) electrical module/host interconnect specifications.

Demo 1 description

This demonstration system consists of the following blocks: an Altera Stratix V GT FPGA, a Gennum 12-dB VSR host channel, a Molex zQSFP+ connector, Gennum Clock-and-Data Recovery ICs, and a Molex 1490nm 4x28G Optical Transceiver Module. The system generates PRBS31 data at 28.05 Gb/s rate within the FPGA which is transmitted over a Gennum VSR host channel having 12 dB of insertion loss through a Molex zQSFP+ connector to the Gennum CDR ICs. The retimed outputs of the CDRs are transmitted to the Molex Optical Module which loops the optical data back to its receiver through 2 km of SM fiber. In the receive direction the data flow is in the reverse order through the cascaded blocks terminating at the PRBS31 error checkers within the Altera FPGA in order to verify that the entire transmit and receive data path through the system is operating error free. An electrical data eye

is shown on a Tektronix DSA8300 Digital Sampling Oscilloscope at one of the Gennum CDR outputs.

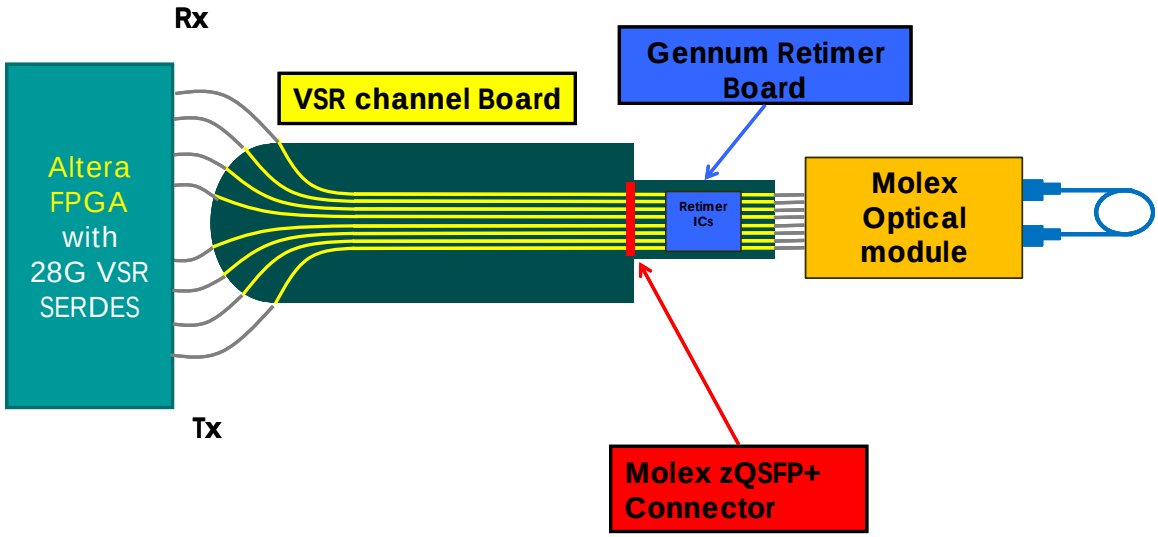

Fig. 3: Demo No. 1 Block Diagram

Demonstration No. 2
Xilinx-TE Connectivity-Fujitsu CEI-28G-VSR Application

Component Overview

Xilinx utilized their Virtex-7 GTZ test chip (built with ceramic package) for the Virtex-7HT FPGA, in the interoperability testing with 4 channels running a PRBS-31 pattern at 25.78Gbps. The serial I/Os have both programmable transmit pre/post-emphasis and active linear receive equalization optimized for VSR channels. A 2-D eye scan is also available at the receiver for link tuning.

TE Connectivity's zQSFP+ connector is a new high speed, high density interconnect that supports data rates from 28 Gbps per lane over the connector's 4 channels, providing an aggregate bandwidth of 100Gbps. The connector interface is fully backwards compatible to the existing QSFP+ modules and cable assemblies. Through a coupled, narrow-edged, blanked- and formed- contact geometry and insert molding design, the zQSFP+ interconnect exhibits superior signal integrity, mechanical and electrical performance. For this demo with Fujitsu's CFP2 transceiver, the connector would normally be a CFP2 connector, but in this case two zQSFP+ connectors have been substituted.

Fujitsu Optical Component's (FOC) CFP2 style transceiver is designed to comply with the OIF 28G-VSR specification, which is the next generation electrical interface to support 100G technology. The introduction of this new interface, together with the high density integration technology of optical and electrical parts, enables the compact sized (about half width of the current CFP) and low power consumption (about 1/3 of the current CFP) transceivers. The target form factor of this transceiver is "CFP2" (http://www.cfp-msa.org/) which is now under creation by CFP-MSA group.

Demo 2 description

The Xilinx Virtex-7 GTZ test chip generates four channels running a PRBS31 pattern at 25.78Gbps. These channels drive a Fujitsu 13 dB insertion loss channel to TE's 28Gbps zQSFP+ connector. The signal then feeds to Fujitsu's CFP2-style optical transceiver which includes an integrated CDR. The signal optically loops through single mode fiber back through the transceiver, through the connector to the chip receiver section ending at the PRBS31 error checkers within the Xilinx chip.

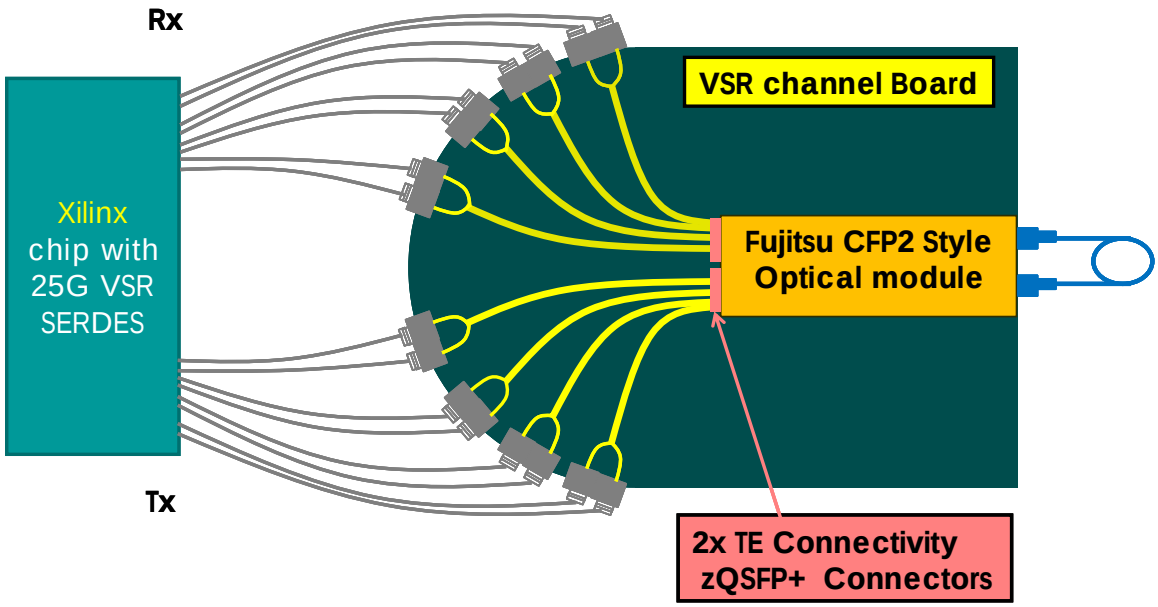

Fig. 4: Demo No. 2 Block Diagram

Demonstration No. 3
IBM-Amphenol-Inphi-Luxtera CEI-28G-VSR Application

Component Overview

IBM's High Speed Serial (HSS) 28G core is available as part of the IBM Cu32 Custom Logic product offering. It provides state-of-the-art jitter performance and adaptive equalization for high density serial communications across high-loss channels, such as backplane and copper cable links.

Amphenol's Expressport™ QSFP E Series Connectors (FS1-E38-X0M0-X0) are designed for 25-28G applications and are backward compatible with current QSFP connector footprints and cage assemblies. The E series connectors also feature a unique ground commoning device which reduces crosstalk at resonant frequencies and lowers common-mode reflections.

Inphi's CMOS 100G Ethernet and OTU4 Quad 25-28G Retimer targets next-generation ultra low power optical modules with new levels of integration and advanced metrics and analysis on-die. Containing transmit and adaptive receive equalization, this device is designed to exceed 28G-VSR requirements for optical module attachment with lowest power in the industry.

Leveraging the benefits of Silicon Photonics, Luxtera's single chip opto-electronic transceiver includes four fully integrated 28Gbps transmit and receive channels powered from a single laser for an aggregate unencoded data rate of up to 112Gbps. The device is targeted for 100Gbps Ethernet, OTN and InfiniBand applications as well as emerging OIF (Optical Internetworking Forum) Short Reach (SR) and Very Short Reach (VSR) electrical interconnect to host systems.

Demo 3 description

Demo 3 demonstrates an electrical to optical 100G OUT4 rate system (4 x 28G) for line card and pluggable optical module applications.

The IBM device generates 4 x 28G lanes with a PRBS31 which pass through the Amphenol QSFP E Series connector HCB/MCB system to the Inphi Retimer. The Inphi device verifies the pattern and calculates BER as the stream passes including non-destructive high resolution eyes. The Retimer feeds the Luxtera optical module for 1490nm optical transport. With optical loopback, the Luxtera receives the stream and sends back to the 2nd Inphi Retimer, which passes the data back through the Amphenol connector, returning to the IBM ASIC for pattern verification and margin analysis.

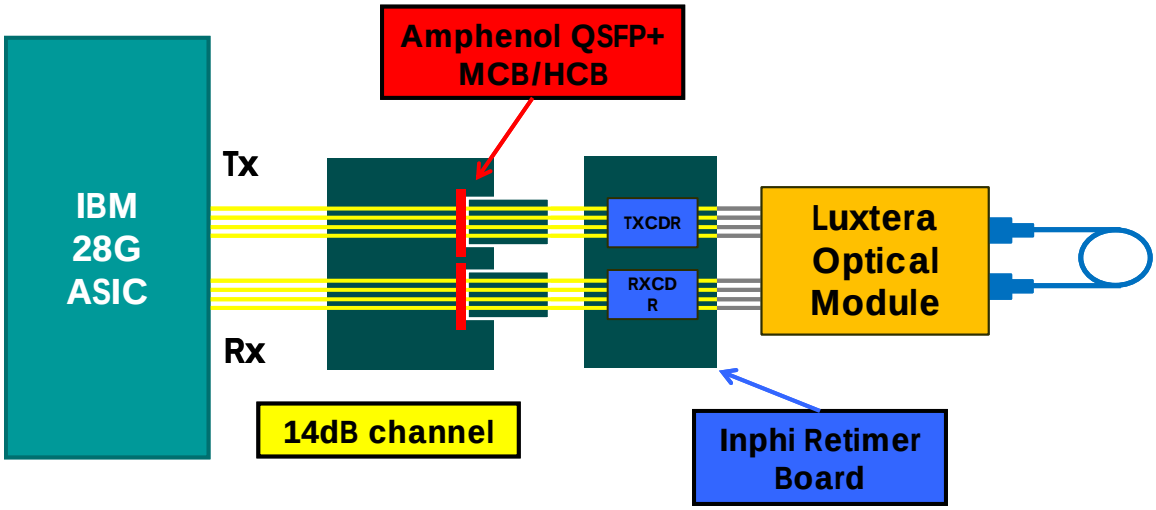

Fig. 5: Demo No. 3 Block Diagram

Demonstration No. 4
IBM-Molex CEI-25G-LR Application

Silicon Overview

IBM's High Speed Serial (HSS) 28G core is available as part of the IBM Cu32 Custom Logic product offering. It provides state-of-the-art jitter performance and adaptive equalization for high density serial communications across high-loss channels, such as backplane and copper cable links.

Connector Overview

Molex's Impact™ backplane connector is designed to support data rates per differential pair of 25+Gbps with superior signal density up to 80 differential pairs per inch. Impact's broad edge coupled geometry provides low cross-talk, low insertion loss and minimal insertion loss deviation across all high-speed channels. The PCB footprint of the Impact connector system is available in two compliant-pin design options on both daughter card and backplane connectors to allow system designers maximum flexibility in balancing signal integrity performance with mechanical stability and PCB manufacturing process limitations. The mating interface provides in-line staggered, bifurcated contacts that provide two points of contact for long-term reliability performance, low mating forces, and minimal electrical interface stub for optimal high speed performance.

Backplane Overview

The Molex Impact Reference Backplane system consists of two daughter cards, a backplane, and two Impact™ mated connectors. The Impact connector is made up of a vertical header on the backplane PCB and a right-angle receptacle on the daughter card PCB. The Impact daughter cards are 110mils thick, 12 layers each, and use Megtron 6 material with VLP foil surface finish.[1] The daughter card trace lengths are 5" from test point to connector and utilize a 5/5/5 trace width and spacing combination. The Impact backplane cards are 249mils thick, 26 layers, and use Megtron 6 material with HVLP foil surface finish. The backplane utilizes either 6/6/6 or 7/10/7 trace width and spacing combinations with channels providing the desired test range of -25db to -35db of loss across a combination of lengths.

Demo 4 description

The goal of this Interop is to demonstrate a 4-lane 100G operation across a backplane link with end-to-end loss in excess of 30dB at 12.9GHz. Each lane will carry a PRBS-31 running at 25.78125Gb/s data rate. PRBS generation and checking is performed on-chip. Error rate and link margins are reported using on-chip diagnostics.

Demo 4 will show an IBM 28G test chip operating over a Molex-supplied reference backplane built with Megtron 6 material and featuring their Impact Backplane Connector product.

[1] Megtron is a registered trademark of Panasonic

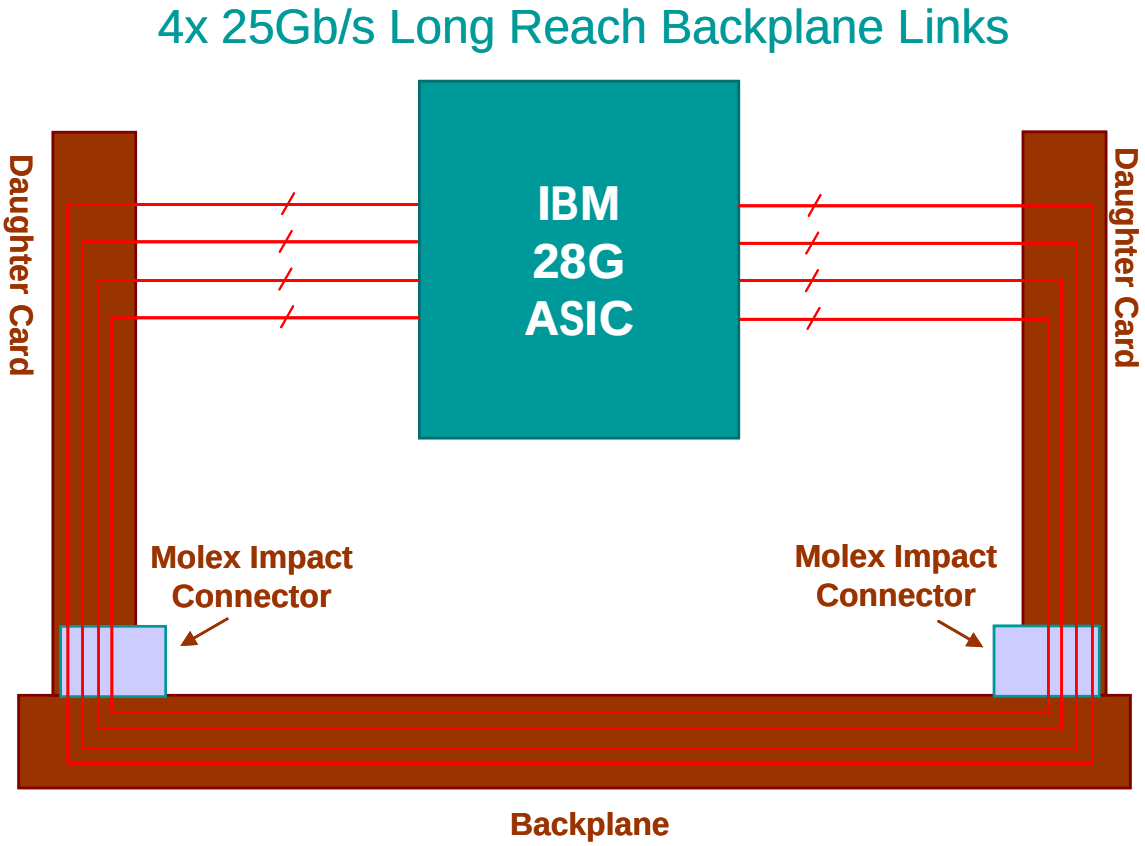

Fig. 6: Demo No. 4 Block Diagram

Demonstration No. 5
IBM-TE Connectivity - CEI-25G-LR Application

Silicon Overview

IBM's High Speed Serial (HSS) 28G core is available as part of the IBM Cu32 Custom Logic product offering. It provides state-of-the-art jitter performance and adaptive equalization for high density serial communications across high-loss channels, such as backplane and copper cable links.

Connector Overview

TE's STRADA Whisper backplane connector is designed to support data rates per differential pair up to 40Gbps. The connector's individually shielded pairs results in noise performance that is less than 1% @ 20 ps signal edge rates and insertion loss of less than 1db and flat past 15GHz. The in-row "horizontal" pair orientation results in zero skew. Since PCB interfaces are a critical element of over-all connector performance, the STRADA Whisper connector footprint has been optimized to provide a balanced solution to the competing requirements of impedance, cross talk and routability.

Backplane Overview

The TE supplied reference backplane channel consists of two daughter cards, a backplane, and two STRADA Whisper connectors. The STRADA Whisper connector is made up of a vertical header and a right-angle receptacle. The IBM 28G ASIC connects to the TE daughter cards through SMA connectors.

The daughter cards are 110mils thick using Megtron 6 material encompassing 14 layers each.[2] All of the differential traces routed from the SMA test points to the skew-less STRADA Whisper connector footprint are 5" in length in a 6-9-6 mil trace width configuration. The traces and other copper in the boards utilize Megtron 6 VLP foil finishes. The signal vias in both the STRADA Whisper connector and SMA test points are counter-bored to within 10 mils of the signal layer. The daughter card contains the STRADA Whisper receptacle.

The backplane, which contains the STRADA Whisper header, is 200mils thick using Megtron 6 material encompassing 20 layers. All of the differential traces routed on the backplane are in a 7-9-7 mil trace width configuration. The traces and other copper in the board utilize a Megtron 6 H-VLP foil finish. The signal vias in the STRADA Whisper connector footprint are counter-bored to within 10mils of the signal layer. The backplane demonstrates lengths of 4, 8, 17, and 30". When combined with a daughter card on each end the total trace length demonstrated in the channel is extended to 14, 18, 17, and 40".

[2] Megtron is a registered trademark of Panasonic.

Demo 5 description
The goal of the demonstration is to exhibit the OIF CEI 25G LR Implementation Agreement (IA) with 4-lane 100G operation across a backplane link with end-to-end loss in excess of 30dB at 12.9GHz. Each lane carries a PRBS-31 pattern running at a 25.78125Gb/s data rate. PRBS generation and checking is performed on-chip.

The demonstration contains an IBM 32nm 28G test chip operating over a TE Connectivity-supplied reference backplane. It is also built with Megtron6 material and implements TE's STRADA Whisper backplane connector product.

The 40" channel, which is used in this demonstration, contains approximately 30 dB of loss from the SMA on one daughter card to the SMA on the other daughter card. The demonstration runs 4 lanes at 25Gbps with 2 additional lanes used in order to increase the amount of XT aggressors.

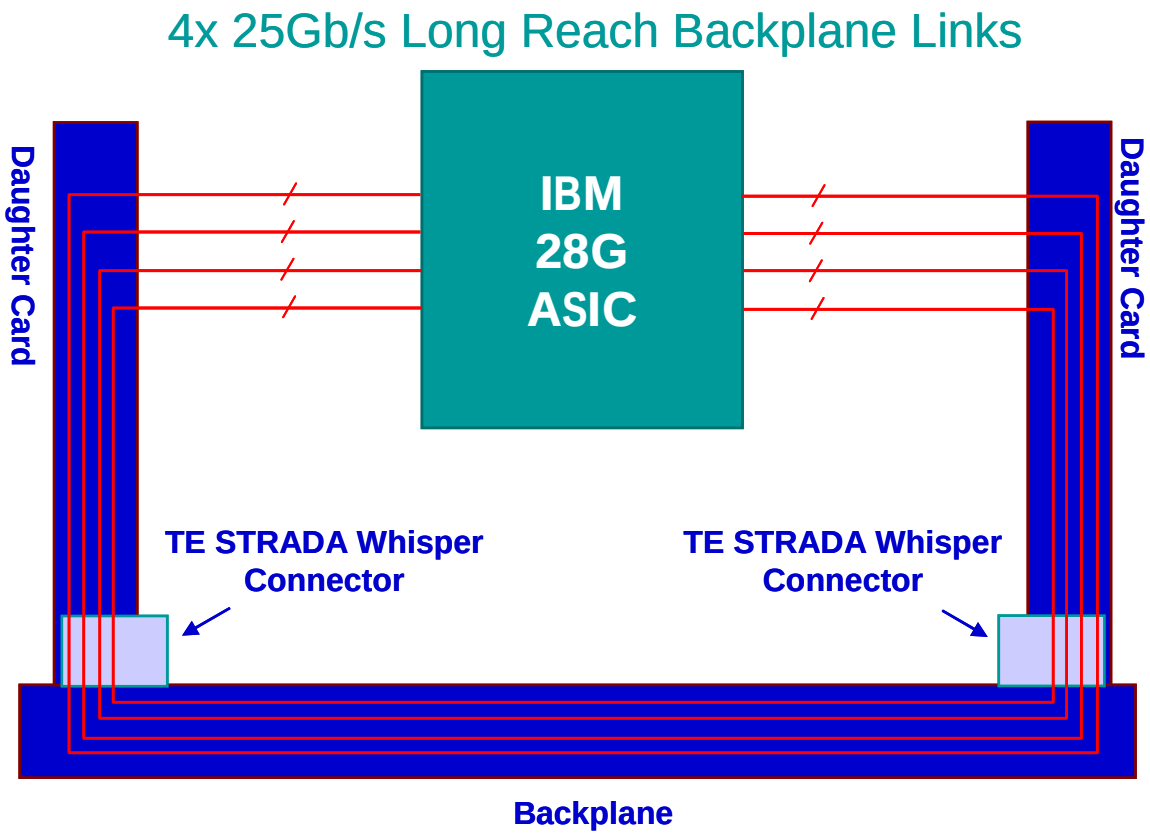

Fig. 7: Demo No. 5 Block Diagram

Conclusions

This interoperability demonstration successfully brought semiconductor, connector, optical module and test equipment vendors together to show that the CEI-25G-LR and CEI-28G-VSR Clauses have evolved from concept to reality and that a viable ecosystem is now in place to enable the commercial success of the next generation of optical module electrical interfaces in the 25 – 28 Gbaud speed range along with the backplane architectures operating with 25 Gbaud channels.