CEI-56G – Signal Integrity to the Forefront

As the next generation of data rates beyond 28Gb/s were being contemplated a number of key questions arose; would the previously reliable NRZ (non return to zero) signaling continue to support our needs at 56Gb/s or would we need to entertain other solutions including higher order modulation schemes. The OIF has faced these questions and is developing a number of new 56Gb/s implementation agreements, preparing to deliver to industry a set of solutions that address a wide array of needs including different signal modulations and different reaches ranging from a few millimeters in a chip to chip implementation up to a meter in a backplane implementation. Throughout this development work signal integrity has been the driving factor, while also debating power consumption and implementation complexity. Also addressed have been developments for establishing test and measurement compliance methodology.

OIF OPTICAL INTERNETWORKING FORUM

CEI-56G – Signal Integrity to the Forefront

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EVERY CONNECTION COUNTS

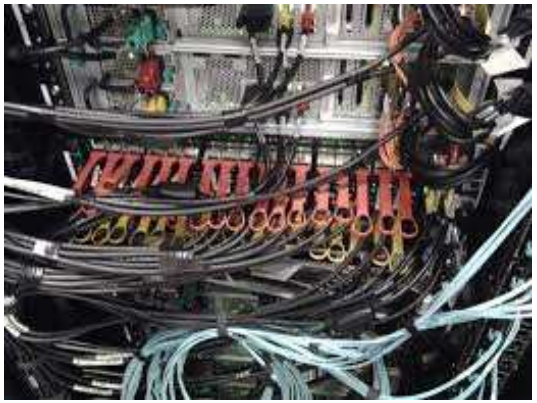
OIF's CEI work has been a significant industry contributor

Name	Rate per pair	Year	Activities that Adopted, Adapted or were influenced by the OIF CEI
CEI-56G	56Gbps	2016	The future is bright
CEI-28G	28 Gbps	2011	InfiniBand EDR, 32GFC, SATA 3.2, SAS-4,100GBASE-KR4, CR4, CAUI4
CEI-11G	11 Gbps	2008	InfiniBand QDR, 10GBASE-KR, 10GFC, 16GFC, SAS-3, RapidIO v3
CEI-6G	6 Gbps	2004	4GFC, 8GFC, InfiniBand DDR, SATA 3.0, SAS-2, RapidIO v2, HyperTransport 3.1
SxI5	3.125 Gbps	2002-3	Interlaken, FC 2G, InfiniBand SDR, XAUI, 10GBASE-KX4, 10GBASE-CX4, SATA 2.0, SAS-1, RapidIO v1
SPI4, SFI4	1.6 Gbps	2001-2	SPI-4.2, HyperTransport 1.03
SPI3, SFI3	0.800 Gbps	2000	(from PL3)

Key Points

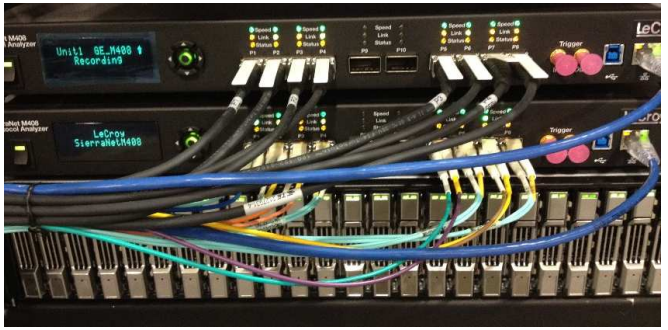
OIF Common Electrical Interconnect (CEI) Implementation Agreements (IAs) and their predecessor documents have served the industry across many applications

- Storage
- Memory
- High Performance Compute
- Networking
- Telecom
- Enterprise



These applications do not all value performance the same

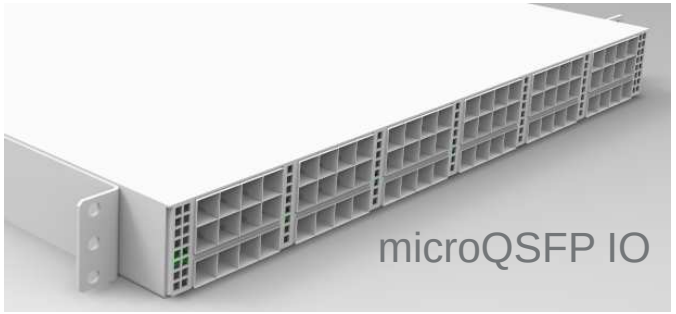
- Latency, power, cost, density, reach, throughput

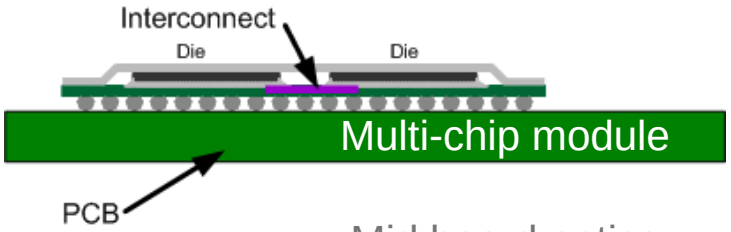


At 56Gbps ……..

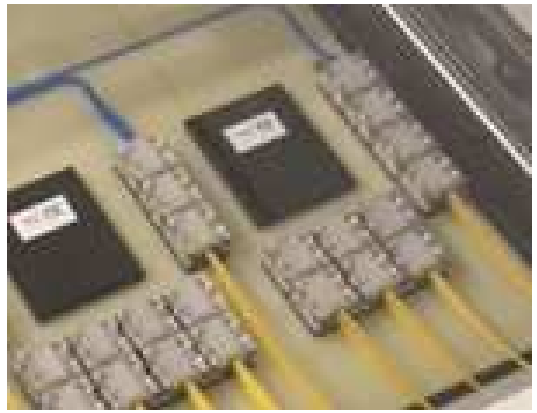
One solution does not look likely to satisfy all requirements

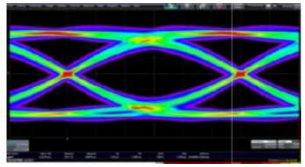
- Modulations: optimize for SI, reach and latency
- Reaches: optimize for SI and power
- Semiconductor packaging: optimize for SI and power
- Equipment architectures
- Density



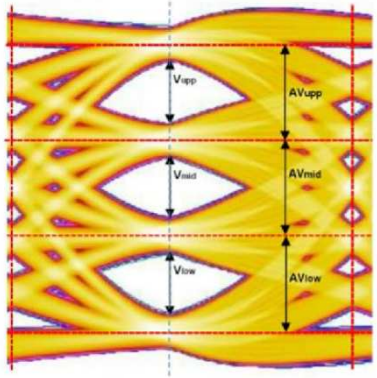


Mid board optics



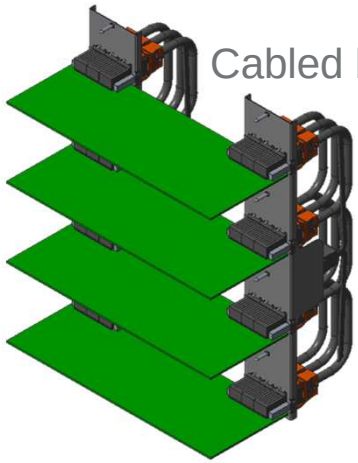


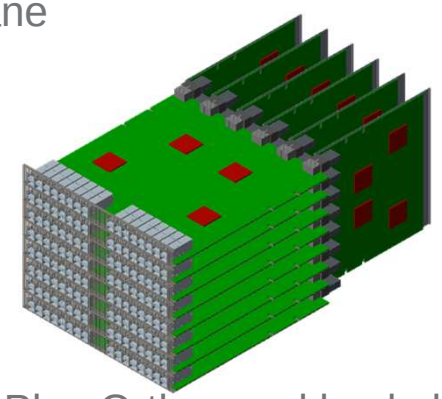
NRZ Modulation



PAM4 modulation

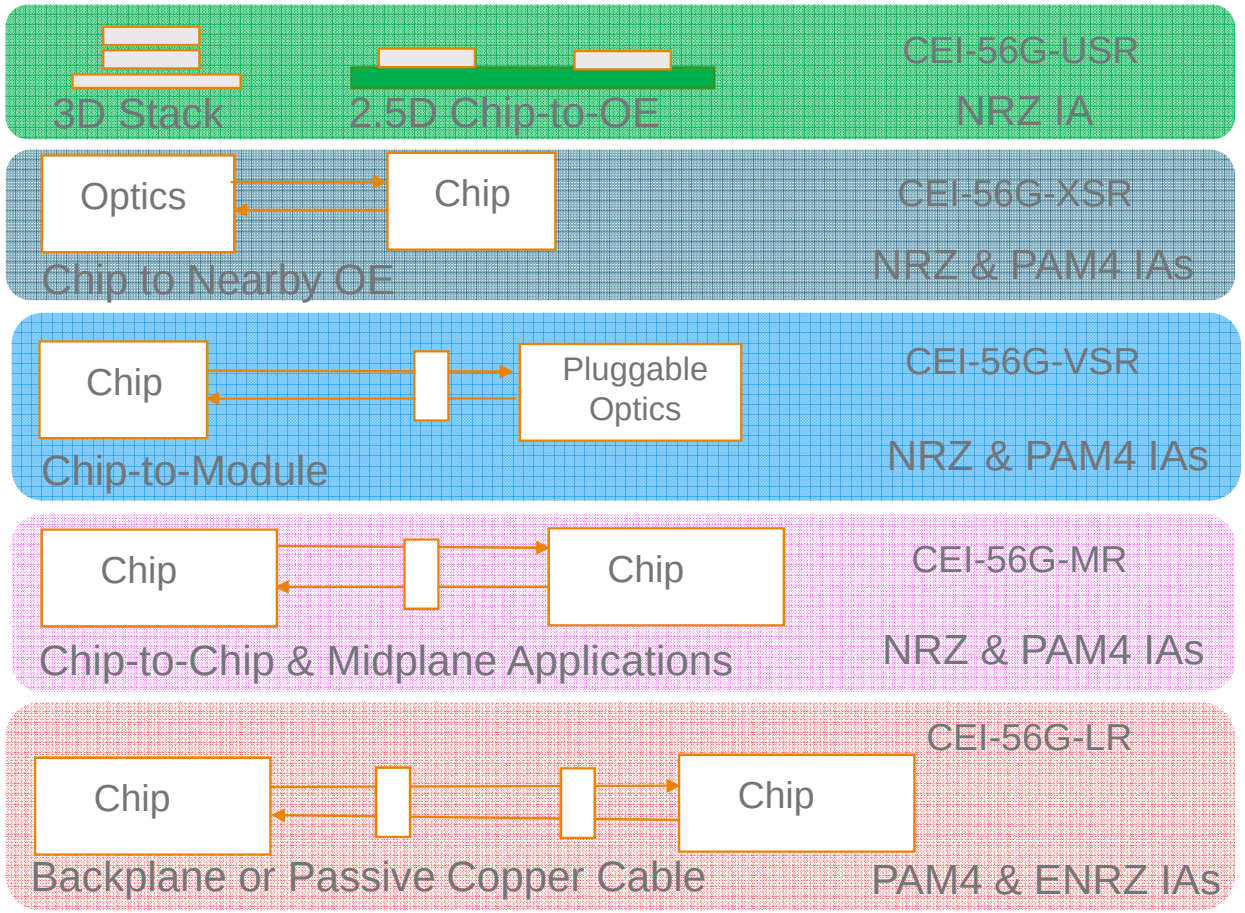
Cabled backplane





Direct Plug Orthogonal backplane

CEI-56G Application Space



- **USR: 2.5D/3D applications**
  - **1 cm, no connectors, no packages**
- **XSR: Chip to nearby optics engine**
  - **5 cm, no connectors**
  - **5-10 dB loss @28 GHz**
- **VSR: Chip-to-module**
  - **10 cm, 1 connector**
  - **10-20 dB loss @28 GHz**
- **MR: Interfaces for chip to chip and midrange backplane**
  - **50 cm, 1 connector**
  - **15-25 dB loss @14 GHz**
  - **20-50 dB loss @28 GHz**
- **LR: Interface for chip to chip over a backplane**
  - **100cm, 2 connectors**
  - **35dB at 14Ghz**

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- **Panelists:**
  - **David Stauffer**

Dr. Stauffer has extensive experience in the design and architecture of high speed SERDES and DDR memory interfaces. His contributions to OIF electrical interface standards span 15 years as a member of the technical staff of Kandou Bus, S.A., and in his previous position with IBM Microelectronics. He has been the chair of the OIF Physical and Link Layer Working Group since 2006, and is currently OIF Secretary/Treasurer. He has also authored contributions to both INCITS T11 Fibre Channel and JEDEC JC-16 standards organizations. Past publications include the text "High Speed Serdes Devices and Applications" (Springer, 2008).

  - **Steve Sekel**

Steve Sekel is the strategic program planner at Keysight Technologies responsible for defining requirements of measurement solutions for next generation data center networking standards and implementation agreements. He currently serves as the OIF Physical and Link Layer Interoperability Working Group chair. Steve has been involved with electronic test and measurement instrumentation for over 35 years. During this time he has held a number of roles in product marketing, project management and design engineering, with some of the leading T&M companies. He had authored contributions focusing on test methodology in OIF CEI working groups and INCITS T11 Fibre Channel 28G projects.

  - **Tom Palkert**

Tom Palkert has worked on high speed SERDES designs from 100m to 56Gbps. He is involved in Ethernet, Fibre channel, InfiniBand and the Optical Internetworking Forum. Tom is a past member of the OIF board of directors, past chair of the OIDA silicon photonics alliance and is currently chair of the Fibre Channel T11.2 Physical Layer Task Group and vice chair of the OIF Physical and Link Layer (PLL) working group.