# Concept to Reality – Interoperability Testing of the Common Electrical Interface (CEI)


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## *Executive Summary*


In just two years the OIF has taken the development of the Common Electrical I/O[1] (CEI), a 6 Gigabit per second (Gbps) and 11 Gbps electrical interface specification, from concept to reality. In December 2004, a private interoperability event was held where OIF member companies successfully demonstrated interoperability of CEI electrical signaling among four silicon providers and four backplane providers.

Four CEI clauses were tested:


[1] see Appendix A CEI Overview for more details of the CEI specification

- CEI-6G-SR for six Gigabit short reach (chip to chip, or chip to mezzanine)
- CEI-6G-LR for six Gigabit long reach (over backplanes & 2 connectors)
- CEI-11G-SR for eleven Gigabit short reach (chip to chip, or chip to mezzanine)
- CEI-11G-LR for eleven Gigabit long reach (over backplanes & 2 connectors)

The backplanes were representative of a wide range of board design techniques including both legacy and greenfield backplanes. The testing emulated the challenges faced by system designers utilizing high-speed electrical signaling. DesignCon West 2005 will showcase working demonstrations of the four CEI clauses, using test scenarios similar to the private interoperability tests.

## *From Concept to Reality in Two Years*

In November of 2002, responding to an industry-wide demand for 6G and 11G high-speed interface standards, the OIF initiated the Common Electrical I/O (CEI) project[2]. The 6G Short Reach (SR), 6G Long Reach (LR) and the 11G Short Reach (SR) specifications are complete. The 11G-LR is in the final stages of development. The completed specifications captured in Implementation Agreements are publicly available on OIF's web site.

http://www.oiforum.com/public/impagreements.html

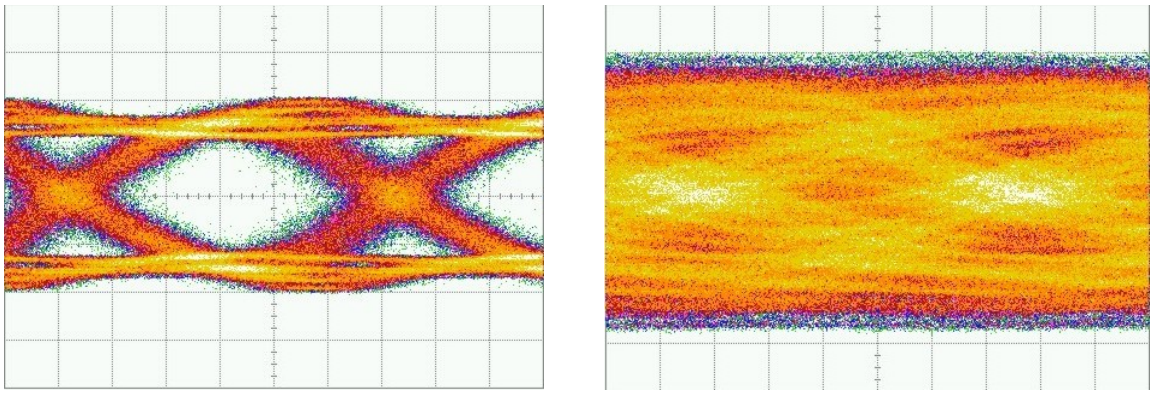
Taking the vision of the industry's need for higher speed interconnects to a multi-vendor interoperability demonstration in just two years is a significant achievement. An entire ecosystem of semiconductor, connector, printed circuit board, backplane and test equipment suppliers have developed solutions that support the CEI electrical signaling. The culmination of this effort was showcased in December 2004, when OIF member companies conducted private interoperability testing. The success of this event validates that an ecosystem now exists to enable system vendors to deliver complete 6G and 11G solutions based on the CEI specification.

## *How CEI can impact today's systems*

The CEI clauses have immediate impact to system designs today. The desire of many system vendors to double or quadruple the bandwidth of existing systems (without increasing the number of backplane traces) is the main driver behind the move towards 6G and 11G. Further validating this trend, Fibre Channel, Infiniband™, IEEE 802.3ae Backplane Ethernet Task Force, Network Processing Forum ,RapidIO™ and PCI-Express™ have announced plans or are in development of signaling at 5 Gbps and beyond.

Another important factor deals with the advancement of optical modules both in performance and footprint reduction. As the form factor of optical modules decreases, the I/O capacity of line cards will become critical. The small form factor XFP optical module, widely available today, provides an immediate application for the 11G SR clause. Greenfield designs for high bandwidth systems can utilize 11G LR as a means to manage design and direct material costs by reducing I/O trace requirements on line cards using increased signaling speed.

[2] For more information on CEI please see Appendix A.



**Transmit Eye** **Receive Eye**

**Figure 1: The Reality of Multi-Gigabit Transmission**

## *Understanding CEI Channels*

The development of an electrical specification for multi-Gigabit transmission presents a daunting challenge. The reality is that as the speed across a passive channel increases, the inherent limitations of the channel between the transmitter and receiver causes the eye at the input to the receiver to close, as shown in Figure 1. Using signal conditioning techniques at the transmitter and equalization techniques at the receiver, the eye can be opened. At these high signaling speeds, the eye at the input to the receiver may be completely closed. Receive equalization must then be used to open the eye. Thus specifying the channel between the transmitter and receiver becomes a critical part of developing a specification for the real system interconnect shown in Figure 2.

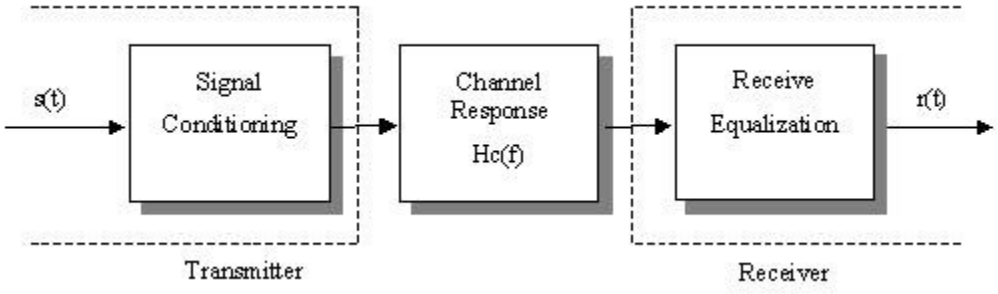



**Figure 2: The System Interconnect**

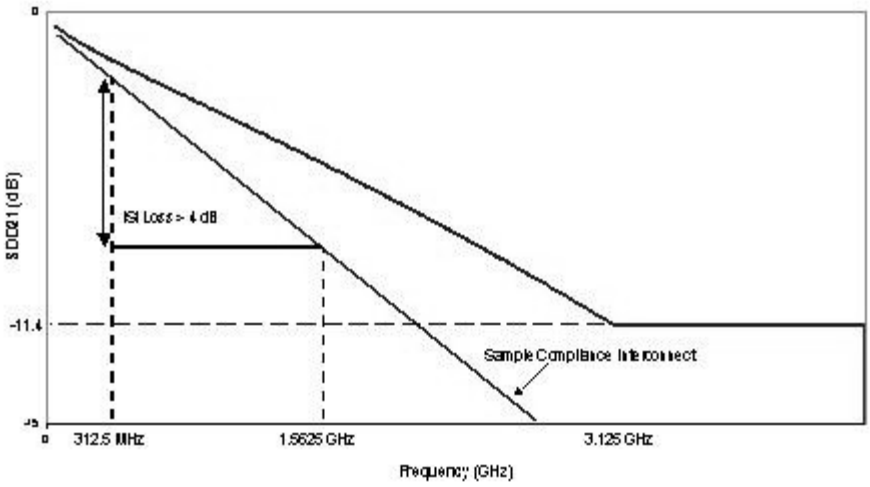



**Figure 3: XAUI Channel Model**

Past specifications, such as TFI-5 or XAUI (shown in Figure 3 above), defined a compliant channel solely by the differential insertion loss of the forward channel versus frequency[3] There are serious limitations to such a basic approach. Relatively few channels, especially channels from legacy-style backplanes, are capable of being usefully characterized by this model. The next problem is that there are other aspects of the channel that can significantly hamper overall performance, such as channel return loss, device return loss, near-end crosstalk[4] and far end crosstalk[5]).

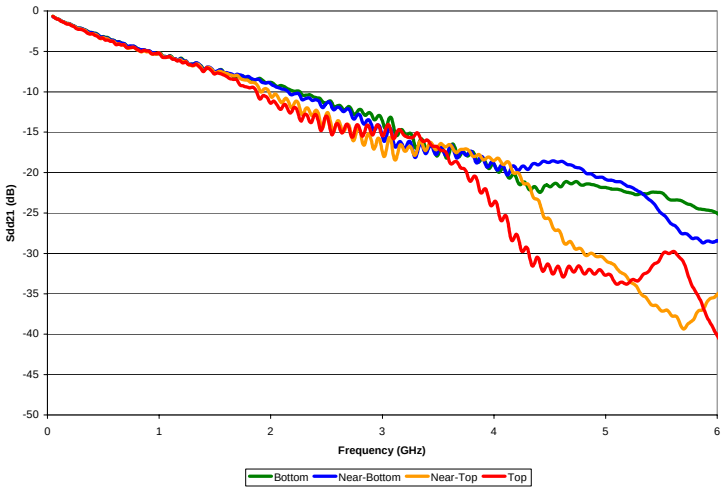



**Figure 4: Impact of Layer Connection**

The plot in Figure 4 above demonstrates the performance of various channels through the entire layer stack-up of a backplane. Ripples and nulls in the performance of various

[3] Commonly referred to as $S_{DD21}$
[4] Commonly referred to as NEXT
[5] Commonly referred to as FEXT

channels caused by the plated through-hole stubs in the backplane are visible. It is easy for an engineer to look at such data and make a qualitative prediction as to the performance of a given channel in comparison to the others. It is not possible, however, by merely looking at this plot to quantitatively state what the BER performance of a given channel will be. This requires substantial analysis and simulation. Hence, channel S-parameters provide a valuable building block for analysis, but do not provide a direct correlation to BER performance.

Therefore, the OIF took a radical departure from the channel compliancy methodology used by previous specifications. The OIF chose to use a statistical analysis methodology which considers all of the aspects of the system synergistically based on a simulated transmitter and receiver. This provides a quantitative prediction of the post receive equalization eye-opening for the channel's target BER performance. Channel compliancy for guaranteed interoperability is then based on having sufficient eye-opening for the stated BER. It is also important to note that the simulated transmitter and receiver represent the minimum requirements of the specification, but do not define the actual algorithm that a silicon vendor is required to implement. Instead, the silicon vendor must develop a solution that will provide equivalent or better performance than the simulated minimally compliant transmitter and receiver for any channel.

Interoperability performed under a single condition, provides only limited insight into the capabilities of devices designed for a specification (such as CEI). Therefore, the OIF turned to its membership to provide channels of relevant interest to the market. As shown in the Test Results section, a wide variety of types of channels were used to test interoperability between devices. Both legacy and greenfield implementations were provided. This allowed testing of channels that exceeded the legacy specifications of XAUI and TFI-5. Varying trace widths, board materials, and use or non-use of stub reduction techniques achieved these types of performance levels. Furthermore, to address market interest in Advanced Telecom Computing Architecture (AdvancedTCA) http://www.picmg.org/newinitiative.stm, representative implementations of this architecture were tested as well.

## *Objectives of CEI Interoperability Testing*

Interoperability is one of the keys to the success of any standard. In order to promote the acceptance and demonstrate the viability of CEI, the OIF sponsored a private, closed-door interoperability demonstration in December of 2004. Proving that CEI is widely supported by various companies across the industry the participants included four semiconductor manufacturers (AMCC, Altera, Vitesse and Xilinx), four backplane vendors (Flextronics, Interconnect Technologies, Molex and Tyco Electronics) and two test equipment companies (Agilent and Tektronix). Cooperation between semiconductor, backplane and test equipment suppliers is crucial to enable implementation and integration of high-speed signaling by system vendors. DesignCon West 2005 will showcase working demonstrations of the four CEI Clauses, using test scenarios similar to the private interoperability tests.

## Backplane Overview

The backplanes used for the interoperability testing event cover the broad range of PCB complexities and design practices commonly used in the industry. The primary channel differences are material performance, total channel length, via construction and connector performance. For the interoperability demonstration, adapting various silicon vendors test boards to a variety of backplane and connector vendors required the use of backplane adaptor cards (introducing additional losses and discontinuities). These cable fit adaptor cards provided SMA to backplane connector specific conversion that would be absent in dedicated solutions. Backplane connectors were thru hole with the exception of one backplane, which utilized surface mount connectors. The backplane participants included:

- Interconnect Technologies, a division of Northrop Grumman, supplied a Dual Star Advanced-TCA architecture solution. Both the backplane and daughtercards were constructed with Nelco N4000-13 SI™ material.

- Molex supplied full duplex backplane channels using GbX™ compliant pin connectors. Channel lengths, including adaptor cards, ranging from 8.0" (0.2 meter) to over 1.0 meter were duplicated in Nelco N4000-13 SI™ and Isola FR408 laminates.

- Tyco Electronics supplied full duplex backplane channels, based on proprietary and ATCA architectures using the Z-PACK HM-Zd™ compliant pin connectors. Various channel lengths from 6" (0.15m) to 50" (1.27m) were constructed from backplane traces that ranged from 1" to 30" and line cards that ranged from 2.5" to 10". Both backplanes and line cards were supplied in Nelco N4000-6, Nelco N4000-13, and Nelco N4000-13 SI™ laminates.

- Flextronics supplied a large, high density backplane implemented in Rogers RO4350™, with over 4000 differential pairs. Channel lengths, including daughter cards, were up to 1.5 meters and included crosstalk aggressors. These were duplicated with multiple types of connectors.

## Silicon Overview

There were four silicon vendors at the InterOp: Altera, AMCC, Vitesse and Xilinx. Each of these vendors devices support transmit pre-emphasis and receive equalization.

- Altera tested using their 6.5 Gbps Serdes developed in 90 nm CMOS technology. Altera's 6.5 Gbps Serdes utilizes de-emphasis and pre-emphasis on the transmitter and a linear equalizer on the receiver.

- AMCC's 11G silicon is based on 0.13u CMOS technology. Transmitter emphasis and receiver equalization is employed.

- Vitesse used their 6G 0.13u CMOS VSC1129 device. It has programmable pre-emphasis transmitters and DFE/FFE receivers with adaptive EQ.

- Xilinx utilized their standard 2VPX20 Virtex-II Pro X™ FPGA, in production since July 2004, for the interoperability testing at 6 and 10 Gbps. The serial I/O's have both programmable transmit pre-emphasis and active receive equalization.

Each of the silicon vendors used different approaches to solve the same problem of operating and interoperating in a difficult channel environment. It is important to note that the CEI specification does not specify any particular implementation.

## *Test Equipment Overview*

Agilent Technologies provided:

- Digital Communications Analyzers (86100C) equivalent time sampling oscilloscopes with dual electrical samplers up to 80 GHz which were used to illustrate the signals at different points in the test set-ups and for time domain reflectometry.

- A 6 GHz bandwidth real-time oscilloscope (E54855A) for system clock and set-up.

- Parallel and serial bit error ratio testers (81250 and N4901B) and a pattern generator (81134A) for high rate pattern generation and non-integral divided clock generation.

- The Physical Layer Test system based on a vector network analyzers (E8362B and N1930A) for measurement of transmission and reflection properties, i.e., *S*-parameters of backplanes.

- Vector signal generators (E4438C and E8267C) for generation of frequency-locked reference clock signals.

Tektronix provided:

- A Communication Signal Analyzer (CSA8200) equivalent time sampling oscilloscope with a dual 20 GHz electrical sampling head which was used to illustrate the signals at different points in the test set-ups and for time domain reflectometry.

- An 8 GHz bandwidth real time oscilloscope (CSA6804B) used to help with clocking and initial set up issues.

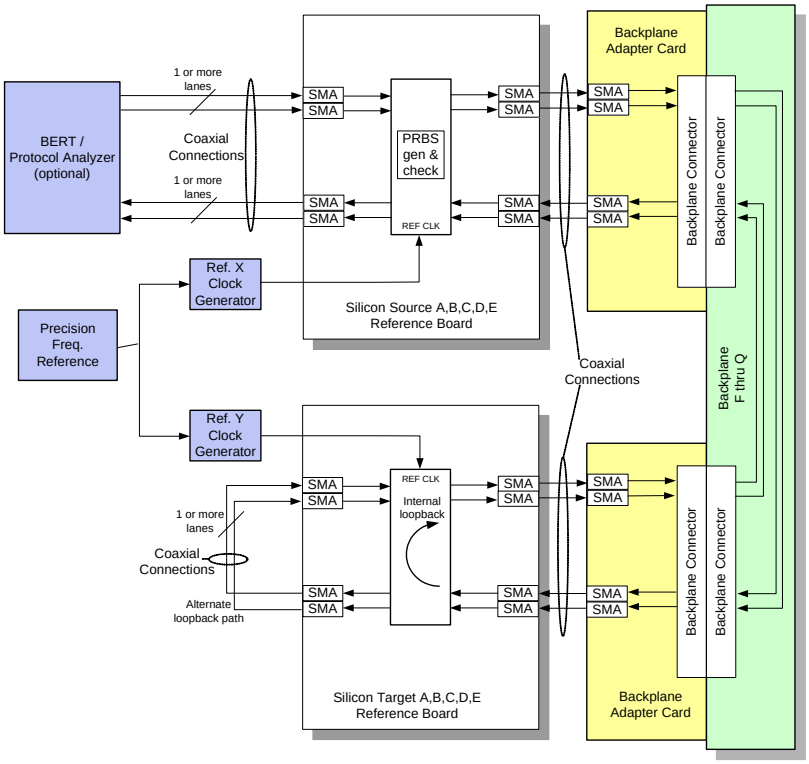



**Figure 5: Test Setup Block Diagram**

## *Test Set Up*

Time domain reflectometry was performed on equivalent time sampling oscilloscopes for trouble-shooting set-ups, matching cable lengths for differential signals and determining impedance profiles. The physical layer test system was used for initial characterization of backplanes. The sampling oscilloscopes were also used to determine signal quality at both transmitter and receiver.

The interoperability tests required frequency locking of the transmitter and receiver system clocks. Since systems from different vendors use different clock dividers, the Vector Signal Generators (VSG) were used to provide phase-locked clock sources. The internal 10 MHz references of two VSGs were tied together and the respective clock rates of the differing vendor's equipment were independently set and provided to the transmitter and receiver.

As shown in Figure 5 above, the Interoperability Demonstration involved a PRBS pattern from a semiconductor source device [A-E] driving a channel from backplane [F-Q] and being received by a semiconductor target device [A-E]. In turn, the target device [A-E] would loop the received signal back to the source device [A-E], where it would be tested for bit errors either by the source device [A-E] or by external test equipment. It was necessary to demonstrate error-free operation over $10^{12}$ transmitted bits, to verify successful operation.

## *Test Results*

Test results are reported anonymously. Each channel provider brought various configurations to cover the various applications previously described. To verify successful operation, it was necessary to demonstrate error-free operation over $10^{12}$ transmitted bits.

### 6G Interop

The 6G Interop participants included Altera, Flextronics, Molex, Northrop Grumman, Tyco Electronics, Vitesse, and Xilinx. Successful interoperability was achieved from 8" to 53" of transmission lines. Legacy-type materials and configurations as well as channels targeted at greenfield applications were part of the interop testing. In addition, interoperability for the 6G SR clause was demonstrated by interconnecting the silicon boards directly through coaxial cables. The table below collates the testing that was done between silicon devices identified as A, B, C over backplanes identified as F thru L.

| **6 G Interop Results** | | **Silicon Source A** | **Silicon Source B** | **Silicon Source C** |
|---|---|---|---|---|
| **Backplane F** Nelco N4000-13SI | **Silicon Target A** | | 21" (0.53 m) | 31" (0.79 m) |
| | **Silicon Target B** | 21" (0.53 m) | 21" (0.53 m) | 21" (0.53 m) |
| | **Silicon Target C** | 31" (0.79 m) | 21" (0.53 m) | |
| **Backplane G** Nelco N4000-13SI | **Silicon Target A** | 49" (1.25 m) | 25" (0.63 m) | 30"-49" (0.76 m-1.25 m) |
| | **Silicon Target B** | 25" (0.63 m) | | 30"-49" (0.76 m-1.25 m) |
| | **Silicon Target C** | 30"-49"(0.76 m-1.25 m) | 30"-49" (0.76 m-1.25 m) | |
| **Backplane H** Isola FR408 | **Silicon Target A** | 39" (1 m) | | 39" (1 m) |
| | **Silicon Target B** | | | 39" (1 m) |
| | **Silicon Target C** | 39" (1 m) | 39" (1 m) | |
| **Backplane I** Nelco N4000-13 | **Silicon Target A** | | 36" (0.91 m) | |
| | **Silicon Target B** | 36" (0.91 m) | | 36" (0.91 m) |
| | **Silicon Target C** | | 36" (0.91 m) | |
| **Backplane J** Nelco N4000-6 | **Silicon Target A** | | 35" (0.89 m) | |
| | **Silicon Target B** | 35" (0.89 m) | | 35" (0.89 m) |
| | **Silicon Target C** | | 35" (0.89 m) | |
| **Backplane K** Rogers Laminate | **Silicon Target A** | 37"-53" (0.94m-1.35 m) | | |
| **Backplane L** Rogers Laminate SMT connector | **Silicon Target A** | 53"(1.35 m) | | 45"-53" (1.14m-1.35 m) |
| | **Silicon Target C** | 45"-53"(1.14 m - 1.35 m) | | |

### 11G Interop

The 11G Interop participants included AMCC, Flextronics, Molex, Northrop Grumman, Tyco Electronics and Xilinx. Successful Interoperability was achieved from 22" to 49" of transmission lines. The 11G interoperability channels are greenfield type applications including among others "improved FR4" materials and backdrilled vias. In addition, interoperability for the 11G SR clause was demonstrated by interconnecting the silicon boards directly through coaxial cables. The table below collates the testing that was done between silicon devices identified as D and E over backplanes identified as M thru Q.

| 11G Interop Results | | Silicon Source D | Silicon Source E |
|---|---|---|---|
| **Backplane M** Nelco 4000-13SI | **Silicon Target D** | 22"(0.56 m) | 22"-31"(0.56 m - 0.79 m) |
| | **Silicon Target E** | 22"-31"(0.56 m - 0.79 m) | |
| **Backplane N** Nelco 4000-13SI | **Silicon Target D** | 25" (0.63 m) | 30" (0.76 m)) |
| | **Silicon Target E** | 30" (0.76 m) | |
| **Backplane O** Isola FR408 | **Silicon Target D** | 25" (0.63 m) | 30"(0.76 m) |
| | **Silicon Target E** | 30"-40"(0.76 m-1.00 m) | |
| **Backplane P** Nelco 4000-13SI | **Silicon Target D** | | 22" -31"(0.56 m - 0.79 m) |
| | **Silicon Target E** | 22" -31"(0.56 m - 0.79 m) | |
| **Backplane Q** Rogers Laminate Surface Mount Connector | **Silicon Target D** | 33" (0.84 m) | 33" - 45" (0.84 m - 1.14 m) |
| | **Silicon Target E** | 33" - 45" (0.84 m - 1.14 m) | |

## *Conclusions*

This interoperability demonstration successfully brought semiconductor, backplane and test equipment vendors together to show that CEI has gone from concept to reality in terms of developing viable backplane and chip-to-chip transmission at speeds of 6 Gbps and 11 Gbps.

Cooperative efforts such as the interoperability demonstration at DesignCon West 2005 show that the ecosystem necessary for 6 and 11 Gbps systems are in place today. This type of cooperation is absolutely essential to enable system vendors to migrate their products to 6 and 11 Gigabit links.

## *Appendix A CEI Overview*

The OIF's unique membership allowed the development of clear objectives for the work of CEI. The following primary objectives were defined.

- Allow single and multi-lane applications
- Support AC coupling
- Support Hot Plug
- Achieve a Bit Error Ratio lower than $10^{-15}$ per lane with a test requirement to verify better than $10^{-12}$ per lane
- Define an 11G-SR link that is SONET/SDH compliant at the optical carrier (OC) interface
- Define a 6G-LR link that accommodates legacy IEEE 802.3 XAUI and TFI-5 compliant backplanes
- The short and long reach links shall interoperate for signal path lengths up to 200mm

The Common Electrical I/O Clauses include the following:

- Electrical and jitter methodologies for new high-speed interfaces and older OIF interfaces such as SxI-5, SFI-4.2, SFI-5.1, SPI-5.1 and TFI-5.
- A CEI-6G-SR Short Reach specification for data lane(s) that support bit rates from 4.976 to 6.375 Gsym/s over Printed Circuit Boards with physical reach from 0 to 200mm and up to 1 connector.
- A CEI-6G-LR Long Reach specification for data lane(s) that support bit rates from 4.976 to 6.375 Gsym/s over Printed Circuit Boards with physical reach from 0 to 1m and up to 2 connectors.
- A CEI-11G-SR Short Reach specification for data lane(s) that support bit rates from 9.95 to 11.1 Gsym/s over Printed Circuit Boards with physical reach from 0 to 200mm and up to 1 connector.
- A CEI-11G-LR Long Reach specification for data lane(s) that support bit rates from 9.95 to 11.1 Gsym/s over Printed Circuit Boards with physical reach from 0 to 1m and up to 2 connectors. The primary focus of the 11G-LR CEI implementation agreement is for non-legacy or greenfield applications, optimized for overall cost-effective system performance including total power dissipation.

The clauses define applicable data characteristics (e.g. DC balance, transition density, maximum run length), channel models and compliance points/parameters CEI specifically excludes any pin-out, management interface, power-supply or connector specification. For more insights, the reader is advised to review the CEI White Paper at:

http://www.oiforum.com/public/documents/CEIWP.pdf.

With the exception of the 11G-LR specification which is nearing completion, the CEI Implementation Agreement has been released and is available on the OIF website.

http://www.oiforum.com/public/impagreements.html

As a separate project, a protocol intended for use with CEI electrical interfaces called CEI Protocol (CEI-P) is also being defined and covers Adaptation, Aggregation and Framing sub-layers. The goal of the Protocol is to facilitate the transport of the next generation of SFI, SPI, TFI and other interfaces.