Network Processing Forum Hardware Working Group

Look-Aside (LA-1B) Interface Implementation Agreement

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LA-1B Editor

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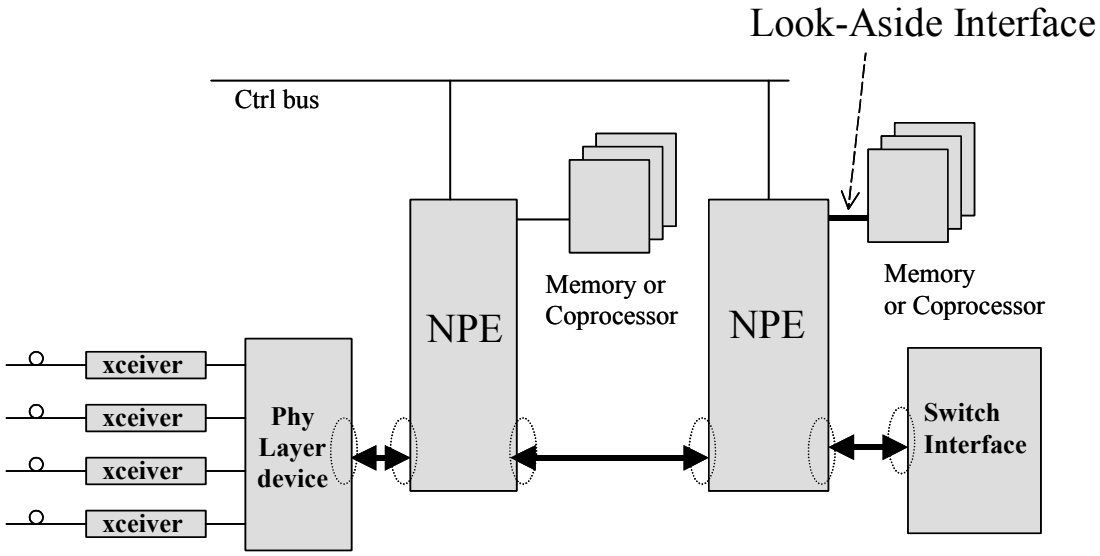
1. Scope and Purpose

This document describes the LA-1B interface draft implementation agreement. LA-1B is intended to increase the performance of the current LA-1 Implementation Agreement (NPF-LA-1-01.1). The Look-Aside interface is intended for devices located adjacent to a network processing element (NPE) that offload certain tasks to attached coprocessors. The Streaming interface (NPF-SI-1-01.0) addresses processing in the data path that is complementary to the Look-Aside interface.

Figure 1: System Block Diagram



The LA-1B interface is targeted to support the lookup requirements for OC-48 through OC-192 line rates. The minimum performance specification for lookup-based coprocessors is four or more lookup operations at OC-48 and one or more lookups at OC-192. Packet count assumptions are for line rate performance using 40-byte packets and 144-bit search keys.

2. Normative References

The following documents contain provisions which, through reference in this text, constitute provisions of this implementation agreement. At the time of publication, the editions indicated were valid. All referenced documents are subject to revision, and parties to agreements based on this implementation agreement are encouraged to investigate the possibility of applying the most recent editions of the following standards:

- JESD8-6 – High Speed Transceiver Logic (HSTL Class II). A 1.5V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits. See http://www.jedec.org/
- JESD8-16 – Bus Interconnect Logic (BIC). A 1.2V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits. See http://www.jedec.org/

3. Acronyms and Abbreviations

The following acronyms and abbreviations are used in this implementation agreement:

- DDR – Double Data Rate
- HSTL – High Speed Transceiver Logic
- BIC – Bus Interconnect Logic
- LA-1 – Network Processor Forum First generation Look-Aside interface
- LA-1B – Network Processor Forum Second generation Look-Aside interface
- # – Denotes an active low signal (e.g. W# for Write-bar)

4. LA-1B Interface Overview

The LA-1B interface is based on separate double data rate (DDR) buses for data inputs and outputs. Using DDR interfaces, data is clocked on the rising and falling edges of the clock signals. This effectively doubles the bandwidth of the interface without increasing the clock speed or the bus width. The LA-1B interface allows a different minimum latency for read and write operations to the same address. Further latency bounds for read and write operations are beyond the scope of this implementation agreement.

Coprocessors such as Network Search Engines (NSE), SRAMs, Content Inspection Engines (CIE) and other LA-1B compliant devices are required to respond to a read command (at the pin interface) as described in the timing diagrams shown in Figure 3 and Figure 4. Note that the interface may also be used with coprocessors that can return out-of-order results.

The LA-1B interface features include but are not limited to:

- Concurrent read and write operation
- Unidirectional read and write interfaces
- Single address bus
- 18 pin DDR data output path.
- 18 pin DDR data input path

4.1. LA-1B Enhancements

This section describes the major LA-1B enhancements with respect to the LA-1 implementation agreement.

- The maximum frequency of operation supported by LA-1B is 500 MHz compared to 200 MHz supported by LA-1.
- LA-1B supports burst of 4 mode in addition to burst of 2 mode supported by LA-1.
- LA-1B supports a 1.2V I/O (JESD8-16) in addition to 1.5V I/O (JESD8-6) supported by LA-1. 1.2V interface mode results in:
  - Lower power dissipation
  - Less noise
  - Allows a more advanced low voltage fabrication process to be used for components.

Notes:

- It is recommended that the 1.5V interface option only be supported for up to 333 MHz operation and the 1.2V interface option be supported for any LA-1B speed. The 1.5V option is supported to allow backward compatibility with existing LA-1 devices.
- Though it is possible to design a 1.2V interface which is 1.5V tolerant allowing interoperability between the existing LA-1 and next generation LA-1B devices, it is not a requirement. LA-1 and LA-1B devices may not interoperate due to differences in electrical characteristics.

4.2. LA-1B Compliance

For a host or a slave device to be LA-1B compliant following requirements have to be satisfied.

Table 1: LA-1B Compliance

LA-1B Burst of 2 Compliant	LA-1B Burst of 4 Compliant
Support one or more speed bins defined in Section 7.4	Support one or more speed bins defined in Section 7.4
Support 1.2 V (JESD8-16) or 1.5 V (JESD8-6) I/Os	Support 1.2 V (JESD8-16) or 1.5 V (JESD8-6) I/Os
Support burst of two mode i.e. 32-bit data alignment shown in Table 3 and Table 4.	Support burst of two mode i.e. 64-bit data alignment shown in Table 5 and Table 6.
Host and slave devices have to support all the required signals as described in Section 5.	Host and slave devices have to support all the required signals as described in Section 5.

5. LA-1 Signal Descriptions

The LA-1B interface transfers information between a Network Processing Element (NPE) and a coprocessor. One LA-1B port includes clock, address, and control pins, plus 16 data + 2 parity pins for write operations and 16 data + 2 parity pins for read operations. Figure 2 shows the bus signals for the LA-1B Interface.

Figure 2: LA-1B Interface Bus Signals

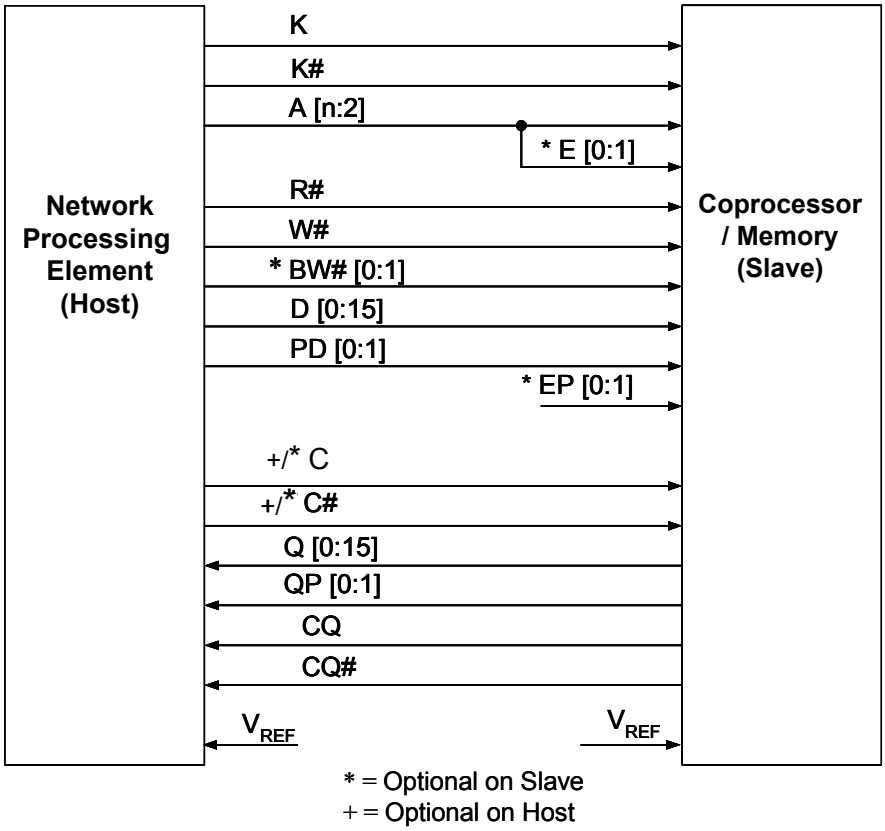


Table 2 describes the LA-1B interface signals. Table 2 is meant to describe the functionality of the signals not the timing. The timing information for each signal is described elsewhere in this document.

Table 2: LA-1B Interface Signals

Signal	Host		Slave		Description
	Std	I/O	Std	I/O	
K K#	Req	Out	Req	In	Clock inputs for LA-1B interface inputs. Rising-edge active. The rising edge of K is used to latch address and control inputs. The rising edge of K and K# are used to latch data. K# is ideally 180 degrees out of phase with K.
C C#	Opt	Out	Opt	In	Clock inputs for LA-1B interface outputs. Rising-edge active. They provide a controlled means of tuning device output data. The rising edge of C is used as the output timing reference for first output data. The rising edge of C# is used as the output reference for second output data. C# is ideally 180 degrees out of phase with C.
CQ CQ#	Req	In	Req	Out	Echo clock outputs for LA-1B interface. The echo clocks are output copies of the output register clocks, C (or K) and C# (or K#). Echo clocks are designed to track changes in output driver delays due to variance in die temperature and supply voltage. The echo clocks are designed to transition with the rest of the data output drivers. CQ rising corresponds with the rising edge of C (or K). CQ falling corresponds with the rising edge of C# (or K#).
A [n:2]	Req	Out	Opt	In	Address pins. For burst of 2 devices, A[1:0] are accessible through BW# signals. For burst of 4 devices, A[2:0] are accessible through BW# signals. Slave devices may implement zero or more address inputs. For host devices, $23 \le n \le 29$ where n is the number of address inputs.
E [1:0]	Req	Out	Opt	In	Port enable. For host devices, functionally equivalent to address outputs. Slave devices shall implement both or none. Enable inputs are sampled at the same times as address inputs.
EP[1:0]	N/A	N/A	Opt	In	Port Enable programming inputs. EP pins determine the sense of the corresponding E pins (e.g., EP1 tied high results in E1 being active high). Required if port enable pins are implemented.
R#	Req	Out	Req	In	Active-low read select input. When low, this input causes the address input to be registered and a read cycle to be initiated.
W#	Req	Out	Req	In	Active-low write select input. When low, this input causes the address input to be registered and a write cycle to be initiated.
BW# [0:1]	Req	Out	Opt	In	Active-low byte-write inputs. When low, these inputs cause their respective bytes to be registered and written if W# had initiated a write cycle. BW0# controls D [0:7] and DP [0], while BW1# controls D [8:15] and DP [1].
D [0:15]	Req	Out	Req	In	Synchronous data inputs. This bus operates in response to W# commands
DP [0:1]	Req	Out	Req	In	Synchronous even parity inputs. Shall be stored and checked by the slave and retrieved and generated by the host. Correct when Exclusive-OR of D [7:0] = DP [0], and Exclusive-OR of D [15:8] = DP [1]. The ability to send correct parity is mandatory. Error handling of incorrect parity is beyond the scope of this document.
Q [0:15]	Req	In	Req	Out	Synchronous data outputs. This bus operates in response to R# commands.
QP [0:1]	Req	In	Req	Out	Synchronous even parity outputs. Shall be stored and checked by the host and retrieved and generated by the slave. Correct when Exclusive-OR of Q [7:0] = QP [0], and Exclusive-OR of Q [15:8] = QP [1]. The ability to send correct parity is mandatory. Error handling of incorrect parity is beyond the scope of this document.
V_{REF}	Req	In	Req	In	Input reference voltage. This input provides a reference voltage for the input buffer trip point.

Notes:
1. Std (Standard) column entries: Req = Required, Opt = Optional, N/A = Not applicable
2. I/O (Signal direction) column entries: In = Input, Out = Output

6. Port Operation Overview

The LA-1B interface ports follow a few simple rules:

- Control inputs are always captured on the rising edge of K clock.
- Address and data are captured on the rising edges of K and K# clocks.
- Read or Write data transfers in progress may not be interrupted and restarted.

6.1. Data Alignment and Organization

Table 3: Control and Data Pin Assignments for 32-Bit Write Data Alignment

Byte Enable	**BW 1#**	**BW 0#**
Data Input pins	**D [15:8]**	**D[7:0]**
Parity Input pins	**DP 1**	**DP 0**
K ↑	Byte 0 Bits [31:24] Parity Bit 0	Byte 1 Bits [23:16] Parity Bit 1
K# ↑	Byte 2 Bits [15:8] Parity Bit 2	Byte 3 Bits [7:0] Parity Bit 3

Table 4: Data Output Pin Assignments for 32-Bit Read Data Alignment

Data Output pins	**Q [15:8]**	**Q [7:0]**
Parity Output pins	**QP 1**	**QP 0**
K ↑	Byte 0 Bits [31:24] Parity Bit 0	Byte 1 Bits [23:16] Parity Bit 1
K# ↑	Byte 2 Bits [15:8] Parity Bit 2	Byte 3 Bits [7:0] Parity Bit 3

Table 5: Control and Data Pin Assignments for 64-Bit Write Data Alignment

Byte Enable	BW 1#	BW 0#
Data Input pins	D [15:8]	D[7:0]
Parity Input pins	DP 1	DP 0
K ↑	Byte 0 Bits [63:54] Parity Bit 0	Byte 1 Bits [53:48] Parity Bit 1
K# ↑	Byte 2 Bits [47:40] Parity Bit 2	Byte 3 Bits [39:32] Parity Bit 3
K ↑	Byte 4 Bits [31:24] Parity Bit 4	Byte 5 Bits [23:16] Parity Bit 5
K# ↑	Byte 6 Bits [15:8] Parity Bit 6	Byte 7 Bits [7:0] Parity Bit 7

Table 6: Data Output Pin Assignments for 64-Bit Read Data Alignment

Data Output pins	Q [15:8]	Q [7:0]
Parity Output pins	QP 1	QP 0
K ↑	Byte 0 Bits [63:54] Parity Bit 0	Byte 1 Bits [53:48] Parity Bit 1
K# ↑	Byte 2 Bits [47:40] Parity Bit 2	Byte 3 Bits [39:32] Parity Bit 3
K ↑	Byte 4 Bits [31:24] Parity Bit 4	Byte 5 Bits [23:16] Parity Bit 5
K# ↑	Byte 6 Bits [15:8] Parity Bit 6	Byte 7 Bits [7:0] Parity Bit 7

6.2. Output Register Control (Slave Device Feature)

LA-1B ports offer two mechanisms for controlling the output data registers. Typically control is handled by the output register clock inputs C and C#. The output register clock inputs can be used to make small phase adjustments in the clocking of the output registers by allowing the user to delay driving data out as much as a few nanoseconds beyond the next rising edges of the K and K# clocks. If the C and C# clock inputs are tied high (or not supported), the device reverts to K and K# control of the outputs, allowing operation as a conventional pipelined read device.

6.3. Echo Clocks

LA-1B ports feature echo clocks, CQ and CQ#, that track the performance of the output drivers. The echo clocks are delayed copies of the output register clocks, C and C# (or K and K# if C and C# are not supported). Echo clocks are designed to track changes in output driver delays due to variance in die temperature and supply voltage. The echo clocks are designed to transition with the rest of the data output drivers. Echo clock output CQ rising tracks C (or K) rising and CQ falling tracks C# (or K#) rising. Similarly CQ# rising tracks C# (or K#) rising and CQ# falling tracks C (or K) rising.

Echo Clocks are always active even if either or both of the read and/or write ports are deselected.

7. Port Specifications

This section describes the read and write operations for LA-1B. For detailed timing diagrams please refer to Figure 3 and Figure 4.

7.1. Write Operations

A write cycle is initiated by asserting W# low at the rising edge of K. The address for the write cycle is provided at the following rising edge of K#. In the same cycle, data is sampled at the rising edge of K and K#. See Figure 3 and Figure 4 for details.

Latency bounds between a write and a read to the same address are out of scope of this implementation agreement.

Table 7: LA-1B Port Write Truth Table

Control inputs		Input next state	D	D
K ↑ (t_n)	K# ↑ (t_n)		K(t_n)	K#(t_n)
W#	E			
X	F	Deselect	X	X
1	T	Deselect	X	X
0	T	Write	D0	D1

Notes:
1. X = Don't Care, H = High, L = Low, F = False, t_n = transition.
2. E = T (True) if E1 and E0 are evaluated true on the rising edge of K#.
3. W# is evaluated on the rising edge of K.
4. D0 and D1 are the first and second data input transfers in a write.
5. Values maybe influenced by BW# signals (refer section 7.3)

7.2. Read Operations

A read cycle is initiated by asserting R# low at the rising edge of K while the read address is present on A. Data is delivered after the next rising edge of K using C and C# as the output timing references. See Figure 3 and Figure 4 for details.

Table 8: LA-1B Port Read Truth Table

Control inputs		Output next state	Q	Q
K ↑ (t_n)		(t_n)	C#(t_{n+1})	C($t_{n+1½}$)
R#	E			
X	F	Deselect	Hi-Z	Hi-Z
1	T	Deselect	Hi-Z	Hi-Z
0	T	Read	Q0	Q1

Notes:
1. X = Don't care, 1 = High, 0 = Low, F = False, t_n = transition.
2. E = T (true) if E1 and E0 are evaluated true on the rising edge of K.
3. R# is evaluated on the rising edge of K.
4. Q0 and Q1 are the first and second data output transfers in a read.

7.3. Byte Write Control

Each write command and associated write address provide the base address for the following write operation. For devices operating in burst of 2 mode, the write operation consists of a 2-beat data transfer where 32-bits of data and 4-bits of even byte parity are written. For devices operating in burst of 4 mode, the write operation consists of a 4-beat data transfer where 64-bits of data and 8-bits of even byte parity are written. If the device supports byte granularity, then the following table is implemented.

Table 9: LA-1B Port Byte Write Truth Table[1]

Operation	K	K#	BW1#	BW0#
Write D [15:0], DP [1:0] at K rising edge	L→H		0	0
Write D [15:0], DP [1:0] at K# rising edge		L→H	0	0
Write D [15:8], DP [1] at K rising edge	L→H		0	1
Write D [15:8], DP [1] at K# rising edge		L→H	0	1
Write D [7:0], DP [0] at K rising edge	L→H		1	0
Write D [7:0], DP [0] at K# rising edge		L→H	1	0
Write nothing at K rising edge	L→H		1	1
Write nothing at K# rising edge		L→H	1	1

Note:
1. Assumes a write cycle was initiated by W# sampled low. BW0# and BW1# are sampled at data in times and can be altered for any portion of the burst write operation provided that input setup and hold requirements are satisfied.

Table 10: Example Write Sequence Using Byte Write Enables

Data In Sample Time	BW1#	BW0#	D [15:8], DP [1]	D [7:0], DP [0]
K ↑	0	1	Data in	Don't care
K# ↑	1	0	Don't care	Data in

Table 11: Resulting Write Operation

Byte 0 D [15:8], DP [1]	Byte 1 D [7:0], DP [0]	Byte 2 D [15:8], DP [1]	Byte 3 D [7:0], DP [0]
Written	Unchanged	Unchanged	Written

7.4. AC Electrical Characteristics

Table 12: LA-1B Slave Port A.C. Electrical Characteristics
Note 11

Description	Symbol	500 MHz		400 MHz		333 MHz		300 MHz		250 MHz		Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Clock Parameters												
Average clock cycle time (K, K#, C, C#) [ns]	KHKH	2.00	2.625	2.50	3.15	3.00	3.465	3.30	4.20	4.00	5.25	
Clock Phase Jitter (K, K#, C, C#) [ns]	KC var		0.15		0.15		0.15		0.15		0.20	4
Clock HIGH time (K, K#, C, C#) [ns]	KHKL	0.80		1.00		1.20		1.32		1.60		7
Clock LOW time (K, K#, C, C#) [ns]	KLKH	0.80		1.00		1.20		1.32		1.60		7
Clock to clock# (K .K#., C .C#.) at KHKH minimum [ns]	KHK#H	0.90		1.125		1.35		1.485		1.80		8
Clock# to clock (K#, K, C#..C) at KHKH minimum [ns]	K#HKH	0.90		1.125		1.35		1.485		1.80		8
Clock to data clock (K, C, K#..C#.) [ns]	KHCH	0.00	0.65	0.00	0.80	0.00	1.00	0.00	1.10	0.00	1.80	9
DLL lock time (K, C) [cycles] (If Enabled)	KC lock	4096		4096		4096		4096		4096		
Output Times												
C, C# HIGH to output valid [ns]	CHQV		0.35		0.35		0.45		0.45		0.45	10
C, C# HIGH to output hold [ns]	CHQX	-0.35		-0.35		-0.45		-0.45		-0.45		10
C HIGH to output High-Z [ns]	CHQZ		0.35		0.35		0.45		0.45		0.45	1, 10
C HIGH to output Low-Z [ns]	CHQX1	-0.35		-0.35		-0.45		-0.45		-0.45		1, 10
CQ, CQ# HIGH to output valid [ns]	CQHQV		0.20		0.20		0.25		0.30		0.35	5
CQ, CQ# HIGH to output hold [ns]	CQHQX	-0.20		-0.20		-0.25		-0.30		-0.35		5
C, C# HIGH to echo clock valid [ns]	CHCQV		0.35		0.35		0.45		0.45		0.45	10
C, C# HIGH to echo clock hold [ns]	CHCQX	-0.35		-0.35		-0.45		-0.45		-0.45		10
Setup Times												
Address valid to K rising edge [ns] **Burst of 2**	AVKH	0.20		0.25		0.30		0.33		0.40		2
Address valid to K rising edge [ns] **Burst of 4**	AVKH	0.25		0.3125		0.375		0.4125		050		
Control inputs valid to K rising edge [ns]	IVKH	0.20		0.25		0.30		0.33		0.40		2, 3
Data-in valid to K, K# rising edge [ns]	DVKH	0.20		0.25		0.30		0.33		0.40		2
Hold Times												
K rising edge to address hold [ns] **Burst of 2**	KHAX	0.20		0.25		0.30		0.33		0.40		2
K rising edge to address hold [ns] **Burst of 4**	KHAX	0.25		0.3125		0.375		0.4125		0.50		
K rising edge to control inputs hold [ns]	KHIX	0.20		0.25		0.30		0.33		0.40		2
K, K# rising edge to data-in hold [ns]	KHDX	0.20		0.25		0.30		0.33		0.40		2

Notes:
1. This parameter is sampled, but not production tested.
2. This is a synchronous device. All addresses, data and control lines must meet the specified setup and hold times for all latching clock edges.
3. Control input signals may not be operated with pulse widths less than KHKL (Min).
4. Clock phase jitter is the variance from clock rising edge to the next expected rising edge of the same clock signal.

5. Echo clock is very tightly controlled to data valid/data hold. By design, there is a ±0.1ns variation from echo clock to data.
6. Min value KHKL or KLKH = 40% of min KHKH regardless of frequency
7. Min value KHK#H or K#HKH = 45% of min KHKH regardless of frequency
8. This parameter is only applicable if C, C# is supported
9. If C, C# is not used then this parameter applies to K, K# clock inputs.
10. These values are applicable for DLL/PLL enabled mode.
11. LA-1B compliant products must support one or more of these speed bin specifications.

7.5. LA-1B Timing Diagrams

Figure 3: LA-1B Read and Write Timing Diagrams for Burst of 2 Mode

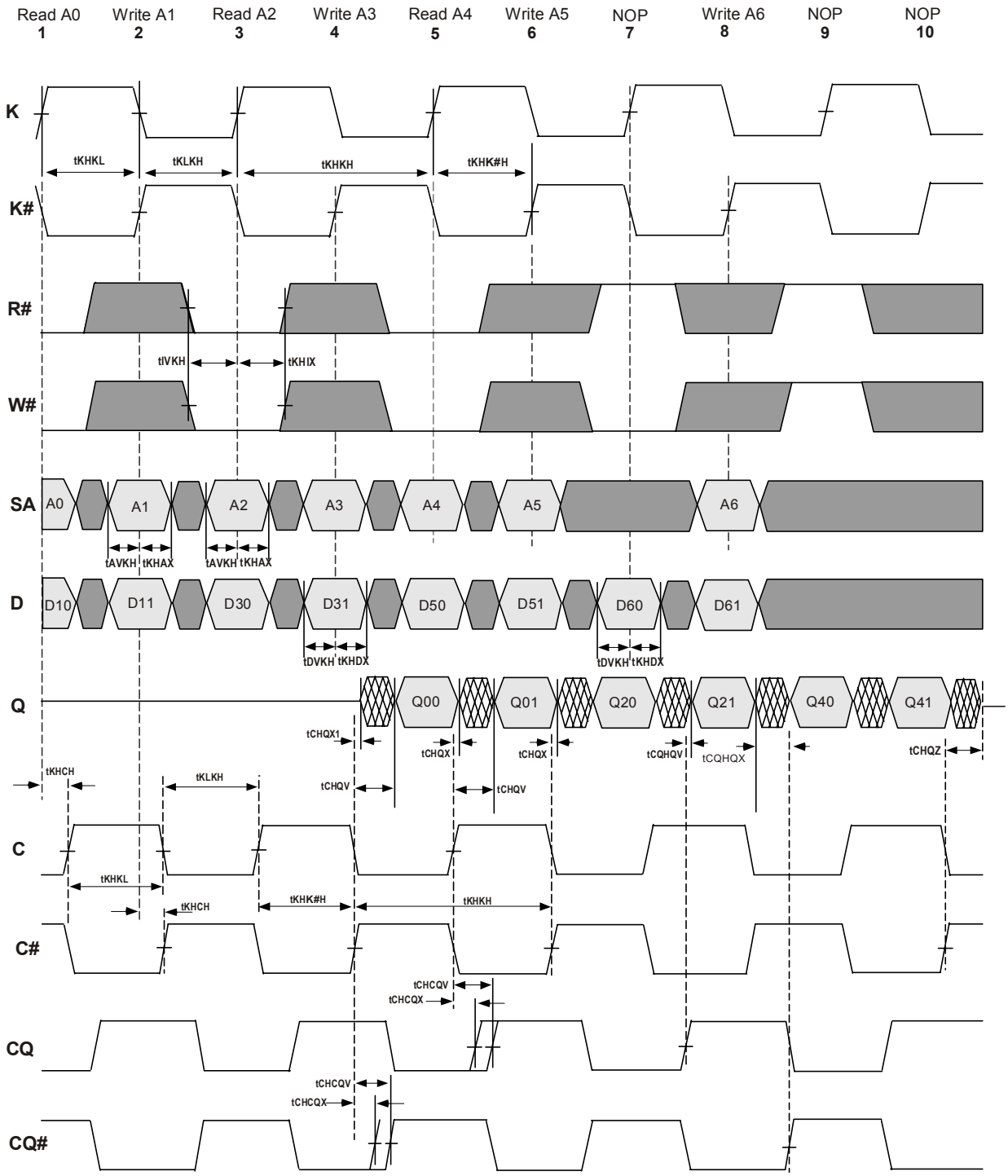
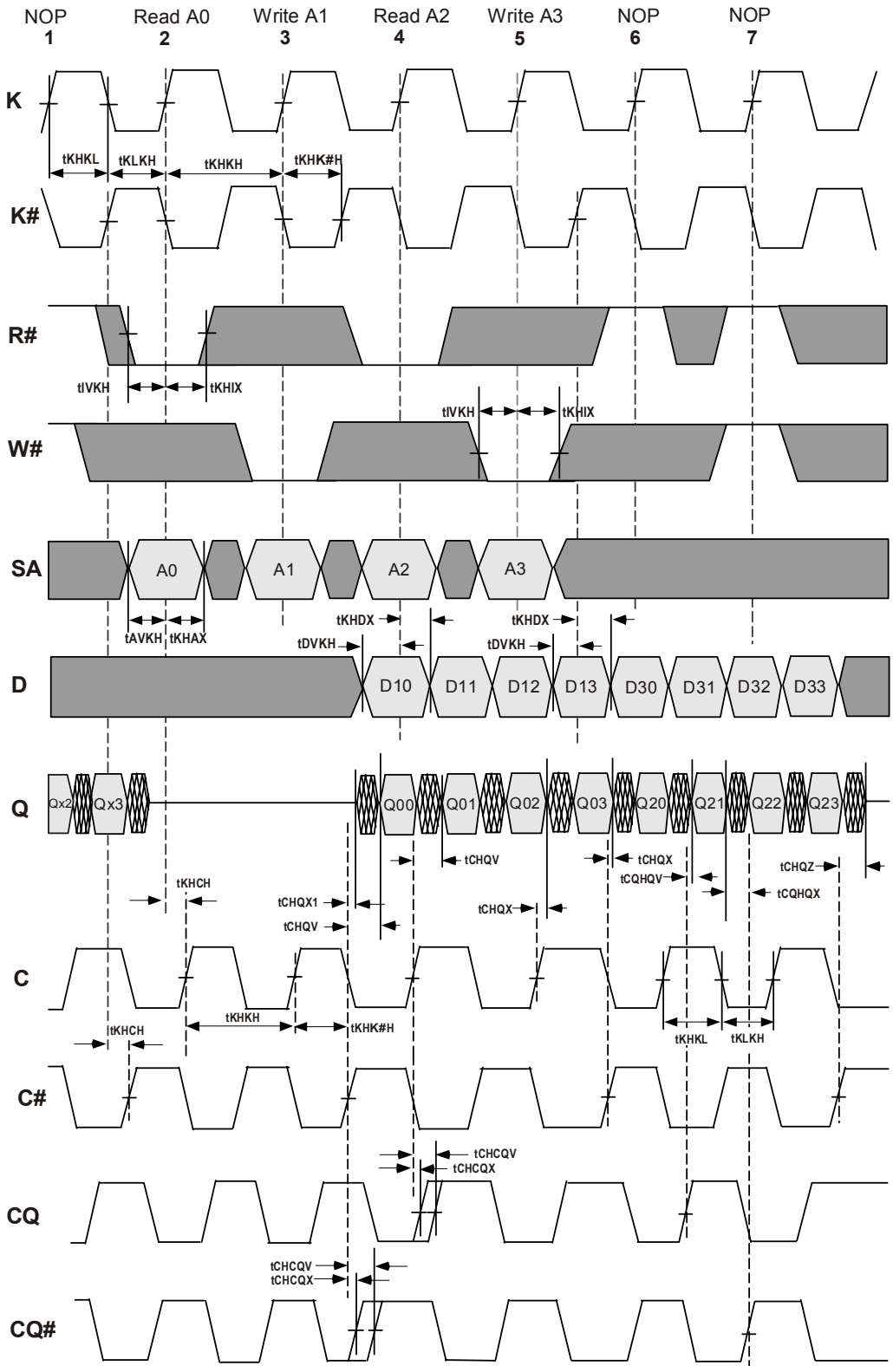


Figure 4: LA-1B Read and Write Timing Diagrams for Burst of 4 Mode

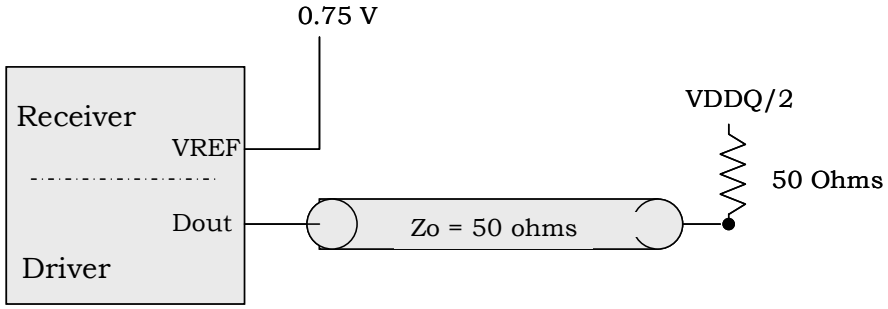


7.6. AC Test Conditions

Note:
- The following is only applicable to the 1.5V interface (JESD8-6) option.
- 1.2V interface parameters are defined in the JESD8-16 standard.

Figure 5: 1.5V Output Load Equivalent

Input Pulse Level	0.25V to 1.25V
Input Rise/Fall Times	0.3ns
Input Timing Reference Levels	0.75V
Output Timing Reference Levels	(VDDQ/2)



7.7. DC Electrical Characteristics

Note:
- The following is only applicable to the 1.5V interface (JESD8-6) option.
- 1.2V interface parameters are defined in the JESD8-16 standard.

Table 13: DC Electrical Characteristics

Symbol	Description	Min.	Max.	Units
V_{IH}	Input high (logic 1) voltage	V_{REF} + 0.1	V_{DDQ} + 0.3	V
V_{IL}	Input low (logic 0) voltage	-0.3	V_{REF} - 0.1	V
V_{OH}	Output high voltage	V_{DDQ} – 0.2	V_{DDQ}	V
V_{OL}	Output low voltage	V_{SS}	0.2	V
V_{DDQ}	Output buffer supply voltage	1.4	1.9	V
V_{REF}	Input reference voltage	0.68	0.95	V

8. Logical Interface

A network processing element (NPE) can use the LA-1B address bus to initiate co-processor actions by reading and writing to memory mapped registers.

Further definition of the LA-1B logical interface is beyond the scope of this implementation agreement.

Appendix A: Informative Annexes

Annex 1: LA-1B Port Depth Expansion

Note the configurations shown in this section may not be supported by all slave devices.

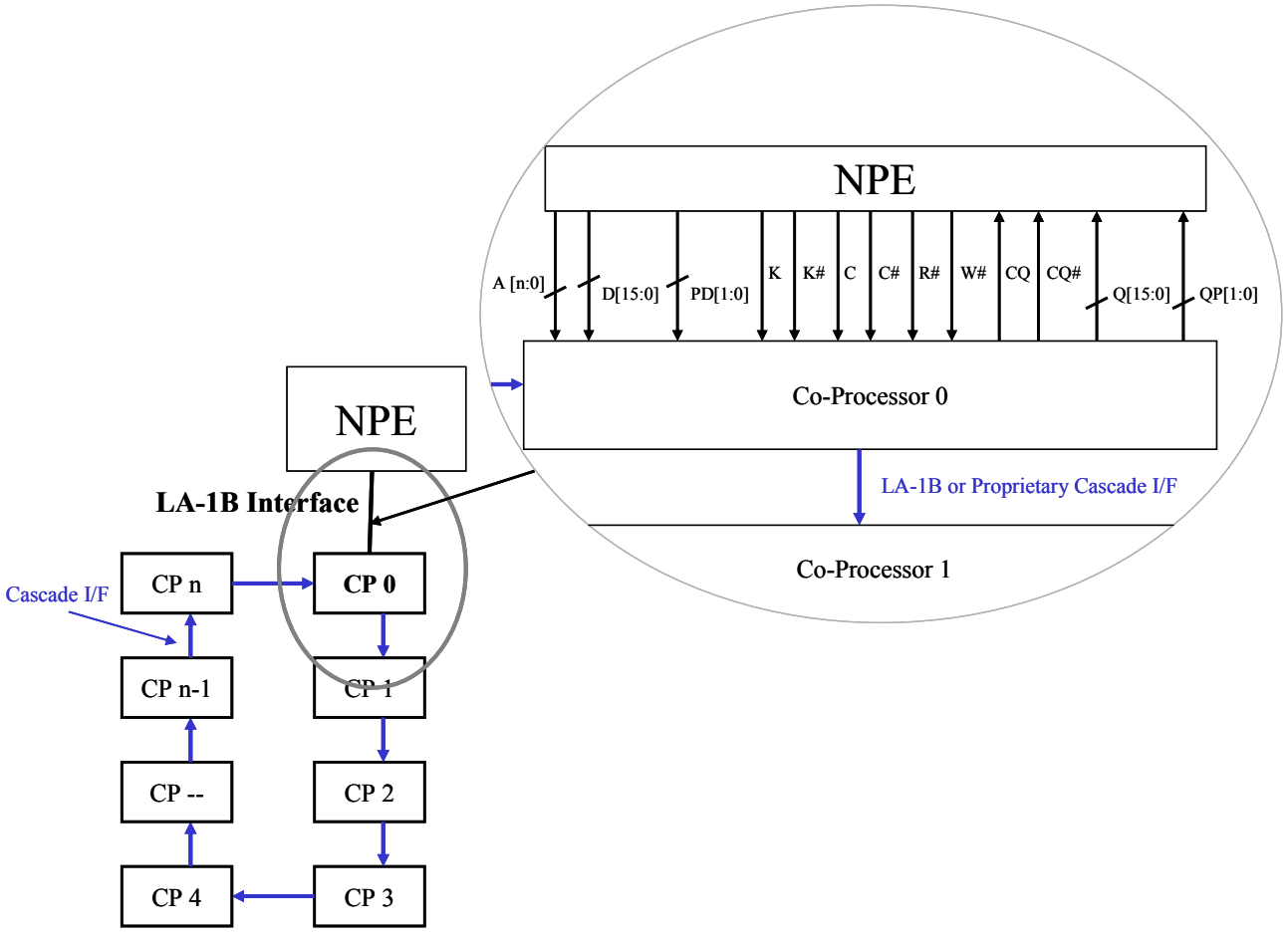
LA-1B Interface allows:

- Point to point cascade schemes (recommended for higher frequency operation)
- Multi-drop cascade schemes

A1.1 Point-to-point cascade configuration

Point-to-point cascade configuration is recommended for higher frequency operations (300 MHz and higher). In this mode the slave device appears as a single load on the host LA-1B interface. Additional devices maybe cascaded as shown in Figure 6 for depth expansion.

Figure 6: Point-to-point cascade configuration



A1.2 Multi-drop cascade configurations

Note the configurations shown in this section are logical suggestions and may not be suitable for higher frequency operations.

Multi-Drop cascade advantages:

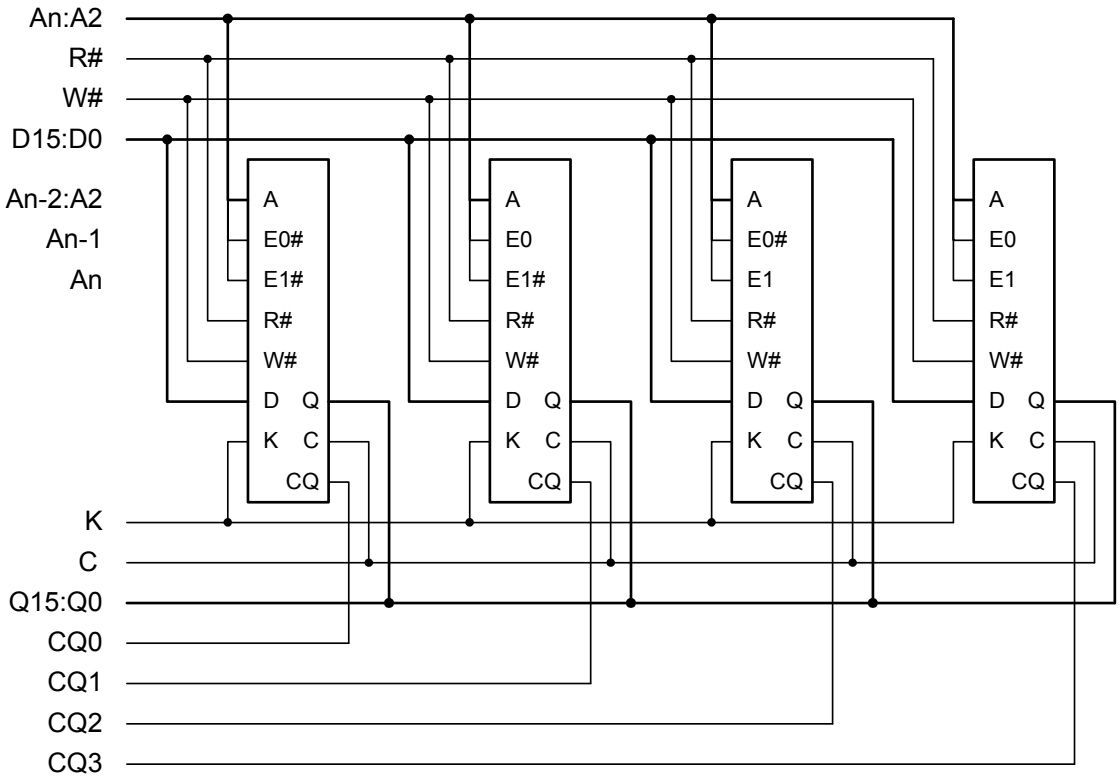
- In addition to depth expansion these configurations allow different type of devices to be connected to the same LA-1B bus at the same time.
- Less pins/complexity for the slave devices

A1.2.1 Depth Expansion with Programmable Port Enable Inputs

LA-1B ports may implement chip enable inputs, E0 and E1. The sense of these inputs, whether they function as active low or active high inputs, may be determined by the state of the programming inputs, EP0 and EP1. For example, if EP1 is held at V_{DD}, E1 functions as an active high enable. If EP1 is held to V_{SS}, E1 functions as an active low chip enable input.

Programmability of the two enable inputs (E1 and E2) allows four banks of depth expansion to be accomplished with no additional logic. By programming the enable inputs of four LA-1B ports in binary sequence (00, 01, 10, 11) and driving the enable inputs with two address outputs, four LA-1B ports can be made to look like one port with a larger address space to the system.

Figure 7: Depth Expansion with Programmable Port Enable Inputs



Note: For simplicity BW# , K# , C# and CQ# are not shown.

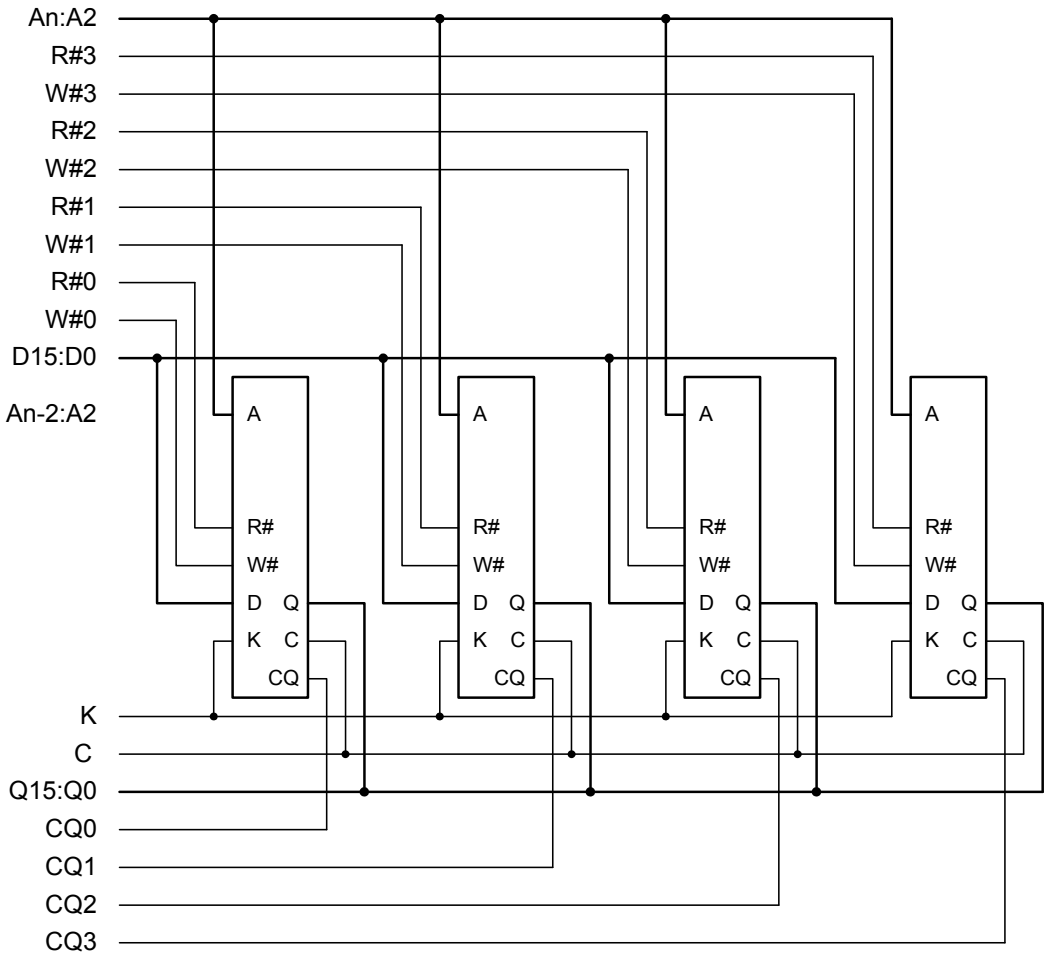
Table 14: Bank Enable Truth Table

	EP1	EP0	E0	E1
Bank 0	VSS	VSS	Active low	Active low
Bank 1	VSS	VDD	Active low	Active high
Bank 2	VDD	VSS	Active high	Active low
Bank 3	VDD	VDD	Active high	Active high

A1.2.2 Depth Expansion without Enable Inputs

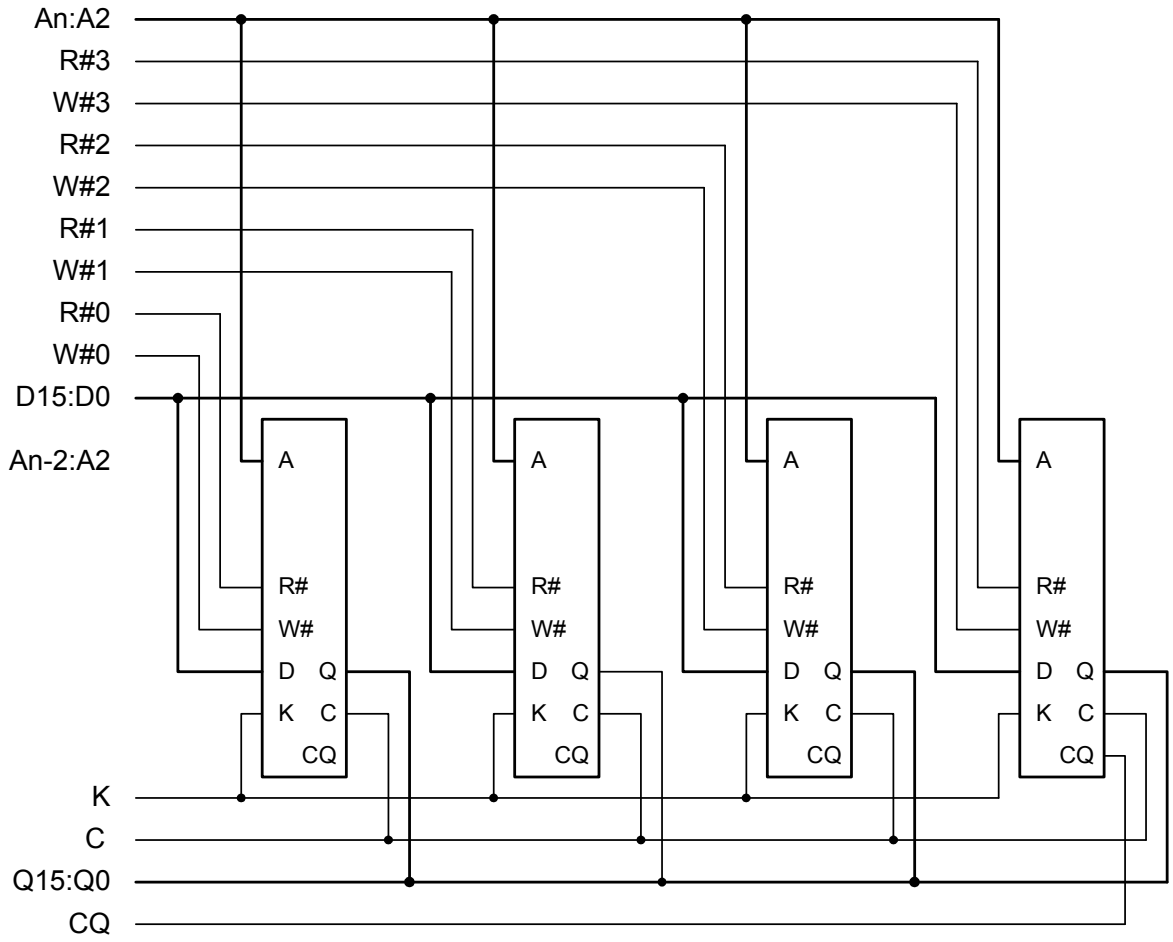
Alternately, LA-1B Ports may implement multiple read write pairs to depth expand as shown in Figure 8 and Figure 9.

Figure 8: Depth Expansion without Enable Inputs



Note: For simplicity BW# , K# , C# and CQ# are not shown.

Figure 9: Depth Expansion without Enable Inputs Using Only Last Echo Clock



Note: For simplicity BW# , K# , C# and CQ# are not shown.

Annex 2: Relationships Between Output Clocks (C, K, CQ) Referenced Timing

A2.1 Overview

The LA-1B implementation agreement provides for three different possible implementations for the data output control on slave devices.

- Using CQ, CQ# echo clock outputs (recommended)
- Using C and C# clocks
- Using K, K# clocks (if the C clocks are both tied high or not supported)

A2.2 C (or K) Clock Referenced Timing

The C and C# (or K, K#) clock referenced timing set is shown in ***italic*** in Figure 10. The specification ties the data output valid event at the beginning of a two-beat data transfer to the rising edge of the C (or K) clock. Data output hold time is referenced to the next rising edge of the C# (or K#) clock and the data valid of the second beat is referenced to the same C# (or K#) edge. Finally, the data output hold time of the second beat of the transfer is referenced to the next rising edge of the C (or K) clock.

A2.3 Echo clock (CQ) referenced timing

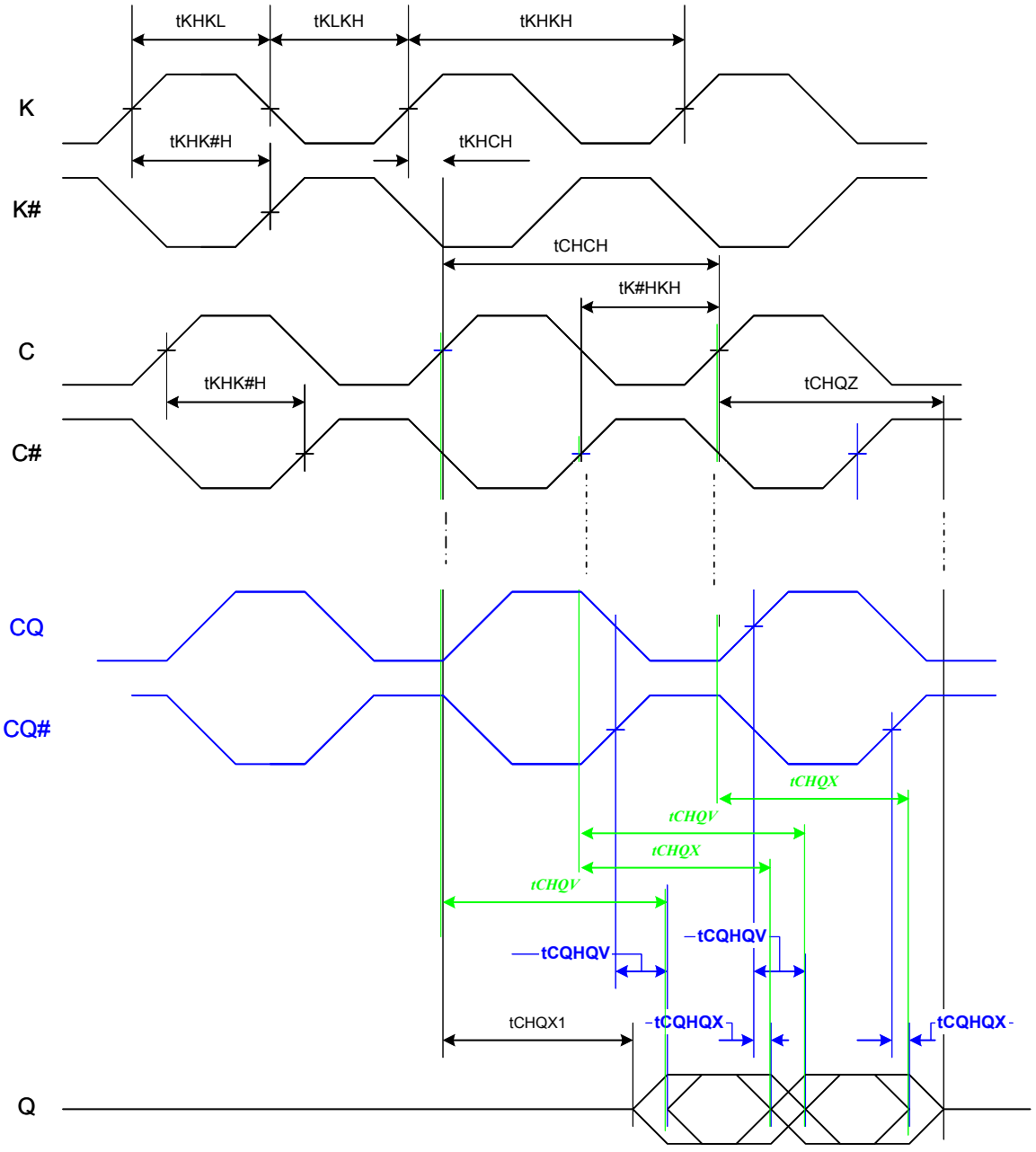
The CQ (and CQ#) clock referenced timing set is shown in **bold** in Figure 10. The LA-1B interface implementation agreement is written with enough latitude to allow output control implementations that utilize a DLL/PLL and implementations that do not utilize a DLL/PLL.

Echo clocks, CQ and CQ# track the performance of the output drivers and are delayed copies of the output register clocks, C and C# (or K and K# if C and C# are not supported). Echo clocks are designed to track changes in output driver delays due to variance in die temperature and supply voltage. The echo clocks are designed to transition with the rest of the data output drivers.

The LA-1B implementation agreement requires that a slave device produce CQ rising edge corresponding to C (or K) rising and CQ falling edge corresponding to C# (or K#) rising. Similarly CQ# rising edge corresponds to C# (or K#) rising and CQ# falling edge corresponds to C (or K) rising.

Echo Clocks are always active even if either or both of the read and/or write ports are deselected.

Figure 10: Output Timing Control Details



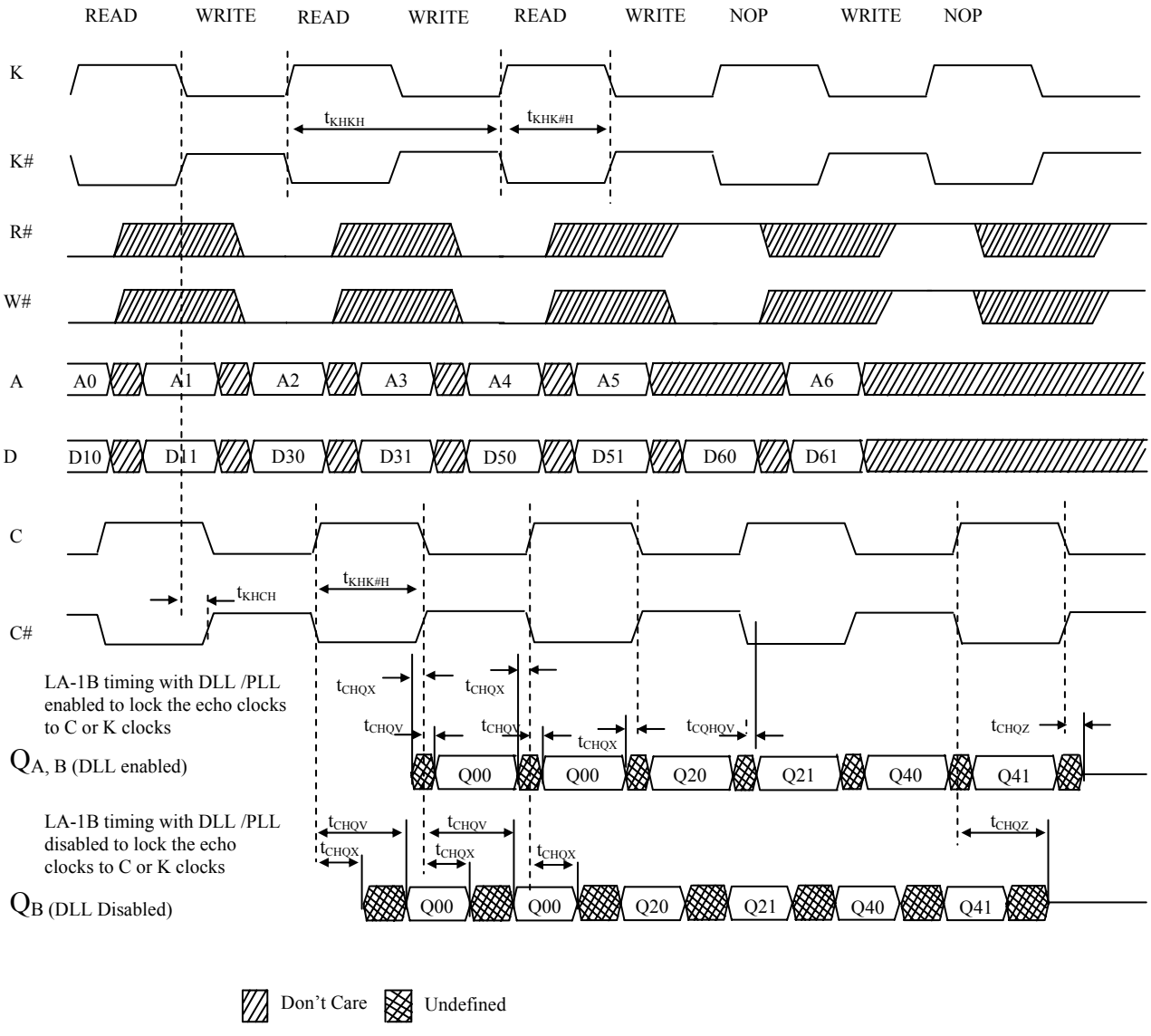
A3.4 Explanation of SRAM Modes

In defining the AC timings of the LA-1B Interface, the implementation agreement accommodates the following types of SRAM models:

A) An SRAM with DLL/PLL based echo clocks (for example QDR™-II)
B) An SRAM with DLL/PLL (enabled or disabled) based echo clocks (for example QDR™ – III)

When a DLL/PLL is used to lock the echo clocks to the input clocks C, C# or K, K#, the output data Q (for memory model type A and B (DLL/PLL enabled)) is tightly coupled to the input clocks. This may incur extra clock cycles of input clock to data output latency difference between the memory model A / B (DLL/PLL enabled) and memory models B (DLL/PLL disabled). Figure 11 illustrates this difference.

Figure 11: Timing Relationship Between Types A and B (DLL/PLL Enabled) Memory Model and Type B (DLL/PLL Disabled) Memory Models



QDR™ RAMs and Quad Data Rate™ RAMs comprise a new family of products developed by Cypress, IDT, NEC Electronics, Renesas Technology and Samsung.

Appendix B: Acknowledgements

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Enigma Semiconductor
Ericsson
Erlang Technologies
ETRI
EZChip
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