White Paper: Multi-Vendor Interoperability Testing of CFP2, CPAK and QSFP28 with CEI-28G-VSR and CEI-25G-LR Interface During ECOC 2013 Exhibition

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1. Executive Summary

The Optical Interworking Forum (OIF) is developing a set of Interoperability Agreements focused on new common electrical interfaces (CEI) applicable to higher speed optical systems requiring interconnect baud rates of 19.60 Gbaud to 28.10 Gbaud using NRZ coding. The OIF is also investigating the standardization and common understanding of thermal performance using a common set of definition metrics in the future. The OIF membership, consisting of semiconductor, connector, optical module suppliers, system suppliers, test equipment providers, allows a unique perspective for developing industry requirements, and a comprehensive understanding of the technology trade-offs necessary to enable the development and support for these requirements.

A multi-vendor interoperability event to demonstrate applications of CEI-28G-VSR, CEI-25G-LR interfaces and work supporting thermal characterization and standardization was successfully demonstrated during ECOC 2013 Exhibition by several members of the OIF Physical and Link Layer (PLL) Working Group. At this event, three optical module form factors, namely the Cisco CPAK, CFP2, and QSFP28, successfully demonstrated support for CEI-28G-VSR interfaces. This new demonstration at ECOC 2013 builds on the previous interoperability events that took place at the OFC 2012, OFC 2013, ECOC 2012 Exhibitions.

Also demonstrated were three interoperability demonstrations that support 25 Gb/s over backplane per CEI-25G-LR. These three demonstrations used back plane connector systems over various lengths of PCB material driven by a daughter card with common quad retimer to show industry support of the interface. These demonstrations were an extension of similar ones shown at ECOC 2012 and were subsequently documented in a previous white paper.

In addition for the first time publicly, OIF members also demonstrated some of the work in thermal modeling, in determining some of the key metrics that can potentially be used to support a future standard.

In all, the ECOC 2013 PLL interoperability builds on the previous interoperability events and consisted of nine individual demonstrations with 13 participating vendors. The nine demos were assembled as examples that the ecosystem for 100Gb/s electrical and optical interfaces is viable and interoperable from multiple sources. It also demonstrated industry cooperation to promote key issues and metrics for successful implementation of next generation communication systems and networks.

1.1 CEI-28G-VSR Interoperability Testing

The first four demonstrations exemplified the interoperability of pluggable optics, their electrical interfaces and connectors, retimers and gearbox IC's that performed error free over IEEE 802.3ba 100GBASE-LR4 optical links, supporting OTU4 data rates and 100GBASE-SR10 from a variety of manufacturers. The four demonstrations were:

- Demo 1: A Xilinx FPGA using a ChipScope Pro IBERT design driving CEI-28G-VSR to a host card with a Finisar CFP2 module with integrated Semtech retimer, plugged into it. At the far side of the link was Cisco CPAK 100GBASE-LR4 module. The modules were optically interoperating at OTU4 G959.1. The Cisco CPAK-100G-LR4 module was driving CEI-28G-VSR into an Inphi 100 GbE gearbox which was looping traffic back through the link. A TE Connectivity's CPAK connector and cage provide the electrical performance required for the CEI-28G-VSR channel while also delivering a mechanical and EMI solution for the Cisco CPAK pluggable module. A Tektronix DSA 8300 sampling scope with Tektronix 80E10 28Gb/s electrical data eye post S/W CTLE monitoring the eye from a Xilinx FPGA VSR channel.

- Demo 2: A MoSys breakout board with MoSys gearbox driving CEI-28G-VSR to a host card with a Finisar CFP2 100GBASE-LR4 module with integrated Semtech retimer, plugged into it. At the far side of the optical link was a Fujitsu CFP2 100GBASE-LR4 module with an integrated Semtech retimer, both operating at OTU4 G959.1. The Fujitsu CFP2 module was plugged into an Applied Micro Evaluation board with an Amphenol CFP2 host connector and was driving CEI-28G-VSR to the Applied Micro 100G Dual rate Gearbox which was looping the traffic back through the link.

- Demo 3: A MoSys breakout board with MoSys gearbox was driving a CEI-28G-VSR channel to a host card with Fujitsu CFP2 module with integrated Semtech re-timer, plugged into it and at the far side of the optical link was a Cisco CPAK-100G-LR4 module plugged into a TE Connectivity CPAK connector and cage operating at OTU4 G959.1 driving CEI-28G-VSR into MoSys breakout board with MoSys gearbox reversing the traffic back through the link.

- Demo 4: An Applied Micro Evaluation board with an Applied Micro 100G Dual rate Gearbox was driving a CEI-28G-VSR channel into a Finisar CFP2 SR10 module and on the far side of the optical link was a Cisco CPAK SR10 module plugged into TE Connectivity's CPAK connector and cage driving the CEI-28G-VSR channel into an Inphi 100 GbE gearbox which was generating a data pattern in the reverse direction of the link.

The fifth demonstration was an example that the infrastructure exists to support CEI-28G-VSR channel in other form factors and media. Gearbox IC's,

re-timers, host board connectors, and alike supporting zQSFP+ and Active Copper cables for short distance interconnects are interoperable between vendors.

- Demo 5: An Inphi 100G Gearbox was driving a CEI-28G-VSR channel through a TE Connectivity zQSFP+ host connector assembly to a TE Connectivity 2m QSFP28G Active Copper Cable assembly with integrated Semtech retimers integrated at either end driving CEI-28G-VSR through to a Molex zQSFP+ host connector assembly to an Applied Micro 100G Gearbox looping traffic back through the link. An Agilent DCA-X 86100D with the 86108B high bandwidth module was used to monitor the electrical eye on the VSR channel.

1.2 Thermal Modeling

For next generation systems, the density and data rate of interconnects will be some of the critical factors that will determine the success in the marketplace. As such, system designers will continue to push the limits of the technology to drive capacity and density higher. This, in turn, will also increase the density of components to the limits of thermal management. Thermal management can limit the performance and reliability of a component or subsystem and affect the overall integrity of the system itself. The intent of the OIF is to develop a document that will provide a degree of standardization and common understanding across the Networking Industry to enable optimized thermal performance using a common set of definitions in the future. The next demonstration highlights the effect of these factor's on thermal management.

Demo 6: Molex and TE Connectivity with a thermal emulator test vehicle, a line card thermal emulator test platform that consists of a simulated line card supporting 8 positions of the proposed CDFP 400Gb/s optical modules. Module heat dissipation and airflow were controlled and temperature was measured at various points to detect the effect of the surface roughness and heat sink material. Thermal efficiency was improved with smoother surfaces.

1.3 CEI-25G-LR Interoperability Testing

The OIF has been at the forefront of the industry with the development of common electrical interface (CEI) implementation agreements (IA) that support 25 Gb/s over backplane architectures (CEI-25G-LR). This development work is important in enabling the industry to re-use conventional chassis, line card, backplane and cabling architectures as they develop equipment that is able to meet the evolving and challenging bandwidth demands of the communications industry. The next 3 demonstrations are examples of continuing industry support of the standards by developing new

products. These standards were initially demonstrated at ECOC 2012 and were documented in an earlier white paper (Frlan 2012).

The demonstrations are:

- Demo 7: MoSys retimer evaluation board driving 4 lanes of CEI-25G-LR through an Amphenol supplied reference backplane channel consisting of two 7 inch daughter cards, a 12 inch long backplane, and two XcededPlus connectors terminated by a MoSys retimer operating at 25.78125 Gb/s error free with a PRBS 2^{-31} (BER<1e-15)

- Demo 8: MoSys retimer evaluation board driving 4 lanes of CEI-25G-LR through Molex Impel backplane connectors and a reference backplane and daughter cards from Molex with total lengths of 17, 21, 30 and 39 inches terminated by a MoSys retimer operating at 25.78125 Gb/s error free with a PRBS 2^{-31} (BER<1e-15)

- Demo 9: MoSys retimer evaluation board driving 4 lanes of CEI-25G-LR through TE Connectivity STRADA-Whisper backplane connectors, two 5 inch daughter cards and a 17 inch TE Connectivity backplane channel terminated by a MoSys retimer operating at 25.78125 Gb/s error free with a PRBS 2^{-31} (BER<1e-15)

2. OIF PLL Multi-Vendor Interoperability Testing Objectives

Interoperability is one of the keys to the success of any standard or implementation agreement. In order to promote the acceptance and demonstrate the viability of CEI-28G-VSR and CEI-25G-LR, the OIF sponsored a private, closed door interoperability Plugfest in August 2013. This Plugfest reiterated that CEI-28G-VSR and CEI-25G-LR are widely supported by an increasing number of companies across the industry with participants including five semiconductor manufacturers (Applied Micro, Inphi, MoSys, Semtech, and Xilinx), three connector vendors (Amphenol, Molex, TE Connectivity), three manufacturers of optical modules (Cisco Systems, Finisar and Fujitsu Optical Components) and two test equipment manufacturers (Agilent and Tektronix). Cooperation between semiconductor, connector, optical module, optical component and test equipment suppliers is crucial to enable implementation and integration of high-speed signaling by system and operator vendors. ECOC 2013 showcased working demonstrations of the CEI-28G-VSR electrical interface implemented on a Cisco CPAK 100GBASE-LR4, Cisco CPAK 100GBASE-SR10, CFP2 100GBASE-LR4 and CFP2 100GBASE-SR10 optical modules and a zQSFP28 Active Copper Cable and demonstrations that addressed the 19.90-25.80 Gbaud CEI-25G-LR interface for backplane applications, using test scenarios similar to the private interoperability tests.

2.1 CEI-28G-VSR, CEI-25G-LR Background Information and Applications

The communications and networking industries' data rates have been increasing along with the demands for higher levels of traffic aggregation. Additionally, the industry desires interoperable interfaces that support these next generation data rates. The OIF has been at the forefront of this demand, leading the industry with the development of CEI implementation agreements (IA) that support up to

- 28.10 GBd in chip-to-module electrical interface applications
- 25 GBd line card to line card “long reach” electrical interface applications
- Thermal interfaces in module to host applications

This development work is unique and timely in enabling the industry to re-use conventional chassis and line-cards as they develop equipment that is able to meet the evolving and challenging bandwidth demands of the communications industry. The CEI-28G-VSR Clause is in the final development phase. The implementation agreement is expected to be published by the end of 2013. The CEI-25G-LR Clause is ratified and available for industry use.

The use of pluggable optical transceivers and direct attach copper cables is a common practice in equipment developed for the communications market. Developing interoperable pluggable solutions that keeps up with the demanding

bandwidth needs of industry is critical to enabling next generation equipment that supports the communications service providers.

2.2 CEI-28G-VSR Specification Channel Requirement

The CEI-28G-VSR application reference diagram is shown in Figure 1. It consists of 100Ω differential PCB traces, vias, one connector and AC coupling capacitors. The CEI-28G-VSR IA is intended to be used for "Very Short Reach" channels, with length up to 150 mm, and loss up to 10.0 dB loss at Nyquist rate. The model that is being initially targeted for the next generation of optical modules is retimed interfaces operating at 25.78 – 28.10 GBd. The overall CEI-28G-VSR link needs to operate with a bit error ratio (BER) of 1e-15 or less. VSR interface supports multiple lanes and is hot pluggable.

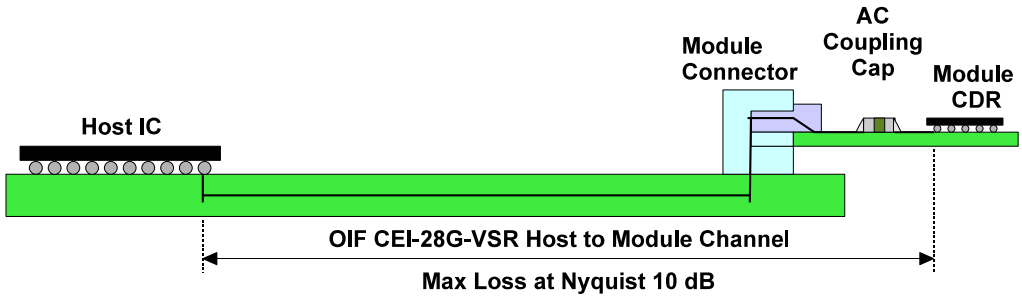

Figure 1: CEI-28-VSR Reference Model

A VSR link supports a maximum loss of 10 dB at Nyquist for operation from 19.60 to 28.10 GBd with NRZ modulation. The link loss budget is divided into a maximum host PCB loss of 7.3 dB, a connector loss of 1.2 dB and a module PCB loss of 1.5 dB, Figure 2 shows a diagram of the loss breakdown. TP1a and TP4a are respectively the host electrical output and input measurement points measured with Host Compliance Board (HCB) with PCB loss of 2.0 dB. TP1 and TP4 are respectively the module electrical input and output measurement points measured with module compliance board (MCB) with PCB loss of 1.25 dB.

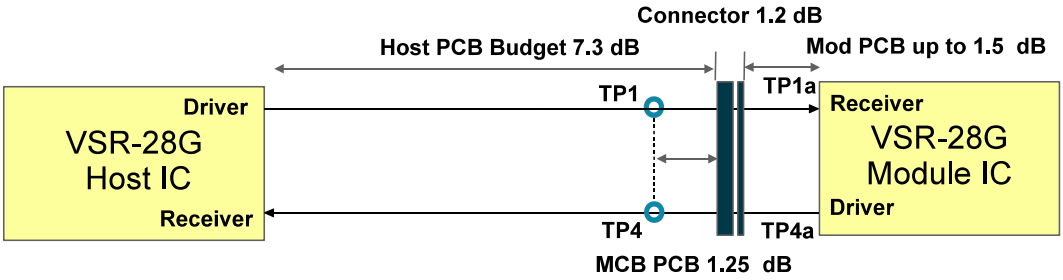

Figure 2: CEI-28G-VSR Reference Model

Figure 3, shows the CEI-28G-VSR channel response scaled for operation at 28 GBd with loss of 10 dB at Nyquist frequency of 14 GHz.

Figure 3: CEI-28G-VSR Channel Response

2.3 CEI-25G-LR Background Information and Applications

As the demands on industry data rates have increased along with the demands for higher levels of traffic aggregation, the communications and networking industries have need of interoperable interfaces that support these next generation data rates. The OIF has been at the forefront of this demand by leading the industry with the development of common electrical interface (CEI) implementation agreements (IA) that support 25 Gb/s over backplane architectures, 28 Gb/s in chip-to-chip applications and 28 Gb/s in

chip-to-module applications. This development work is important in enabling the industry to re-use conventional chassis, line card and cabling architectures as they develop equipment that is able to meet the evolving and challenging bandwidth demands of the communications industry.

CEI-25G-LR is a recent OIF Clause which address the needs of 25 Gb/s Long Reach backplane applications. The CEI-25G-LR Clause was recently ratified along with CEI-28G-SR as part of the Common Electrical I/O (CEI) 3.0 Implementation Agreement. The CEI-28G-VSR Clause is under development and is expected to be ratified later this year.

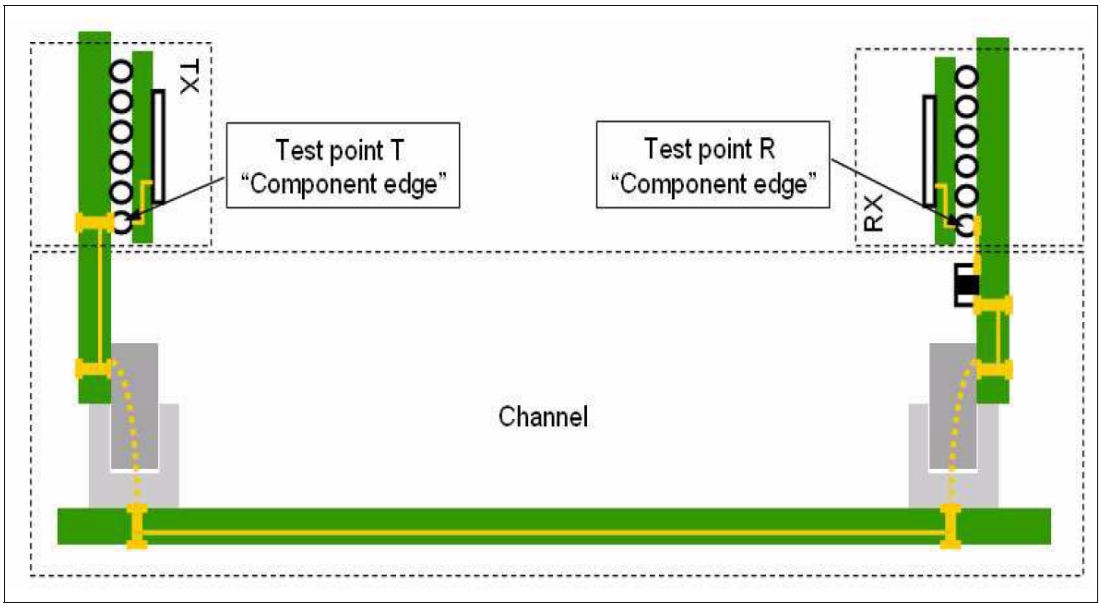

Figure 4: CEI-25G-LR Reference Model

As shown in Figure 4, backplane architectures are commonly used in communications equipment. Developing 25 Gb/s backplane channel specifications is important to enable the industry to continue use of this architecture in switches, routers, transport and data center equipment. The CEI-25G-LR channel consists of 100Ω differential PCB traces, vias and up to two connectors. As this IA is targeted to longer reach backplane applications total allowable channel loss can be up to 25 dB at Nyquist rate and the transmitter is able to generate a maximum swing of 1200 mVppd and is required to have an FIR equalizer. The receiver implementation is not mandated and can be vendor specific.

3 Demonstrations

3.1 Demo 1: CEI-28G-VSR CPAK / CFP2 100GBASE-LR4 Modules

Supported by: Cisco, Finisar, Inphi, Semtech, TE Connectivity, Tektronix, Xilinx

3.1.1 Component Overview

Cisco CPAK Module: The Cisco CPAK 100GBASE-LR4 module (CPAK-100G-LR4) is IEEE 802.3ba compliant and supports link lengths of up to 10 km over standard single-mode fiber (SMF, G.652). The module delivers an aggregate bandwidth of 100 gigabits per second, carried over four LAN wavelength-division multiplexing (WDM) wavelengths operating at a nominal 25 Gbps per lane. The module utilizes Cisco's advanced complementary metal-oxide semiconductor (CMOS) photonic technology to provide industry-leading optical integration, performance, low power consumption, and scalability. It is compatible with other 100GBASE-LR4 compliant modules such as CFP, to support high-bandwidth 100-Gb optical links over standard single-mode fiber terminated with SC connectors. Nominal power consumption is less than 5.5W

Finisar CFP2 Module: Finisar CFP2 100GBASE-LR4 modules use a quad 28G DFB DML PIC (Photonic Integrated Circuit) TOSA and quad 28G PIN PIC ROSA, with four 2x28G Semtech CDRs. This results in nominal 6 W total module power dissipation, and a significantly reduced cost structure compared to Gen1 28G EML TOSA technology.

Inphi Gearbox: The Inphi IN112510-LD is a single-chip, low-power tri-rate CMOS PHY for 10:4 gearbox/10:10 retimer applications in 10/40G/100G Ethernet and OTU4 line cards and optical modules. Optimized for low-latency operation, it delivers high system performance and ultra-low jitter for demanding applications. It is designed to significantly exceed CEI-28G-VSR requirements and allows real-time monitoring of link margin and protocol checking as well as dynamic high resolution eye scan diagnostics.

MoSys Gearbox: The MoSys LineSpeed™ 100G Multi-Mode Gearbox IC (MSH310) is a single-chip, low-power CMOS device designed to support 10:4 gearbox or 10:10 retiming applications for 10G, 40G and 100G Ethernet and OTU4 line cards and optical modules. The device features a strong self-adapting equalizer for extended reach on both the 10G and 25G lanes and supports standards ranging from CEI-28G-VSR to CEI-25G-LR. The device includes on-chip PRBS generation, error checking and diagnostic capabilities.

Semtech Retimers: Leveraging a generation of innovation in 10G module CDRs, Semtech's GN2425 and GN2426 are low-power retimers optimized for reference-free 25-28Gbps operation in next-generation optical modules and active cables.

By resetting the jitter budgets within the module in both directions, Semtech's CDRs are perfect for challenging new applications such as 100GBASE-LR4/ER4 and OTU4 CFP2 optical modules. The GN2425 and GN2426 feature best-in-class receive sensitivity, input jitter tolerance and output jitter, allowing for reliable signal recovery and clean, wide-open transmit eyes.

TE Connectivity Connectors: TE Connectivity's CPAK connector and cage provide the electrical performance required for the CEI-28G-VSR channel while also delivering a mechanical and EMI solution for the Cisco CPAK pluggable module. The connector uses conventional stamped and formed design techniques combined with shielding methods to deliver a 28Gb/s low noise solution. The same connector supports both 100G BASE-LR4 and 100G BASE-SR10 applications. The CPAK cage provides a riding heat sink design for thermal management and fully integrated EMI and mechanical support features. The connector and cage can be applied in both single sided and belly to belly 28Gb/s installations.

Xilinx FPGA: The Xilinx 7 Series HT family of FPGAs utilize heterogeneous stacked 3D IC device integrating both FPGA slices and high performance 25-28.05 GBd transceivers via a silicon interposer. The FPGA slices, implemented on a 28nm high-performance/low-power (HPL) process, contains 580,480 logic cells, 1,680 DSP slices, 33,840Kbits of block RAM (BRAM), 48x 13.1 GBd GTH transceivers and 8x 28.05 GBd GTZ transceivers. The GTZ transceivers are designed to exceed the OIF-28G-VSR electrical specification and are targeted specifically to interoperate with CFP2 optical modules and are arranged to directly connect to CFP2 connectors. For the demonstration, the device has been configured with a ChipScope Pro IBERT design where the device is simultaneously transmitting and receiving PRBS-31 and checking the received data for errors.

3.1.2 Demo 1 Description

This demonstration system consists of the following blocks: Xilinx FPGA, evaluation board with a CFP2 connector and cage system, a Finisar CFP2 100GBASE-LR4 module with integrated Semtech retimer IC, a Cisco CPAK 100GBASE-LR4 module with integrated retimer IC, and an Inphi 100G gearbox and evaluation board with a TE CPAK connector and cage. A PRBS31 data pattern is generated from the Xilinx FPGA across for lanes at 27.95 Gb/s per lane to meet OTN requirements. 100G Ethernet rates at 4x25.78 is also supported by the devices in this demonstration. The Xilinx FPGA is connected to the Semtech Retimer IC inside the Finisar CFP2 100GBASE-LR4 module via the CEI-28G-VSR interface across the evaluation board representing approximately 8dB of loss. The Tx and Rx inputs on the Xilinx FPGA and Semtech retimer are sufficient to ensure error free operation in both directions to the CEI-28G-VSR electrical requirement. The Finisar CFP2 100GBASE-LR4 optical module

transmits and receives the data to the Cisco CPAK 100GBASE-LR4 optical module over 10km of single mode fiber. The Cisco CPAK 100GBASE-LR4 module with its integrated retimer from is then connected electrically to an Inphi gearbox on the Cisco CPAK/Inphi evaluation board (Figure 6) with a CEI-28G-VSR channel connecting the retimer to gearbox. Similarly, PRBS 31 traffic is generated in the other direction from the Inphi gearbox following the return path of 10km of fiber between the Cisco CPAK 100GBASE-LR4 module and Finisar CFP2 LR4 modules and terminating at the Xilinx FPGA. Data integrity is monitored by the Xilinx FPGA and Inphi gearbox device to ensure error free operation and data integrity over extended time (>8 Hours) to conform to the IEEE and OIF standards. Figure 7 is a screen capture from the Xilinx ChipScope Pro IBERT indicating error free operation on channels 0 through 3 of the 100GBASE-LR4 link taken at the PlugFest. The combination of Cisco CPAK and CFP2 100GBASE-LR4 modules from Cisco and Finisar and electrical components from Xilinx, Inphi and Semtech, show extensive industry interoperability across both optical and electrical interfaces required to meet both Ethernet and OTN standards.

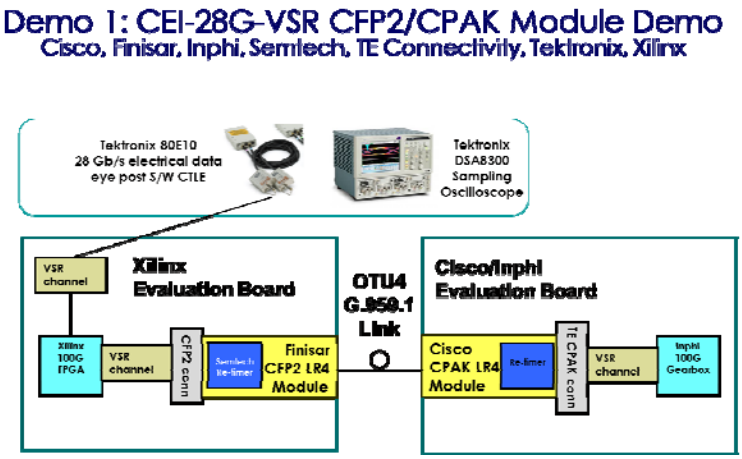

Figure 5: Demo 1 Block Diagram

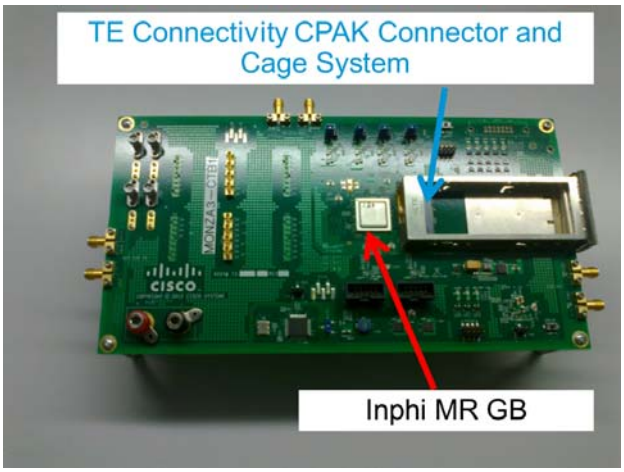

Figure 6: Cisco / Inphi Evaluation Board

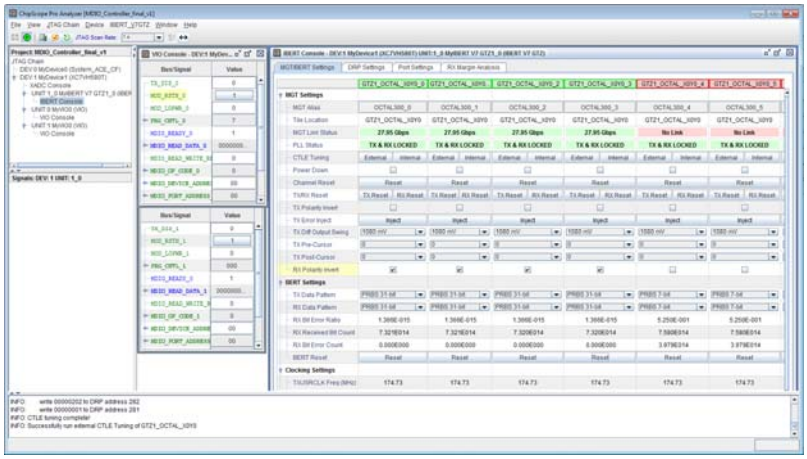

Figure 7: Screen Capture from Xilinx ChipScope Pro IBERT

3.2 Demo 2: CEI-28G-VSR CFP2 100GBASE-LR4 Modules

Supported by: Amphenol, Applied Micro, Finisar, Fujitsu, MoSys, Semtech

3.2.1 Component Overview

Amphenol CFP2 Connector: The Amphenol CFP2 connector designed for Optical Modules running at speeds greater then 10Gb/s up to 25Gb/s per lane. The module electrical interface has been generically specified to allow for supplier-specific customization around various “4 x 10 Gbit/s” interfaces, but can support up to 8 x 25 Gbit/s or 4 x 25 Gbit/s electrical interface configurations. The upcoming CFP4 will use the same technology but reduce the number of lanes to 4 x 28Gb/s lanes, giving more than twice density for 100Gb/s.

Applied Micro Gearbox IC: The S28110PRI Gearbox II from Applied Micro is a fully integrated bidirectional 10:4 mux/demux and 10:10 retimer for 100Gbps,

40Gbps and 10Gbps interconnect applications. It operates at both Ethernet and OTN rates while offering industry leading transmit jitter performance and receive sensitivity. It comes with a host of diagnostic features such as receiver eye monitors, PRBS mon/gen, and virtual lane identification. It is compliant with the OIF-28G-VSR and OIF-28G-SR specifications on the 28Gbps interface while carrying an industrial temperature rating.

Finisar CFP2 Module: Finisar CFP2 100GBASE-LR4 modules use a quad 28G DFB DML PIC (Photonic Integrated Circuit) TOSA and quad 28G PIN PIC ROSA, with four 2x28G Semtech CDRs. This results in nominal 6 W total module power dissipation, and a significantly reduced cost structure compared to Gen1 28G EML TOSA technology.

Fujitsu CFP2 Module: The FOC (Fujitsu Optical Components) CFP2 100GBASE-LR4 module operating at OTU4 data rates is IEEE 802.3ba and OTU4 G.959.1 compliant. The module realizes transmitter good eye performance and receiver high sensitivity utilizing 4ch 28G integrated TOSA and 4ch 28G integrated ROSA.

MoSys Gearbox: The MoSys LineSpeed™ 100G Multi-Mode Gearbox IC (MSH310) is a single-chip, low-power CMOS device designed to support 10:4 gearbox or 10:10 retiming applications for 10G, 40G and 100G Ethernet and OTU4 line cards and optical modules. The device features a strong self-adapting equalizer for extended reach on both the 10G and 25G lanes and supports standards ranging from CEI-28G-VSR to CEI-25G-LR. The device includes on-chip PRBS generation, error checking and diagnostic capabilities.

Semtech Retimers: Leveraging a generation of innovation in 10G module CDRs, Semtech's GN2425 and GN2426 are low-power retimers optimized for reference-free 25-28Gbps operation in next-generation optical modules and active cables. By resetting the jitter budgets within the module in both directions, Semtech’s CDRs are perfect for challenging new applications such as 100GBASE-LR4/ER4 and OTU4 CFP2 optical modules. The GN2425 and GN2426 feature best-in-class receive sensitivity, input jitter tolerance and output jitter, allowing for reliable signal recovery and clean, wide-open transmit eyes.

3.2.2 Test Equipment Overview

Test equipment supplied to the PLL Interop demonstration by Tektronix includes the following:

DSA8300 Sampling Oscilloscope: The DSA8300 Series is a modular oscilloscope system that allows for electrical and optical sampling modules. For the OIF Interop, Tektronix provides the 80E10B Electrical Module. When used with the DSA8300 Series, this new module provides sub-100 femtosecond intrinsic jitter, low vertical noise, >45GHz bandwidth performance to enable high

fidelity measurements of OIF 28G-VSR system.

3.2.3 Demo 2 description

This demonstration system consists of the following blocks: a MoSys gearbox, evaluation board and CFP2 breakout board, a Finisar CFP2 LR4 module with integrated Semtech retimer IC, a Fujitsu CFP2 LR4 module with integrated Semtech retimer IC, and an Applied Micro 100G gearbox and evaluation board with the Amphenol CFP2 connector. A PRBS31 data pattern is generated from the gearbox device across for lanes at 27.95 Gb/s per lane to meet OTN requirements. 100G Ethernet rates at 4x25.78 is also supported by the devices in this demonstration. The MoSys gearbox is connected to the Semtech Retimer IC inside the Finisar CFP2 LR4 module via an evaluation board and breakout board representing approximately 8dB of loss. The Tx and Rx inputs on the MoSys gearbox and Semtech retimer are sufficient to ensure error free operation in both directions to the CEI-28G-VSR electrical requirement. The Finisar CFP2 LR4 optical module transmits and receives the data to the Fujitsu CFP2 LR4 optical module over 10km of single mode fiber. The Fujitsu module with its integrated retimer from Semtech is then connected electrically through the Amphenol CFP2 connector to an Applied Micro gearbox through using an integrated breakout board with a CEI-28G-VSR channel connecting the retimer to gearbox. Similarly, PRBS 31 traffic is generated in the other direction from the Applied Micro gearbox following the return path of 10km of fiber between the Fujitsu CFP2 and Finisar CFP2 LR4 modules and terminating at the MoSys gearbox. Data integrity is monitored by both gearbox devices to ensure error free operation and data integrity over extended time (>8 Hours) to conform to the IEEE and OIF standards. The combination of CFP2 LR4 modules from Finisar and Fujitsu and electrical components from Applied Micro, MoSys and Semtech, show extensive industry interoperability across both optical and electrical interfaces required to meet both Ethernet and OTN standards.

Demo 2: CEI-28G-VSR CFP2 Module Demo
(Amphenol, Applied Micro, Finisar, Fujitsu, MoSys, Semtech)

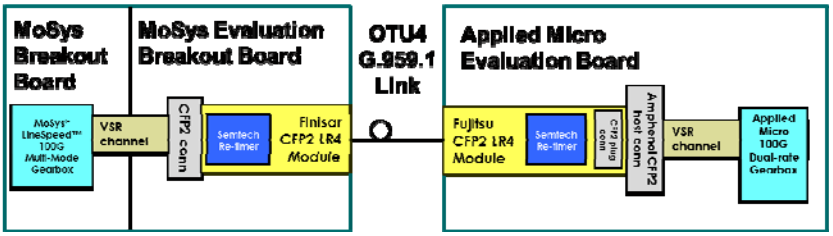

Figure 8: Demo 2 Block Diagram

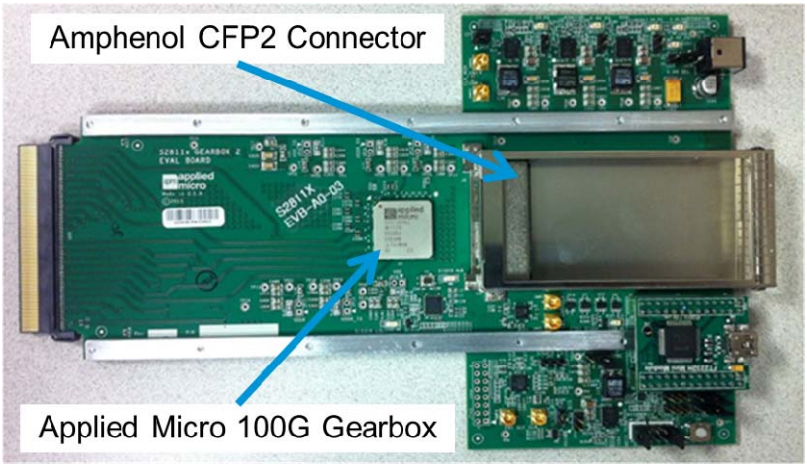

Figure 9: Applied Micro CFP2 Evaluation Board

3.3 Demo 3: CEI-28G-VSR CPAK / CFP2 100GBASE-LR4 Modules

Supported by: Cisco, Fujitsu, MoSys, Semtech, TE Connectivity

3.3.1 Component Overview

Cisco CPAK Module: The Cisco CPAK 100GBASE-LR4 module (CPAK-100G-LR4) is IEEE 802.3ba compliant and supports link lengths of up to 10 km over standard single-mode fiber (SMF, G.652). Currently in production, it delivers an aggregate bandwidth of 100 gigabits per second, carried over four LAN wavelength-division multiplexing (LAN-WDM) wavelengths operating at a nominal 25 Gbps per lane. The module utilizes Cisco's advanced complementary metal-oxide semiconductor (CMOS) photonic technology to provide industry-leading optical integration, performance, low power consumption, and scalability. It is compatible with other 100GBASE-LR4

compliant modules such as CFP, to support high-bandwidth 100-Gb optical links over standard single-mode fiber terminated with SC connectors. Nominal power consumption is less than 5.5W

Fujitsu CFP2 Module: The FOC (Fujitsu Optical Components) CFP2 100GBASE-LR4 module operating at OTU4 data rates is IEEE 802.3ba and OTU4 G.959.1 compliant. The module realizes transmitter good eye performance and receiver high sensitivity utilizing 4ch 28G integrated TOSA and 4ch 28G integrated ROSA.

MoSys Gearbox: The MoSys LineSpeed™ 100G Multi-Mode Gearbox IC (MSH310) is a single-chip, low-power CMOS device designed to support 10:4 gearbox or 10:10 retiming applications for 10G, 40G and 100G Ethernet and OTU4 line cards and optical modules. The device features a strong self-adapting equalizer for extended reach on both the 10G and 25G lanes and supports standards ranging from CEI-28G-VSR to CEI-25G-LR. The device includes on-chip PRBS generation, error checking and diagnostic capabilities.

Semtech Retimers: Leveraging a generation of innovation in 10G module CDRs, Semtech's GN2425 and GN2426 are low-power retimers optimized for reference-free 25-28Gbps operation in next-generation optical modules and active cables. By resetting the jitter budgets within the module in both directions, Semtech's CDRs are perfect for challenging new applications such as 100GBASE-LR4/ER4 and OTU4 CFP2 optical modules. The GN2425 and GN2426 feature best-in-class receive sensitivity, input jitter tolerance and output jitter, allowing for reliable signal recovery and clean, wide-open transmit eyes.

TE Connectivity: TE Connectivity's CPAK connector and cage provide the electrical performance required for the CEI-28G-VSR channel while also delivering a mechanical and EMI solution for the Cisco CPAK pluggable module. The connector uses conventional stamped and formed design techniques combined with shielding methods to deliver a 28Gb/s low noise solution. The same connector supports both 100GBASE-LR4 and 100GBASE-SR10 applications. The CPAK cage provides a riding heat sink design for thermal management and fully integrated EMI and mechanical support features. The connector and cage can be applied in both single sided and belly to belly 28Gb/s installations.

3.3.2 Demo 3 Description

This demonstration system consists of the following blocks: a MoSys gearbox, evaluation board and CFP2 breakout board, a Fujitsu CFP2 100GBASE-LR4 module with integrated Semtech retimer IC a Cisco CPAK 100GBASE-LR4 module with integrated retimer IC on a Cisco CPAK evaluation breakout board with a TE CPAK connector and cage, a MoSys gearbox, evaluation board. A

PRBS31 data pattern is generated from the gearbox device across for lanes at 27.95 Gb/s per lane to meet OTN requirements. 100G Ethernet rates at 4x25.78 is also supported by the devices in this demonstration. The MoSys gearbox is connected to the Semtech Retimer IC inside the Fujitsu CFP2 100GBASE-LR4 module via an evaluation board and breakout board representing approximately 8dB of loss. The Tx and Rx inputs on the MoSys gearbox and Semtech retimer are sufficient to ensure error free operation in both directions to the CEI-28G-VSR electrical requirement. The Fujitsu CFP2 100GBASE-LR4 optical module transmits and receives the data to the Cisco CPAK 100GBASE-LR4 optical module over 10km of single mode fiber. The Cisco CPAK module with its integrated retimer is then connected electrically to the MoSys gearbox through an integrated breakout board with a CEI-28G-VSR channel connecting the retimer to gearbox. Similarly, PRBS31 traffic is generated in the other direction by looping back from the MoSys gearbox following the return path of 10km of fiber between the Cisco CPAK module and Fujitsu CFP2 100GBASE-LR4 modules and terminating at the MoSys gearbox. The bit error rate is monitored by both gearbox devices. The link operated error free over an 8 hour period conforming to the IEEE and OIF standards. The combination of Cisco CPAK and CFP2 100GBASE-LR4 modules from Cisco and Fujitsu and electrical components from MoSys and Semtech, along with electrical connectors from TE Connectivity show extensive industry interoperability across both optical and electrical interfaces required to meet both Ethernet and OTN standards.

Demo 3: CEI-28G-VSR CFP2/CPAK Module Demo
(Applied Micro, Cisco, MoSys, Semtech, TE Connectivity)

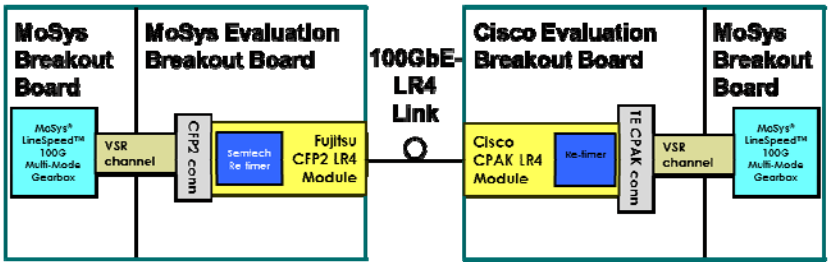

Figure 10: Demo 3 Block Diagram

3.4 Demo 4: CEI-28G-VSR CPAK / CFP2 100GBASE-SR10 Modules

Supported by Applied Micro, Cisco, Finisar, Inphi, TE Connectivity

3.4.1 Component Overview

Applied Micro Gearbox IC: Applied Micro Gearbox IC: The S28110PRI Gearbox II from Applied Micro is a fully integrated bidirectional 10:4 mux/demux and 10:10 retimer for 100Gbps, 40Gbps and 10Gbps interconnect applications. It operates at both Ethernet and OTN rates while offering industry leading transmit jitter performance and receive sensitivity. It comes with a host of diagnostic features such as receiver eye monitors, PRBS mon/gen, and virtual lane identification. It is compliant with the OIF-28G-VSR and OIF-28G-SR specifications on the 28Gbps interface while carrying an industrial temperature rating.

Cisco CPAK Module: The Cisco CPAK 100GBASE-SR10 module supports link lengths of 100m and 150m on laser-optimized OM3 and OM4 multifiber cables, respectively. The module delivers high-bandwidth 100-gigabit links over 24-fiber ribbon cable terminated with MPO/MTP connectors. It can also be used in 10 x 10-Gb mode along with ribbon-to-duplex-fiber breakout cables for connectivity to ten 10GBASE-SR optical interfaces.

Finisar CFP2 Module: Finisar CFP2 Module: Finisar CFP2 100GBASE-SR10 modules use a 10x10G VCSEL array, and a 10x10G PIN array, which results in 3 W total module power dissipation. These modules can also be used for breakout applications to connect to ten 10GBASE-SR optical modules in links up to 300 meters.

Inphi Gearbox: The Inphi IN112510-LD is a single-chip, low-power tri-rate CMOS PHY for 10:4 gearbox/10:10 retimer applications in 10/40G/100G Ethernet and OTU4 line cards and optical modules. Optimized for low-latency operation, it delivers high system performance and ultra-low jitter for demanding applications. It is designed to significantly exceed CEI-28G-VSR requirements and allows real-time monitoring of link margin and protocol checking as well as dynamic high resolution eye scan diagnostics.

TE Connectivity Connectors: TE Connectivity's CPAK connector and cage provide the electrical performance required for the CEI-28G-VSR channel while also delivering a mechanical and EMI solution for the Cisco CPAK pluggable module. The connector uses conventional stamped and formed design techniques combined with shielding methods to deliver a 28Gb/s low noise solution. The same connector supports both 100G BASE-LR4 and 100G BASE-SR10 applications. The CPAK cage provides a riding heat sink design for thermal management and fully integrated EMI and mechanical support features. The connector and cage can be applied in both single sided and belly to belly 28Gb/s installations.

3.4.2 Demo 4 Description

This demonstration system consists of the following blocks: An Applied Micro evaluation board with the Applied Micro 100G gearbox IC, a Finisar CFP2

100GBASE-SR10 module, a Cisco/Inphi evaluation board with a Cisco CPAK 100GBASE-SR10 module, an Inphi 100G gearbox IC and a TE Connectivity Cisco CPAK electrical connector and cage system. A PRBS31 data pattern was generated by the Applied Micro Gearbox IC and sent to the Finisar CFP2 100GBASE-SR10 module via a CEI-28G-VSR channel with CPPI signaling. The Finisar CFP2 100GBASE-SR10 module was connected to the Cisco CPAK 100GBASE-SR10 module with 100m of OM3 24-fiber ribbon cable. The Cisco CPAK 100GBASE-SR10 module sent the received data through the CEI-28G-VSR channel with CPPI signaling to the Inphi gearbox IC. For the return link, a PRBS31 data pattern was generated by the Inphi gearbox IC and sent, again to the Cisco CPAK 100GBASE-SR10 module via the CEI-28G-VSR channel with CPPI signaling. The Cisco CPAK 100GBASE-SR10 module transmitter was connected to the Finisar CFP2 100GBASE-SR10 receiver through the 100m 24 fiber OM3 ribbon cable. The Finisar CFP2 module sent the received data stream through the CEI-28G-VSR channel with CPPI signaling to the Applied Micro gearbox IC. Data streams in either direction of the link operated error free for 10^{15} bits.

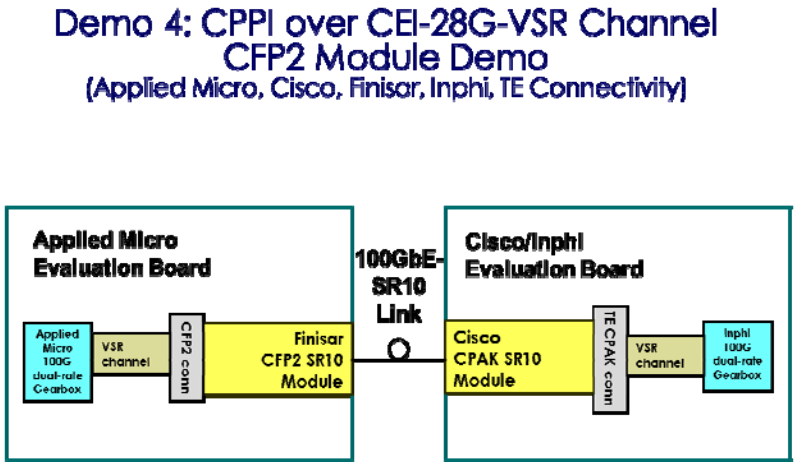

Figure 11: Demo 4 Block Diagram

3.5 Demo 5: CEI-28G-VSR QSFP28 Active Copper Cable Application

Supported by: Agilent, Applied Micro, Inphi, Molex, Semtech, TE Connectivity,

Participating companies in Demo 5 were Agilent providing a digital sampling oscilloscope, Applied Micro providing a 100G Gearbox, Inphi also providing a 100G Gearbox, Molex providing a zQSFP+ host connector assembly, Semtech providing a Clock and Data Recovery chip (CDRs), and TE Connectivity providing a 2m QSFP28G Active Copper Cable assembly and a zQSFP+ host connector assembly.

3.5.1 Component Overview

Applied Micro Gearbox IC: Applied Micro Gearbox IC: The S28110PRI Gearbox II from Applied Micro is a fully integrated bidirectional 10:4 mux/demux and 10:10 retimer for 100Gbps, 40Gbps and 10Gbps interconnect applications. It operates at both Ethernet and OTN rates while offering industry leading transmit jitter performance and receive sensitivity. It comes with a host of diagnostic features such as receiver eye monitors, PRBS mon/gen, and virtual lane identification. It is compliant with the OIF-28G-VSR and OIF-28G-SR specifications on the 28Gbps interface while carrying an industrial temperature rating.

Inphi Gearbox: The Inphi's IN112510-LD is a single-chip, low-power tri-rate CMOS PHY for 10:4 gearbox/10:10 retimer applications in 10/40G/100G Ethernet and OTU4 line cards and optical modules. Optimized for low-latency operation, it delivers high system performance and ultra-low jitter for demanding applications. It is designed to significantly exceed CEI-28G-VSR requirements and allows real-time monitoring of link margin and protocol checking as well as dynamic high resolution eye scan diagnostics.

Molex zQSFP+: Molex zQSFP+ [1] connectors compatible with QSFP28 are used on one of the MCB boards. The zQSFP+ system from Molex supports next-generation CEI-28G-VSR, 100 Gbps Ethernet and InfiniBand Enhanced Data Rate (EDR) applications with excellent cooling, improved signal integrity (SI), superior electro-magnetic interference (EMI) protection and low power consumption.

Semtech Re-Timer: Semtech's GN2425/26 are low-power retimers, leveraging a generation of innovation in 10G module CDRs, optimized for reference-free 25-28.1 GBd operation in next-generation optical modules and active cables. By resetting the jitter budgets within the module in both directions, Semtech's CDRs are optimized for challenging new applications such as 100GBASE-LR4/ER4 and OTU4 CFP2 optical modules. The GN2425/26 feature superior receive sensitivity, input jitter tolerance and output jitter, allowing for reliable signal recovery and clean, wide-open transmit eyes.

TE Connectivity Connector: TE Connectivity's zQSFP+ connector is a new high speed, high density interconnect that supports data rates from 28 Gbps per lane over the connector's 4 channels, providing an aggregate bandwidth of 100Gbps. The connector interface is fully backwards compatible to the existing QSFP+ modules and cable assemblies. Through a coupled, narrow-edged, blanked- and formed- contact geometry and insert molding design, the zQSFP+ interconnect exhibits robust industry compliant signal integrity, as well as mechanical and electrical performance. The zQSFP+ cage offers excellent thermal performance and enhanced EMI protection.

The active copper cable assembly supplied by TE Connectivity leverages TE's Madison Cable brand InfiniTwist cable to provide a four channel, 5.8 mm diameter cable assembly with reduced diameter for improved airflow and improved flexibility for ease of cable management. The cable assembly's QSFP-28G end points house the Semtech clock and data recovery (CDR) chips mentioned above, enabling the use of the highly flexible 34 AWG differential pairs in the InfiniTwist cable.

[1] zQSFP is trade mark of Molex Inc and is compatible with QSFP28 as defined by SFF-8661.

3.5.2 Demo 5 Test Equipment

Test equipment supplied to the PLL Interop demonstration by Agilent Technologies included the following:

86100D DCA-X Oscilloscope: Modular platform that accommodates up to 4 measurement modules and 16 measurement channels. Includes 86108B high bandwidth module, Option 200 Enhanced Jitter Analysis and Option 201 Advanced Waveform Analysis software.

3.5.3 Demo 5 Description

This demonstration system consists of the following blocks: an Applied Micro 100G Gearbox, an Inphi 100G Gearbox, , a Molex zQSFP+ connector and cage, a Semtech VSR host channel, a TE zQSFP+ connector and cage, mated with Semtech 25-28G Retimer ICs packaged within a TE Connectivity QSFP-28G Active Copper Cable (ACC) Assembly. The system generates PRBS31 data at 25.78 Gb/s rate within the Inphi Gearbox which is transmitted over the 10dB Semtech VSR channel through the TE zQSFP+ connector to the inputs of the Semtech CDR ICs in the TE QSFP-28G ACC modules. The retimed outputs of the CDRs are transmitted across a 34 AWG 8-pair cable. The electrical outputs at the far-end of the QSFP-28G ACC assembly are terminated at the PRBS31 error checkers within the Applied Micro Gearbox in order to verify that the entire data path originating at the Inphi Gearbox is operating error free. Similarly, PRBS31 data is sourced from the Applied Micro 100G Gearbox and terminated at the Inphi 100G Gearbox again verifying error free operation An electrical data eye is shown on an Agilent DCA-X 86100D Digital Sampling Oscilloscope at one of the Semtech CDR outputs using the built-in CTLE S/W function within the oscilloscope to display an equalized electrical data eye.

Demo 5 operated error free on three lanes full duplex at 25.78Gb/s with a PRBS31 data pattern. One of the Semtech CDR outputs that recovered the signal through the CEI-28G-VSR channel was displayed on the Agilent DCA-X Oscilloscope, with the scope applying a S/W CTLE function per OIF CEI-28G-VSR specifications in order to display a VSR data eye.

Demo 5: CEI-28G-VSR QSFP28 ACC Demo
(Agilent, Applied Micro, Inphi, Molex, Semtech, TE Connectivity)

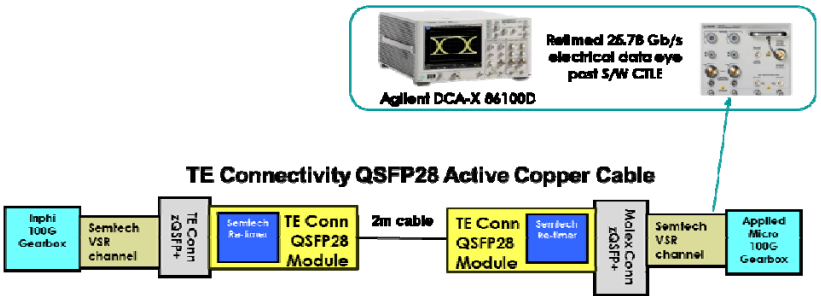

Figure 12: Demo 5 Block Diagram

3.6 Demo 6: Module to Host Thermal Interface Modeling

Supported by: Molex, TE Connectivity

3.6.1 Thermal Interface Background Information and Applications

The Module to Host Thermal Interface application reference diagram is shown in Figure 13. It consists of a pluggable optical transceiver that is dissipating power mounted in a cage on the host board (line card) and the cage has a heat sink to aid in transferring the thermal energy from the optical module into the airflow provided by the host line card for the purpose of managing the system's thermal environment. Insufficient thermal conduction between the optical module and heat sink will increase the temperature of the internal components. High operating temperatures may reduce system performance, reduce product reliability and possibly cause the product to shut down. A representative graph of the effect of different fin geometry on the case temperature of seven horizontally mounted optical modules under three different air flow rates is shown in Figure 14. This illustrates the effect that a heat sink variation can have on a pluggable optical transceiver case temperature. Historically, as data rates increase the power dissipation of the optical module increases resulting in increased power densities and a requirement for more tightly controlled thermal interfaces. The intent of the OIF's effort in this case is to develop a document that will provide a degree of standardization and common understanding across the Networking Industry. For additional information, see the OIF's white paper on this subject.

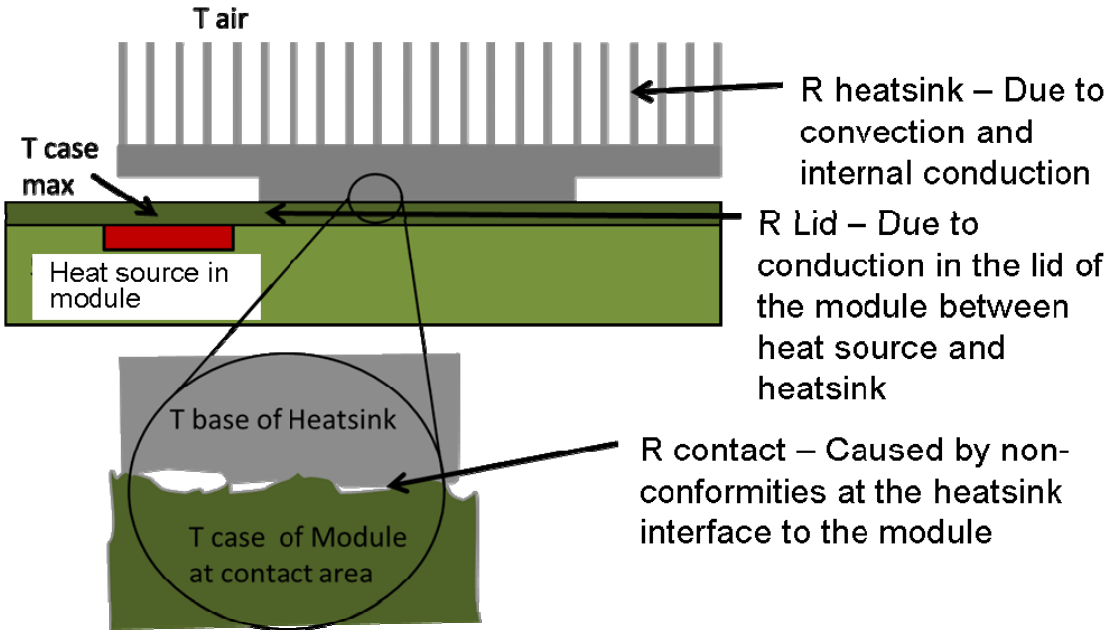

Figure 13: Module to Host Thermal Interface

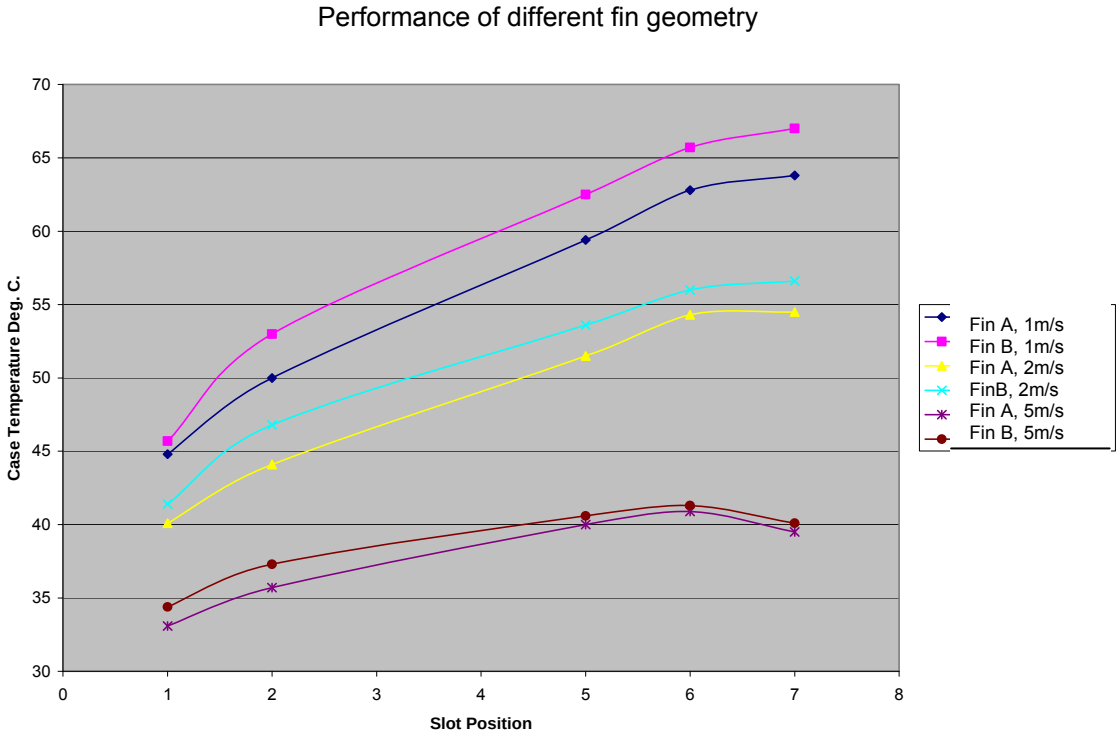

Figure 14: Performance of Different Heat Sink Fin Geometry

3.6.2 Demo 6: Thermal Interface of Pluggable Modules

Participating companies in Demo 6 were Molex and TE Connectivity with a thermal emulator test vehicle, simulating a line card with thermally programmable pluggable modules, and various heat sink solutions in support of the OIF's active project to develop an Implementation Agreement defining standardized thermal interfaces between pluggable modules and hosts.

3.6.3 Demo 6 Thermal Interface Overview

Currently there is no standardized thermal interface definition between a pluggable module and a host. This is because pluggable modules are developed by various independent MSAs, as well as individual contributors with no wide-spread standardization. The OIF has a current project in process to develop an Implementation Agreement that plans to provide a standardized methodology of defining thermal interfaces on optical modules that can be shared across industry. To support that project Molex and TE Connectivity have teamed up to demonstrate the effects of some of the variables that must be considered in a module to host thermal interface.

3.6.4 Demo 6 Description

This demonstration consists of a line card thermal emulator test platform that consists of a simulated line card supporting 8 positions of the proposed CDFP 400Gb/s optical module that is in process of being defined by the CDFP MSA. This emulator allows the 8 pluggable positions to be powered to various levels of power dissipation, monitors the heat sink temperatures, is able to vary the flow rate of the cooling air passing over the modules/heat sinks and monitors air pressure. Using such a test platform enables an investigation of single variable and multiple variable scenarios in a controlled setting. In the demonstration that was completed in August 2013, Molex and TE considered two different heat sink materials (Aluminum and Zinc), and two different heat sink surface roughness's on the aluminum samples. It has been demonstrated that smoother surfaces do enhance the thermal transfer efficiency but not to the degree anticipated (approx 1 deg C). It is thought that there might have been additional variables in the test set-up that need to be investigated further. Based on this result, secondary data was captured looking at transceiver roughness and heat sink flatness, which suggests that further work should be done. Other areas for future consideration that were not specifically considered in this demo include surface flatness, heat sink geometry (cross section, orientation, surface area) and potentially, thermal interface materials.

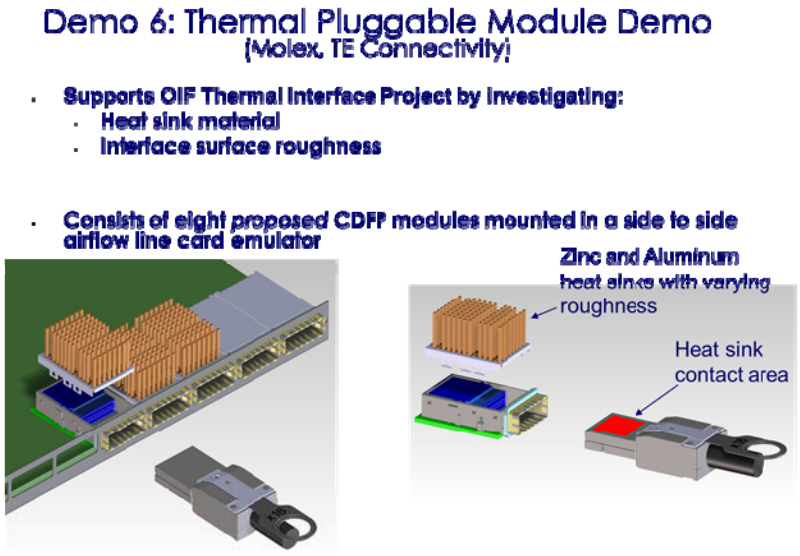

Figure 15: Demo 6 - Thermal Pluggable Module

3.7 Demo 7: CEI-25G-LR Backplane Application Interoperability

Supported by: MoSys and Amphenol

3.7.1 Component Overview

MoSys Re-Timer: MoSys LineSpeed™ 100G Quad Retimer (MSH210) is a single chip low power CMOS IC designed to support full duplex 100 Gigabit links for optical transceivers, active and passive copper cable, extended line card or backplane applications. All SerDes on the PHY IC are equipped with Tx equalization and a strong self-adapting Rx equalizer to support a wide range of IEEE and OIF standards ranging from short reach to extended reach and data rates up to 28 Gbps. The device includes on chip pattern generators, error checking and monitoring capabilities.

Amphenol Connector: Amphenol Xcede connector family of connectors provide superior signal integrity performance up to 28Gb/s, The Xcede2 coming out in 2014 will provide performance to 56Gb/s. The Xcede plus used in this back plane demonstration has dedicated tooling for 85 or 100 Ohm impedance, lower insertion loss and supports embedded capacitor technology.

Amphenol Backplane: The Amphenol supplied reference backplane channel consists of two daughter cards, a backplane, and two XcedePlus connectors. The XcedePlus connector is ideal for the 25Gb/s per lane we demonstrating here. It is backward compatible with legacy Excede connectors so new daughter cards can be used in existing systems. The MoSys SerDes connects to the Amphenol daughter cards through 2.4mm connectors.

The daughter cards are a 20 layer PCB with Megtron6 for the high sped signal layers. There are various breakout layers and with a total etch length of 7".

The backplane is also a 20 layer PCB employing Megtron6 in the high speed signal layers. The total etch length used in the demo is 12 inches. The 85 Ohm differential pairs are made up of a 7.0 / 5.0 / 7.0 geometry.

3.7.2 Demo 7 Description

The goal of the demonstration is to exhibit the OIF CEI 25G LR Implementation Agreement (IA) with 4-lane 100G operation across a backplane link with end-to-end loss of >25dB at 12.9GHz. Each lane carries a PRBS-31 pattern running at a 25.78125Gb/s data rate. PRBS generation and checking is performed on-chip.

The demonstration contains a MoSys retimer IC operating over a Amphenol-supplied reference backplane. The insertion loss of the backplane is 16db and the paddle cards combine for another 5db for a total loss of 21db.

The 12 inch backplane channel and two 3.5 inch line cards, which are used in this demonstration, contains approximately 20dB of loss from the 2.4mm connector on one daughter card to the 2.4mm connector on the other daughter card. An additional 6 dB of loss is on the MoSys retimer Evaluation Board for a total channel loss of 26dB. The demonstration ran 4 lanes of bidirectional traffic at 25.78Gbps resulting in 4 NEXT (near end cross talk) lanes, in row and in column, and 3 FEXT (far end cross talk) lanes, in row and in column acting on victim pairs in order to increase the amount of crosstalk.

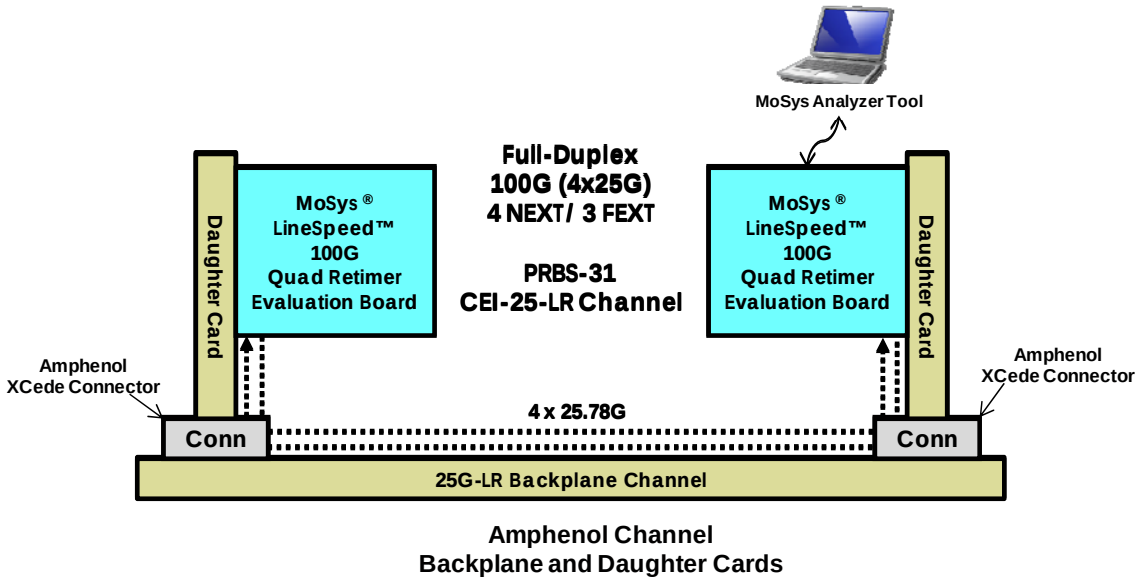

Figure 16: Demo 7 Block Diagram

3.8 Demo 8: CEI-25G-LR Backplane Application

Supported by: MoSys and Molex

3.8.1 Component Overiew

MoSys Retimer: MoSys LineSpeed™ 100G Quad Retimer (MSH210) is a single chip low power CMOS IC designed to support full duplex 100 Gigabit links for optical transceivers, active and passive copper cable, extended line card or backplane applications. All SerDes on the PHY IC are equipped with Tx equalization and a strong self-adapting Rx equalizer to support a wide range of IEEE and OIF standards ranging from short reach to extended reach and data rates up to 28 Gbps. The device includes on chip pattern generators, error checking and monitoring capabilities.

Molex Connector: The Impel™ Backplane Connector System provides a scalable price-for-performance solution enabling customers to secure a high-speed 25Gbps – 40Gbps connector with industry leading density. The Impel™ Connector System provides the footprint and interface that will enable customers to migrate to faster data rates (40Gbps), through an optimized electrical structure that leverages tightly coupled differential pairs with improved pair-to-pair isolation. The Impel™ backplane connector family is a 92ohm solution providing low cross-talk and high signal bandwidth while minimizing channel performance variation across every differential pair within the system.

Molex Backplane: The Impel Backplane system consists of a Reference Backplane (BP), and 2 Reference Daughter Cards (DC), using the 4-pair Impel™ Backplane Connector solution (BP = 171315-1807 and DC = 171320-1038).

The reference backplane uses Megtron 6 material, is 6.35mm thick with trace width and spacing of 7mils/8mils/7mils and controlled to a nominal impedance of 90ohms. There are 4 different trace lengths are available on Impel™ Reference BP: 0.166 meter, 0.286 meter, 0.516 meter, and 0.746 meter. The Reference Backplane is designed for 90ohm differential impedance to reduce impedance discontinuity between Impel™ backplane connector, backplane connector via, and differential traces.

There are 2 Daughter-card boards used in conjunction with the Reference Backplane. The Reference Backplane Daughter-card boards are made with Megtron 6 material with a provided total thickness of 3.05mm. The Reference Backplane Daughter-card boards utilize 5mils/5mils/5mils for trace width and spacing, are controlled to a nominal impedance of 100ohms, and contribute to a total of 5-inches, (0.127m), of trace length. Each DC board utilizes the Impel™ part number 171320-1038 in conjunction with 2.92mm RF connectors. The total channel lengths in the mated condition of DC to BP are as follows: 0.42 meter, 0.54 meter, 0.77 meter and 1 meter.

3.8.2 Demo 8 Description

The goal of the demonstration is to exhibit the OIF CEI 25G LR Implementation Agreement (IA) with 4-lane 100G operation across a backplane link with end-to-end loss of >25dB at 12.9GHz. Each lane carries a PRBS-31 pattern running at a 25.78125Gb/s data rate. PRBS generation and checking is performed on-chip.

The demonstration contains a MoSys retimer operating over a Molex-supplied reference backplane.

The 0.286 meter backplane channel and two 0.27 meter line cards, which are used in this demonstration, contains approximately 21dB of loss from the 2.92mm connector on one daughter card to the 2.92mm connector on the other daughter card. An additional 6 dB of loss is on the MoSys retimer evaluation board for a total channel loss of 27dB. The demonstration runs 4 lanes of bidirectional traffic at 25.78Gbps resulting in 4 NEXT (near end cross talk) lanes, in row and in column, and 3 FEXT (far end cross talk) lanes, in row and in column acting on victim pairs in order to increase the amount of crosstalk.

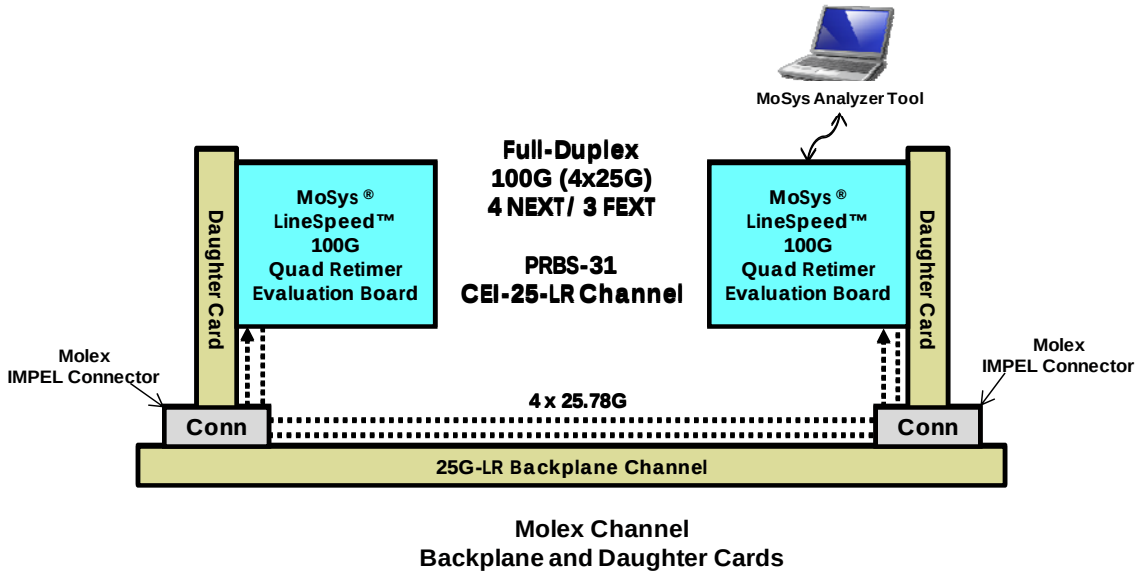

Figure 17: Demo 8 Block Diagram

3.9 Demo 9: CEI-25G-LR Application

Supported by: MoSys and TE Connectivity

3.9.1 Component Overview

MoSys Retimer: MoSys LineSpeed™ 100G Quad Retimer IC (MSH210) is a single chip low power CMOS IC designed to support full duplex 100 Gigabit links for optical transceivers, active and passive copper cable, extended line card or backplane applications. All SerDes on the PHY IC are equipped with Tx equalization and a strong self-adapting Rx equalizer to support a wide range of IEEE and OIF standards ranging from short reach to extended reach and data rates up to 28 Gbps. The device includes on chip pattern generators, error checking and monitoring capabilities.

TE Connectivity Connector: TE's STRADA Whisper backplane connector is designed to support data rates per differential pair up to 40Gbps. The connector's individually shielded pairs results in noise performance that is less than 1% @ 20 ps signal edge rates and insertion loss of less than 1db and flat past 15GHz. STRADA Whisper connectors are available in both 100 ohm and 85 ohm versions and can be supplied with embedded capacitors. The in-row "horizontal" pair orientation results in zero skew. Since PCB interfaces are a critical element of over-all connector performance, the STRADA Whisper connector footprint has been engineered to optimize the technical tradeoffs of impedance, cross talk and route-ability.

TE Connectivity Backplane: The TE supplied reference backplane channel consists of two daughter cards, a backplane, and two STRADA Whisper connectors. The STRADA Whisper connector is made up of a vertical header and a right-angle receptacle. The MoSys SerDes connects to the TE daughter cards through 2.4mm connectors.

The daughter cards are 110mils thick using Megtron 6 material encompassing 14 layers each.[2] All of the differential traces routed from the 2.4mm test points to the skew-less STRADA Whisper connector footprint are 5 inches in length in a 6-9-6 mil trace width configuration. The traces and other copper in the boards utilize Megtron 6 VLP foil finishes. The signal vias in both the STRADA Whisper connector and 2.4mm test points are counter-bored to within 10 mils of the signal layer. The daughter card contains the STRADA Whisper receptacle.

The backplane, which contains the STRADA Whisper header, is 200mils thick using Megtron 6 material encompassing 20 layers. All of the differential traces routed on the backplane are in a 7-9-7 mil trace width configuration. The traces and other copper in the board utilize a Megtron 6 H-VLP foil finish. The signal vias in the STRADA Whisper connector footprint are counter-bored to within 10mils of the signal layer. The backplane demonstrates lengths of 4, 8, 17, and 30". When combined with a daughter card on each end the total trace length demonstrated in the channel is extended to 14, 18, 27, and 40 inches.

3.9.2 Demo 9 description

The goal of the demonstration is to exhibit the OIF CEI 25G LR Implementation Agreement (IA) with 4-lane 100G operation across a backplane link with end-to-end loss of >25dB at 12.9GHz. Each lane carries a PRBS-31 pattern running at a 25.78125Gb/s data rate. PRBS generation and checking is performed on-chip.

The demonstration contains a MoSys retimer operating over a TE Connectivity-supplied reference backplane. It is built with Megtron6 material and implements TE's STRADA Whisper backplane connector product.

The 17 inch backplane channel and two 5 inch line cards, which are used in this demonstration, contains approximately 22dB of loss from the 2.4mm connector on one daughter card to the 2.4mm connector on the other daughter card. An additional 6 dB of loss is on the MoSys retimer Evaluation Board for a total channel loss of 28dB. The demonstration runs 4 lanes of bidirectional traffic at 25.78Gbps resulting in 4 NEXT (near end cross talk) lanes, in row and in column, and 4 FEXT (far end cross talk) lanes, in row and in column acting on victim pairs in order to increase the amount of crosstalk.

[2] Megtron is a registered trademark of Panasonic.

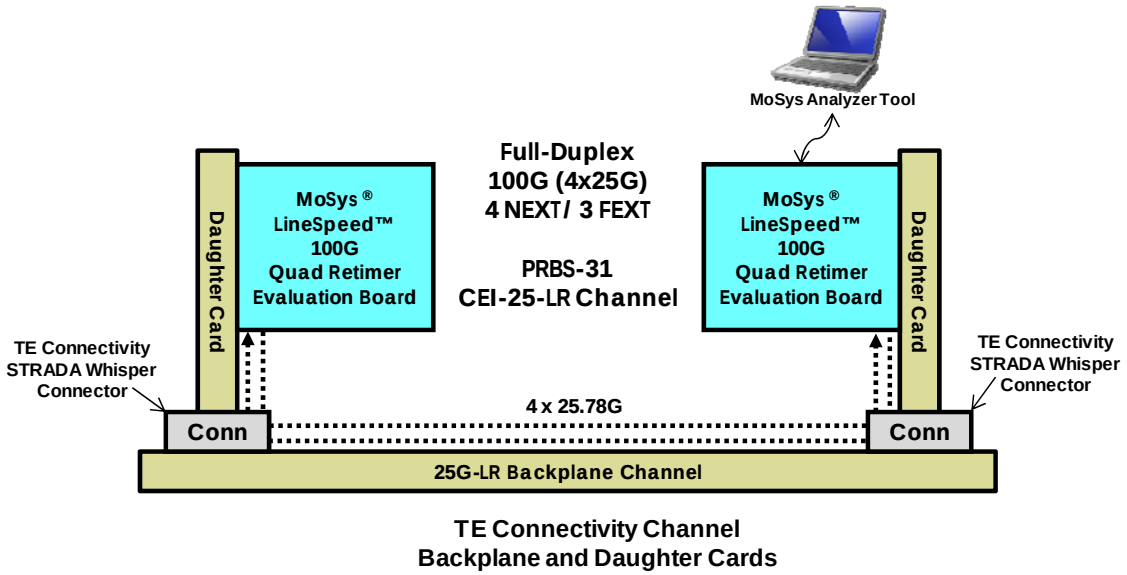

Figure 18: Demo 9 Block Diagram

4. Conclusions

This interoperability demonstration successfully brought semiconductor, connector, optical module and test equipment vendors together to show OIF CEI-28G-VSR instantiation of Cisco CPAK and CFP2 as well as QSFP28 active copper cable assembly. OIF CEI-28G-VSR is widely accepted and now the IEEE 802.3bm CAUI-4 specification is being developed largely based on OIF CEI-28G-VSR specification. OIF CEI-28G-VSR is the key building block for next generation 100 GbE, OTN, 32 GFC (Fibre Channel), and IB EDR (InfiniBand) retimed optical modules.

The thermal interface demonstration represents the OIF's first ever public showing of the work that is in process to develop a thermal interface implementation agreement. While this work is on-going, the demo shows the industry cooperation that is necessary to define the planned implementation agreement.