Implementation Agreement for the High Bandwidth Coherent Driver Modulator (HB-CDM)

IA # OIF-HB-CDM-01.0

November 30, 2018

Implementation Agreement created and approved
by the Optical Internetworking Forum
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TITLE: **Implementation Agreement for High Bandwidth Coherent Driver Modulator (HB-CDM)**

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ABSTRACT: This Implementation Agreement specifies key aspects of High Bandwidth Coherent Driver Modulators operating at rates up to 64GBd.

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Document Revision History

Document	Date	Revisions/Comments
OIF-HB-CDM-01.0	Nov 30, 2018	First release

1 Introduction

This document details an Implementation Agreement for a High Bandwidth Coherent Driver Modulator (HB-CDM) targeting modulation and data-rate agnostic coherent applications having nominal symbol rates up to 64Gbaud. The IA aims to identify and specify the common features and properties of coherent transmitters to enable them to broadly meet the needs of current and future coherent systems.

This Implementation Agreement defines the following: (1) Required functionality; (2) High speed electrical interfaces; (3) Low speed electrical interfaces; (4) Electro-Optical Specifications and Operating Characteristics; (5) Mechanical requirements.

A single electro-mechanical form factor is defined in this revision of the HB-CDM IA labeled as Type 1, and uses a surface mount configuration. Further form factors may appear in future revisions of this IA, hence the naming of the initial variant is kept as "Type 1".

The IA defines an SPI bus to control the Driver in the HB-CDM, including frame format and electrical specifications. The document includes vendor specific options for analog control using the optional Vendor Specific – Analog pins defined in the pin list, but these have not been standardized in this document.

The IA does not define the technologies used to implement the IA, nor the expected optical transmission performance of coherent systems using transmit components conforming to the IA.

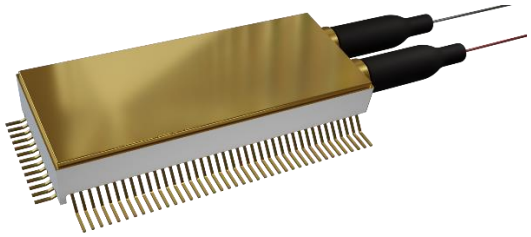


Figure 1-1 Type1 HB-CDM module

2 Functionality

This Implementation Agreement specifies a single opto-electronic module with the functionality shown in Figure 2-1 and consisting of an integrated Coherent Driver and a Polarization Multiplexed Quadrature Modulator.

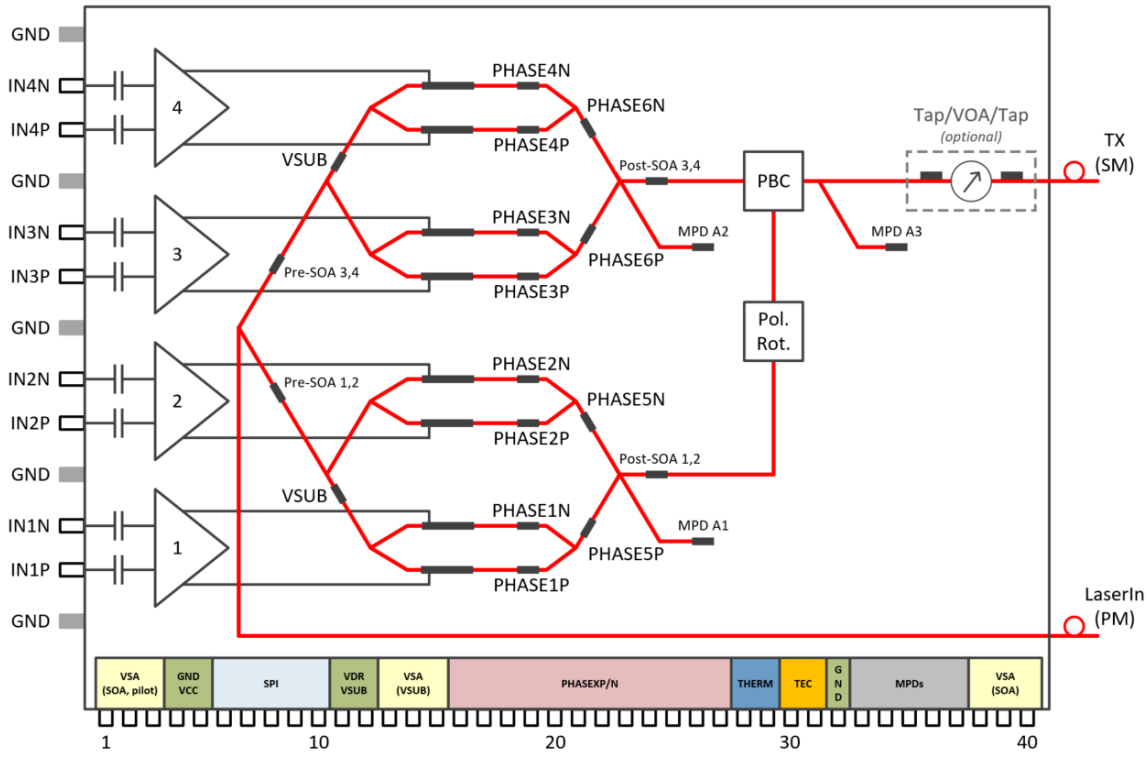


Figure 2-1 Functional schematic for the HB-CDM

Notes:

1. While one configuration for the position of the SM and PM fibers is shown here, the reverse orientation is equally acceptable for compliance.
2. An output shutter and VOA are optional
3. The MPDs are optional
4. The Vpilot tone modulation is optional
5. Pre and Post SOAs are optional
6. Per polarization PDs may be complementary or tap structures

The differential RF modulation inputs are fed to the Driver stage to amplify the electrical signals to match the modulator electrode requirements to induce sufficient optical phase change.

The PM fiber optical input is split and independently modulated by quadrature modulators, then recombined with their polarizations orthogonal to each other

using a Polarization Rotator. The resulting optical signal is output through a Single Mode fiber.

3 Mechanical

3.1 Type 1 Overview

The primary electro-mechanical form factor (Type 1) uses a surface mount configuration with the low speed electrical interface signals applied from the left side of the package (viewed from top, optical south).

The outline mechanical size of the HB-CDM is shown in Table 3-1. These figures represent an informative specification with the key compliance of the module being compatible with the Landing Pad definitions in Section 4.

HB-CDM Form Factor	Width (mm)	Height (mm)	Length[1] (mm)	RF (pitch)	DC (pitch)
Type 1	≤12	≤5.5	≤30	SMT pins (0.8mm)	SMT pins (0.7mm)

Table 3-1 Outline mechanical size of the HB-CDM

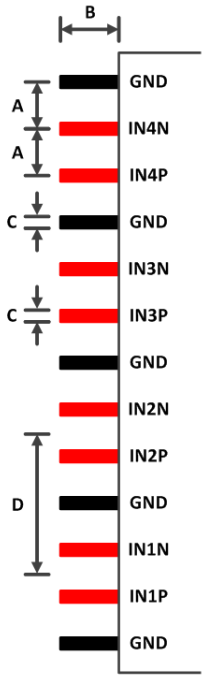
Notes:
1. Extensions to the Length parameter while keeping to the same pad frame are permitted and deemed compliant to the Implementation Agreement

The top surface of the module is defined as the Hot Area (opposite side to the PCB).

4 High Speed Electrical Interface

4.1 High Speed Electrical Interface

The high speed electrical output interface uses surface mounted pins in a differential co-planar waveguide arrangement (GSSG), with shared ground pins. The pin definitions and pitches shall be as detailed in Table 4-1, Table 4-2, and Figure 3-1. It is noted that alternate channel configurations for the differential signals shown are acceptable.



Parameter	Value	
Interface type	Differential	
Channel number	4	
Channel configuration	G-S-S-G	
Signal line coupling	AC	
Signal line impedance	100 Ohm Differential	
Channel pin-out	1 2 3 4	
Differential pin-out	Signal Complimentary Signal	P N

Table 4-1 High speed electrical interface description.

Parameter	Symbol	Min	Typ	Max	Units
Signal/Ground lead pitch	A		0.8		mm
Signal/Ground lead length	B	1.75	2.0	2.25	mm
Signal/Ground lead width	C	0.15	0.2	0.25	mm
Channel pitch	D		2.4		mm

Table 4-2 Type 1 high speed electrical interface dimensions.

Figure 4-1 High speed electrical interface definition.

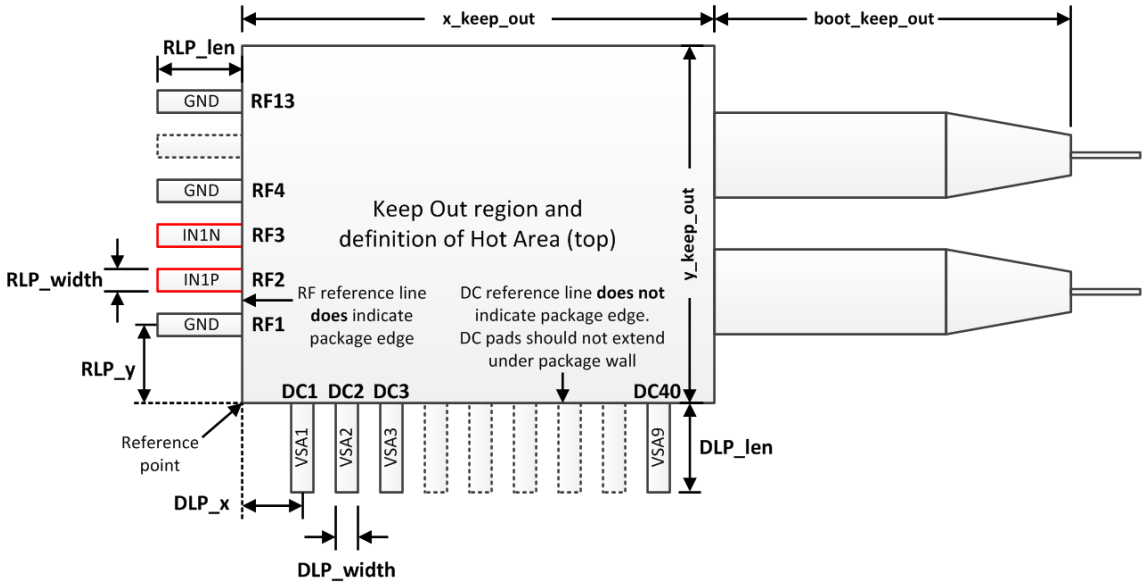


Figure 4-2 Type 1 RF and DC Landing Pads

		Type 1 PCB Landing Dimensions (mm)			
Dimension		**Min.**	**Typ.**	**Max.**	**Note:**
DC Control	Pitch		0.70		Fixed
	DLP_x		1.00		Fixed
	DLP_width	0.35			
	DLP_len	3.10			
	x_keep_out	Standard		30	
		Extended		55	
	boot_keep_out			15	
RF Signal	Pitch		0.80		Fixed
	RLP_y		1.20		Fixed
	RLP_width	0.35			Stack-up dependent
	RLP_len	2.55			
	y_keep_out			13	

Table 4-3 Type 1 Landing Pad Dimension Table

5 Low Speed Electrical Interface

5.1 Low Speed Electrical Interface

The low speed electrical connections are provided through 40 signals with the orientation shown in Figure 5-1 and numbered as shown in Table 5-1. An HB-CDM vendor may choose to populate fewer signals, but the definitions of the populated signals should match those in the table. While Vendor-Specific-Analog (VSA) signals are optional, each has an assumed function as shown. If a vendor chooses to use VSA signals for alternative functions, the electrical specification should match the listed function to allow electrical compatibility so as not to damage module or host.

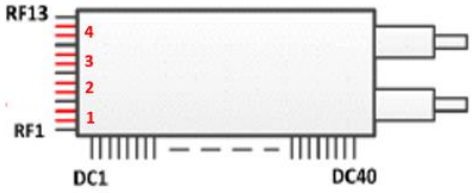


Figure 5-1 RF and DC signal orientation

For Table 5-1, refer to Figure **2-1** for reference numbers for PHASE#, MPD# and SOA#

Pin DC#	Signal Name	Description	Pin DC#	Signal Name	Description
1	VSA1	VSA / pre-SOA 3, 4 Anode (current)	21	PHASE3N	MZ Phase control or VSA
2	VSA2	VSA / pre-SOA 1, 2 Anode (current)	22	PHASE4P	MZ Phase control
3	VSA3	VSA / Pilot (voltage)	23	PHASE4N	MZ Phase control or VSA
4	GND	Ground	24	PHASE5P	MZ Phase control
5	VCC	3.3V supply	25	PHASE5N	MZ Phase control or VSA
6	SPI-RST	SPI Reset	26	PHASE6P	MZ Phase control
7	SPI-MISO	SPI MasterInSerialOut	27	PHASE6N	MZ Phase control or VSA
8	SPI-MOSI	SPI MasterOutSerialIn	28	THERMP	Thermistor +
9	SPI-CLK	SPI Clock	29	THERMN	Thermistor -
10	SPI-CS	SPI ChipSelect	30	TECN	TEC power -
11	VDR-BIAS	Driver far end bias	31	TECP	TEC power +
12	VSUB1	MZ substrate bias (voltage)	32	GND	Ground
13	VSA4	VSA / MZ substrate bias2	33	MPD-A3	Monitor PD Anode 3 or VSA
14	VSA5	VSA / MZ substrate bias3	34	MPD-C3	Monitor PD Cathode 3 or VSA
15	VSA6	VSA / MZ substrate bias4 (or GND)	35	MPD-A1	Monitor PD Anode 1 or VSA
16	PHASE1P	MZ Phase control	36	MPD-A2	Monitor PD Anode 2 or VSA
17	PHASE1N	MZ Phase control or VSA	37	MPD-C12	Monitor PD Cathode 1 and 2 or VSA
18	PHASE2P	MZ Phase control	38	VSA7	VSA / post SOA 1, 2 Anode (current)
19	PHASE2N	MZ Phase control or VSA	39	VSA8	VSA / post SOA 3 ,4 Anode (current)
20	PHASE3P	MZ Phase control	40	VSA9	VSA / post SOA Cathode (current)

Table 5-1 Low speed electrical interface definition

Notes:

1. VSA1 and VSA2 use common Cathode to GND for the pre-SOA
2. Thermistor function may be implemented with a single THERMP pin in which case THERMN becomes VSA (optionally connected to GND).
3. PHASE#N controls may be omitted for single-end bias adjust implementations and VSA used in place
4. VOA functionality may be included and controlled by VSA pins

6 Electro-Optical Specifications

Basic operating characteristics and specifications are listed in Table 6-1 at the End of Life over the operating temperature and frequency ranges.

Parameter		Unit	Min	Typ	Max	Remarks/Note
Operating frequency	C-band	THz	191.35		196.20	Note 1
	L-band		186.00		191.50	
Optical input power		dBm			18	Peak power
Insertion loss		dB			16	Per polarization
PDL		dB			1	
Optical return loss		dB		27		Input and output
Parent MZI ER		dB		22		
Child MZI ER		dB		25		
Polarization ER		dB		20		
Monitor PD bias voltage	Option 3.3	V	3.14	3.3	3.46	Note 2
	Option 5.0		4.75	5.0	5.25	
Monitor PD responsivity (combined, referred to output power)		mA/W	10		800	Note 3
Monitor PD Bandwidth (combined)		GHz	1			Note 3
Monitor PD Bandwidth (per pol)		GHz	0.1			Note 3
VOA control voltage (optional)		V	0		9	Note 4
Thermistor resistance		kOhm		10		At 25°C
Thermistor beta value		K		3930		
TEC voltage		V	-2.5		2.5	Note 6
TEC current		A	-1.8		1.8	Note 6
Driver Supply Voltage		V	3.14	3.3	3.46	
VDR-BIAS (Driver far end termination)		V			6.0	
Maximum differential input swing		mVpp	600			Note 7
Minimum differential input swing		mVpp			300	Note 7
RF differential impedance		Ohm		100		
S21 E/O Bandwidth (3dB), referenced to 1GHz		GHz	35			+/- 1GHz span moving average See Figure 8-1
S11 electrical return loss						See Figure 8-2
I/Q skew (channels 1/2 or 3/4)		ps			50	
Total skew		ps			100	
I/Q skew variation (channels 1/2 or 3/4)		ps			1.5	
Total skew variation		ps			4	
Low frequency cut-off		MHz			1	
ESD (HBM)		V	250			
Operating humidity (non-condensing)		%RH	5		85	
Operating temperature	Standard	°C	-5		75	Note 5
	Preferred		-5		80	
Power dissipation		W			4.5	Note 6

Table 6-1 Electro-Optical Specifications and Operating Characteristics

Notes:

1. Minimum supported range. At least one of the two frequency bands shall be supported.
2. Vendor shall state which Bias Voltage Option or Options are allowed.
3. Monitor PDs are optional.
4. The VOA shall be of type "normally bright".
5. The operating temperature is defined as the minimum/maximum of the HB-CDM case "hot zone" surface temperature.
6. Over the Standard Operating Temperature as defined in the table.
7. Peak to peak differential. HB-CDM contains AC coupling capacitors. Normative input swing is 300 to 600mVppd.
8. THD is not defined in this IA and remains Application Specific and should be included in the HB-CDM Vendor Specification.

7 Power Sequencing Requirements

The following baseline power sequence is recommended but informative as HB-CDM vendors and customers have the flexibility to change with agreement between them:

Power On:

1. TEC enable
2. Enable substrate bias and set voltage VSUB to the maximum VDR-BIAS value
3. Enable driver VCC (3.3V supply)
4. Establish driver VDR-BIAS within 1s
5. Adjust substrate bias VSUB to final set point
6. Enable SOAs if present
7. Enable remaining pins

Power Off:

1. Disable SOAs if present
2. Disable VDR-BIAS
3. Disable VCC within 1s
4. Disable substrate bias VSUB
5. Disable remaining pins

8 RF Frequency Response

8.1 Measurement Methods

The HB-CDM electrical-to-optical S_{21} transfer function and S_{11} electrical return loss frequency responses shall be measured *differentially* to evaluate conformance to the RF masks in Section 8.2.

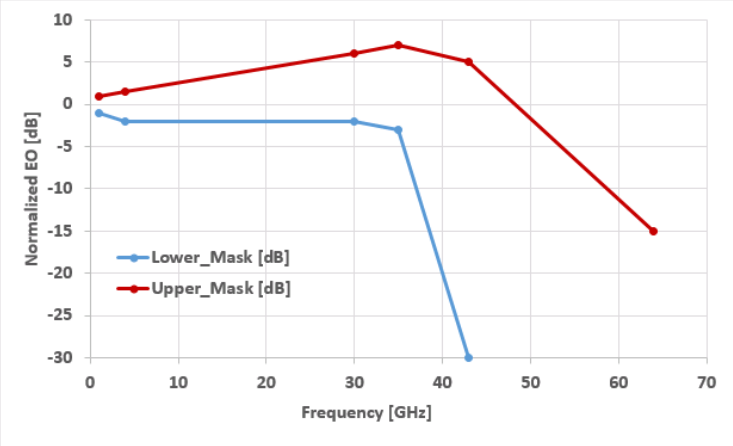
For these measurements, the HB-CDM shall be *soldered* to the measurement test fixture, and the collected data shall be de-embedded to the *RF reference point*. The *RF reference point* is defined as the point on the Host PCB RF traces that is 2.5mm beyond the maximum extent of the HB-CDM RF lead pad.

The masks of Figures Figure 8-1 andFigure 8-2 show a *target* range for the electrical-to-optical S_{21} transfer function and S_{11} electrical return loss frequency response, allowing for component to component variations. These masks will be revised in a future revision of the document as more component and system level performance data becomes available.

8.2 EO S_{21} Transfer Function Mask

The ideal RF frequency response for the transmit chain of a coherent modem – consisting of the DAC at the output of the ASIC, the differential signal traces between the DSP and the HB-CDM – is a low pass response which is flat up to the targeted signal bandwidth and rolls off steeply beyond that. Given that the losses of the signal traces between the DSP ASIC and the HB-CDM increase gradually with frequency, it is generally preferred that the RF frequency response of the HB-CDM increases gradually with frequency up to the targeted signal bandwidth, and then rolls off steeply.

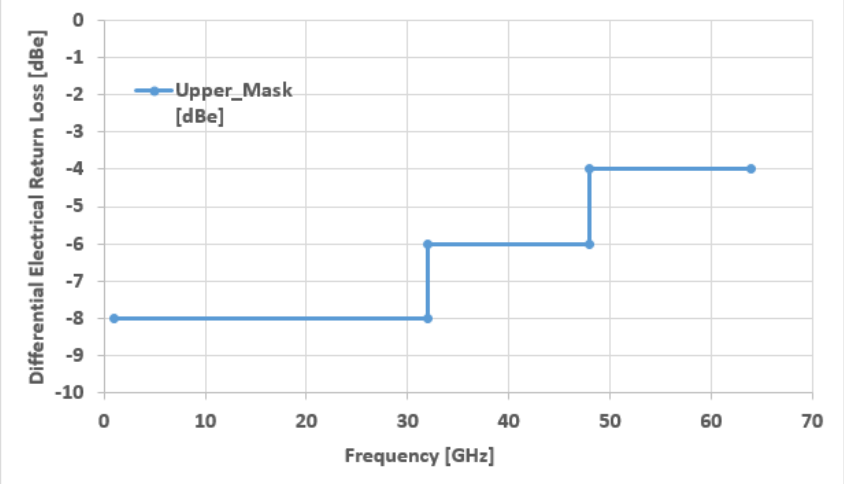
The S_{21} transfer functions shall be measured at a HB-CDM gain condition and temperature agreed with the customer. All S_{21} responses shall be normalized to the response at 1GHz. It is assumed that any Driver functionality that manipulates the S_{21} transfer function (i.e. bandwidth adjust functions) can be utilized to obtain compliance with the masks provided in this section.



Frequency [GHz]	Lower_Mask [dB]	Upper_Mask [dB]
1	-1	1
4	-2	1.5
30	-2	6
35	-3	7
43	-30	5
64		-15

Figure 8-1 Normalized EO S_{21} transfer function mask

8.2.1 Electrical Return Loss Mask



Frequency [GHz]	Upper_Mask [dBe]
1	-8
32	-8
32	-6
48	-6
48	-4
64	-4

Figure 8-2 Differential S_{11} electrical return loss mask

10 Fiber Types

The input and output optical fiber types are defined in Table 10-1.

Parameter		Unit	Min	Typ	Max	Note
"Minimum bend radius" specification for PM fiber output		mm			7.5	1, 2
"Minimum bend radius" specification for SM fiber input	Option 1	mm			5.0	3
	Option 2				7.5	4
Fiber cladding diameter (SM and PM)		µm		125		
Fiber coating diameter (SM and PM)		µm		250		
PM fiber colour				Transparent		
SM fiber colour				Red		

Table 10-1 Input fiber characteristics.

Notes:

1. The polarization state in the PM fiber shall be aligned to the slow axis of the PM fiber.
2. The slow axis of the PM fiber shall be aligned to the connector key.
3. The Option 1 SMF shall be compliant to ITU-T Recommendations G.657.B3 and G.652.D.
4. The Option 2 SMF shall be compliant to ITU-T Recommendations G.657.B2 and G.652.D.

11 SPI Based Low Speed Electrical Interface

The Low Speed control method for the Driver inside the HB-CDM is SPI and the following sections describe the Voltage Specifications, Read/Write Datagram, Operation Diagrams and Timing Specifications. Register definitions are not contained in this Implementation Agreement as these are deemed Vendor Specific and are not required to enable hardware compatibility between HB-CDM vendor units. The HB-CDM is defined as the *Client* or *Slave* in the SPI interface with the terms used interchangeably.

Hardware features controlled by the SPI interface may include, but are not required or limited to:

- Gain control
- Equalization/Peaking control
- Reading the output signal level
- Die temperature reading

Signal name	In/Out	Function
SCLK	In	SPI Clock
MISO	Out	Master In Serial Out
MOSI	In	Master Out Serial In
CS	In	Chip Select (active low)
RST	In	Reset (active low)

Table 11-1 SPI Control Signals

11.1 SPI Interface Voltage and Control Specifications

The SPI used is a full duplex synchronous serial interface originally defined by Motorola. The key voltage and control specifications are summarized in Table 11-2.

Parameter	Conditions	Unit	Value	
			Min	Max
SPI control voltage	Logical 0	V		0.8
	Logical 1		2	
IO Standard	LVCMOS	V	3	3.6
SCLK cycle time		ns	50	1000
SCLK frequency[1]		MHz	1	20
Time delay between asserting CS and toggling SCLK		ns	25	
Data register width	Address+Op-code	bit	16	

	Data block	bit	16
Data register shift direction			MSB first
Clock polarity			Idle state for CLK is low
Clock phases			Data is latched on the leading edge of CLK, data changes on the trailing edge
Client select state for data transmission			Chip select for read/write commands (active low)
Client reset (via Reset pin)			Asynchronous Reset (active low)

Table 11-2 SPI voltage and control specification.

Notes:

1. SPI control can be operated by any specific frequency within the Min/Max range.

11.2 SPI Read / Write Datagram

Table 11-3 depicts the data structure of the SPI command datagram. The protocol is designed to work with OIF IA compliant HB-ICR receivers using SPI control, where the HB-ICR addressing will reside in memory addresses 0x0000 to 0x01fff and the HB-CDM will reside in memory addresses 0x0200 to 0x03fff.

	Opcode – 16b																Data Block – 16b													
	HB-CDM device select						Chan* Address		Register Address							RW	Data in via MOSI, or Data out via MISO													
Bit#	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0	R/W	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Value	0	0	0	0	0	1	00 = 1 01 = 2 10 = 3 11 = 4		Select register							0=W 1=R	Data													

* Chan Address references are defined in Figure 2-1.

Table 11-3 SPI data telegram structure.

When an SPI controlled HB-ICR and a HB-CDM are connected in-system, they may share all the SPI signaling without duplication as shown in Figure 11-1 below as long as unique addressing and highZ MISO modes are available for both devices.

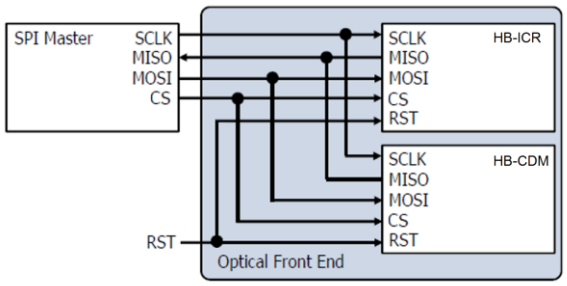


Figure 11-1 Connection example of SPI controlled HB-ICR and HB-CDM, when MISO sharing by address space is enabled on both devices

11.3 SPI Read / Write Operation Timing Diagrams

Figure 11-2 and Figure 11-3 show the SPI write operation timing and the SPI read timing operation.

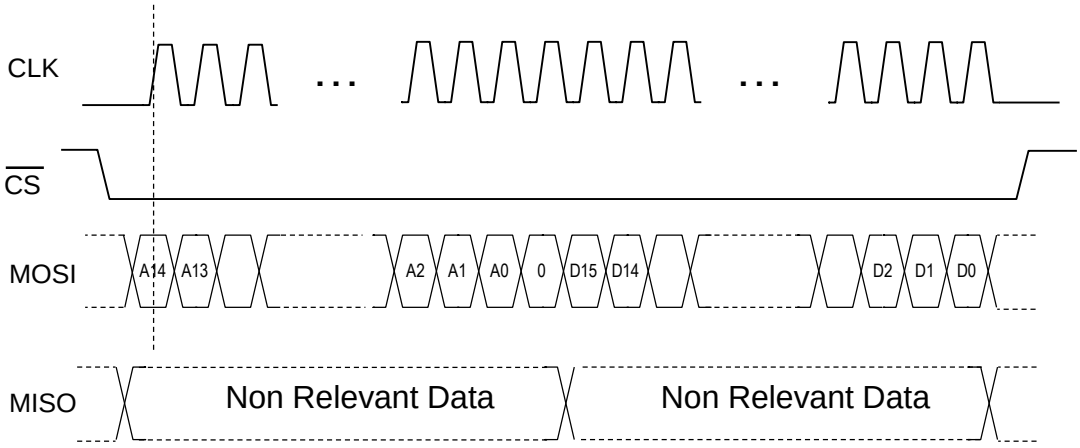


Figure 11-2 SPI write operation timing diagram.

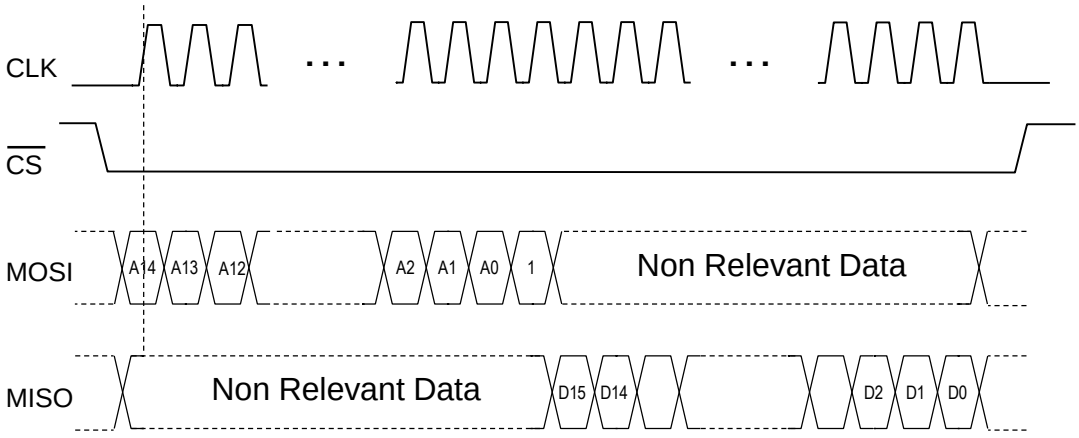


Figure 11-3 SPI read operation timing diagram.

11.4 SPI Timing Specifications

The SPI timing specifications are summarized in Table 11-4 and illustrated in Figure 11-4 and Figure 11-5. The SPI client hardware reset is defined as asynchronous. After the reset, the Driver configuration should be returned to its defaults.

Description	Condition	Symbol	Unit	Value	
				min.	max.
CLK clock frequency			MHz	1	20
CLK clock period		t_{CK}	ns	50	1000
CLK peak-peak jitter			ps		500
CLK high time		t_{CKH}	ns	20	550
CLK low time		t_{CKL}	ns	20	550
CLK 10%-90% rise time	15 - 18 pF capacitive load	t_{CKR}	ns	0.5	5
CLK 10%-90% fall time		t_{CKF}	ns	0.5	5
CSN to SPI CLK↑ setup time		t_{CSCK}	ns	50	1000
CLK ↓ to SPI CSN hold time		t_{CKCS}	ns	50	1000
CLK ↓to SPI MISO valid time	15 - 18 pF capacitive load	t_{CKSO}	ns	2	11
MISO 10%-90% rise time	15 - 18 pF capacitive load	t_{SOR}	ns	0.5	5
MISO 10%-90% fall time		t_{SOF}	ns	0.5	5
MOSI to SPI CLK↑ edge setup time		t_{MOCK}	ns	8	
MOSI to SPI CLK↑ edge hold time		t_{CKMO}	ns	8	
MOSI 10%-90% rise time		t_{MOR}	ns	0.5	5
MOSI 10%-90% fall time		t_{MOF}	ns	0.5	5
Min. SPI access inactive time		t_{CSCS}	ns	$5*t_{CK}$	
RSN time		t_{RS}	ns	t_{CK}	
RSN10%-90% rise time	15 - 18 pF capacitive load	t_{RSR}	ns	0.5	5
RSN10%-90% fall time		t_{RSF}	ns	0.5	5

Table 11-4 SPI read / write timing specifications.

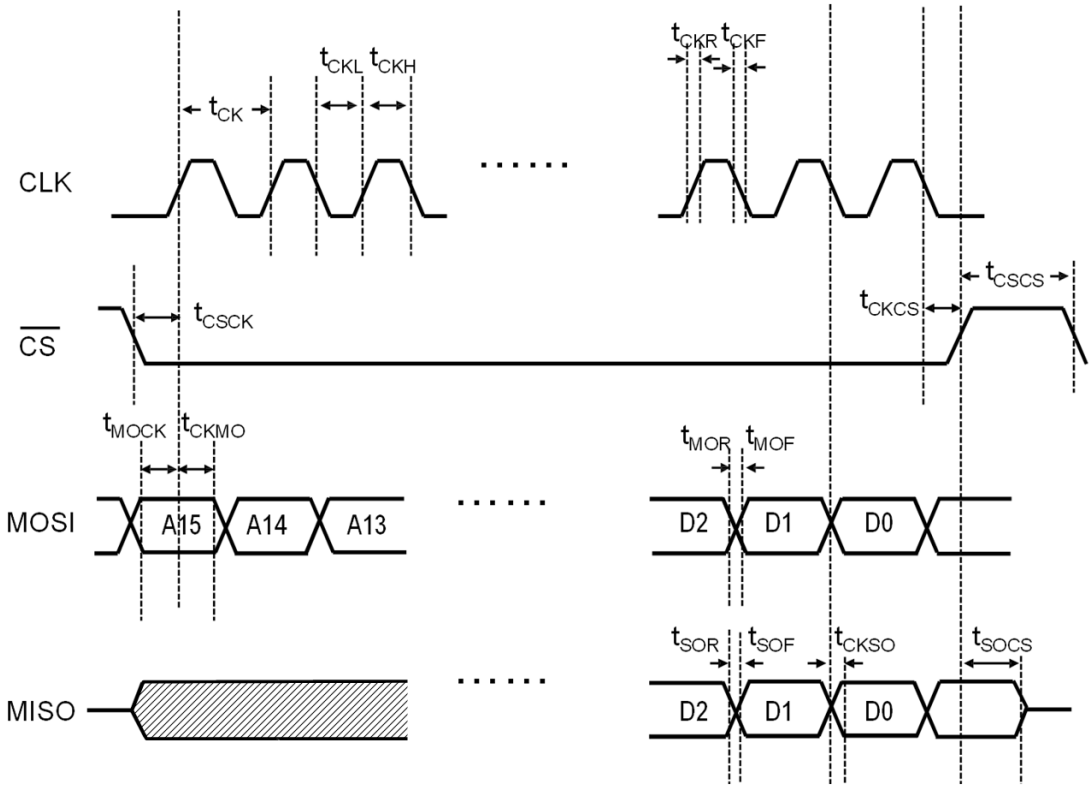


Figure 11-4 SPI client read/write timing.

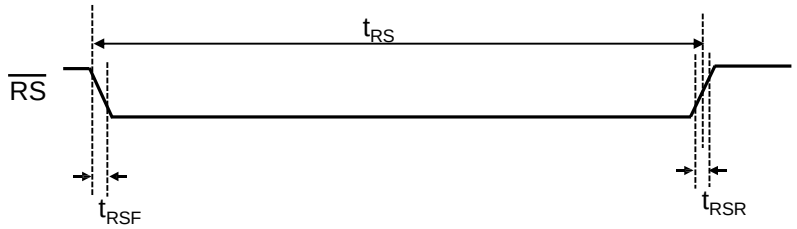


Figure 11-5 SPI client reset timing – asynchronous.

11.5 SPI Registers Specification

Register maps are not defined as part of this Implementation Agreement except for Address 0x0200 which should be reserved for a 16bit Driver manufacturer vendor ID to allow device specific register maps and capabilities to be loaded.

The Vendor ID should follow the LSB 16bits of the 24bit Organizationally Unique Identifier (OUI) code system assigned to device manufacturers by the IEEE. If a manufacturer doesn't have an OUI, another unique identifier may be used as the Vendor ID.

Further information on OUI numbers is available from:

https://en.wikipedia.org/wiki/Organizationally_unique_identifier

Currently assigned OUI numbers are listed here:

http://standards-oui.ieee.org/oui.txt

Extra functions that could be provided as part of the SPI register map include:

- Gain control
- Equalization/Peaking control
- Peak detector reading
- Unique serial number tracking ability
- Temperature readout

For a HB-CDM module to be compliant to this Implementation Agreement, only the Address 0x0200 device manufacturer register is a strict requirement, all other functions are optional.

12 References

12.1 Normative references

12.2 Informative references

- OIF-DPC-RX-01.2 – Implementation Agreement for Integrated Dual Polarization Intradyne Coherent Receivers (November 2013)
- OIF-CFP2-ACO-01.0 – Implementation Agreement for Analogue Coherent Optics Module (January 2016)
- OIF-HBPMQ-TX-01.0 – Implementation Agreement for the High Bandwidth Integrated Polarization Multiplexed Quadrature Modulators

13 Appendix A: Glossary

ADC	Analog to Digital Converter
AGC	Automatic Gain Control
BS	Beam Splitter
CMRR	Common Mode Rejection Ratio
DSP	Digital Signal Processor
Gbaud	10^9 Symbols per second
IA	Implementation Agreement
HB-ICR	High Bandwidth Intradyne Coherent Receiver
MPD	Monitor Photodiode
MSA	Multi-Source Agreement
OIF	Optical Internetworking Forum
PBS	Polarization Beam Splitter
PCB	Printed Circuit Board
SPI	Serial Port Interface
THD	Total Harmonic Distortion
VOA	Variable Optical Attenuator

14 Appendix C: Open issues / current work items

None

15 Appendix D: List of companies belonging to OIF when document is approved

Acacia Communications
ADVA Optical Networking
Alibaba
Amphenol Corp.
Analog Devices
Applied Optoelectronics, Inc.
Arista Networks
Barefoot Networks
BizLink Technology Inc.
Broadcom Inc.
Cadence Design Systems
Cavium
CenturyLink
China Telecom Global Limited
Ciena Corporation
Cisco Systems
Corning
Credo Semiconductor (HK) LTD
Dell, Inc.
EFFECT Photonics B.V.
Elenion Technologies, LLC
Epson Electronics America, Inc.
eSilicon Corporation
Fiberhome Technologies Group
Finisar Corporation
Foxconn Interconnect Technology, Ltd.
Fujikura
Fujitsu
Furukawa Electric Japan
Global Foundries
Google
Hewlett Packard Enterprise (HPE)
Hitachi
Huawei Technologies Co., Ltd.
IBM Corporation
Infinera
Innovium
Lumentum
MACOM Technology Solutions
Marvell Semiconductor, Inc.
Maxim Integrated Inc.
MaxLinear Inc.
MediaTek
Mellanox Technologies
Microsemi Inc.
Microsoft Corporation
Mitsubishi Electric Corporation
Molex
Multilane SAL Offshore
NEC Corporation
NeoPhotonics
Nokia
NTT Corporation
O-Net Communications (HK) Limited
Oclaro
Optomind Inc.
Orange
PETRA
Precise-ITC, Inc.
Qorvo
Ranovus
Renesas Electronics Corporation
Rianta Solutions, Inc.
Rockley Photonics
Rosenberger Hochfrequenztechnik GmbH & Co. KG
Roshmere
Samtec Inc.
Semtech Canada Corporation
SiFotonics Technologies Co., Ltd.
Sino-Telecom Technology Co., Inc.
Socionext Inc.
Spirent Communications
Sumitomo Electric Industries
Sumitomo Osaka Cement

Inphi
Integrated Device Technology
Intel
Invecas, Inc.
IPG Photonics Corporation
JCRFO
Juniper Networks
Kandou Bus
KDDI Research, Inc.
Keysight Technologies, Inc.
Lightwave Logic
Synopsys, Inc.
TE Connectivity
Tektronix
Telefonica SA
TELUS Communications, Inc.
UNH InterOperability Laboratory (UNH-IOL)
Verizon
Viavi Solutions Deutschland GmbH
Xelic
Xilinx
Yamaichi Electronics Ltd.
ZTE Corporation