Implementation Agreement For Generation 2.0 100G Long-Haul DWDM Transmission Module – Electromechanical (Gen.2 MSA-100GLH)

Premininaly Draft IA # OIF-MSA-100GLH-EM-02.0

Date Approved
August 27, 2013

Implementation Agreement created and approved
by the Optical Internetworking Forum
www.oiforum.com

OPTICAL INTERNETWORKING FORUM

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TITLE: Implementation Agreement for Generation 2.0 100G Long-Haul DWDM Transmission Module – Electromechanical (MSA-100GLH)

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ABSTRACT: This Implementation Agreement specifies key electromechanical aspects of a 100G Long-Haul DWDM Transmission Module, for applications such as 100G PM-QPSK long-haul DWDM transmission. Key aspects include: module mechanical dimensions, electrical connector and pin assignment, module hardware signaling pins, high-speed electrical characteristics, power supply, power dissipation, and management interface.

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DATE: **January 14, 2013**

Revision	***Date***	***Change Notes***	***By***
Premininaly draft	Jan. 14, 2013		
Premininaly draft B	Apr. 23, 2013	Location of PIN A1 indicate in Figure 15, 17 and 19 9.6 Pin Assignment Information delete of Appendix D and E 10.2 Informative references [I5] Revision update to latest version	Atul Srivastava

5 Introduction

This document details an Implementation Agreement (IA) for a Generation 2.0 100G Long-Haul DWDM Transmission Module – Electromechanical (MSA-100GLH) for optical line interface applications. While specifically addressing 100G PM-QPSK long-haul DWDM transmission applications [I1], this IA strives to remain modulation format and data rate agnostic whenever practical to maximize applicability to future market requirements.

This IA specifies key electromechanical aspects of the Generation 2.0 100G Long-Haul DWDM Transmission Module (hereafter termed MSA-100GLH) that include the following: module mechanical dimensions, electrical connector and pin map, module hardware signaling pins, high-speed electrical characteristics, power supply, power dissipation, and management interface.

6 Functional Description

A functional block diagram of the MSA-100GLH is illustrated in Figure 1: Generation 2.0 100G Long-Haul DWDM Transmission Module (MSA-100GLH) Functional Diagram

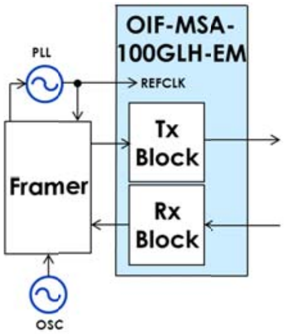


Figure 1A: Application Diagram 1 for 1 MSA Transponder w **Framer**

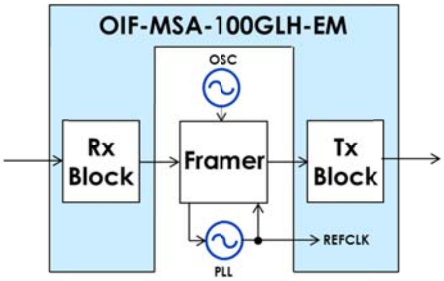


Figure **1B: Application Diagram 2 for 1 MSA Re-generator w Framer**

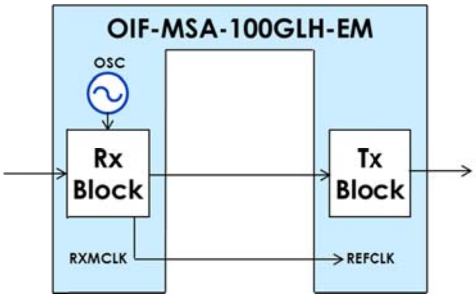


Figure 1C: Application Diagram 3 for 1 MSA Re-generator w/o Framer

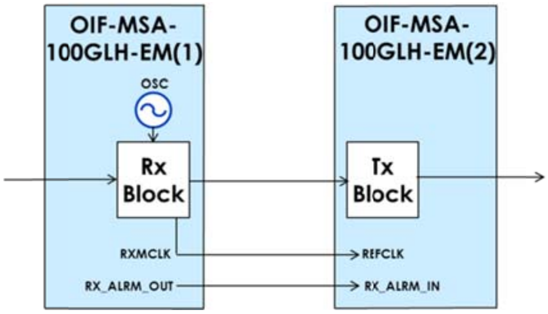
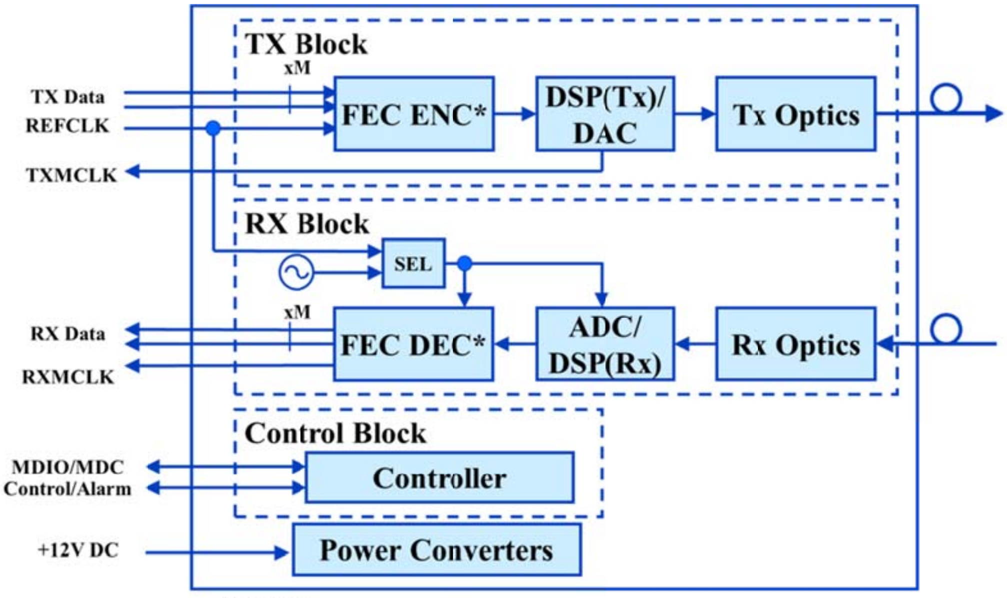


Figure 1D: Application Diagram 4 for 2 MSA Re-generator w/o Framer

Note: In normal operation, Tx have to use Rx recovered clock for REFCLK in Figure 1C and 1D.

. Key module functions include transmitter optics, receiver optics, interface ICs, module controller supporting an MDIO/MDC management interface, and power conversion for a single +12V DC power supply from the host. The MSA-100GLH is not hot pluggable, but is fastened to the host system board during line card assembly. The interface IC(s) and module electrical interface are generically specified to allow vendor specific customization of multilane “M-lane” ~ 11 Gbit/s interfaces. Module electrical interfaces include but are not limited to the following:

a) Simple bit multiplex
b) OTL4.10 [I2]
c) SFI-S [I3]
~~d) OTL3.4 [I2] (for 40G applications, see informative Appendix D)~~



*Optional

Figure 1: Generation 2.0 100G Long-Haul DWDM Transmission Module (MSA-100GLH) Functional Diagram

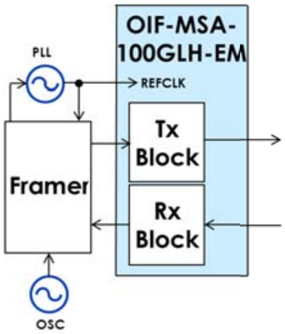


Figure 1A: Application Diagram 1 for 1 MSA Transponder w Framer

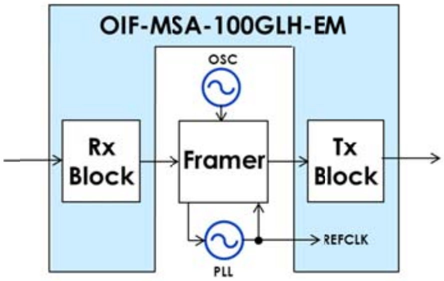


Figure 1B: Application Diagram 2 for 1 MSA Re-generator w Framer

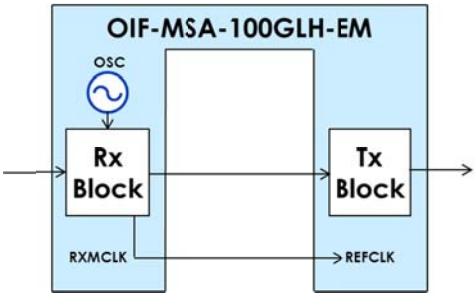


Figure 1C: Application Diagram 3 for 1 MSA Re-generator w/o Framer

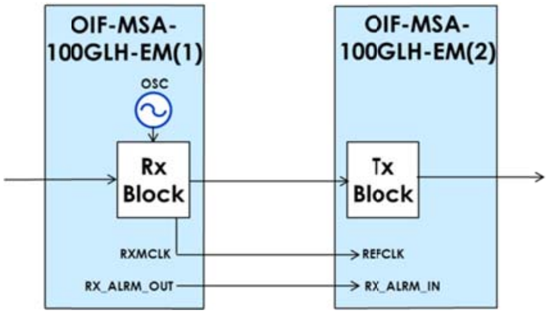


Figure 1D: Application Diagram 4 for 2 MSA Re-generator w/o Framer

Note: In normal operation, Tx have to use Rx recovered clock for REFCLK in Figure 1C and 1D.

7 Module Management Interface Description

The MSA-100GLH utilizes MDIO IEEE 802.3 Clause 45 [N1] for its management interface. The MSA-100GLH MDIO hardware implementation is specified in Section 8.6. The MSA-100GLH MDIO register set specifications are defined in [I5]. When multiple MSA-100GLH are connected via a single bus, a particular MSA-100GLH may be selected by using the MDIO Physical Port Address pins.

8 Electrical Specifications

8.1 Operating Case Temperature

The MSA-100GLH operating case temperature is specified in Table 1.

8.2 Electrical Power Supply and Power Dissipation

The MSA-100GLH is powered by a single +12V DC supply from the host board. This power supply is specified in Table 1. All voltages are measured at the electrical connector interface.

The MSA-100GLH power dissipation is specified in Table 1.

Table 1: MSA-100GLH Performance Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
+12V DC Supply Voltage	V_{CC}	11.4	12.0	12.6	V	+/- 5%
+12V DC Supply Current	I_{CC}			4.0	A	Notes 1 & 2
Power Supply Noise	V_{rip}			1	%p-p	1Hz – 20MHz
Power Dissipation	P_w			45	W	
Operating Case Temperature		0		70	°C	

Note: The parameter min and max values are specified End-of-Life within the overall relevant operating case temperature range. The typical values are referenced to +25°C, nominal power supply, Beginning-of -Life.

Note 1: Maximum current per pin shall not exceed 750mA.

Note 2: Icc max specified for current rating purposes. Normal operating current (Icc) must not exceed Pw / Vcc.

8.3 High Speed Pin Electrical Specifications

8.3.1 Transmitter Data (TX)

The Transmitter Data (TX) signals shall comply with CEI-11G-MR Low Swing option as per Clauses 9.3.1. and 9.3.1.2 [N2]. Full Swing support is not required. The recommended termination of the TX pins is given in Figure 2.

8.3.2 Receiver Data (RX)

The Receiver Data (RX) signals shall comply with CEI-11G-MR Clause 9.3.3 [N2]. The recommended termination of the RX pins is given in Figure 2.

8.3.3 Reference Clock (REFCLK)

The host shall supply a reference clock (REFCLK) at 1/16 of the electrical lane rate. The host shall optionally supply a reference clock (REFCLK) at 1/64 of the electrical lane rate.

The REFCLK shall be CML differential AC coupled and terminated with 50 Ohm internal V_{TT} within the MSA-100GLH, as shown in Figure 2. A frequency locked relationship is required between the transmit data lanes (TX/TXDSC) and the reference clock (REFCLK). There is no required phase relationship between the data lanes and the reference clock. The REFCLK frequency shall not deviate from nominal by more than ±20 ppm. Detailed reference clock characteristics for the MSA-100GLH are given in Table 2.

Table 2: MSA-100GLH Reference Clock (REFCLK) Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Impedance	Z_d	80	100	120	Ω	
Frequency	f		1/16			Of electrical lane rate - default
			1/64			Of electrical lane rate - optional
Frequency Stability	Δf	-20		+20	ppm	
Differential Voltage	V_{DIFF}	400		1600	mV	Peak-to-Peak Differential
Clock Duty Cycle	CDC	40		60	%	
Clock Rise/Fall Time	$t_{r/f}$	200		1250	ps	1/64 electrical lane rate
		50		315	ps	1/16 electrical lane rate

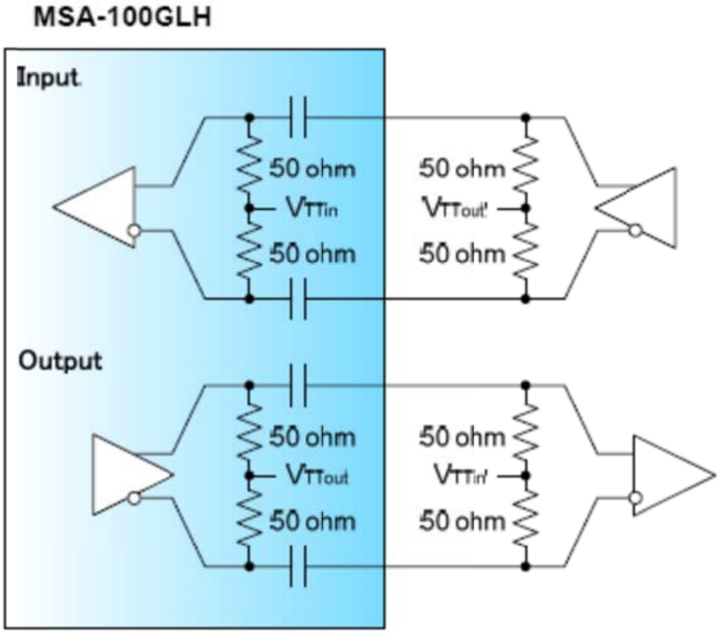


Figure 2: High Speed I/O for Data and Clocks

8.3.4 Transmitter Monitor Clock (TXMCLK)

The MSA-100GLH optionally may supply a transmitter monitor clock (TXMCLK). This clock is intended to be used as a reference for measurements of the module optical transmit signal. If provided, the clock shall operate at 1/8 of the transmitter optical symbol rate for 32Gb applications[1]. This rate is optimized for triggering high-speed sampling scopes. Clock termination is shown in Figure 2. TXMCLK characteristics are summarized in Table 3.

8.3.5 Receiver Monitor Clock (RXMCLK)

The MSA-100GLH optionally may supply a receiver monitor clock (RXMCLK). This clock is intended to be used as a reference for measurements of the module receive data. If provided, the clock shall operate at 1/16 of the receiver electrical lane data rate. The RXMCLK may optionally operate at 1/64 of the receiver electrical lane data rate. Clock termination is shown in Figure 2. RXMCLK characteristics are summarized in Table 3.

Table 3: Optional TXMCLK and RXMCLK Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Impedance	Z_d	80	100	120	Ω	
Frequency - TXMCLK			1/8			Of TX optical symbol rate - default
Frequency - RXMCLK			1/16			Of RX electrical lane data rate - default
			1/64			Of RX electrical lane data rate - optional
Output Differential Voltage	V_{DIFF}	400		1600	mV	Peak-to-Peak Differential
Clock Duty Cycle	CDC	40		60	%	

8.4 Control Pins (non-MDIO) Functional Description

The control functions between a host and a MSA-100GLH are conducted through a set of dedicated, non-data hardware signal pins on the 168-pin electrical connector and via an MDIO interface. The signal pins work together with the MDIO interface to form a complete HOST/MSA-100GLH management interface. Upon module initialization, the control functions are available. Pins allocated to control functions in the 168-pin electrical connector are listed in Table 4.

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[1] For 40G applications, other clock rates may be necessary for operating with available test equipment.

Table 4: MSA-100GLH Control Pins (non-MDIO)

Pin #	Symbol	Description	I/O	Logic	"H"	"L"	Pull-up /down
B20	PRG_CNTL1	Programmable Control 1 Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled	I	3.3V LVCMOS	Per MDIO document		Pull-Up[1]
B19	PRG_CNTL2	Programmable Control 2 For Future Use	I	3.3V LVCMOS			Pull-Up[1]
B18	PRG_CNTL3	Programmable Control 3 For Future Use	I	3.3V LVCMOS			Pull-Up[1]
B13	PM_SYNC	Performance Monitoring Sync Rising edge synchronizes PM statistics counters	I	3.3V LVCMOS			Pull-Down[2]
B11	TX_DIS	Transmitter Disable "0": transmitter enabled "1" or NC: transmitter disabled	I	3.3V LVCMOS	Disable	Enable	Pull-Up[1]
B10	MOD_LOPWR	Module Low Power "0": power-on enabled "1" or NC: module in low power (safe) mode	I	3.3V LVCMOS	Low Power	Enable	Pull-Up[1]
B9	MOD_ RSTn	Module Reset "0": resets the module "1": module enabled	I	3.3V LVCMOS	Enable	Reset	Pull-Down[2]

Note 1: Pull-Up resistor (4.7k - 10kOhm) is located within the MSA-100GLH.
Note 2: Pull-Down resistor (4.7k - 10kOhm) is located within the MSA-100GLH.

8.4.1 Programmable Control Pins (PRG_CNTLs)

The Programmable Control pins (PRG_CNTL) allow the host to program certain MSA-100GLH control functions via a hardware pin. The intention is to allow for maximum design and debug flexibility. The default setting for Control 1 is control of the Transmit & Receive Reset. Controls 2 and 3 are for future use.

8.4.1.1 Programmable Control 1 Pin (PRG_CNTL1)

Programmable Control 1 Pin (PRG_CNTL1) is an input pin from the host, operating with programmable logic. It is pulled up in the MSA-100GLH. It can be re-programmed over MDIO registers to another MDIO control register while the module is in any steady state except Reset. The default function is Transmit & Receive circuitry reset (TRXIC_RSTn) with active-low logic. When TRXIC_RSTn is asserted (driven low), the digital transmit and receive circuitry is reset clearing all FIFOs and/or resetting all CDRs. When de-asserted, the digital transmit and receive circuitry shall resume normal operation.

8.4.1.2 Programmable Control 2 Pin (PRG_CNTL2)

Programmable Control 2 Pin (PRG_CNTL2) is an input from the host, operating with programmable logic. It is pulled up in the MSA-100GLH. It can be re-programmed over MDIO registers to another MDIO control register while the module is in any steady state except Reset. It is reserved for future use.

8.4.1.3 Programmable Control 3 Pin (PRG_CNTL3)

Programmable Control 3 Pin (PRG_CNTL3) is an input from the host, operating with programmable logic. It is pulled up in the MSA-100GLH. It can be re-programmed over MDIO registers to another MDIO control register while the module is in any steady state except Reset. It is reserved for future use.

8.4.1.4 Performance Monitoring Synchronization (PM_SYNC)

The Performance Monitoring Synchronization pin (PM_SYNC) is an input from the host. The purpose of this pin is to provide a synchronization pulse from the host time reference source for synchronizing module-level performance monitoring data collection with host system performance monitoring data collection. The default time period of this signal is 1 second. Use of PM_SYNC is optional for the MSA-100GLH.

8.4.1.5 Transmitter Disable Pin (TX_DIS)

The Transmitter Disable pin (TX_DIS) is an input from the host, operating with active-high logic. This pin is pulled up in the MSA-100GLH. When TX_DIS is asserted, all of the optical outputs inside a MSA-100GLH shall be switched off. When this pin is de-asserted, optical transmitters shall be switched on according to a predefined TX power-on process defined by module vendor specification. The timing diagram for TX_DIS pin is illustrated in Figure 3. Values for t_off and t_on are application specific and not specified in this IA.

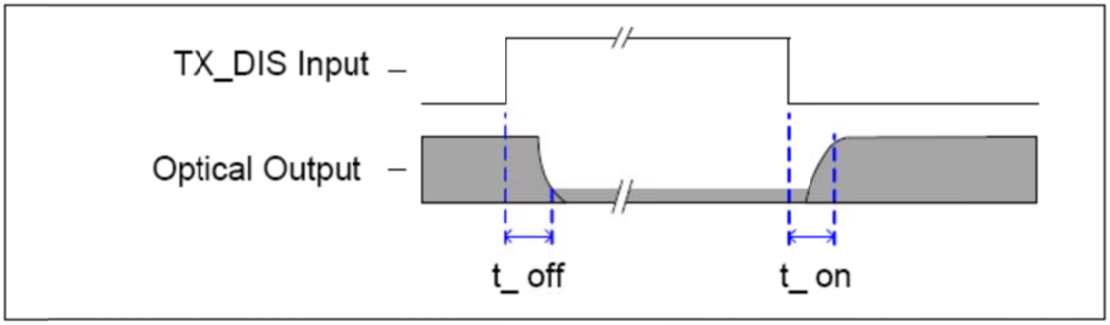


Figure 3: Transmitter Disable (TX_DIS) Timing Diagram

8.4.1.6 Module Low Power Pin (MOD_LOPWR)

The Module Low Power pin (MOD_LOPWR) is an input from the host, operating with active-high logic. It is pulled up in the MSA-100GLH. When MOD_LOPWR is asserted, the MSA-100GLH shall be in the low power state and will stay in the low power state as long as it is asserted. When de-asserted, the MSA-100GLH shall initiate the High-Power-Up process.

In Low Power mode, the MSA-100GLH shall communicate via the MDIO management interface. While the module is in Low Power mode, it has a maximum power consumption of 6W.

The timing diagram for the MOD_LOPWR pin is illustrated in Figure 4. Values for t_MOD_LOPWR_on and t_ MOD_LOPWR_off are application specific and not specified in this IA.

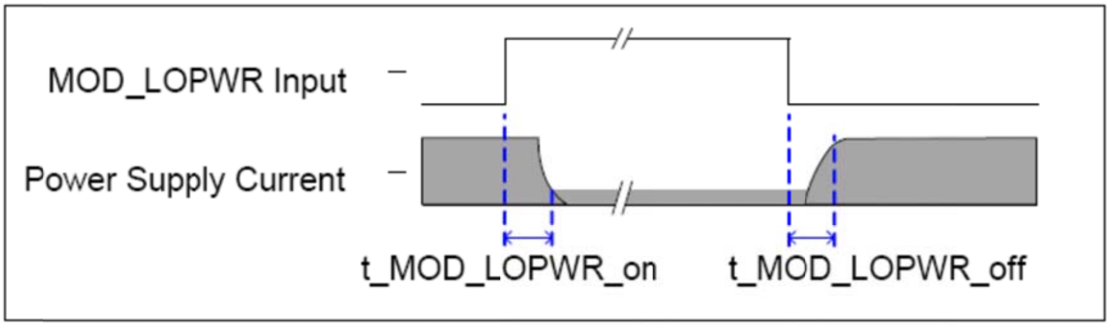


Figure 4: Module Low Power (MOD_LOPWR) Timing Diagram

8.4.1.7 Module Reset Pin (MOD_RSTn)

The Module Reset pin (MOD_RSTn) is an input from the host, operating with active-low logic. This pin is pulled down in the MSA-100GLH. When MOD_RSTn is asserted (driven low), the MSA-100GLH enters the Reset state. When de-asserted, the MSA-100GLH exits the Reset state and shall begin an initialization process as part of the overall module start-up sequence.

8.5 Alarm Pins (non-MDIO) Functional Description

Alarm indications from the MSA-100GLH to the host are conducted through a set of dedicated, non-data hardware signal pins on the 168-pin electrical connector and via an MDIO interface. The signal pins work together with the MDIO interface to form a complete HOST/MSA-100GLH management interface. Upon module initialization, the alarm indication functions are available. Pins allocated to alarm functions in the 168-pin electrical connector are listed in Table 5**.**

Table 5: MSA-100GLH Alarm Pins (non-MDIO)

Pin #	Symbol	Description	I / O	Logic	"H"	"L"	Pull-up/down
B16	PRG_ALRM1	Programmable Alarm 1 set over MDIO	O	3.3V LVCMOS			
B15	PRG_ALRM2	Programmable Alarm 2 set over MDIO	O	3.3V LVCMOS			
B14	PRG_ALRM3	Programmable Alarm 3 set over MDIO	O	3.3V LVCMOS			
B8	RX_LOS	Receiver Loss of Signal	O	3.3V LVCMOS	LOS	OK	
A78	MOD_ABS	Module Absent "0": module present "1" or NC: module absent	O	GND	Absent	Present	Pull-Down[1]
B7	GLB_ALRMn	Global Alarm	O	3.3V LVCMOS w/ Open Drain	OK	Alarm	Note 2
A11	RX_ALRM_OUT	Receiver Alarm transfer output for Re-generator mode	O	3.3V LVCMOS	Alarm	OK	
A12	RX_ALRM_IN	Receiver Alarm transfer input for Re-generator mode	I	3.3V LVCMOS	Alarm	OK	

Note 1: Pull-down resistor (<100Ohm) is located within the MSA-100GLH. A Pull-Up resistor should be located on the host.

Note 2: Pull-Up resistor on host.

8.5.1 Programmable Alarm Pins (PRG_ALRMs)

The Programmable Alarm pins enable the host system to program MSA-100GLH supported alarms to dedicated hardware pins.

8.5.1.1 Programmable Alarm 1 Pin (PRG_ALRM1)

Programmable Alarm 1 Pin (PRG_ALRM1) is an output to the host, operating with programmable logic. It can be re-programmed over MDIO registers to another MDIO alarm register while the MSA-100GLH is in any steady state except Reset. The default function is High Power On (HIPWR_ON) indicator with active-high logic.

8.5.1.2 Programmable Alarm 2 Pin (PRG_ALRM2)

Programmable Alarm 2 Pin (PRG_ALRM2) is an output to the host, operating with programmable logic. It can be re-programmed over MDIO registers to another MDIO alarm register while the MSA-100GLH is in any steady state except Reset. The default function is Module Ready (MOD_READY) indicator with active-high logic.

The default function MOD_READY is used by the MSA-100GLH during the module initialization. When asserted, it indicates the MSA-100GLH has completed the necessary initialization process and is ready to transmit and receive data.

8.5.1.3 Programmable Alarm 3 Pin (PRG_ALRM3)

Programmable Alarm 3 Pin (PRG_ALRM3) is an output to the host, operating with programmable logic. It can be re-programmed over MDIO registers to another MDIO alarm register while the MSA-100GLH is in any steady state except Reset. The default function is Module Fault (MOD_FAULT) indicator with active-high logic.

The default function MOD_FAULT is used by the MSA-100GLH during module initialization. When asserted, it indicates the MSA-100GLH has entered into a fault state.

8.5.2 Receiver Loss of Signal Pin (RX_LOS)

The Receiver Loss of Signal pin (RX_LOS) is an output to the host, operating with active-high logic. When asserted, it indicates received optical power in the MSA-100GLH is lower than the expected value. The optical power at which RX_LOS is asserted is application specific and specified by the host system or module vendor. The timing diagram for the RX_LOS pin is illustrated in Figure 5. Values for t_loss_on and t_ loss_off are application specific and not specified in this IA.

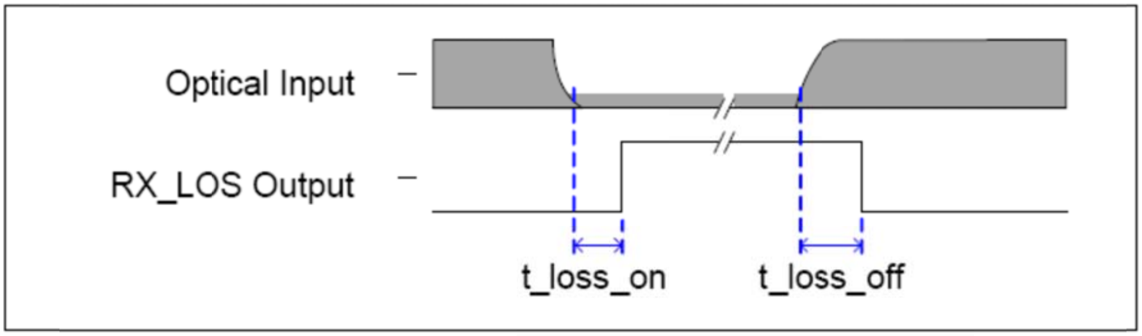


Figure 5: Receiver Loss of Signal (RX_LOS) Timing Diagram

8.5.3 Module Absent Pin (MOD_ABS)

The Module Absent (MOD_ABS) pin is an output from the MSA-100GLH to the host. It is pulled up on the host board and is pulled down to ground in the MSA-100GLH. MOD_ABS asserts a “Low” condition when the MSA-100GLH is plugged into a host socket. MOD_ABS is asserted “High” when the MSA-100GLH is physically absent from a host socket.

8.5.4 Global Alarm Pin (GLB_ALRMn)

The Global Alarm pin (GLB_ALRMn) is an output to the host, operating with active-low logic. When GLB_ALRMn is asserted (driven low), it indicates that a Fault/Alarm/Warning/Status (FAWS) condition has occurred. It is driven by the logical OR of all fault, alarm, warning and status conditions latched in the latched registers. Masking Registers are provided so that GLB-ALRMn may be programmed to assert only for specific fault/alarm/warning/status conditions. It is recommended that the host board be designed to support high-priority event handling service to respond to the assertion of this pin. Upon the assertion of this pin, the host event handler identifies the source of the fault by reading the latched registers over the MDIO interface. The reading action clears the latched registers, which in turn causes the MSA-100GLH to de-assert (driven high) the GLB_ALRMn pin.

The timing diagram for the GLB_ALRMn pin is illustrated in Figure 6. Values for t_GLB_ALRM_on and t_ GLB_ALRMn_off are application specific and not specified in this IA.

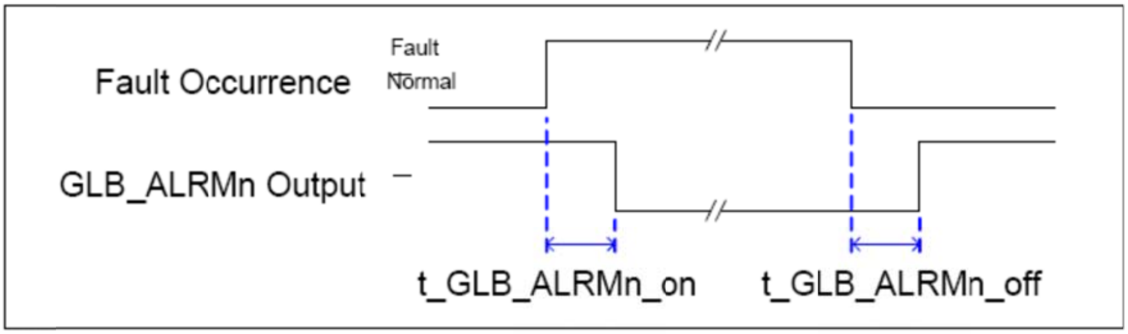


Figure 6: Global Alarm (GLB_ALRMn) Timing Diagram

Note: In this Figure the Fault Occurrence is shown transitioning to a "Normal" status. In order for this transition to occur, a read of the alarm register must have occurred such that the fault has been received.

8.5.5 Receiver Alarm transfer output for Re-generator mode Pin (RX_ALRM_OUT)

The Receiver Alarm transfer output for Re-generator mode Pin (RX_ALRM_OUT) is an output to another connected MSA-100GLH for Re-generator application, operating with active-low logic. When RX_ALRM_OUT is asserted (driven low), it indicates that condition such as a Loss Of Signal/Loss Of Frame has occurred at RX. The timing diagram for the RX_ALRM_OUT pin is application specific and not specified in this IA.

8.5.6 Receiver Alarm transfer input for Re-generator mode Pin (RX_ALRM_IN)

The Receiver Alarm transfer input for Re-generator mode Pin (RX_ALRM_IN) is an input from another connected MSA-100GLH for Re-generator application, operating with active-low logic. When RX_ALRM_IN is asserted (driven low), the MSA-100GLH shall generate AIS(Alarm Indication Signal) condition, or similar signal at the TX. The timing diagram for the RX_ALRM_IN pin is application specific and not specified in this IA.

8.6 Module Management Interface Pins (MDIO) Description

The MSA-100GLH supports control, alarm and monitoring functions via dedicated hardware pins and via an MDIO bus. The MSA-100GLH MDIO electrical interface consists of 7 pins: 1 pin for MDIO, 1 pin for MDC, and 5 MDIO Physical Port Address pins. MDC is the MDIO clock line driven by the host. MDIO is the bidirectional data line driven by both the host and module, depending upon the data direction. Pins allocated to instantiate the MDIO interface in the MSA-100GLH electrical connector are listed in Table 6.

Table 6: MSA-100GLH MDIO Management Interface Pins

Pin #	Symbol	Description	I/O	Logic	"H"	"L"	Pull-up /down
A28	MDIO	Management Data I/O bi-directional	I/O	1.2V LVCMOS			
A27	MDC	MDIO Clock	I	1.2V LVCMOS			
B21	PRTADR0	MDIO Physical Port Address bit 0	I	1.2V LVCMOS			
B22	PRTADR1	MDIO Physical Port Address bit 1	I	1.2V LVCMOS			
B23	PRTADR2	MDIO Physical Port Address bit 2	I	1.2V LVCMOS			
B24	PRTADR3	MDIO Physical Port Address bit 3	I	1.2V LVCMOS			
B25	PRTADR4	MDIO Physical Port Address bit 3	I	1.2V LVCMOS			

8.6.1 Management Data Input/Output Pin (MDIO)

The MDIO specification is defined in IEEE 802.3 Clause 45 [N1]. The MSA-100GLH shall support 4.0 Mbit/s maximum data rate. The MSA-100GLH uses an MDIO with 1.2V LVCMOS logic.

8.6.2 Management Data Clock Pin (MDC)

The host specifies a maximum MDC rate of 4.0 MHz and MSA-100GLH hence shall support a maximum MDC rate up to 4.0 MHz. The timing diagram for the MDIO and MDC pins is illustrated in Figure 7: Module MDIO & MDC Timing Diagram

The MSA-100GLH shall support a minimal setup (t_{setup}) and hold (t_{hold}) time in its MDIO implementation (see Table 9).

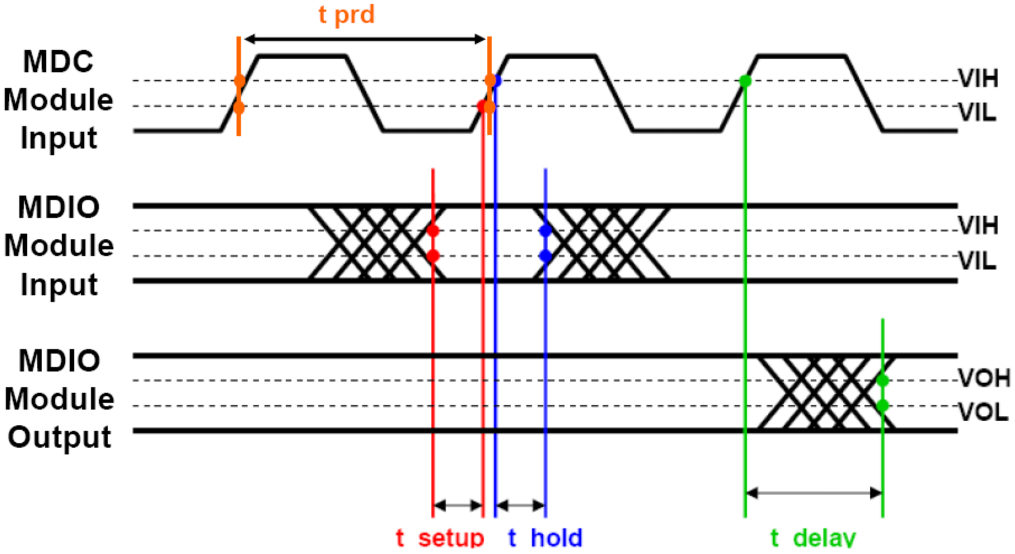


Figure 7: Module MDIO & MDC Timing Diagram

Note: Measured at Module MDIO & MDC pins.

8.6.3 MDIO Physical Port Address Pins (PRTADRs)

The MDIO Physical Port Address pins (PRTADRs) are used by the host system to address all of the MSA-100GLHs contained within its management domain. PRTADR0 corresponds to the LSB in the physical port addressing scheme. The 5-pin Physical Port Address lines are driven by the host to set the module Physical Port Address which should match the address specified in the MDIO Frame. It is recommended that the Physical Port Addresses not be changed while the MSA-100GLH is powered on.

8.7 Hardware Signaling Pin Electrical Specifications

8.7.1 Control & Alarm Pins: 3.3V LVCMOS Electrical Characteristics

The hardware control and alarm pins specified as 3.3V LVCMOS functionality described above shall meet the electrical characteristics described in Table 7. Figure 8 illustrates the recommended reference pin input and output terminations.

Table 7: 3.3V LVCMOS Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	3.2	3.3	3.4	V
Input High Voltage	VIH	2	-	VCC+0.3	V
Input Low Voltage	VIL	-0.3	-	0.8	V
Input Leakage Current	IIN	-10	-	+10	µA
Output High Voltage (I_{OH}=-100 µA)	VOH	VCC-0.2	-	-	V
Output Low Voltage (I_{OL}= 100 µA)	VOL	-	-	0.2	V

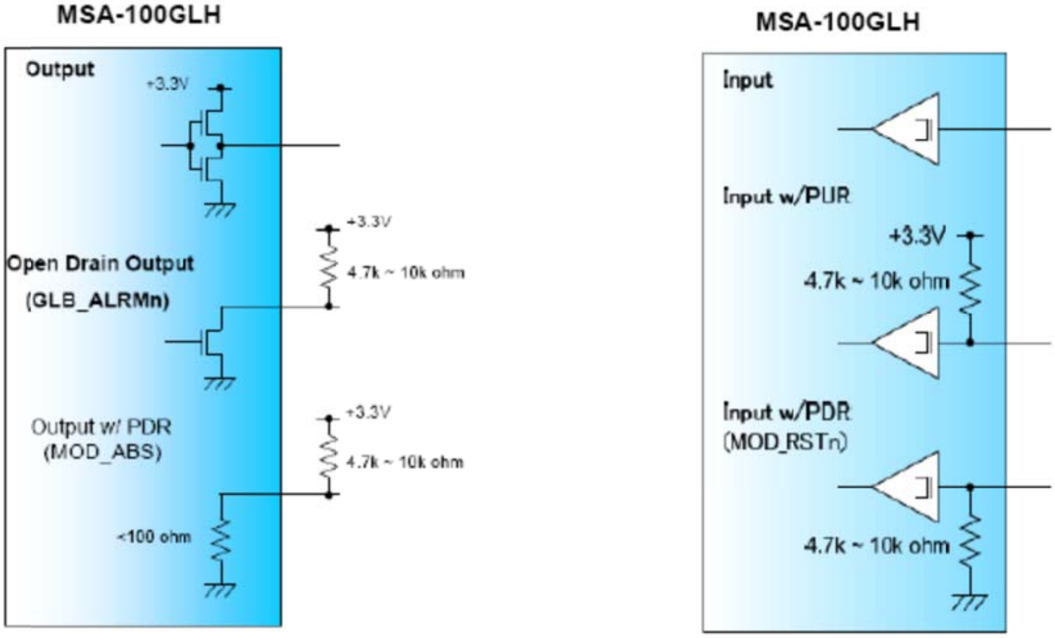


Figure 8: Reference +3.3V LVCMOS Input/Output Terminations

8.7.2 MDIO Interface Pins: 1.2V LVCMOS Electrical Characteristics

The MDIO pins specified as 1.2V LVCMOS functionality described above shall meet the electrical characteristics described in Table 8. Figure 9 illustrates the recommended reference pin input and output terminations.

Table 8: 1.2V LVCMOS Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input High Voltage	VIH	0.84	-	1.5	V
Input Low Voltage	VIL	-0.3	-	0.36	V
Input Leakage Current	IIN	-100	-	+100	µA
Output High Voltage	VOH	1.0	-	1.5	V
Output Low Voltage	VOL	-0.3	-	0.2	V
Output High Current	IOH	-	-	-4	mA
Output Low Current	IOL	+4	-	-	mA
Input Capacitance	Ci	-	-	10	pF

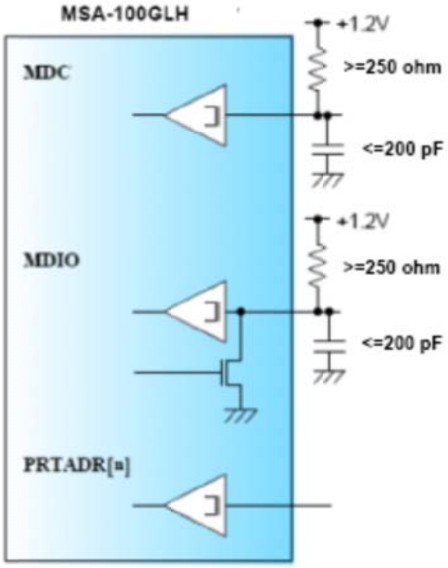


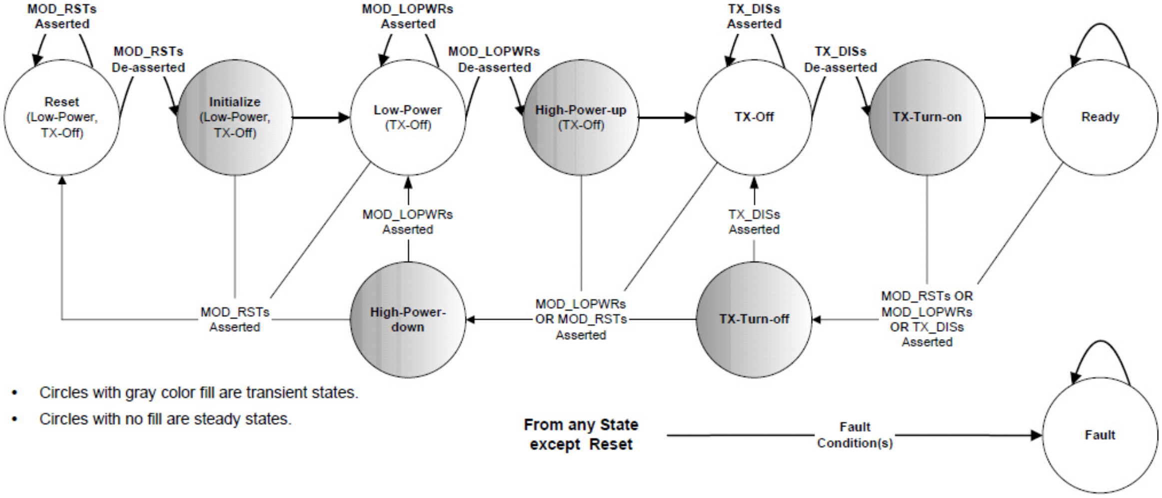
Figure 9: Reference MDIO Interface Termination

Note: MDC pull-up resistor is optional.

Note: Host termination resistor value of 560 Ohms is recommended. This value provides the best balance of performance for both open-drain and active tri-state driver in the module. Host termination resistor values below 560 Ohms are allowed, to a minimum of 250 Ohms, but this degrades driver performance. Host termination resistor values above 560 Ohms are allowed, but this degrades open-drain driver performance.

8.8 Hardware Signaling Pin Timing Specifications

The MSA-100GLH is designed to have a tightly coupled interface with host systems. A simplified overview of the recommended start-up sequence is illustrated in Figure 10. This Figure indicates steady state conditions, transient state conditions and associated signaling flags to indicate state transitions. A complete description is defined in the MDIO management interface specification [I5].



- Circles with gray color fill are transient states.
- Circles with no fill are steady states.

Figure 10: MSA-100GLH Simplified Start-Up Flow Diagram

The MSA-100GLH is designed to support a range of optical transport applications. Many of the timing parameters associated with the module hardware control and alarm pins are application specific and thus are not specified in this IA. A summary of the timing parameters for the MSA-100GLH is given in Table 9.

Table 9: Hardware Signaling Pins Timing Parameters Summary

Parameter	Symbol	Min	Max	Unit	Notes
Transmitter Disabled (TX_DIS asserted)	t_off				Application specific. Defined by module vendor.
Transmitter Enabled (TX_DIS de-asserted)	t_on				Application specific. Defined by module vendor.
MOD_LOPWR on	t_MOD_LOPWR_on				Application specific. Defined by module vendor.
MOD_LOPWR off	t_MOD_LOPWR_off				Application specific. Defined by module vendor.
Module Reset Assert	MOD_RSTn				Application specific. Defined by module vendor.
Module Reset De-assert	MOD_RSTn				Application specific. Defined by module vendor.
Module Absent	MOD_ABS				Application specific. Defined by module vendor.
Receiver Loss of Signal Assert Time	t_loss_on				Application specific. Defined by module vendor.
Receiver Loss of Signal	t_loss_off				Application specific.

De-assert Time					Defined by module vendor.
Global Alarm Assert Delay Time	t_GLB_ALRMn_on				This is a logical "OR" of associated MDIO alarm & status registers. See MDIO spec for details.
Global Alarm De-assert Delay Time	t_GLB_ALRMn_off				This is a logical "OR" of associated MDIO alarm & status registers. See MDIO spec for details.
Management Interface Clock Period	t_{prd}	250		ns	MDC is 4 MHz rate; duty cycle = 50% ± 10% (typ.)
Host MDIO setup time	t_{setup}	10		ns	
Host MDIO hold time	t_{hold}	10		ns	
Module MDIO delay time	t_{delay}		175	ns	
Performance Monitoring Synchronization (PM_SYNC) (optional)					Default period=1 sec. ; min high/low time = 100msec.

9 Mechanical Specifications

9.1 Mechanical Overview

The MSA-100GLH is designed to be assembled into a host system line card. The MSA-100GLH is electrically connected to the host line card by a 168 position connector specified herein and is physically fastened to the host line card by mounting screws through the host line card PCB. The MSA-100GLH supports two optical fiber pigtails, one for optical transmit and one for optical receive. These optical fiber pigtails are terminated and attached to host line card face plate. The MSA-100GLH is not designed to be hot-pluggable. Its power and initialization sequencing in the host line card are specified by the host line card and transponder vendors.

9.2 Electrical Connector

The Hirose FX10A-168P/S-SV(83) connector assembly [N3] is specified for the host line card – MSA-100GLH electrical connector. This connector is a two component (header, receptacle), 168 position, board mounted style assembly. It meets CEI-11G-MR [N2] signal integrity performance and provides 4mm - 8mm mated stack height flexibility by header component changes only, i.e. the MSA-100GLH receptacle component remains fixed. Detailed mechanical specifications and layout design application notes may be found at [N3].

The Hirose FX10B-168P/S-SV(83) connector assembly [N3] is also specified as an option for the host line card – MSA-100GLH electrical connector. The FX10A connector style has guidepost features whereas the FX10B style does not. The FX10A and FX10B components are mate compatible and may be interchanged. Manufacturers can select either FX10A or FX10B version as appropriate for their design flow.

9.2.1 Module Electrical Connector

The MSA-100GLH electrical connector is the Hirose FX10A-168S-SV(83) receptacle connector assembly[N3] illustrated in Figure 11. Pin orientation is also indicated in Figure 11. The Hirose FX10B-168S-SV(83) receptacle is also an option for the MSA-100GLH electrical connector.

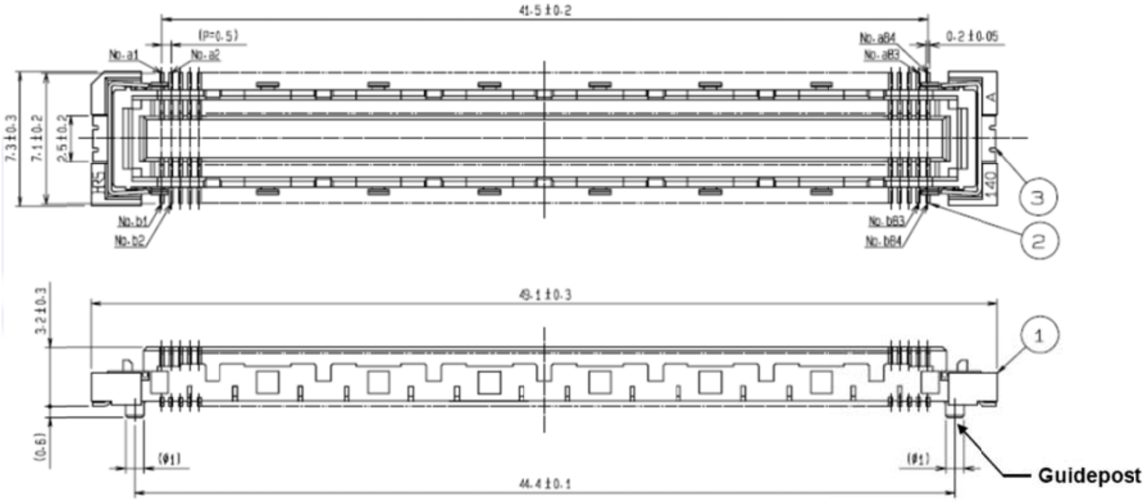


Figure 11: Hirose FX10A-168S-SV(83) Receptacle Connector Assembly

9.2.2 Host Electrical Connector

The host line card electrical connector is the Hirose FX10A-168P-SV(83) header connector assembly[N3] illustrated in Figure 12. Pin orientation is also indicated in Figure 12. The Hirose FX10B-168P-SV(83) header is also an option for the host line card electrical connector.

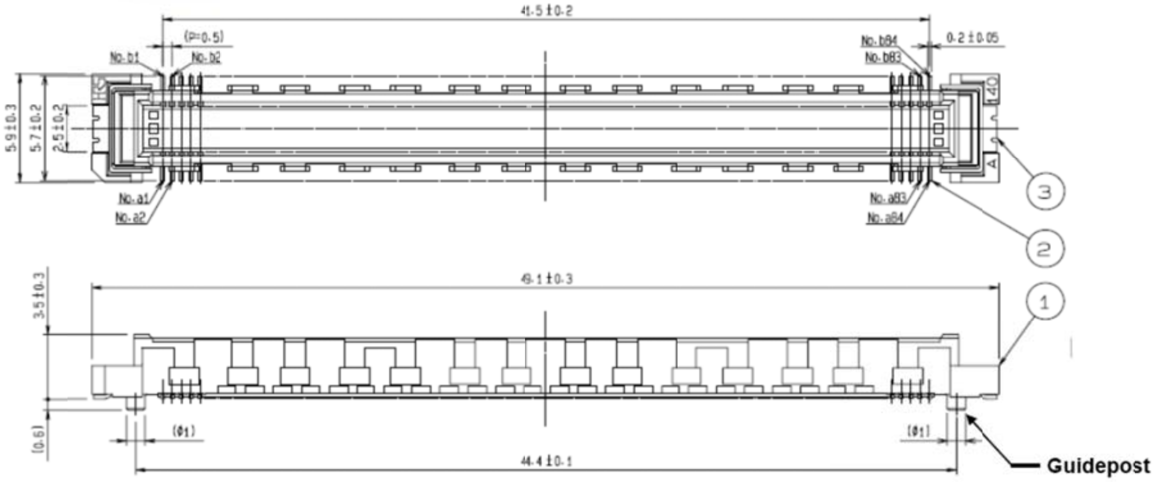


Figure 12: Hirose FX10A-168P-SV(83) Header Connector Assembly

9.2.3 Host-Module Connector Alignment

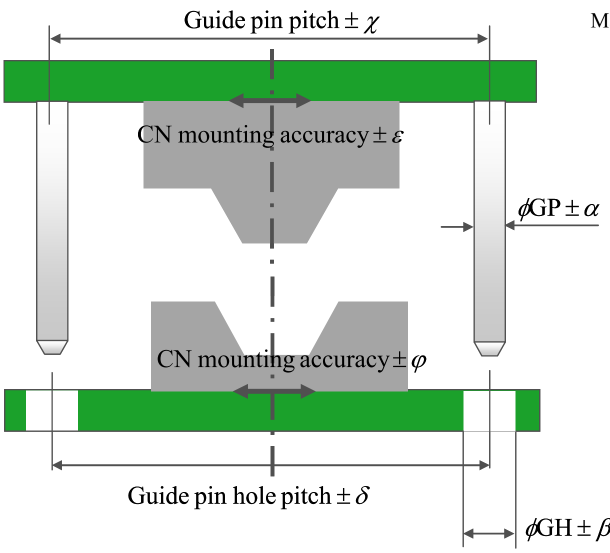
For alignment of host – MSA 100GLH connector mating, misalignment should be smaller that the maximum allowable misalignment value of the connector (CN) mating. Maximum gap between the connector guide pin (GP) and the PCB guide pin hole (GH) is:

$$\text{Maximum Gap} = \frac{\phi GH - \phi GP}{2} \leq \text{Maximum misalignment of the CN}$$

to assure CN mating after inserting guide pins into the guide pin hole. If

$$\text{Maximum Gap} = \frac{\phi GH - \phi GP}{2} \geq \text{Maximum misalignment of the CN}$$

this may cause connector and contact deformation. Tolerance of GP and GH is defined in Figure 13. Maximum allowable misalignment should be ≤0.42mm for FX10.



Maximum Gap should be

Maximum Gap =

$$\frac{(\phi GH-\beta)-(\phi GP+\alpha)}{2} \ge \chi+\delta+\varepsilon+\varphi$$

$$\phi GH \ge \phi GP+(\chi+\delta+\varepsilon+\varphi)\times 2+\alpha+\beta$$

$$\frac{\phi GH-\phi GP}{2} \ge \frac{(\chi+\delta+\varepsilon+\varphi)\times 2+\alpha+\beta}{2}$$

$$\frac{(\chi+\delta+\varepsilon+\varphi)\times 2+\alpha+\beta}{2} \le \text{Maximum misalignment of the CN}$$

$$\frac{(\chi+\delta+\varepsilon+\varphi)\times 2+\alpha+\beta}{2} \le 0.42\ [\text{mm}]$$

Maximum allowable misalignment of the FX10

Figure 13: FX10 Connector Alignment

9.3 Module Dimensions

Two options are specified for the MSA-100GLH mechanical dimensions:

1) Flattop
2) Integrated Heat Sink

The flattop option is specified to allow customization of the MSA-100GLH bolt-on heat sink for supporting a wide array of optical transport applications. With this option, the bolt-on heat sink is specified by the host system designer, allowing maximum flexibility in their system design while maintaining a common module form factor.

The integrated heat sink option is specified to simplify the host system design and supports module thermal performance per the maximum power consumption specified in Section 8.2.

Mechanical dimensions of the MSA-100GLH with non-conductive sheet are specified in Figure 14. If a non-conductive sheet is used, the thickness is specified as 0.15 +/- 0.05mm.

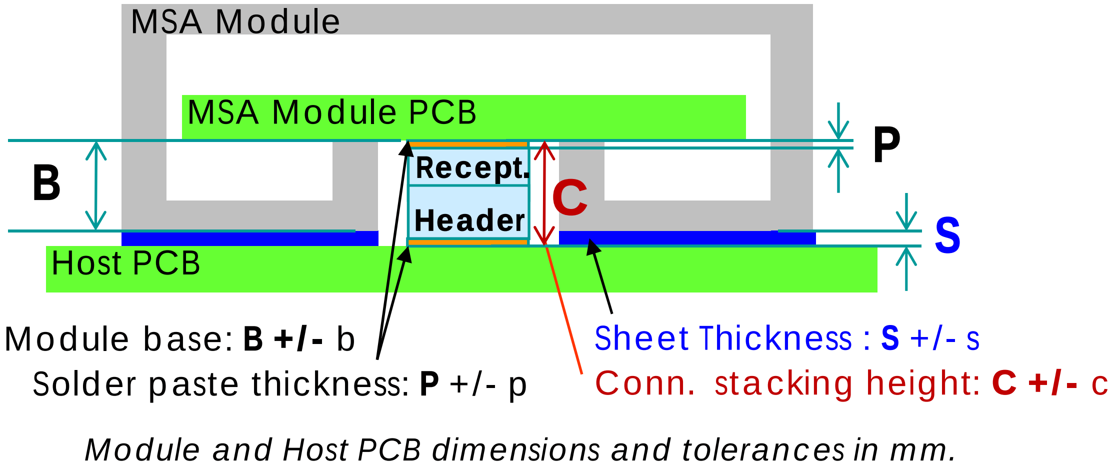


Figure 14: MSA-100GLH Non-conductive Sheet Dimensions

Note: The module vendor must ensure the module connector receptacle component is placed to enable the module to properly mate with the host connector header when the minimum height header component (i.e. C=4mm) is used by the host.

9.3.1 Flattop

Mechanical dimensions of the MSA-100GLH flattop module are specified in Figure 15. The maximum module size is specified as: 101.6mm x 127.0mm (4” x 5”)

Figure 15 also specifies the receptacle connector position, connector guide pin locations and module mounting hole locations.

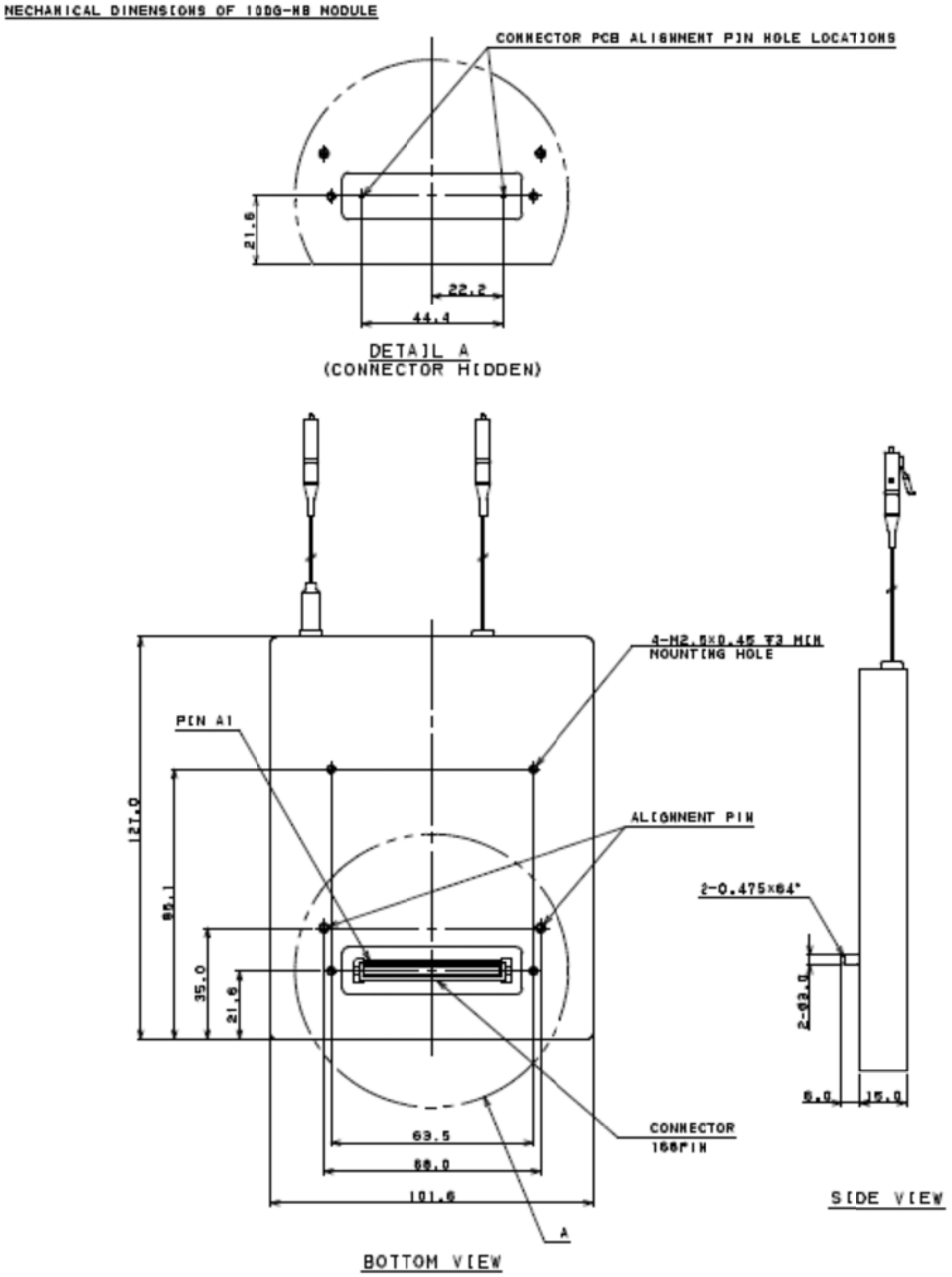


Figure 15: MSA-100GLH Flattop mechanical dimensions - bottom/side views

The module heat sink mounting hole locations for the flattop option are specified in Figure 16. These mounting holes are not applicable to the MSA-100GLH with an integrated heat sink.

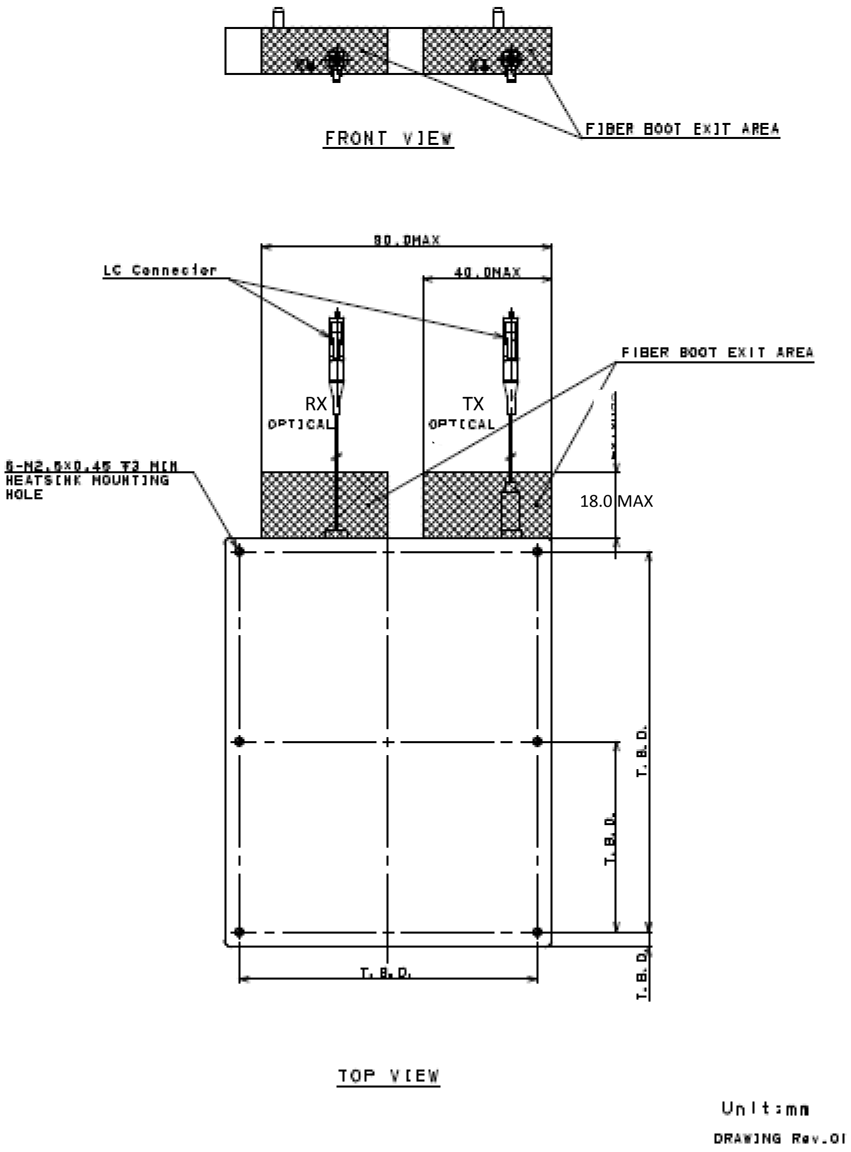


Figure 16: MSA-100GLH Flattop mechanical dimensions - top view

9.3.2 Integrated Heat Sink

Mechanical dimensions of the MSA-100GLH with integrated heat sink are specified in Figure 17. The maximum module size is specified as: 101.6mm x 127.0mm (4” x 5”)

Figure 17 also specifies the receptacle connector position, connector guide pin locations and module mounting hole locations.

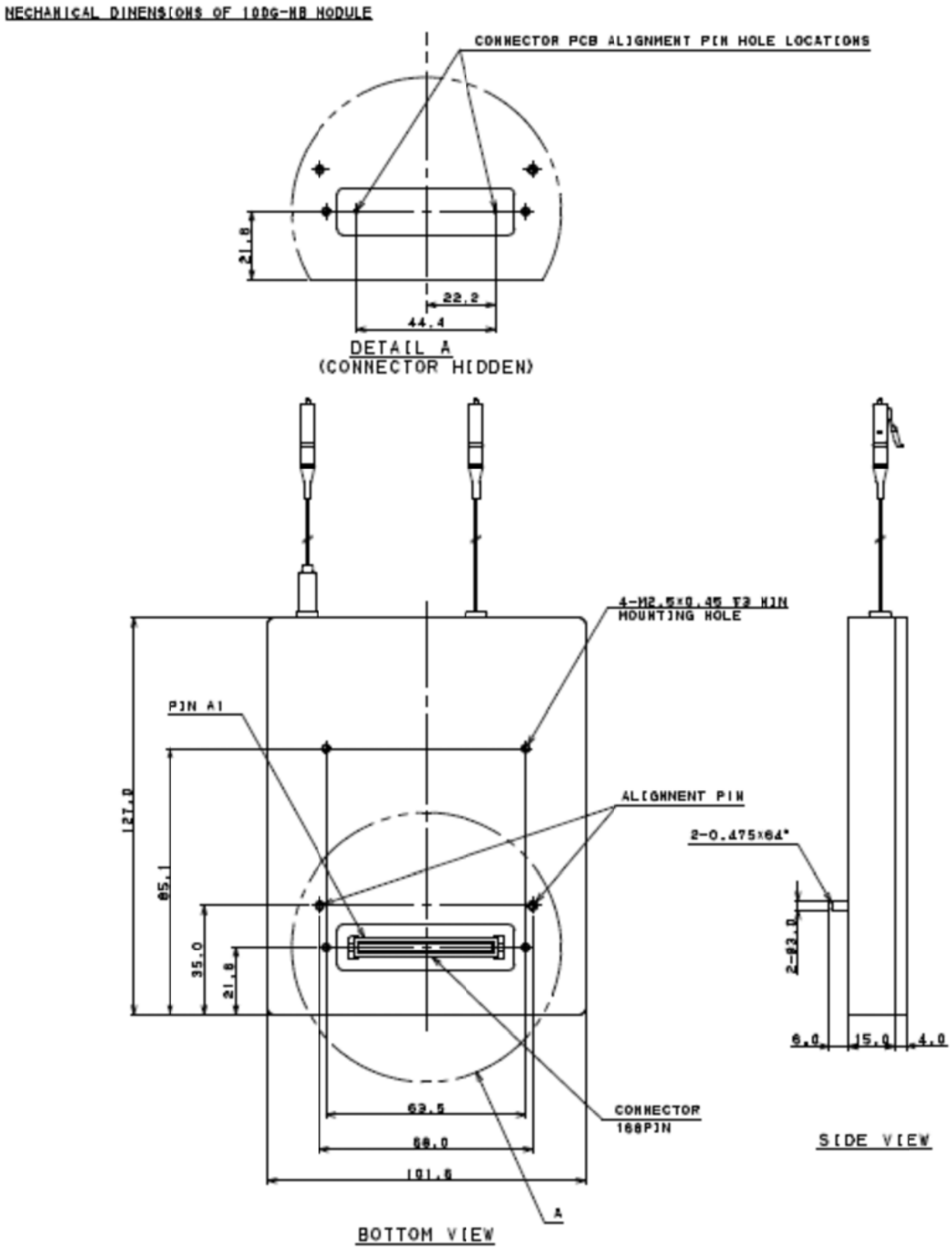


Figure 17: Mechanical Dimensions of MSA-100GLH with Integrated Heat Sink

The top view of the MSA-100GLH is illustrated in Figure 18. The integrated heat-sink fin orientation and dimensions are module-vendor specific and are not specified in this document. However, the module height is required to fit within the maximum height dimension specified in Figure 17.

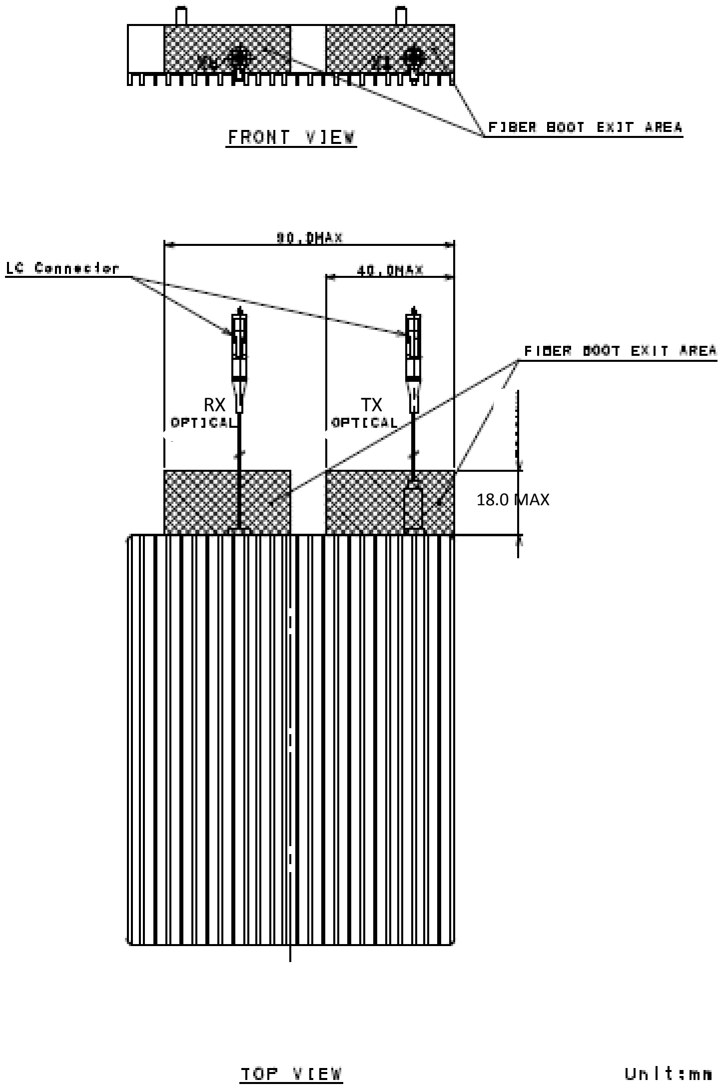


Figure 18: MSA-100GLH with Integrated Heat Sink - top view

9.4 Host System Dimensions

The recommended host system dimensions including host board layout are given in Figure 19. PCB design guidelines for the Hirose FX10 connector assembly may be found at Reference [I4].

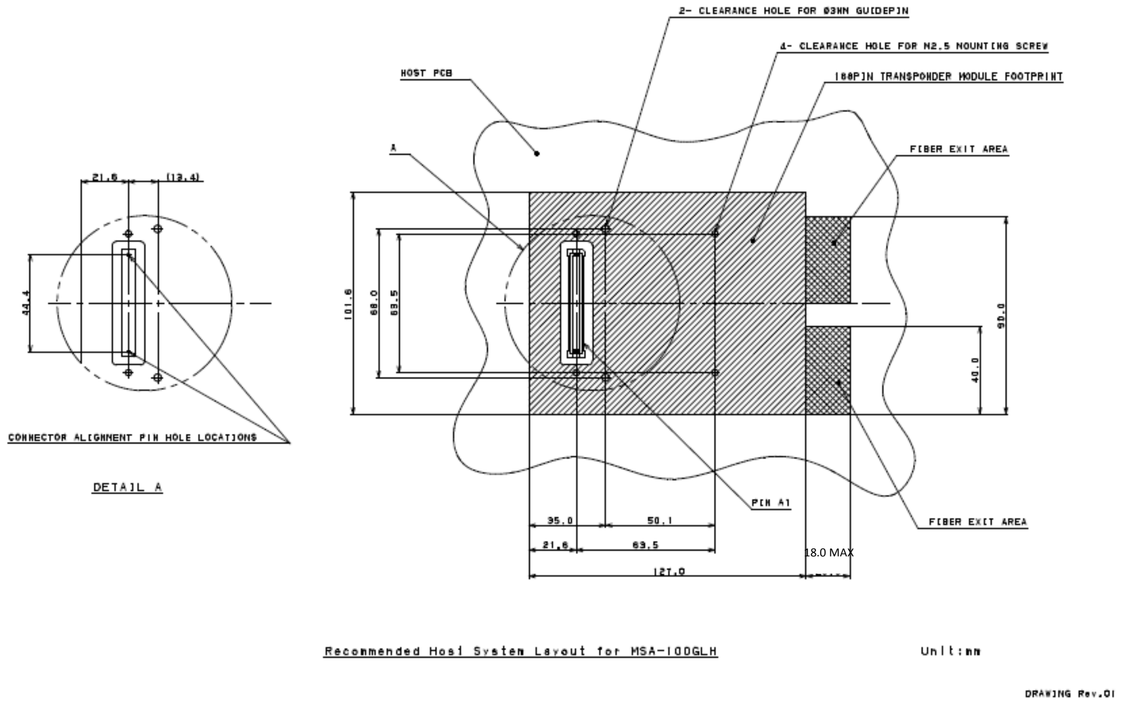


Figure 19: Recommended Host System Layout for MSA-100GLH

9.5 Module Optical Fiber Ports

The MSA-100GLH optical transmit and receive fiber pigtail port location, dimensions and orientation are specified in Figure 20. The fiber pigtail type, length and connector type parameters are vendor specified and not specified in this document. The fiber boot exit area is solely for the purpose of indicating where the fibers are to exit the module side-wall with fiber boots for strain relief.

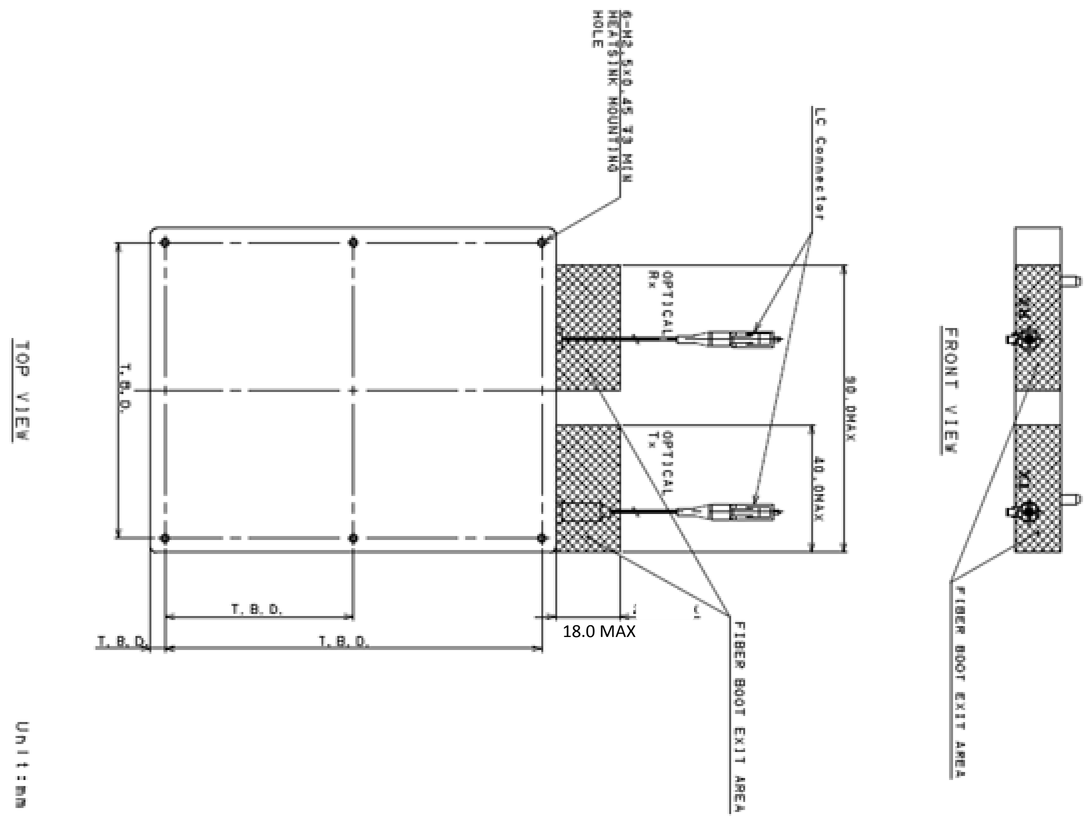
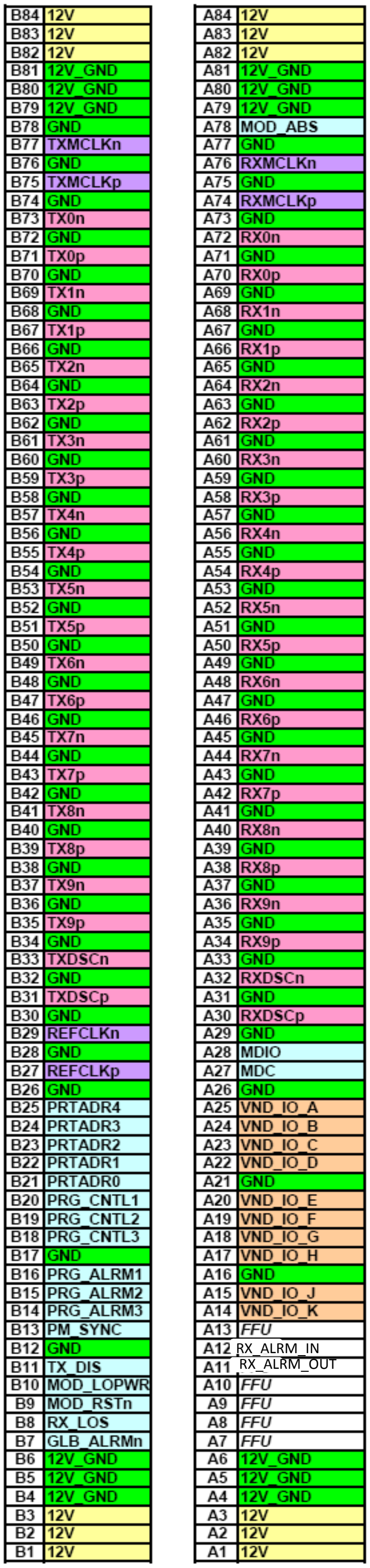


Figure 20: MSA-100GLH Optical Fiber Port Location and Dimensions

9.6 Pin Assignment

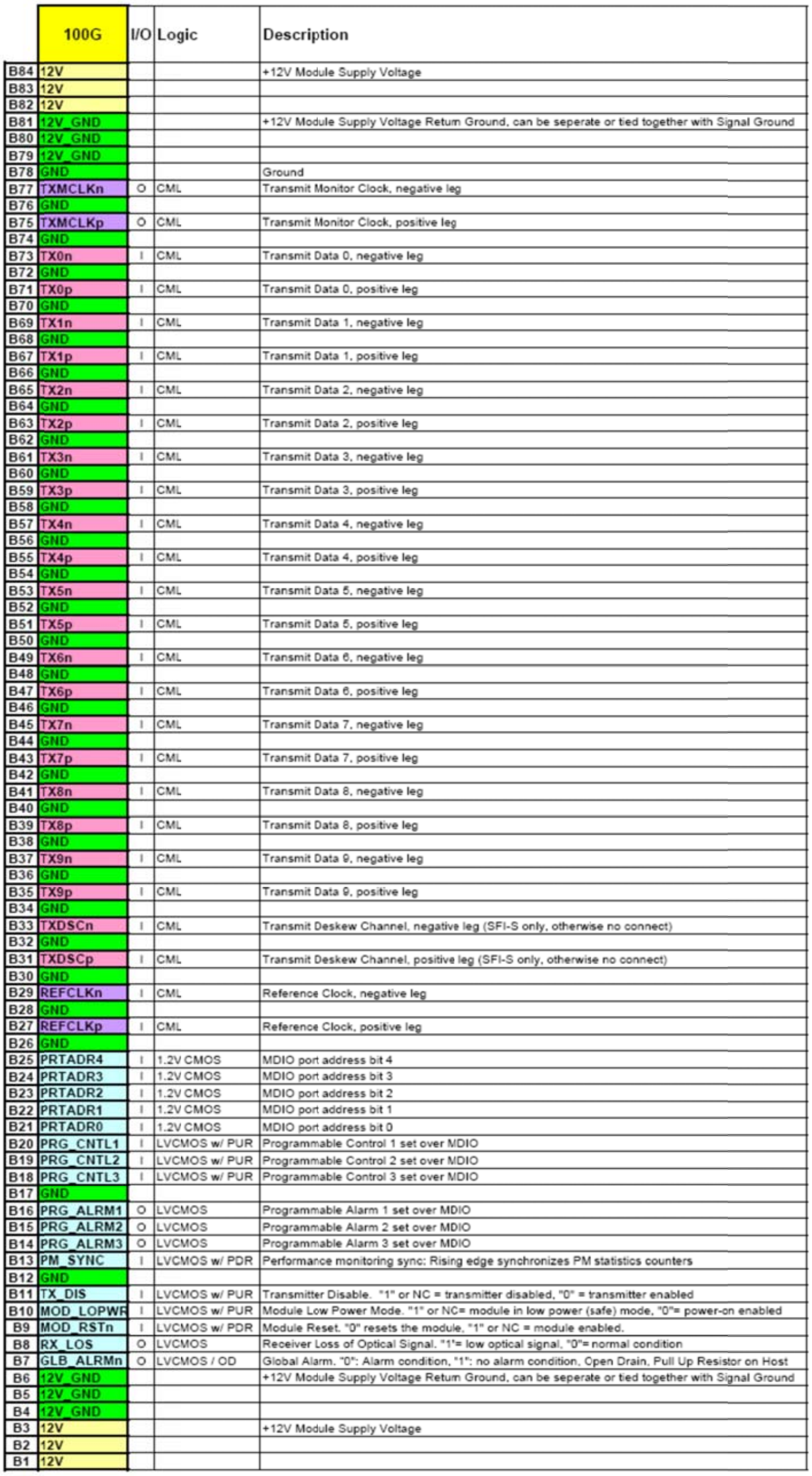
The MSA-100GLH electrical connector has 168 pin positions that are arranged in a dual-row assembly. The pin assignment is specified in Table 10. Detailed description of the pin assignment is given in Table 11 and Table 12. The pin orientation is illustrated in Figure 17.

Table 10: MSA-100GLH Pin-Map (Note: Pins for future use (FFU) should be left unconnected on both the host board and the MSA module)



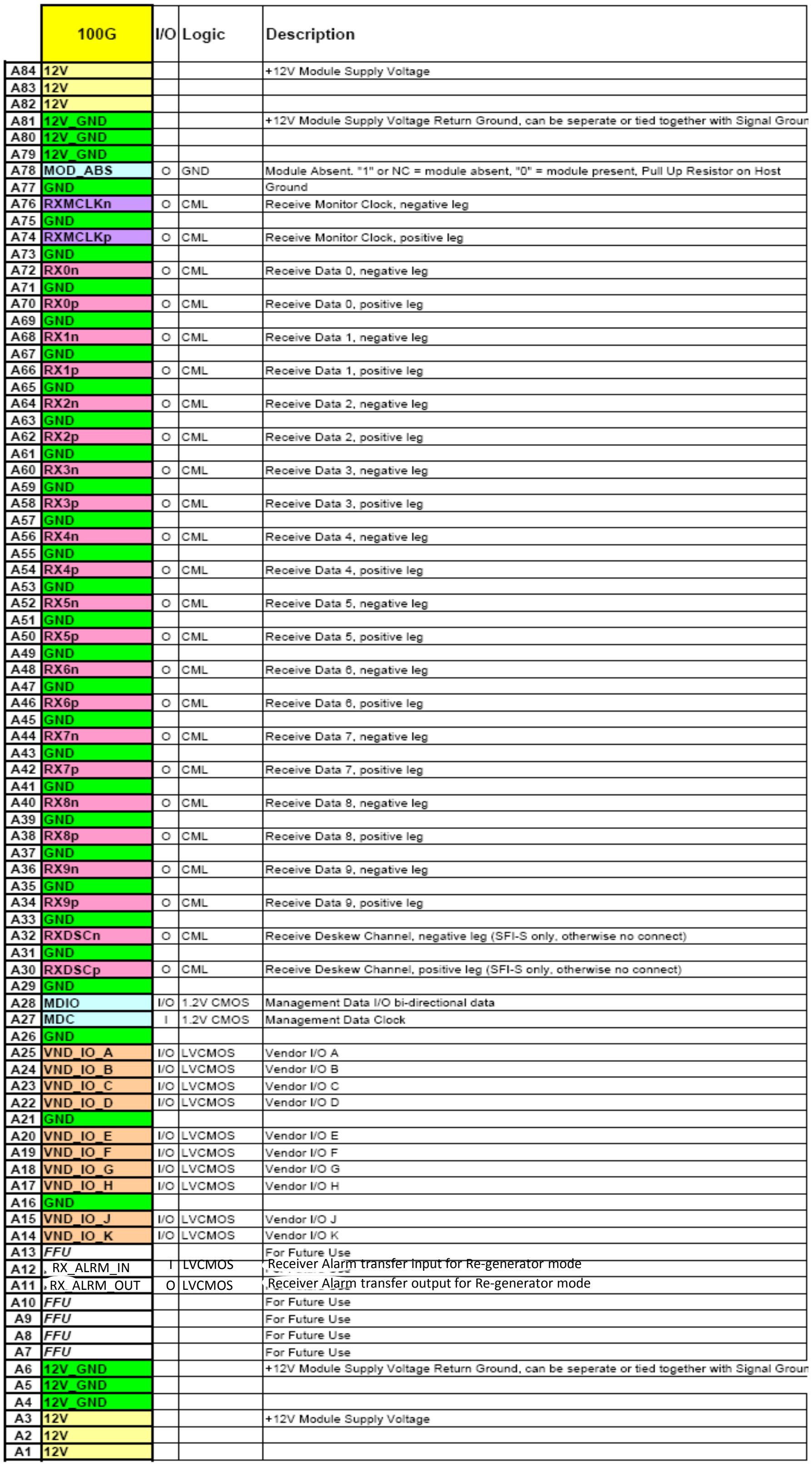
B84	12V	A84	12V
B83	12V	A83	12V
B82	12V	A82	12V
B81	12V_GND	A81	12V_GND
B80	12V_GND	A80	12V_GND
B79	12V_GND	A79	12V_GND
B78	GND	A78	MOD_ABS
B77	TXMCLKn	A77	GND
B76	GND	A76	RXMCLKn
B75	TXMCLKp	A75	GND
B74	GND	A74	RXMCLKp
B73	TX0n	A73	GND
B72	GND	A72	RX0n
B71	TX0p	A71	GND
B70	GND	A70	RX0p
B69	TX1n	A69	GND
B68	GND	A68	RX1n
B67	TX1p	A67	GND
B66	GND	A66	RX1p
B65	TX2n	A65	GND
B64	GND	A64	RX2n
B63	TX2p	A63	GND
B62	GND	A62	RX2p
B61	TX3n	A61	GND
B60	GND	A60	RX3n
B59	TX3p	A59	GND
B58	GND	A58	RX3p
B57	TX4n	A57	GND
B56	GND	A56	RX4n
B55	TX4p	A55	GND
B54	GND	A54	RX4p
B53	TX5n	A53	GND
B52	GND	A52	RX5n
B51	TX5p	A51	GND
B50	GND	A50	RX5p
B49	TX6n	A49	GND
B48	GND	A48	RX6n
B47	TX6p	A47	GND
B46	GND	A46	RX6p
B45	TX7n	A45	GND
B44	GND	A44	RX7n
B43	TX7p	A43	GND
B42	GND	A42	RX7p
B41	TX8n	A41	GND
B40	GND	A40	RX8n
B39	TX8p	A39	GND
B38	GND	A38	RX8p
B37	TX9n	A37	GND
B36	GND	A36	RX9n
B35	TX9p	A35	GND
B34	GND	A34	RX9p
B33	TXDSCn	A33	GND
B32	GND	A32	RXDSCn
B31	TXDSCp	A31	GND
B30	GND	A30	RXDSCp
B29	REFCLKn	A29	GND
B28	GND	A28	MDIO
B27	REFCLKp	A27	MDC
B26	GND	A26	GND
B25	PRTADR4	A25	VND_IO_A
B24	PRTADR3	A24	VND_IO_B
B23	PRTADR2	A23	VND_IO_C
B22	PRTADR1	A22	VND_IO_D
B21	PRTADR0	A21	GND
B20	PRG_CNTL1	A20	VND_IO_E
B19	PRG_CNTL2	A19	VND_IO_F
B18	PRG_CNTL3	A18	VND_IO_G
B17	GND	A17	VND_IO_H
B16	PRG_ALRM1	A16	GND
B15	PRG_ALRM2	A15	VND_IO_J
B14	PRG_ALRM3	A14	VND_IO_K
B13	PM_SYNC	A13	*FFU*
B12	GND	A12	RX_ALRM_IN
B11	TX_DIS	A11	RX_ALRM_OUT
B10	MOD_LOPWR	A10	*FFU*
B9	MOD_RSTn	A9	*FFU*
B8	RX_LOS	A8	*FFU*
B7	GLB_ALRMn	A7	*FFU*
B6	12V_GND	A6	12V_GND
B5	12V_GND	A5	12V_GND
B4	12V_GND	A4	12V_GND
B3	12V	A3	12V
B2	12V	A2	12V
B1	12V	A1	12V

Table 11: MSA-100GLH Electrical Connector - Row B Pin Description



	100G	I/O	Logic	Description
B84	12V			+12V Module Supply Voltage
B83	12V			
B82	12V			
B81	12V_GND			+12V Module Supply Voltage Return Ground, can be seperate or tied together with Signal Ground
B80	12V_GND			
B79	12V_GND			
B78	GND			Ground
B77	TXMCLKn	O	CML	Transmit Monitor Clock, negative leg
B76	GND			
B75	TXMCLKp	O	CML	Transmit Monitor Clock, positive leg
B74	GND			
B73	TX0n	I	CML	Transmit Data 0, negative leg
B72	GND			
B71	TX0p	I	CML	Transmit Data 0, positive leg
B70	GND			
B69	TX1n	I	CML	Transmit Data 1, negative leg
B68	GND			
B67	TX1p	I	CML	Transmit Data 1, positive leg
B66	GND			
B65	TX2n	I	CML	Transmit Data 2, negative leg
B64	GND			
B63	TX2p	I	CML	Transmit Data 2, positive leg
B62	GND			
B61	TX3n	I	CML	Transmit Data 3, negative leg
B60	GND			
B59	TX3p	I	CML	Transmit Data 3, positive leg
B58	GND			
B57	TX4n	I	CML	Transmit Data 4, negative leg
B56	GND			
B55	TX4p	I	CML	Transmit Data 4, positive leg
B54	GND			
B53	TX5n	I	CML	Transmit Data 5, negative leg
B52	GND			
B51	TX5p	I	CML	Transmit Data 5, positive leg
B50	GND			
B49	TX6n	I	CML	Transmit Data 6, negative leg
B48	GND			
B47	TX6p	I	CML	Transmit Data 6, positive leg
B46	GND			
B45	TX7n	I	CML	Transmit Data 7, negative leg
B44	GND			
B43	TX7p	I	CML	Transmit Data 7, positive leg
B42	GND			
B41	TX8n	I	CML	Transmit Data 8, negative leg
B40	GND			
B39	TX8p	I	CML	Transmit Data 8, positive leg
B38	GND			
B37	TX9n	I	CML	Transmit Data 9, negative leg
B36	GND			
B35	TX9p	I	CML	Transmit Data 9, positive leg
B34	GND			
B33	TXDSCn	I	CML	Transmit Deskew Channel, negative leg (SFI-S only, otherwise no connect)
B32	GND			
B31	TXDSCp	I	CML	Transmit Deskew Channel, positive leg (SFI-S only, otherwise no connect)
B30	GND			
B29	REFCLKn	I	CML	Reference Clock, negative leg
B28	GND			
B27	REFCLKp	I	CML	Reference Clock, positive leg
B26	GND			
B25	PRTADR4	I	1.2V CMOS	MDIO port address bit 4
B24	PRTADR3	I	1.2V CMOS	MDIO port address bit 3
B23	PRTADR2	I	1.2V CMOS	MDIO port address bit 2
B22	PRTADR1	I	1.2V CMOS	MDIO port address bit 1
B21	PRTADR0	I	1.2V CMOS	MDIO port address bit 0
B20	PRG_CNTL1	I	LVCMOS w/ PUR	Programmable Control 1 set over MDIO
B19	PRG_CNTL2	I	LVCMOS w/ PUR	Programmable Control 2 set over MDIO
B18	PRG_CNTL3	I	LVCMOS w/ PUR	Programmable Control 3 set over MDIO
B17	GND			
B16	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1 set over MDIO
B15	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2 set over MDIO
B14	PRG_ALRM3	O	LVCMOS	Programmable Alarm 3 set over MDIO
B13	PM_SYNC	I	LVCMOS w/ PDR	Performance monitoring sync: Rising edge synchronizes PM statistics counters
B12	GND			
B11	TX_DIS	I	LVCMOS w/ PUR	Transmitter Disable. "1" or NC = transmitter disabled, "0" = transmitter enabled
B10	MOD_LOPWR	I	LVCMOS w/ PUR	Module Low Power Mode. "1" or NC= module in low power (safe) mode, "0"= power-on enabled
B9	MOD_RSTn	I	LVCMOS w/ PDR	Module Reset. "0" resets the module, "1" or NC = module enabled.
B8	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal. "1"= low optical signal, "0"= normal condition
B7	GLB_ALRMn	O	LVCMOS / OD	Global Alarm. "0": Alarm condition, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
B6	12V_GND			+12V Module Supply Voltage Return Ground, can be seperate or tied together with Signal Ground
B5	12V_GND			
B4	12V_GND			
B3	12V			+12V Module Supply Voltage
B2	12V			
B1	12V			

Table 12: MSA-100GLH Electrical Connector - Row A Pin Description (Note: Pins for future use (FFU) should be left unconnected on both the host board and the module)



	100G	I/O	Logic	Description
A84	12V			+12V Module Supply Voltage
A83	12V			
A82	12V			
A81	12V_GND			+12V Module Supply Voltage Return Ground, can be seperate or tied together with Signal Groun
A80	12V_GND			
A79	12V_GND			
A78	MOD_ABS	O	GND	Module Absent. "1" or NC = module absent, "0" = module present, Pull Up Resistor on Host
A77	GND			Ground
A76	RXMCLKn	O	CML	Receive Monitor Clock, negative leg
A75	GND			
A74	RXMCLKp	O	CML	Receive Monitor Clock, positive leg
A73	GND			
A72	RX0n	O	CML	Receive Data 0, negative leg
A71	GND			
A70	RX0p	O	CML	Receive Data 0, positive leg
A69	GND			
A68	RX1n	O	CML	Receive Data 1, negative leg
A67	GND			
A66	RX1p	O	CML	Receive Data 1, positive leg
A65	GND			
A64	RX2n	O	CML	Receive Data 2, negative leg
A63	GND			
A62	RX2p	O	CML	Receive Data 2, positive leg
A61	GND			
A60	RX3n	O	CML	Receive Data 3, negative leg
A59	GND			
A58	RX3p	O	CML	Receive Data 3, positive leg
A57	GND			
A56	RX4n	O	CML	Receive Data 4, negative leg
A55	GND			
A54	RX4p	O	CML	Receive Data 4, positive leg
A53	GND			
A52	RX5n	O	CML	Receive Data 5, negative leg
A51	GND			
A50	RX5p	O	CML	Receive Data 5, positive leg
A49	GND			
A48	RX6n	O	CML	Receive Data 6, negative leg
A47	GND			
A46	RX6p	O	CML	Receive Data 6, positive leg
A45	GND			
A44	RX7n	O	CML	Receive Data 7, negative leg
A43	GND			
A42	RX7p	O	CML	Receive Data 7, positive leg
A41	GND			
A40	RX8n	O	CML	Receive Data 8, negative leg
A39	GND			
A38	RX8p	O	CML	Receive Data 8, positive leg
A37	GND			
A36	RX9n	O	CML	Receive Data 9, negative leg
A35	GND			
A34	RX9p	O	CML	Receive Data 9, positive leg
A33	GND			
A32	RXDSCn	O	CML	Receive Deskew Channel, negative leg (SFI-S only, otherwise no connect)
A31	GND			
A30	RXDSCp	O	CML	Receive Deskew Channel, positive leg (SFI-S only, otherwise no connect)
A29	GND			
A28	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data
A27	MDC	I	1.2V CMOS	Management Data Clock
A26	GND			
A25	VND_IO_A	I/O	LVCMOS	Vendor I/O A
A24	VND_IO_B	I/O	LVCMOS	Vendor I/O B
A23	VND_IO_C	I/O	LVCMOS	Vendor I/O C
A22	VND_IO_D	I/O	LVCMOS	Vendor I/O D
A21	GND			
A20	VND_IO_E	I/O	LVCMOS	Vendor I/O E
A19	VND_IO_F	I/O	LVCMOS	Vendor I/O F
A18	VND_IO_G	I/O	LVCMOS	Vendor I/O G
A17	VND_IO_H	I/O	LVCMOS	Vendor I/O H
A16	GND			
A15	VND_IO_J	I/O	LVCMOS	Vendor I/O J
A14	VND_IO_K	I/O	LVCMOS	Vendor I/O K
A13	*FFU*			For Future Use
A12	RX_ALRM_IN	I	LVCMOS	Receiver Alarm transfer input for Re-generator mode
A11	RX_ALRM_OUT	O	LVCMOS	Receiver Alarm transfer output for Re-generator mode
A10	*FFU*			For Future Use
A9	*FFU*			For Future Use
A8	*FFU*			For Future Use
A7	*FFU*			For Future Use
A6	12V_GND			+12V Module Supply Voltage Return Ground, can be seperate or tied together with Signal Groun
A5	12V_GND			
A4	12V_GND			
A3	12V			+12V Module Supply Voltage
A2	12V			
A1	12V			

10 References

10.1 Normative references

[N1] IEEE 802.3ba™ -2010 "Amendment: Media Acces Control Parameters, Physical Layers and Management Parameters for 40Gb/s and 100Gb/s Operation", Clause 45 – MDIO (March, 2010)
[N2] OIF-CEI-02.0 - Common Electrical I/O (CEI) - Electrical and Jitter Interoperability agreements for 6G+ bps and 11G+ bps I/O *(February 2005)*
[N3] Hirose FX10 Datasheets: http://www.hiroseusa.com/Special_downloads18.asp

10.2 Informative references

[I1] OIF-FD-100G-DWDM-01.0 - 100G Ultra Long Haul DWDM Framework Document *(June 2009)*
[I2] ITU-T Rec. G.709/Y.1331 (draft revised v3.4 – Oct. 2009) Interfaces for the Optical Transport Network (OTN)
[I3] OIF-SFI-S-01.0 – Scalable Serdes Framer Interface (SFI-S): Implementation for Interfaces Beyond 40G for Physical Layer Devices (Nov. 2008)
[I4] Hirose FX10 PCB Routing Guideline: http://www.hiroseusa.com/FX10_PCB_routing_guideline_v1.1.pdf
[I5] CFP MSA Management Interface Specification V2.0, r09 (April 10, 2012)

11 Appendix A: Glossary

ADC	Analog Digital Converter
CDR	Clock and Data Recovery
CN	Connector
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
DEC	Decoder
DSP	Digital Signal Processor
DWDM	Dense Wavelength Division Multiplex
ENC	Encoder
FEC	Forward Error Correction
FFU	For Future Use
Gbaud	10^9 Symbols Per Second
GH	Guide pin Hole
GND	Ground
GP	Guide Pin
IA	Implementation Agreement
LVCMOS	Low Voltage CMOS
MDC	Management Data Clock
MDIO	Management Data Input/Output
NC	No Connect
OIF	Optical Internetworking Forum
OTL	Optical channel Transport Lane
PCB	Printed Circuit Board
PM-QPSK	Polarization Multiplexed Quaternary Phase Shift Keying
RX	Receiver

SFI	Serdes Framer Interface
TX	Transmitter
VND	Vendor

12 Appendix B: Open Issues / current work items

None.

13 Appendix C: List of companies belonging to OIF when document is approved

Acacia Communications
ADVA Optical Networking
Agilent Technologies
Alcatel-Lucent
Altera
AMCC
Amphenol Corp.
Anritsu
Applied Communication Sciences
AT&T
Avago Technologies Inc.
Broadcom
Brocade
Centellax, Inc.
China Telecom
Ciena Corporation
Cisco Systems
ClariPhy Communications
Coriant
Cortina Systems
CPqD
Department of Defense
Deutsche Telekom
Emcore
Ericsson
FCI USA LLC
Fiberhome Technologies Group
Finisar Corporation
Fujitsu
Furukawa Electric Japan
Google
Hewlett Packard
Hitachi
Hittite Microwave Corp
Huawei Technologies
IBM Corporation
Infinera
Kandou
KDDI R&D Laboratories
LeCroy
LSI Corporation
Luxtera
M/A-COM Technology Solutions, Inc.
Marben Products
Metaswitch
Mindspeed
Mitsubishi Electric Corporation
Molex
MoSys, Inc.
MultiPhy Ltd
NEC
NeoPhotonics
NTT Corporation
Oclaro
Optelian
Orange
PETRA
Picometrix
PMC Sierra
QLogic Corporation
Ranovus
Semtech
Skorpios Technologies
Sumitomo Electric Industries
Sumitomo Osaka Cement
TE Connectivity
Tektronix
Tellabs
TELUS Communications, Inc.
TeraXion
Texas Instruments
Time Warner Cable
TriQuint Semiconductor
u2t Photonics AG

Inphi
Intel
JDSU
Juniper Networks
Kaiam
US Conec
Verizon
Xilinx
Xtera Communications
Yamaichi Electronics Ltd.

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