OIF-MSA-100GLH-EM-02.1



OIF OPTICAL INTERNETWORKING FORUM

Implementation Agreement For Generation 2.0 100G Long-Haul DWDM Transmission Module – Electromechanical (Gen.2 MSA-100GLH)

IA # OIF-MSA-100GLH-EM-02.1

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ABSTRACT: This Implementation Agreement specifies key electromechanical aspects of a 100G Long-Haul DWDM Transmission Module, for applications such as 100G PM-QPSK long-haul DWDM transmission. Key aspects include: module mechanical dimensions, electrical connector and pin assignment, module hardware signaling pins, high-speed electrical characteristics, power supply, power dissipation, and management interface.



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1 <u>Table of Contents</u>

1	Tab	le of Contents	4						
2	List	t of Figures	5						
3									
4	Document Revision History6								
5	Inti	roduction	7						
6		actional Description							
7	Мо	dule Management Interface Description	.10						
8		ctrical Specifications	.10						
8	8.1	Operating Case Temperature							
1	8.2	Electrical Power Supply and Power Dissipation	.10						
8	8.3	High Speed Pin Electrical Specifications	.11						
1	8.4 Control Pins (non-MDIO) Functional Description								
8	8.5 Alarm Pins (non-MDIO) Functional Description								
8	8.6	Module Management Interface Pins (MDIO) Description	.19						
8	8.7	Hardware Signaling Pin Electrical Specifications	.21						
1	8.8	Hardware Signaling Pin Timing Specifications	.23						
9	Me	chanical Specifications	.25						
(9.1	Mechanical Overview	.25						
(9.2	Electrical Connector	.25						
(9.3	Module Dimensions	.28						
(9.4	Host System Dimensions	.33						
(9.5	Module Optical Fiber Ports	.34						
(9.6	Pin Assignment	.35						
10	Ref	erences							
	10.1	Normative references	.40						
•	10.2	Informative references	.40						
11	Ap	pendix A: Glossary	.40						
12									
13		pendix C: List of companies belonging to OIF when document is							
ap		ed	.42						



2 <u>List of Figures</u>

FIGURE 1: 100G LONG-HAUL DWDM TRANSMISSION MODULE (MSA-100GLH) FUNCTIONA	L
DIAGRAM	8
FIGURE 2: HIGH SPEED I/O FOR DATA AND CLOCKS	
FIGURE 3: TRANSMITTER DISABLE (TX DIS) TIMING DIAGRAM	15
FIGURE 4: MODULE LOW POWER (MOD_LOPWR) TIMING DIAGRAM	16
FIGURE 5: RECEIVER LOSS OF SIGNAL (RX_LOS) TIMING DIAGRAM	18
FIGURE 6: GLOBAL ALARM (GLB_ALRMN) TIMING DIAGRAM	19
FIGURE 7: MODULE MDIO & MDC TIMING DIAGRAM	21
FIGURE 8: REFERENCE +3.3V LVCMOS INPUT/OUTPUT TERMINATIONS	22
FIGURE 9: REFERENCE MDIO INTERFACE TERMINATION	23
FIGURE 10: MSA-100GLH SIMPLIFIED START-UP FLOW DIAGRAM	24
FIGURE 11: HIROSE FX10A-168S-SV(83) RECEPTACLE CONNECTOR ASSEMBLY	26
FIGURE 12: HIROSE FX10A-168P-SV(83) HEADER CONNECTOR ASSEMBLY	27
FIGURE 13: FX10 CONNECTOR ALIGNMENT	28
FIGURE 14: MSA-100GLH NON-CONDUCTIVE SHEET DIMENSIONS	29
FIGURE 15: MSA-100GLH FLATTOP MECHANICAL DIMENSIONS - BOTTOM/SIDE VIEWS	30
FIGURE 16: MSA-100GLH FLATTOP MECHANICAL DIMENSIONS - TOP VIEW	31
FIGURE 17: MECHANICAL DIMENSIONS OF MSA-100GLH WITH INTEGRATED HEAT SINK	32
FIGURE 18: MSA-100GLH WITH INTEGRATED HEAT SINK - TOP VIEW	33
FIGURE 19: RECOMMENDED HOST SYSTEM LAYOUT FOR MSA-100GLH	34
FIGURE 20: MSA-100GLH OPTICAL FIBER PORT LOCATION AND DIMENSIONS	35

3 <u>List of Tables</u>

TABLE 1: MSA-100GLH PERFORMANCE SPECIFICATIONS	10
TABLE 2: MSA-100GLH REFERENCE CLOCK (REFCLK) CHARACTERISTICS	12
TABLE 3: OPTIONAL TXMCLK AND RXMCLK CHARACTERISTICS	13
TABLE 4: MSA-100GLH CONTROL PINS (NON-MDIO)	14
TABLE 5: MSA-100GLH ALARM PINS (NON-MDIO)	17
TABLE 6: MSA-100GLH MDIO MANAGEMENT INTERFACE PINS	20
TABLE 7: 3.3V LVCMOS ELECTRICAL CHARACTERISTICS	21
TABLE 8: 1.2V LVCMOS ELECTRICAL CHARACTERISTICS	22
TABLE 9: HARDWARE SIGNALING PINS TIMING PARAMETERS SUMMARY	24
TABLE 10: MSA-100GLH PIN-MAP	37
TABLE 11: MSA-100GLH ELECTRICAL CONNECTOR - ROW B PIN DESCRIPTION	38
TABLE 12: MSA-100GLH ELECTRICAL CONNECTOR - ROW A PIN DESCRIPTION	39

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DATE:

January 14, 2013

Revision Date **Change Notes** By Preliminary draft Jan. 14, 2013 Preliminary draft B Apr. 23, 2013 Location of PIN A1 indicate in Atul Figure 15, 17 and 19 Srivastava 9.6 Pin Assignment Information delete of Appendix D and E 10.2 Informative references [15] Revision update to latest version Preliminary draft IA # OIF-Aug. 27,2013 **Draft IA Release** Atul MSA-100GLH-EM-02.0 Srivastava Draft IA # OIF-MSA-Jul. 31,2014 Modify document as per ballot Atul 100GLH-EM-02.1 comments in oif2014.182.00 Srivastava 6 Functional Description Comment add of Figure 1A-1D Error of repetition delete of Figure 1A-1D 8.3 High Speed Pin Electrical Specifications Comment add 10.2 Informative references [12] [14] [15] Revision update to latest version



		13 Appendix C	
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Draft IA # OIF-MSA-	May 4, 2015	13 Appendix C	Atul
100GLH-EM-02.3	-	Updated list of current members	Srivastava

5 <u>Introduction</u>

This document details an Implementation Agreement (IA) for a Generation 2.0 100G Long-Haul DWDM Transmission Module – Electromechanical (MSA-100GLH) for optical line interface applications. While specifically addressing 100G PM-QPSK long-haul DWDM transmission applications [I1], this IA strives to remain modulation format and data rate agnostic whenever practical to maximize applicability to future market requirements.

This IA specifies key electromechanical aspects of the Generation 2.0 100G Long-Haul DWDM Transmission Module (hereafter termed MSA-100GLH) that include the following: module mechanical dimensions, electrical connector and pin map, module hardware signaling pins, high-speed electrical characteristics, power supply, power dissipation, and management interface.

6 <u>Functional Description</u>

A functional block diagram of the MSA-100GLH is illustrated in Figure 1: Generation 2.0 100G Long-Haul DWDM Transmission Module (MSA-100GLH) Functional Diagram. Key module functions include transmitter optics, receiver optics, interface ICs, module controller supporting an MDIO/MDC management interface, and power conversion for a single +12V DC power supply from the host. The MSA-100GLH is not hot pluggable, but is fastened to the host system board during line card assembly. The interface IC(s) and module electrical interface are generically specified to allow vendor specific customization of multilane "M-lane" \sim 11 Gbit/s interfaces. Module electrical interfaces include but are not limited to the following:

a) Simple bit multiplex
b) OTL4.10 [I2]
c) SFI-S [I3]
d) OTL3.4 [I2] (for 40G applications, see informative Appendix D)

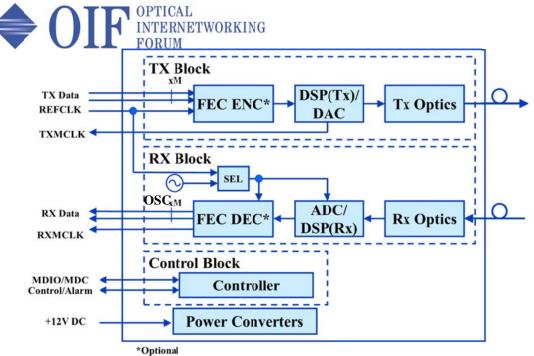


Figure 2: Generation 2.0 100G Long-Haul DWDM Transmission Module (MSA-100GLH) Functional Diagram

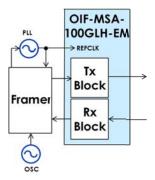


Figure 1A: Application Diagram 1 for 1 MSA Transponder w Framer

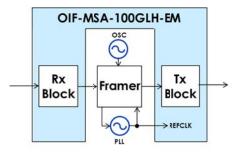


Figure 1B: Application Diagram 2 for 1 MSA Re-generator w Framer

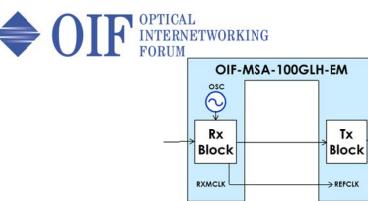


Figure 1C: Application Diagram 3 for 1 MSA Re-generator w/o Framer

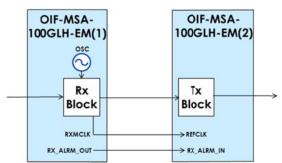


Figure 1D: Application Diagram 4 for 2 MSA Re-generator w/o Framer

Figure 1A thru 1D shows the applications and clock sources for these applications. For re-generator application, MSA-100GLH shall provide an internal clock (OSC) and switch to this internal clock when the other clock sources are not valid

Note: In normal operation, Tx have to use Rx recovered clock for REFCLK in Figure 1C and 1D. The Alarm Indication Signal (AIS) is transmitted downstream in certain cases e.g. LOF, LOS at Rx. In such cases a local reference clock is used to transmit the AIS since a viable recovered receiver clock may not be available.

The AIS can be triggered by (i) by the Module based on Rx condition or (ii) using RX_ALRM_IN pin. This feature is Optional.

The module's local reference clock could be used to drive the Tx side when generating AIS.



The MSA-100GLH utilizes MDIO IEEE 802.3 Clause 45 [N1] for its management interface. The MSA-100GLH MDIO hardware implementation is specified in Section 8.6. The MSA-100GLH MDIO register set specifications are defined in [15]. When multiple MSA-100GLH are connected via a single bus, a particular MSA-100GLH may be selected by using the MDIO Physical Port Address pins.

8 <u>Electrical Specifications</u>

8.1 **Operating Case Temperature**

The MSA-100GLH operating case temperature is specified in Table 1.

8.2 Electrical Power Supply and Power Dissipation

The MSA-100GLH is powered by a single +12V DC supply from the host board. This power supply is specified in Table 1. All voltages are measured at the electrical connector interface.

The MSA-100GLH power dissipation is specified in Table 1.

Parameter	Symbol	Min	Тур	Max	Unit	Note
+12V DC Supply Voltage	V _{cc}	11.4	12.0	12.6	V	+/- 5%
+12V DC Supply Current	I _{CC}			4.0	А	Notes 1 & 2
Power Supply Noise	V _{rip}			1	%р-р	1Hz – 20MHz
	-					
Power Dissipation	Pw			45	W	
Operating Case Temperature		0		70	°C	

Table 1: MSA-100GLH Performance Specifications

Note: The parameter min and max values are specified End-of-Life within the overall relevant operating case temperature range. The typical values are referenced to +25°C, nominal power supply, Beginning-of -Life.

Note 1: Maximum current per pin shall not exceed 750mA.

Note 2: Icc max specified for current rating purposes. Normal operating current (Icc) must not exceed Pw / Vcc.



8.3 High Speed Pin Electrical Specifications

8.3.1 Transmitter Data (TX)

The Transmitter Data (TX) signals shall comply with CEI-11G-MR Low Swing option as per Clauses 9.3.1. and 9.3.1.2 [N2]. Full Swing support is not required. The recommended termination of the TX pins is given in Figure 3.

8.3.2 Receiver Data (RX)

The Receiver Data (RX) signals shall comply with CEI-11G-MR Clause 9.3.3 [N2]. The recommended termination of the RX pins is given in Figure 3.

8.3.3 Reference Clock (REFCLK)

The host shall supply a reference clock (REFCLK) at 1/16 of the electrical lane rate. The host shall optionally supply a reference clock (REFCLK) at 1/64 of the electrical lane rate.

The REFCLK shall be CML differential AC coupled and terminated with 50 Ohm internal V_{TT} within the MSA-100GLH, as shown in Figure 3. A frequency locked relationship is required between the transmit data lanes (TX/TXDSC) and the reference clock (REFCLK). There is no required phase relationship between the data lanes and the reference clock. The REFCLK frequency shall not deviate from nominal by more than ± 20 ppm. Detailed reference clock characteristics for the MSA-100GLH are given in Table 2.

When the two MSA client interfaces are connected back-to-back for regenerator application then the two DC blocking capacitors are used in series and this will change the filter cutoff frequency.



Table 2: MSA-100GLH Reference Clock	(REFCLK) Characteristics
-------------------------------------	--------------------------

Parameter	Symbol	Min	Тур	Max	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency	f		1/16			Of electrical lane rate -
						default
			1/64			Of electrical lane rate -
						optional
Frequency	Δf	-20		+20	ppm	
Stability						
Differential	V _{DIFF}	400		1600	mV	Peak-to-Peak Differential
Voltage						
Clock Duty Cycle	CDC	40		60	%	
Clock Rise/Fall	t _{r/f}	200		1250	ps	1/64 electrical lane rate
Time		50		315	ps	1/16 electrical lane rate

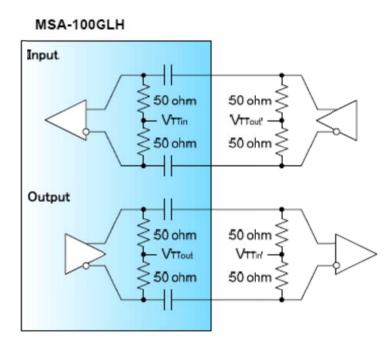


Figure 3: High Speed I/O for Data and Clocks

8.3.4 Transmitter Monitor Clock (TXMCLK)

The MSA-100GLH optionally may supply a transmitter monitor clock (TXMCLK). This clock is intended to be used as a reference for measurements of the module optical transmit signal. If provided, the clock shall operate at 1/8 of the transmitter optical symbol rate for 32Gb

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applications¹. This rate is optimized for triggering high-speed sampling scopes. Clock termination is shown in Figure 3. TXMCLK characteristics are summarized in Table 3.

8.3.5 Receiver Monitor Clock (RXMCLK)

The MSA-100GLH optionally may supply a receiver monitor clock (RXMCLK). This clock is intended to be used as a reference for measurements of the module receive data. If provided, the clock shall operate at 1/16 of the receiver electrical lane data rate. The RXMCLK may optionally operate at 1/64 of the receiver electrical lane data rate. Clock termination is shown in Figure 3. RXMCLK characteristics are summarized in Table 3.

Parameter	Symbol	Min	Тур	Max	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency - TXMCLK			1/8			Of TX optical symbol rate - default
Frequency - RXMCLK			1/16			Of RX electrical lane data rate - default
			1/64			Of RX electrical lane data rate - optional
Output Differential Voltage	V _{DIFF}	400		1600	mV	Peak-to-Peak Differential
Clock Duty Cycle	CDC	40		60	%	

Table 3: Optional TXMCLK and RXMCLK Characteristics

8.4 Control Pins (non-MDIO) Functional Description

The control functions between a host and a MSA-100GLH are conducted through a set of dedicated, non-data hardware signal pins on the 168-pin electrical connector and via an MDIO interface. The signal pins work together with the MDIO interface to form a complete HOST/MSA-100GLH management interface. Upon module initialization, the control functions are available. Pins allocated to control functions in the 168-pin electrical connector are listed in Table 4.

¹ For 40G applications, other clock rates may be necessary for operating with available test equipment.



Pin #	Symbol	Description	I / 0	Logic	"H"	"L"	Pull-up /down
B20	PRG_CNTL1	Programmable Control 1 Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled	Ι	3.3V LVCMOS	Per MDIC document		Pull-Up ¹
B19	PRG_CNTL2	Programmable Control 2 For Future Use	Ι	3.3V LVCMOS			Pull-Up ¹
B18	PRG_CNTL3	Programmable Control 3 For Future Use	Ι	3.3V LVCMOS			Pull-Up ¹
B13	PM_SYNC	Performance Monitoring Sync Rising edge synchronizes PM statistics counters	Ι	3.3V LVCMOS			Pull-Down ²
B11	TX_DIS	Transmitter Disable "0": transmitter enabled "1" or NC: transmitter disabled	Ι	3.3V LVCMOS	Disable	Enable	Pull-Up ¹
B10	MOD_LOPWR	Module Low Power "0": power-on enabled "1" or NC: module in low power (safe) mode	Ι	3.3V LVCMOS	Low Power	Enable	Pull-Up ¹
В9	MOD_RSTn	Module Reset "0": resets the module "1": module enabled	Ι	3.3V LVCMOS	Enable	Reset	Pull-Down ²

Note 1: Pull-Up resistor (4.7k - 10kOhm) is located within the MSA-100GLH.

Note 2: Pull-Down resistor (4.7k - 10kOhm) is located within the MSA-100GLH.

8.4.1 Programmable Control Pins (PRG_CNTLs)

The Programmable Control pins (PRG_CNTL) allow the host to program certain MSA-100GLH control functions via a hardware pin. The intention is to allow for maximum design and debug flexibility. The default setting for Control 1 is control of the Transmit & Receive Reset. Controls 2 and 3 are for future use.

8.4.1.1 Programmable Control 1 Pin (PRG_CNTL1)

Programmable Control 1 Pin (PRG_CNTL1) is an input pin from the host, operating with programmable logic. It is pulled up in the MSA-100GLH. It can be re-programmed over MDIO registers to another MDIO control register while the module is in any steady state except Reset. The default function is Transmit & Receive circuitry reset (TRXIC_RSTn) with active-low logic. When TRXIC_RSTn is asserted (driven low), the digital transmit and receive circuitry is reset clearing all FIFOs and/or resetting all CDRs. When de-asserted, the digital transmit and receive circuitry shall resume normal operation.

8.4.1.2 Programmable Control 2 Pin (PRG_CNTL2)

Programmable Control 2 Pin (PRG_CNTL2) is an input from the host, operating with programmable logic. It is pulled up in the MSA-100GLH. It can be re-programmed over MDIO registers to another MDIO control register while the module is in any steady state except Reset. It is reserved for future use.

8.4.1.3 Programmable Control 3 Pin (PRG_CNTL3)



Programmable Control 3 Pin (PRG_CNTL3) is an input from the host, operating with programmable logic. It is pulled up in the MSA-100GLH. It can be re-programmed over MDIO registers to another MDIO control register while the module is in any steady state except Reset. It is reserved for future use.

8.4.1.4 Performance Monitoring Synchronization (PM_SYNC)

The Performance Monitoring Synchronization pin (PM_SYNC) is an input from the host. The purpose of this pin is to provide a synchronization pulse from the host time reference source for synchronizing module-level performance monitoring data collection with host system performance monitoring data collection. The default time period of this signal is 1 second. Use of PM_SYNC is optional for the MSA-100GLH.

8.4.1.5 Transmitter Disable Pin (TX_DIS)

The Transmitter Disable pin (TX_DIS) is an input from the host, operating with active-high logic. This pin is pulled up in the MSA-100GLH. When TX_DIS is asserted, all of the optical outputs inside a MSA-100GLH shall be switched off. When this pin is de-asserted, optical transmitters shall be switched on according to a predefined TX power-on process defined by module vendor specification. The timing diagram for TX_DIS pin is illustrated in Figure 4. Values for t_off and t_on are application specific and not specified in this IA.

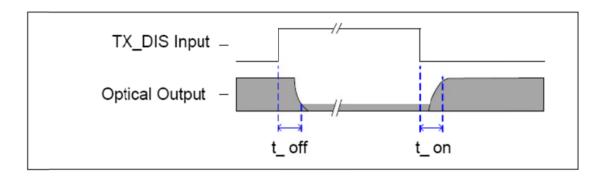


Figure 4: Transmitter Disable (TX_DIS) Timing Diagram

8.4.1.6 Module Low Power Pin (MOD_LOPWR)

The Module Low Power pin (MOD_LOPWR) is an input from the host, operating with activehigh logic. It is pulled up in the MSA-100GLH. When MOD_LOPWR is asserted, the MSA-100GLH shall be in the low power state and will stay in the low power state as long as it is asserted. When de-asserted, the MSA-100GLH shall initiate the High-Power-Up process.

In Low Power mode, the MSA-100GLH shall communicate via the MDIO management interface. While the module is in Low Power mode, it has a maximum power consumption of 6W.

The timing diagram for the MOD_LOPWR pin is illustrated in Figure 5. Values for $t_MOD_LOPWR_on$ and $t_MOD_LOPWR_off$ are application specific and not specified in this IA.



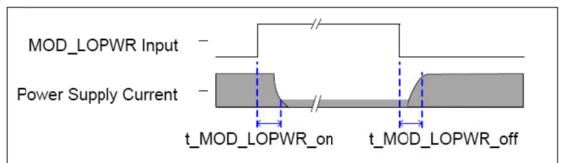


Figure 5: Module Low Power (MOD_LOPWR) Timing Diagram

8.4.1.7 Module Reset Pin (MOD_RSTn)

The Module Reset pin (MOD_RSTn) is an input from the host, operating with active-low logic. This pin is pulled down in the MSA-100GLH. When MOD_RSTn is asserted (driven low), the MSA-100GLH enters the Reset state. When de-asserted, the MSA-100GLH exits the Reset state and shall begin an initialization process as part of the overall module start-up sequence.

8.5 Alarm Pins (non-MDIO) Functional Description

Alarm indications from the MSA-100GLH to the host are conducted through a set of dedicated, non-data hardware signal pins on the 168-pin electrical connector and via an MDIO interface. The signal pins work together with the MDIO interface to form a complete HOST/MSA-100GLH management interface. Upon module initialization, the alarm indication functions are available. Pins allocated to alarm functions in the 168-pin electrical connector are listed in Table 5.



Pin #	Symbol	Description	I / 0	Logic	"H"	"L"	Pull- up/down
B16	PRG_ALRM1	Programmable Alarm 1 set over MDIO	0	3.3V LVCMOS			
B15	PRG_ALRM2	Programmable Alarm 2 set over MDIO	0	3.3V LVCMOS			
B14	PRG_ALRM3	Programmable Alarm 3 set over MDIO	0	3.3V LVCMOS			
B8	RX_LOS	Receiver Loss of Signal	0	3.3V LVCMOS	LOS	OK	
A78	MOD_ABS	Module Absent "0": module present "1" or NC: module absent	0	GND	Absent	Present	Pull-Down ¹
B7	GLB_ALRMn	Global Alarm	0	3.3V LVCMOS w/ Open Drain	ОК	Alarm	Note 2
A11	RX_ALRM_O UT	Receiver Alarm transfer output for Re-generator mode	0	3.3V LVCMOS	ОК	Alarm	
A12	RX_ALRM_IN	Receiver Alarm transfer input for Re-generator mode	Ι	3.3V LVCMOS	OK	Alarm	

Table 5: MSA-100GLH Alarm Pins (non-MDIO)

Note 1: Pull-down resistor (<1000hm) is located within the MSA-100GLH. A Pull-Up resistor should be located on the host.

Note 2: Pull-Up resistor on host.

8.5.1 Programmable Alarm Pins (PRG_ALRMs)

The Programmable Alarm pins enable the host system to program MSA-100GLH supported alarms to dedicated hardware pins.

8.5.1.1 Programmable Alarm 1 Pin (PRG_ALRM1)

Programmable Alarm 1 Pin (PRG_ALRM1) is an output to the host, operating with programmable logic. It can be re-programmed over MDIO registers to another MDIO alarm register while the MSA-100GLH is in any steady state except Reset. The default function is High Power On (HIPWR_ON) indicator with active-high logic.

8.5.1.2 Programmable Alarm 2 Pin (PRG_ALRM2)

Programmable Alarm 2 Pin (PRG_ALRM2) is an output to the host, operating with programmable logic. It can be re-programmed over MDIO registers to another MDIO alarm register while the MSA-100GLH is in any steady state except Reset. The default function is Module Ready (MOD_READY) indicator with active-high logic.

The default function MOD_READY is used by the MSA-100GLH during the module initialization. When asserted, it indicates the MSA-100GLH has completed the necessary initialization process and is ready to transmit and receive data.

8.5.1.3 Programmable Alarm 3 Pin (PRG_ALRM3)



Programmable Alarm 3 Pin (PRG_ALRM3) is an output to the host, operating with programmable logic. It can be re-programmed over MDIO registers to another MDIO alarm register while the MSA-100GLH is in any steady state except Reset. The default function is Module Fault (MOD_FAULT) indicator with active-high logic.

The default function MOD_FAULT is used by the MSA-100GLH during module initialization. When asserted, it indicates the MSA-100GLH has entered into a fault state.

8.5.2 Receiver Loss of Signal Pin (RX_LOS)

The Receiver Loss of Signal pin (RX_LOS) is an output to the host, operating with active-high logic. When asserted, it indicates received optical power in the MSA-100GLH is lower than the expected value. The optical power at which RX_LOS is asserted is application specific and specified by the host system or module vendor. The timing diagram for the RX_LOS pin is illustrated in Figure 6. Values for t_loss_on and t_ loss_off are application specific and not specified in this IA.

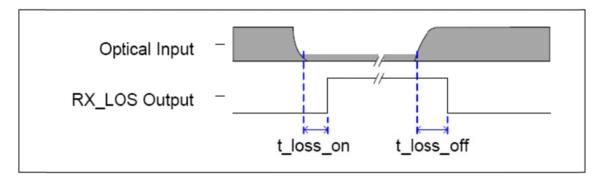


Figure 6: Receiver Loss of Signal (RX_LOS) Timing Diagram

8.5.3 Module Absent Pin (MOD_ABS)

The Module Absent (MOD_ABS) pin is an output from the MSA-100GLH to the host. It is pulled up on the host board and is pulled down to ground in the MSA-100GLH. MOD_ABS asserts a "Low" condition when the MSA-100GLH is plugged into a host socket. MOD_ABS is asserted "High" when the MSA-100GLH is physically absent from a host socket.

8.5.4 Global Alarm Pin (GLB_ALRMn)

The Global Alarm pin (GLB_ALRMn) is an output to the host, operating with active-low logic. When GLB_ALRMn is asserted (driven low), it indicates that a Fault/Alarm/Warning/Status (FAWS) condition has occurred. It is driven by the logical OR of all fault, alarm, warning and status conditions latched in the latched registers. Masking Registers are provided so that GLB-ALRMn may be programmed to assert only for specific fault/alarm/warning/status conditions. It is recommended that the host board be designed to support high-priority event handling service to respond to the assertion of this pin. Upon the assertion of this pin, the host event handler identifies the source of the fault by reading the latched registers over the MDIO interface. The reading action clears the latched registers, which in turn causes the MSA-100GLH to de-assert (driven high) the GLB_ALRMn pin.



The timing diagram for the GLB_ALRMn pin is illustrated in Figure 7. Values for t_GLB_ALRM_on and t_GLB_ALRMn_off are application specific and not specified in this IA.

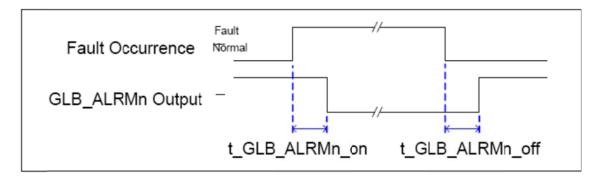


Figure 7: Global Alarm (GLB_ALRMn) Timing Diagram

Note: In this Figure the Fault Occurrence is shown transitioning to a "Normal" status. In order for this transition to occur, a read of the alarm register must have occurred such that the fault has been received.

8.5.5 Receiver Alarm transfer output for Re-generator mode Pin (RX_ALRM_OUT)

The Receiver Alarm transfer output for Re-generator mode Pin (RX_ALRM_OUT) is an output to another connected MSA-100GLH for Re-generator application, operating with active-low logic. When RX_ALRM_OUT is asserted (driven low), it indicates that condition such as a Loss Of Signal/Loss Of Frame has occurred at RX. The timing diagram for the RX_ALRM_OUT pin is application specific and not specified in this IA.

8.5.6 Receiver Alarm transfer input for Re-generator mode Pin (RX_ALRM_IN)

The Receiver Alarm transfer input for Re-generator mode Pin (RX_ALRM_IN) is an input from another connected MSA-100GLH for Re-generator application, operating with active-low logic. When RX_ALRM_IN is asserted (driven low), the MSA-100GLH shall generate AIS(Alarm Indication Signal) condition, or similar signal at the TX. The timing diagram for the RX_ALRM_IN pin is application specific and not specified in this IA.

8.6 Module Management Interface Pins (MDIO) Description

The MSA-100GLH supports control, alarm and monitoring functions via dedicated hardware pins and via an MDIO bus. The MSA-100GLH MDIO electrical interface consists of 7 pins: 1 pin for MDIO, 1 pin for MDC, and 5 MDIO Physical Port Address pins. MDC is the MDIO clock line driven by the host. MDIO is the bidirectional data line driven by both the host and module, depending upon the data direction. Pins allocated to instantiate the MDIO interface in the MSA-100GLH electrical connector are listed in Table 6.



Table 6: MSA-100GLH MDIO Management Interface Pins

Pin	Symbol	Description	Ι	Logic	"H"	"L"	Pull-up
#			/				/down
			0				
A28	MDIO	Management Data I/O bi-directional	Ι	1.2V			
			/	LVCMOS			
			0				
A27	MDC	MDIO Clock	Ι	1.2V			
				LVCMOS			
B21	PRTADR0	MDIO Physical Port Address bit 0	Ι	1.2V			
				LVCMOS			
B22	PRTADR1	MDIO Physical Port Address bit 1	Ι	1.2V			
				LVCMOS			
B23	PRTADR2	MDIO Physical Port Address bit 2	Ι	1.2V			
				LVCMOS			
B24	PRTADR3	MDIO Physical Port Address bit 3	Ι	1.2V			
				LVCMOS			
B25	PRTADR4	MDIO Physical Port Address bit 3	Ι	1.2V			
				LVCMOS			

8.6.1 Management Data Input/Output Pin (MDIO)

The MDIO specification is defined in IEEE 802.3 Clause 45 [N1]. The MSA-100GLH shall support 4.0 Mbit/s maximum data rate. The MSA-100GLH uses an MDIO with 1.2V LVCMOS logic.

8.6.2 Management Data Clock Pin (MDC)

The host specifies a maximum MDC rate of 4.0 MHz and MSA-100GLH hence shall support a maximum MDC rate up to 4.0 MHz. The timing diagram for the MDIO and MDC pins is illustrated in Figure 8: Module MDIO & MDC Timing Diagram

The MSA-100GLH shall support a minimal setup (t_{setup}) and hold (t_{hold}) time in its MDIO implementation (see Table 9).

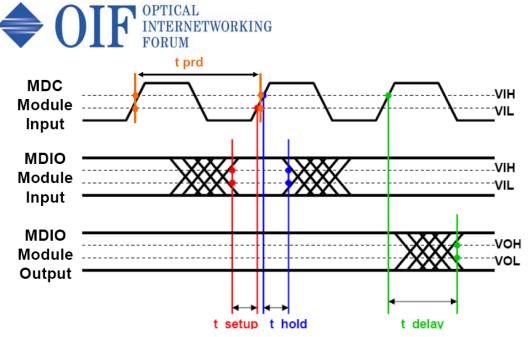


Figure 8: Module MDIO & MDC Timing Diagram

Note: Measured at Module MDIO & MDC pins.

8.6.3 MDIO Physical Port Address Pins (PRTADRs)

The MDIO Physical Port Address pins (PRTADRs) are used by the host system to address all of the MSA-100GLHs contained within its management domain. PRTADR0 corresponds to the LSB in the physical port addressing scheme. The 5-pin Physical Port Address lines are driven by the host to set the module Physical Port Address which should match the address specified in the MDIO Frame. It is recommended that the Physical Port Addresses not be changed while the MSA-100GLH is powered on.

8.7 Hardware Signaling Pin Electrical Specifications

8.7.1 Control & Alarm Pins: 3.3V LVCMOS Electrical Characteristics

The hardware control and alarm pins specified as 3.3V LVCMOS functionality described above shall meet the electrical characteristics described in Table 7. Figure 9 illustrates the recommended reference pin input and output terminations.

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	VCC	3.2	3.3	3.4	V
Input High Voltage	VIH	2	-	VCC+0.3	V
Input Low Voltage	VIL	-0.3	-	0.8	V
Input Leakage Current	IIN	-10	-	+10	μA
Output High Voltage (I_{OH} =-100 μ A)	VOH	VCC-0.2	-	-	V
Output Low Voltage (I_{OL} = 100 μ A)	VOL	-	-	0.2	V

Table 7: 3.3V LVCMOS Electrical Characteristics



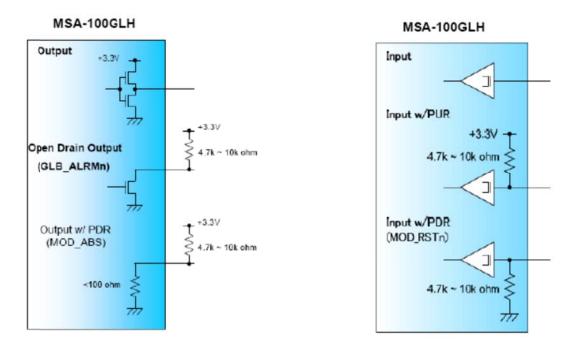


Figure 9: Reference +3.3V LVCMOS Input/Output Terminations

8.7.2 MDIO Interface Pins: 1.2V LVCMOS Electrical Characteristics

The MDIO pins specified as 1.2V LVCMOS functionality described above shall meet the electrical characteristics described in Table 8. Figure 9 illustrates the recommended reference pin input and output terminations.

Parameter	Symbol	Min	Тур	Max	Unit
Input High Voltage	VIH	0.84	-	1.5	V
Input Low Voltage	VIL	-0.3	-	0.36	V
Input Leakage Current	IIN	-100	-	+100	μA
Output High Voltage	VOH	1.0	-	1.5	V
Output Low Voltage	VOL	-0.3	-	0.2	V
Output High Current	IOH	-	-	-4	mA
Output Low Current	IOL	+4	-	-	mA
Input Capacitance	Ci	-	-	10	pF

Table 8: 1.2V	V LVCMOS Electrical	Characteristics
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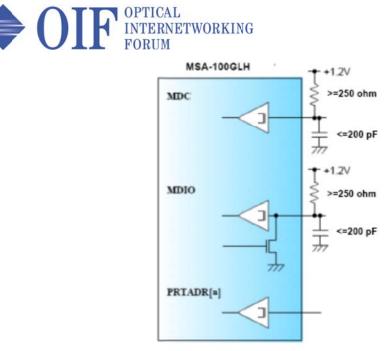


Figure 10: Reference MDIO Interface Termination

Note: MDC pull-up resistor is optional.

Note: Host termination resistor value of 560 Ohms is recommended. This value provides the best balance of performance for both open-drain and active tri-state driver in the module. Host termination resistor values below 560 Ohms are allowed, to a minimum of 250 Ohms, but this degrades driver performance. Host termination resistor values above 560 Ohms are allowed, but this degrades open-drain driver performance.

8.8 Hardware Signaling Pin Timing Specifications

The MSA-100GLH is designed to have a tightly coupled interface with host systems. A simplified overview of the recommended start-up sequence is illustrated in Figure 11. This Figure indicates steady state conditions, transient state conditions and associated signaling flags to indicate state transitions. A complete description is defined in the MDIO management interface specification [15].

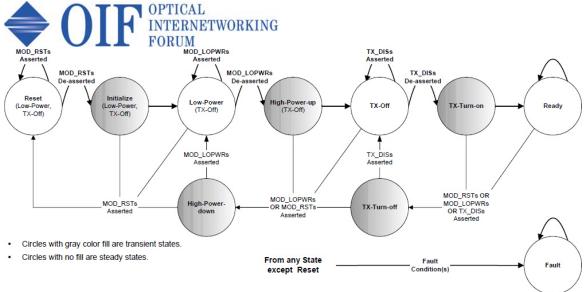


Figure 11: MSA-100GLH Simplified Start-Up Flow Diagram

The MSA-100GLH is designed to support a range of optical transport applications. Many of the timing parameters associated with the module hardware control and alarm pins are application specific and thus are not specified in this IA. A summary of the timing parameters for the MSA-100GLH is given in Table 9.

Parameter	Symbol	Min	Max	Unit	Notes
Transmitter Disabled	t_off				Application specific.
(TX_DIS asserted)					Defined by module
					vendor.
Transmitter Enabled	t_on				Application specific.
(TX_DIS de-asserted)					Defined by module
					vendor.
MOD_LOPWR on	t_MOD_LOPWR_on				Application specific.
					Defined by module
					vendor.
MOD_LOPWR off	t_MOD_LOPWR_off				Application specific.
					Defined by module
					vendor.
Module Reset Assert	MOD_RSTn				Application specific.
					Defined by module
					vendor.
Module Reset De-assert	MOD_RSTn				Application specific.
					Defined by module
		-			vendor.
Module Absent	MOD_ABS				Application specific.
					Defined by module
					vendor.
Receiver Loss of Signal	t_loss_on				Application specific.
Assert Time					Defined by module
					vendor.
Receiver Loss of Signal	t_loss_off				Application specific.

Table 9: Hardware	Signaling F	Pins Timing	Parameters Summary



De-assert Time	OITOM				Defined by module
					vendor.
Global Alarm Assert	t_GLB_ALRMn_on				This is a logical
Delay Time					"OR" of associated
					MDIO alarm &
					status registers. See
					MDIO spec for
					details.
Global Alarm De-assert	t_GLB_ALRMn_off				This is a logical
Delay Time					"OR" of associated
-					MDIO alarm &
					status registers. See
					MDIO spec for
					details.
Management Interface	t _{prd}	250		ns	MDC is 4 MHz rate;
Clock Period	-				duty cycle =
					50% ± 10% (typ.)
Host MDIO setup time	t _{setup}	10		ns	
Host MDIO hold time	t_{hold}	10		ns	
Module MDIO delay	$\mathbf{t}_{ ext{delay}}$		175	ns	
time					
Performance					Default period=1 sec.
Monitoring					; min high/low time
Synchronization					= 100msec.
(PM_SYNC) (optional)					

9 <u>Mechanical Specifications</u>

9.1 Mechanical Overview

The MSA-100GLH is designed to be assembled into a host system line card. The MSA-100GLH is electrically connected to the host line card by a 168 position connector specified herein and is physically fastened to the host line card by mounting screws through the host line card PCB. The MSA-100GLH supports two optical fiber pigtails, one for optical transmit and one for optical receive. These optical fiber pigtails are terminated and attached to host line card face plate. The MSA-100GLH is not designed to be hot-pluggable. Its power and initialization sequencing in the host line card are specified by the host line card and transponder vendors.

9.2 Electrical Connector

The Hirose FX10A-168P/S-SV(83) connector assembly [N3] is specified for the host line card – MSA-100GLH electrical connector. This connector is a two component (header, receptacle), 168 position, board mounted style assembly. It meets CEI-11G-MR [N2] signal integrity performance and provides 4mm - 8mm mated stack height flexibility by header component changes only, i.e. the MSA-100GLH receptacle component remains fixed. Detailed mechanical specifications and layout design application notes may be found at [N3].

The Hirose FX10B-168P/S-SV(83) connector assembly [N3] is also specified as an option for the host line card – MSA-100GLH electrical connector. The FX10A connector style has guidepost



features whereas the FX10B style does not. The FX10A and FX10B components are mate compatible and may be interchanged. Manufacturers can select either FX10A or FX10B version as appropriate for their design flow.

9.2.1 Module Electrical Connector

The MSA-100GLH electrical connector is the Hirose FX10A-168S-SV(83) receptacle connector assembly[N3] illustrated in Figure 12. Pin orientation is also indicated in Figure 12. The Hirose FX10B-168S-SV(83) receptacle is also an option for the MSA-100GLH electrical connector.

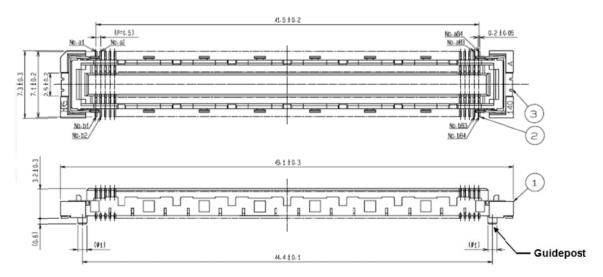


Figure 12: Hirose FX10A-168S-SV(83) Receptacle Connector Assembly

9.2.2 Host Electrical Connector

The host line card electrical connector is the Hirose FX10A-168P-SV(83) header connector assembly[N3] illustrated in Figure 13. Pin orientation is also indicated in Figure 13. The Hirose FX10B-168P-SV(83) header is also an option for the host line card electrical connector.

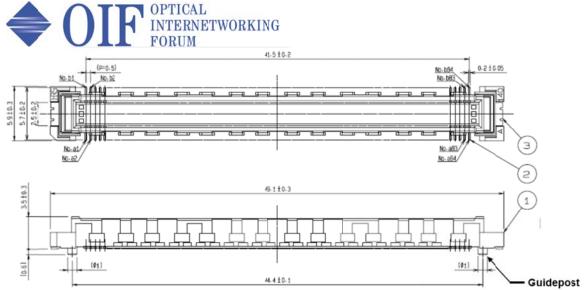


Figure 13: Hirose FX10A-168P-SV(83) Header Connector Assembly

9.2.3 Host-Module Connector Alignment

For alignment of host – MSA 100GLH connector mating, misalignment should be smaller that the maximum allowable misalignment value of the connector (CN) mating. Maximum gap between the connector guide pin (GP) and the PCB guide pin hole (GH) is:

Maximum Gap =

$$\frac{\phi GH - \phi GP}{2} \le \text{Maximum misalignment of the CN}$$

to assure CN mating after inserting guide pins into the guide pin hole. If

Maximum Gap =

$$\frac{\phi GH - \phi GP}{2} \ge \text{Maximum misalignment of the CN}$$

this may cause connector and contact deformation. Tolerance of GP and GH is defined in Figure 14. Maximum allowable misalignment should be ≤ 0.42 mm for FX10.



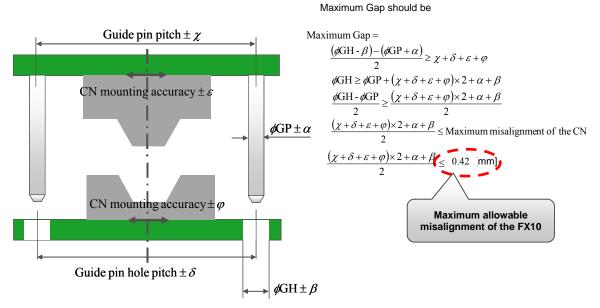


Figure 14: FX10 Connector Alignment

9.3 Module Dimensions

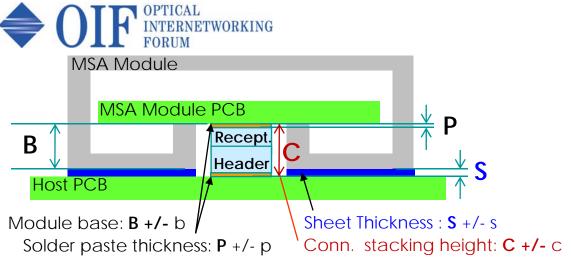
Two options are specified for the MSA-100GLH mechanical dimensions:

- 1) Flattop
- 2) Integrated Heat Sink

The flattop option is specified to allow customization of the MSA-100GLH bolt-on heat sink for supporting a wide array of optical transport applications. With this option, the bolt-on heat sink is specified by the host system designer, allowing maximum flexibility in their system design while maintaining a common module form factor.

The integrated heat sink option is specified to simplify the host system design and supports module thermal performance per the maximum power consumption specified in Section 8.2.

Mechanical dimensions of the MSA-100GLH with non-conductive sheet are specified in Figure 15. If a non-conductive sheet is used, the thickness is specified as 0.15 ± 0.05 mm.



Module and Host PCB dimensions and tolerances in mm.

Figure 15: MSA-100GLH Non-conductive Sheet Dimensions

Note: The module vendor must ensure the module connector receptacle component is placed to enable the module to properly mate with the host connector header when the minimum height header component (i.e. C=4mm) is used by the host.

9.3.1 Flattop

Mechanical dimensions of the MSA-100GLH flattop module are specified in Figure 16. The maximum module size is specified as: 101.6mm x 127.0mm (4" x 5")

Figure 16 also specifies the receptacle connector position, connector guide pin locations and module mounting hole locations.



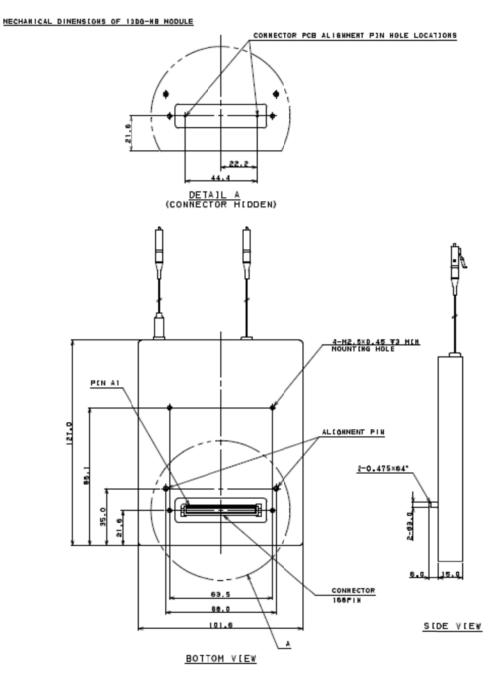


Figure 16: MSA-100GLH Flattop mechanical dimensions - bottom/side views

The module heat sink mounting hole locations for the flattop option are specified in Figure 17. These mounting holes are not applicable to the MSA-100GLH with an integrated heat sink.



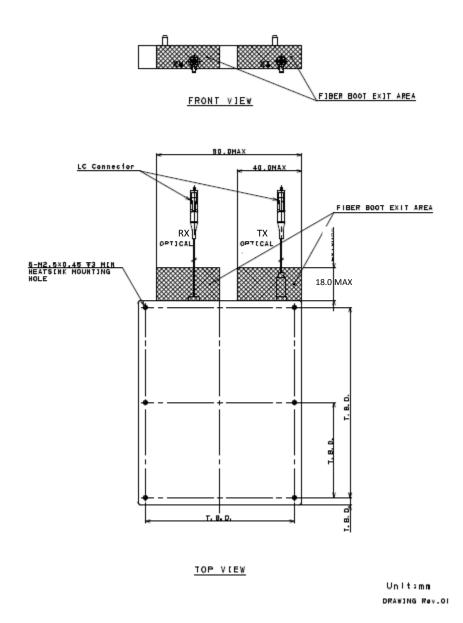


Figure 17: MSA-100GLH Flattop mechanical dimensions - top view

9.3.2 Integrated Heat Sink

Mechanical dimensions of the MSA-100GLH with integrated heat sink are specified in Figure 17. The maximum module size is specified as: 101.6mm x 127.0mm (4" x 5")

Figure 17 also specifies the receptacle connector position, connector guide pin locations and module mounting hole locations.

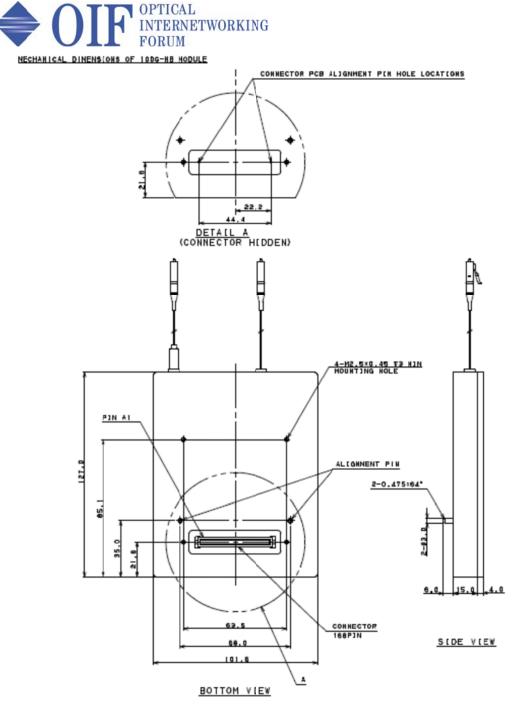


Figure 18: Mechanical Dimensions of MSA-100GLH with Integrated Heat Sink

The top view of the MSA-100GLH is illustrated in Figure 19. The integrated heat-sink fin orientation and dimensions are module-vendor specific and are not specified in this document. However, the module height is required to fit within the maximum height dimension specified in Figure 17.



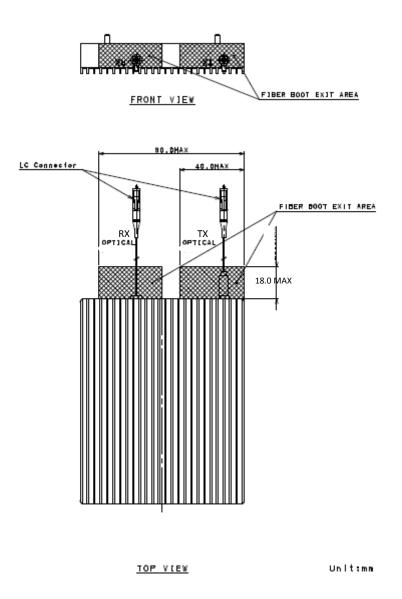


Figure 19: MSA-100GLH with Integrated Heat Sink - top view

9.4 Host System Dimensions

The recommended host system dimensions including host board layout are given in Figure 20. PCB design guidelines for the Hirose FX10 connector assembly may be found at Reference [I4].



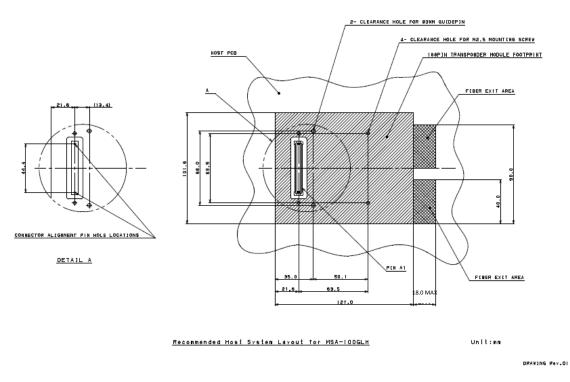


Figure 20: Recommended Host System Layout for MSA-100GLH

9.5 Module Optical Fiber Ports

The MSA-100GLH optical transmit and receive fiber pigtail port location, dimensions and orientation are specified in Figure 21. The fiber pigtail type, length and connector type parameters are vendor specified and not specified in this document. The fiber boot exit area is solely for the purpose of indicating where the fibers are to exit the module side-wall with fiber boots for strain relief.

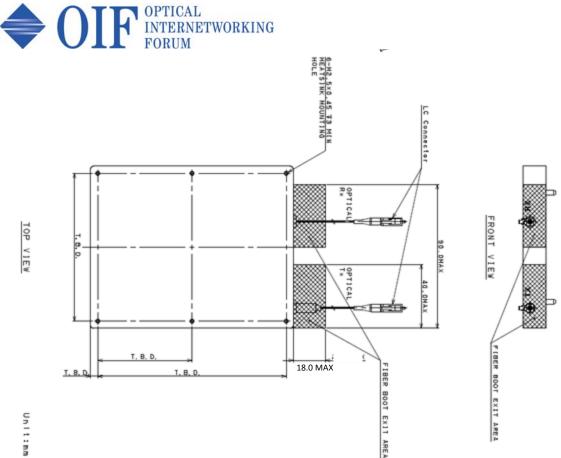


Figure 21: MSA-100GLH Optical Fiber Port Location and Dimensions

9.6 Pin Assignment

The MSA-100GLH electrical connector has 168 pin positions that are arranged in a dual-row assembly. The pin assignment is specified in Table 10. Detailed description of the pin assignment is given in





Table 10: MSA-100GLH Pin-Map (Note: Pins for future use (FFU) should be left unconnected on both the host board and the MSA module)

B84 12V A84 12V B83 12V A83 12V B81 12V A81 12V B81 12V GND A71 GND B87 TXMCLKN A73 GND A74 B73 TXON A73 GND A74 B71 TXOP A71 GND A74 B71 TXOP A63 GND A68 B66 GND A68 RX1n B65 B66 GND A63 GND B65 B63 TX2n A63 GND B65				
B82 12V A82 12V B81 12V_GND A81 12V_GND B80 12V_GND A81 12V_GND B87 12V_GND A81 12V_GND B71 TXMCLKn A73 12V_GND B77 TXMCLKP A75 GND B76 TXMCLKP A75 GND B73 TXMCLKP A75 GND B74 GND A74 RXMCLKP B73 TXMCLK A73 GND B74 GND A74 RXMCLKP B73 TXMCLK A73 GND B74 GND A74 RXMCLKP B71 TX0 A71 GND B68 GND A68 RX1 B66 GND A66 RX1 B66 GND A66 RX1 B66 GND A68 RX3 B63 TX2 A63 GND B64<	B84	12V	A84	12V
B81 12V_GND A81 12V_GND B80 12V_GND A80 12V_GND B80 12V_GND A71 12V_GND B79 12V_GND A71 12V_GND B77 TXMCLKN A77 GND B76 GND A74 RXMCLKN B75 TXMCLKP A75 GND B74 GND A74 RXMCLKN B73 TX0n A73 GND B74 GND A73 GND B71 TX0p A71 GND B71 TX0p A71 GND B76 GND A68 RX1n B66 GND A68 RX1n B66 GND A66 RX1n B67 TX1p A63 GND B64 GND A64 RX2p B63 TX2p A63 GND B57 TX4n A57 GND B58			A83	12V
B80 12V_GND A80 12V_GND B79 12V, GND A71 B70 B77 GND A71 GND B78 GND A78 MOD_ABS B77 TXMCLKn A77 GND B76 GND A74 RXMCLKn B73 TXMCLKp A73 GND B73 TX0n A73 GND B73 TX0n A73 GND B73 TX0n A73 GND B73 TX0n A73 RX0n B73 TX0n A73 RX0n B70 GND A71 GND B66 GND A66 RX1n B66 GND A66 RX1n B66 GND A66 RX1n B67 TX1p A63 GND B64 GND A68 RX3p B65 TX2p A63 GND B58 GND		12V	A82	
B80 12V_GND A80 12V_GND B79 12V, GND A71 B70 B77 GND A71 GND B78 GND A78 MOD_ABS B77 TXMCLKn A77 GND B76 GND A74 RXMCLKn B73 TXMCLKp A73 GND B73 TX0n A73 GND B73 TX0n A73 GND B73 TX0n A73 GND B73 TX0n A73 RX0n B73 TX0n A73 RX0n B70 GND A71 GND B66 GND A66 RX1n B66 GND A66 RX1n B66 GND A66 RX1n B67 TX1p A63 GND B64 GND A68 RX3p B65 TX2p A63 GND B58 GND	B81	12V_GND	A81	12V_GND
B78 GND A78 MOD ABS B77 TXMCLKn A77 GND B76 GND A76 RXMCLKn B75 TXMCLKP A75 GND B73 TX0 A73 GND B70 GND A71 GND B66 GND A66 RX1n B66 GND A66 RX1n B65 TX2n A63 GND B64 GND A64 RX2n B65 TX4n A57 GND B55 TX4n A57 GND B55 TX4n A57 GND B55 TX4n	B80	12V_GND	A80	12V_GND
B77 TXMCLKn A76 RXMCLKn B75 TXMCLKp A75 GND B74 GND A74 RXMCLKp B73 TXMCL A75 GND B74 GND A72 GND B73 TXMCL A72 GND B71 TX0n A73 GND B70 GND A71 GND B71 TX0p A71 GND B70 GND A71 GND B60 TX1n A69 GND B66 GND A66 RX1n B66 GND A66 RX1n B61 TX2n A63 GND B62 GND A68 RX3n B63 TX2p A63 GND B64 GND A56 RND B55 GND A53 RX3n B54 GND A54 RX4p B53 TX5n				
B76 GND A76 RXMCLKp B74 GND A74 RXMCLKp B73 TX0n A73 GND B72 GND A72 RX0n B71 TX0p A71 GND B70 GND A70 RX0p B69 TX1p A69 GND B66 GND A68 RX1n B66 GND A68 RX1p B66 GND A68 RX1p B66 GND A68 RX1p B66 GND A64 RX2n B63 TX2p A65 GND B64 GND A68 RX3n B65 TX3n A61 GND B66 GND A58 RX4p B58 GND A52 GND B54 GND A54 RX4p B55 TX4p A50 RX5p B44 GND <td< td=""><td>B78</td><td>GND</td><td>A78</td><td>MOD_ABS</td></td<>	B78	GND	A78	MOD_ABS
B75 TXMCLKp A75 GND B74 RXMCLKp A73 GND B73 TX0n A73 GND B71 TX0n A73 GND B71 TX0p A71 GND B71 TX0p A71 GND B71 TX0p A71 GND B66 GND A68 RX1n B67 TX1p A67 GND B66 GND A66 RX1p B66 GND A63 RX2n B61 TX3n A63 GND B62 GND A63 RX3p B57 TX4n A57 GND B63 RX5p A53 GND B56 GND A56 RX4n B55 TX4n A55 GND B56 GND A51 GND B54 GND A51 GND B54 GND A				
B74 GND A74 RXMCLKp B72 GND A72 RX0n B71 TX0p A71 GND B71 TX0p A71 GND B70 GND A70 RX0p B69 TX1n A69 GND B69 TX1n A67 GND B66 GND A66 RX1n B67 TX1p A67 GND B66 GND A66 RX1n B67 TX1n A67 GND B63 TX2p A63 GND B64 GND A62 RX2p B63 TX2p A63 GND B64 GND A56 GND B55 GND A56 GND B56 GND A56 GND B53 TX5n A53 GND B54 GND A54 RX4p B53 TX5n A53<				
B73 TX0n A73 GND B72 GND A71 GND B71 TX0p A71 GND B70 GND A70 RX0p B69 TX1n A69 GND B68 GND A68 RX1n B66 GND A66 RX1p B66 GND A66 RX1p B66 GND A62 RX2n B63 TX2p A63 GND B64 GND A62 RX2p B66 GND A62 RX2p B61 TX3n A61 GND B56 GND A56 RX4n B53 TX4n A57 GND B56 GND A52 GND B51 TX5n A53 GND B52 GND A52 RX6n B44 GND A44 RX6n B47 TX6n A43 <td></td> <td></td> <td></td> <td></td>				
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B35 TX9p A35 GND B34 GND A34 RX9p B33 TXDSCn A33 GND B33 TXDSCn A33 GND B32 GND A32 RXDSCn B31 TXDSCp A31 GND B30 GND A32 RXDSCn B31 TXDSCp A31 GND B30 GND A32 RXDSCp B31 TXDSCp A31 GND B20 REFCLKn A29 GND B23 RTADR4 A25 VND IO B26 GND A26 GND B26 GND A26 GND B26 FRTADR3 A24 VND IO B21 PRTADR1 A22 VND IO B22 PRTADR1 A20 VND IO B20 PRG_CNTL2 A19 VND IO B19 PRG_CNTL3 A18 VND IO				
B34 GND A34 RX9p B33 TXDSCn A33 GND B32 GND A33 GND B31 TXDSCp A31 GND B31 TXDSCp A31 GND B30 GND A30 RXDSCn B31 TXDSCp A31 GND B30 GND A30 RXDSCn B30 GND A30 RXDSCp B29 REFCLKp A27 MDC B26 GND A26 GND B26 GND A26 GND B26 PRTADR3 A24 VND IO B23 PRTADR3 A24 VND IO B23 PRTADR3 A24 VND IO B21 PRTADR3 A24 VND IO B22 PRTADR1 A20 VND IO B20 PRG_CNTL2 A19 VND IO B19 PRG_CNTL2 A19 VND IO G				
B33 TXDSCn A33 GND B32 GND A32 RXDSCn B31 TXDSCp A31 GND B31 TXDSCp A31 GND B31 TXDSCp A31 GND B30 GND A30 RXDSCp B29 REFCLKn A28 MDIO B27 REFCLKp A27 MDC B26 GND A28 MDIO B27 REFCLKp A27 MDC B26 RTADR3 A24 VND 0 B25 PRTADR3 A24 VND 0 B23 PRTADR4 A25 VND 0 B21 PRTADR2 A23 VND 0 B21 PRTADR1 A22 VND 0 E B19 PRG_CNTL1 A10 VND 0 E B18 PRG_ALRM1 A16 GND A13 FFU B14				
B32 GND A32 RXDSCn B31 TXDSCp A31 GND B30 GND A30 RXDSCp B39 GND A30 RXDSCp B29 REFCLKn A29 GND B28 GND A28 MDIO B27 REFCLKp A27 MDC B26 GND A26 GND B26 GND A26 GND B26 GND A26 GND B27 REFCLKp B27 MDC B26 GND A26 GND B27 B26 GND A28 VND IO A B23 PRTADR2 A23 VND IO B B20 PRG_CNTL2 A19 VND IO E B19 PRG_CNTL3 A18 VND IO G B16 PRG_ALRM3 A15 VND IO J B14 PRG_ALRM3 A11 RX ALRM_OUT <td></td> <td></td> <td></td> <td></td>				
B31 TXDSCp A31 GND B30 GND A30 RXDSCp B29 REFCLKn A30 GND B28 GND A30 RXDSCp B29 REFCLKn A29 GND B26 GND A28 MDIO B27 REFCLKp A27 MDC B26 GND A26 GND B27 REFCLKP A27 MDC B26 GND A28 VID D B26 GND A28 VID D B25 PRTADR3 A24 VND IO A B22 PRTADR3 A22 VND IO D B21 PRTADR1 A22 VND IO D B21 PRADR1 A10 GND A11 RX IND IO F B19 PRG_CNTL2 A19 VND IO F B16 PRG_ALRM3 A14<				
B30 GND A30 RXDSCp B29 REFCLKn A29 GND B28 GND A28 MDIO B27 REFCLKp A27 MDC B27 REFCLKp A27 MDC B26 GND A26 GND B25 PRTADR4 A25 VND IO A B24 PRTADR3 A24 VND IO B B23 PRTADR2 A23 VND IO C B22 PRTADR1 A22 VND IO C B23 PRTADR2 A23 VND IO C B21 PRG_CNTL1 A10 VND IO E B19 PRG_CNTL2 A18 VND IO F B18 PRG_ALRM1 A16 GND B15 PRG_ALRM3 A14 VND IO K B13 PRG_ALRM3 A14 VND IO K B14 PRG_ALRM3 A14 RX ALRM_IN B11 TX DIS A11 RX ALRM_IOUT B14 PRG_ALRM2 <td></td> <td></td> <td></td> <td></td>				
B29 REFCLKn A29 GND B28 GND A28 MDIO B27 REFCLKp A27 MDIO B27 REFCLKP A27 MDIO B26 GND A26 GND B26 GND A26 GND B26 GND A26 GND B25 PRTADR4 A25 VND_IO_A B24 PRTADR2 A23 VND_IO_C B22 PRTADR1 A22 VND_IO_C B21 PRTADR2 A23 VND_IO_E B20 PRG_CNTL1 A20 VND_IO_F B18 PRG_CNTL3 A18 VND_IO_G B17 GND A17 VND_IO_H B16 PRG_ALRM2 A15 VND_IO_K B13 PM_GALRM3 A14 VND_IO_K B13 PM_OD_RSTN A17 FFU B8 RX_LOS A8 FFU B8 RX_LOS A8 <				
B28 GND A28 MDIO B27 REFCLKp A27 MDC B26 GND A26 GND B25 PRTADR4 A25 VND_IO_A B25 PRTADR3 A24 VND_IO_B B23 PRTADR3 A24 VND_IO_C B21 PRTADR1 A22 VND_IO_D B22 PRTADR1 A22 VND_IO_D B21 PRTADR0 A21 GND B20 PRG_CNTL1 A20 VND_IO_E B19 PRG_CNTL2 A19 VND_IO_F B18 PRG_CNTL3 A18 VND_IO_G B16 PRG_ALRM1 A16 GND B15 PRG_ALRM3 A14 VND_IO_K B13 PM_SYNC A11 RX_ALRM_OUT B10 MOD_LOPWR A11 RX_ALRM_OUT B10 MOD_RSTIN A9 FFU B4 RS_LOS A8 FFU B5 12V_GND			A30	RXDSCp
B27 REFCLKp A27 MDC B26 GND A26 GND A26 GND B25 PRTADR4 A25 VND IO A A24 VND IO B B24 PRTADR3 A24 VND IO B A23 VND IO C B23 PRTADR2 A23 VND IO C B22 PRTADR1 A22 VND IO C B21 PRTADR1 A22 VND IO C B32 PRTADR1 A22 VND IO C B21 PRG_CNTL1 A10 VND IO F B18 PRG_CNTL2 A18 VND IO F B18 PRG_CNTL3 A18 VND IO F A17 VND IO H B16 PRG_ALRM1 A16 GND A17 VND IO J B15 PRG_ALRM3 A14 VND IO K A13 FFU B11 TX DIS A11 RX ALRM IN A11 RX ALRM_OUT B10 MOD_LOPWR A10 FFU B8 RX_LOS A8 FFU B16<				
B26 GND A26 GND B25 PRTADR4 A25 VND_IO_A B24 PRTADR3 A24 VND_IO_B B23 PRTADR2 A23 VND_IO_D B22 PRTADR1 A22 VND_IO_D B21 PRTADR0 A21 GND B20 PRG_CNTL1 A20 VND_IO_E B19 PRG_CNTL2 A18 VND_IO_F B18 PRG_CNTL3 A18 VND_IO_G B17 GND A17 VND_IO_H B16 PRG_ALRM1 A16 GND B17 GND A12 VND_IO_K B13 PRG_ALRM2 A15 VND_IO_K B13 PM_SYNC A13 FFU B10 MOD_LOPWR A10 FFU B9 MOD_LOPWR A11 RX_ALRM_OUT B16 12V_GND A5 12V_GND B3 12V A3 12V B3 12V				
B25 PRTADR4 A25 VND_IO_A B24 PRTADR3 A24 VND_IO_B B23 PRTADR2 A23 VND_IO_C B22 PRTADR1 A22 VND_IO_D B23 PRTADR1 A22 VND_IO_D B20 PRG_CNTL1 A20 VND_IO_F B19 PRG_CNTL2 A19 VND_IO_F B19 PRG_CNTL3 A18 VND_IO_G B16 PRG_ALRM1 A16 GND B15 PRG_ALRM3 A14 VND_IO_K B13 PM_SYNC A13 FFU B10 MOD_RSTIN A9 FFU B8 RX_LOS A8 FFU B6 12V_GND A6 12V_GND B5 12V_GND A5 12V_GND B3 12V A3 12V				
B24 PRTADR3 A24 VND_IO_B B23 PRTADR1 A23 VND_IO_C B21 PRTADR1 A22 VND_IO_D B21 PRTADR0 A21 GND B21 PRTADR1 A22 VND_IO_C B21 PRTADR0 A21 GND B20 PRTADR1 A20 VND_IO_E B19 PRG_CNTL1 A19 VND_IO_F B19 PRG_CNTL3 A18 VND_IO_G B17 GND A17 VND_IO_H B16 PRG_ALRM1 A16 GND B15 PRG_ALRM2 A15 VND_IO_K B13 PM_SYNC A13 FFU B11 TX_DIS A11 RX_ALRM_IN B11 TX_DIS A11 RX_ALRM_OUT B10 MOD_LOPWR A10 FFU B8 RX_LOS A8 FFU B6 12V_GND A5 12V_GND B3 12V				
B23 PRTADR2 A23 VND IO C B22 PRTADR1 A22 VND IO D B21 PRTADR0 A21 GND B20 PRG_CNTL1 A20 VND IO E B19 PRG_CNTL2 A19 VND IO F B18 PRG_CNTL3 A18 VND IO F B16 PRG_ALRM1 A16 GND B15 PRG_ALRM2 A15 VND IO K B14 PRG_ALRM3 A14 VND IO K B13 PMS YNC A13 FFU B14 PRG_ALRM3 A14 VND IO K B13 PM SYNC A13 FFU B11 TX_DIS A11 RX_ALRM_IN B11 TX_DIS A11 RX_ALRM_OUT B16 12V_GND A5 12V_GND B4 12V_GND A5 12V_GND B3 12V A3 12V				
B22 PRTADR1 A22 VND_IO_D B21 PRG_CNTL1 A21 GND B20 PRG_CNTL2 A19 VND_IO_F B19 PRG_CNTL3 A18 VND_IO_F B16 PRG_CNTL3 A18 VND_IO_H B16 PRG_ALRM1 A16 GND B15 PRG_ALRM2 A15 VND_IO_J B13 PMG_SALRM3 A14 VND_IO_K B13 PMG_SALRM3 A11 RX_ALRM_IN B14 PRG_ALRM3 A11 RX_ALRM_OUT B12 GND A12 RX_ALRM_OUT B14 PRG_ALRM3 A11 RX_ALRM_OUT B14 PRG_ALRM3 A11 RX_ALRM_OUT B14 PRG_ALRM3 A11 RX_ALRM_OUT B14 PRG_ALRM3 A11 RX_ALRM_OUT B16 IZV_GND A6 <i>FFU</i> B8 RX_LOS A8 <i>FFU</i> B6 IZV_GND A5 IZV_GND <tr< td=""><td></td><td></td><td></td><td></td></tr<>				
B21 PRTADR0 A21 GND B20 PRG_CNTL1 A20 VND_IO_E B19 PRG_CNTL2 A19 VND_IO_F B18 PRG_CNTL3 A18 VND_IO_G B17 GND A17 VND_IO_H B16 PRG_ALRM1 A16 GND B15 PRG_ALRM2 A15 VND_IO_J B14 PRG_ALRM3 A14 VND_IO_K B13 PM_SYNC A13 FFU B14 RX ALRM_0 A12 B10 MOD_LOPWR A11 RX ALRM_IN B11 TX_DIS A11 RX ALRM_OUT B10 MOD_LOPWR A10 FFU B8 RX_LOS A8 FFU B4 B2V_GND A5 12V_GND B5 12V_GND A5 12V_GND B3 12V A3 12V				
B20 PRG_CNTL1 A20 VND_IO_E B19 PRG_CNTL2 A19 VND_IO_F B18 PRG_CNTL3 A19 VND_IO_F B17 GND A17 VND_IO_H B16 PRG_ALRM1 A16 GND B15 PRG_ALRM2 A15 VND_IO_H B14 PRG_ALRM3 A14 VND_IO_K B13 PMG_ALRM3 A14 VND_IO_K B13 PMG_ALRM3 A14 VND_IO_K B13 PM_SYNC A13 FFU B12 GND A12 RX_ALRM_IN B11 TX_DIS A11 RX_ALRM_OUT B10 MOD_LOPWR A10 FFU B8 RX_LOS A8 FFU B6 12V_GND A6 12V_GND B4 12V_GND A4 12V_GND B3 12V A3 12V				
B19 PRG_CNTL2 A19 VND_IO_F B18 PRG_CNTL3 A18 VND_IO_G B17 GND A17 VND_IO_G B16 PRG_ALRM1 A16 GND B14 PRG_ALRM2 A15 VND_IO_J B13 PRG_ALRM3 A14 VND_IO_K B13 PRG_SOL A13 FFU B12 GND A12 RX_ALRM_OUT B14 PRG_ALRM3 A14 VND_IO_J B13 PM_SYNC A13 FFU B12 GND A12 RX_ALRM_OUT B11 RX_ALRM A11 RX_ALRM_OUT B10 MOD_LOPWR A10 FFU B1 B2 GND A6 FFU B1 B2 GND A5 12V_GND B5 12V_GND A5 12V_GND A3 B3 12V A3 12V A3				
B18 PRG_CNTL3 A18 VND_IO_G B17 GND A17 VND_IO_H B16 PRG_ALRM1 A16 GND B15 PRG_ALRM2 A15 VND_IO_J B14 PRG_ALRM3 A14 VND_IO_K B13 PM_SYNC A13 FFU B12 GND A12 RX_ALRM_IN B11 TX_DIS A11 RX_ALRM_OUT B10 MOD_LOPWR A10 FFU B8 RX_LOS A8 FFU B6 12V_GND A6 12V_GND B5 12V_GND A5 12V_GND B3 12V A3 12V				
B17 GND A17 VND IO_H B16 PRG_ALRM1 A16 GND B15 PRG_ALRM2 A15 VND IO_J B14 PRG_ALRM3 A14 VND IO_K B13 PM_SYNC A13 FFU B14 PRG_ALRM3 A14 VND IO_K B13 PM_SYNC A13 FFU B12 GND A12 RX_ALRM_IN B11 TX_DIS A11 RX_ALRM_OUT B10 MOD_LOPWR A10 FFU B8 RX_LOS A8 FFU B6 12V_GND A6 12V_GND B5 12V_GND A5 12V_GND B3 12V A3 12V				
B16 PRG_ALRM1 A16 GND B15 PRG_ALRM2 A15 VND IO_J B14 PRG_ALRM3 A14 VND_IO_K B13 PRG_SYNC A13 FFU B12 GND A12 RX_ALRM_IN B11 TX_DIS A11 RX_ALRM_OUT B10 MOD_LOPWR A10 FFU B9 MOD_RSTn A9 FFU B6 T2V_GND A6 TEV_GND B5 12V_GND A5 12V_GND B3 12V A3 12V B3 12V A3 12V				
B15 PRG_ALRM2 A15 VND_IO_J B14 PRG_ALRM3 A14 VND_IO_K B13 PMS_ALRM3 A14 VND_IO_K B13 PMS_ALRM3 A13 FFU B12 GND A12 RX_ALRM_IN B11 TX_DIS A11 RX_ALRM_OUT B10 MOD_LOPWR A10 FFU B9 MOD_RSTIN A9 FFU B6 RX_LOS A8 FFU B6 12V_GND A6 12V_GND B5 12V_GND A5 12V_GND B3 12V A3 12V B2 12V A2 12V				
B14 PRG_ALRM3 A14 VND_IO_K B13 PM_SYNC A13 FFU B12 GND A12 RX ALRM_IN B11 TX_DIS A11 RX_ALRM_IN B11 TX_DIS A11 RX_ALRM_OUT B0 MOD_LOPWR A10 FFU B8 RX_LOS A8 FFU B6 12V_GND A6 12V_GND B5 12V_GND A5 12V_GND B3 12V A3 12V				
B12 GND A12 RX_ALRM_IN B11 TX_DIS A11 RX_ALRM_OUT B10 MOD_LOPWR A10 FFU B9 MOD_RSTn A9 FFU B7 GLB_ALRMn A7 FFU B6 12V_GND A6 12V_GND B5 12V_GND A5 12V_GND B3 12V A3 12V B3 12V A2 12V				
B12 GND A12 RX_ALRM_IN B11 TX_DIS A11 RX_ALRM_OUT B10 MOD_LOPWR A10 FFU B9 MOD_RSTn A9 FFU B7 GLB_ALRMn A7 FFU B6 12V_GND A6 12V_GND B5 12V_GND A5 12V_GND B3 12V A3 12V B3 12V A2 12V	B13	PM_SYNC	A13	FFU
B11 TX DIS A11 RX ALRM_OUT B10 MOD_LOPWR A10 FFU B10 MOD_RSTn A9 FFU B8 RX_LOS A8 FFU B6 12V_GND A6 12V_GND B6 12V_GND A6 12V_GND A5 12V_GND B3 12V A3 12V A3 12V	B12	GND	A12	RX_ALRM_IN
B9 MOD_RSTn A9 FFU B8 RX_LOS A8 FFU B7 GLB_ALRMn A7 FFU B6 12V_GND A6 12V_GND B4 12V_GND A5 12V_GND B3 12V A3 12V_GND B2 12V A2 12V	B11	TX_DIS		RX_ALRM_OUT
B9 MOD_RSTn A9 FFU B8 RX_LOS A8 FFU B7 GLB_ALRMn A7 FFU B6 12V_GND A6 12V_GND B4 12V_GND A5 12V_GND B3 12V A3 12V_GND B2 12V A2 12V	B10	MOD_LOPWR		
B7 GLB ALRMn A7 FFU B6 12V_GND A6 12V_GND B5 12V_GND A5 12V_GND B4 12V_GND A4 12V_GND B3 12V A3 12V B2 12V A2 12V	B9	MOD_RSTn	A9	
B6 12V_GND A6 12V_GND B5 12V_GND A5 12V_GND B4 12V_GND A4 12V_GND B3 12V A3 12V B2 12V A2 12V	B8	RX_LOS	A8	
B6 12V_GND A6 12V_GND B5 12V_GND A5 12V_GND B4 12V_GND A4 12V_GND B3 12V A3 12V B2 12V A2 12V		GLB_ALRMn		
B4 12V_GND A4 12V_GND B3 12V A3 12V B2 12V A2 12V		12V GND		12V_GND
B4 12V_GND A4 12V_GND B3 12V A3 12V B2 12V A2 12V				
B2 12V A2 12V		12V_GND		12V_GND
	0.00	12V		
B1 12V A1 12V			A2	
	B2			



	100G	1/0	Logic	Description
B84				+12V Module Supply Voltage
B83 B82		-		
	12V GND	-		+12V Module Supply Voltage Return Ground, can be seperate or tied together with Signal Ground
	12V_GND			
B79 B78		-		Ground
	XMCLKn	0	CML	Transmit Monitor Clock, negative leg
B76	GND	0	CM	Transmit Hanitas Clash, nasiliya las
B74	TXMCLKp GND	Ŭ	CML	Transmit Monitor Clock, positive leg
	TX0n	1	CML	Transmit Data 0, negative leg
B72 B71	TX0p	1	CML	Transmit Data 0, positive leg
B70	GND			
B69 B68	TX1n GND	1	CML	Transmit Data 1, negative leg
B67	TX1p	1	CML	Transmit Data 1, positive leg
B66	GND TX2n	1	CML	Transmit Data 2. negative leg
B64	GND			1.18U.24U.0.5.8U.0.8.81.1.8.9
B63 B62	TX2p GND	1	CML	Transmit Data 2, positive leg
	TX3n	1	CML	Transmit Data 3, negative leg
B60	GND		CMI	
B59 B58	TX3p GND		CML	Transmit Data 3, positive leg
B57	TX4n	1	CML	Transmit Data 4, negative leg
B56 B55	GND TX4p	1	CML	Transmit Data 4, positive leg
B54	GND			
B53 B52	TX5n GND	1	CML	Transmit Data 5, negative leg
B51	TX5p	1	CML	Transmit Data 5, positive leg
B50	GND TX6n		CML	Transmit Data 6, negative leg
B49			CML.	Transmit Data 0, negative reg
	ТХбр	1	CML	Transmit Data 6, positive leg
B46 B45	GND TX7n	1	CML	Transmit Data 7, negative leg
B44	GND			
B43 B42	TX7p GND	1	CML	Transmit Data 7, positive leg
B41	TX8n	1	CML	Transmit Data 8, negative leg
B40	GND TX8p	1	CML	Transmit Data 8, positive leg
B38	GND			menanic outers, positive reg
B37 B36	TX9n	1	CML	Transmit Data 9, negative leg
	ТХ9р	1	CML	Transmit Data 9, positive leg
B34				Transmit Dankar Obarral analysis in (OT) O anto alternize an analysis
B32	TXDSCn GND	1	CML	Transmit Deskew Channel, negative leg (SFI-S only, otherwise no connect)
	TXDSCp	1	CML	Transmit Deskew Channel, positive leg (SFI-S only, otherwise no connect)
B30 B29	GND REFCLKn	1	CML	Reference Clock, negative leg
B28	GND			
B27 B26	REFCLKp	1	CML	Reference Clock, positive leg
B25	PRTADR4		1.2V CMOS	MDIO port address bit 4
	PRTADR3 PRTADR2	1	1.2V CMOS 1.2V CMOS	MDIO port address bit 3 MDIO port address bit 2
	PRTADR2	1	1.2V CMOS	MDIO port address bit 2 MDIO port address bit 1
B21	PRTADRO		1.2V CMOS	MDIO port address bit 0
	PRG_CNTL1 PRG_CNTL2			Programmable Control 1 set over NDIO Programmable Control 2 set over NDIO
B18	PRG_CNTL3			Programmable Control 3 set over MDIO
B17 B16	GND PRG_ALRM1	0	LVCMOS	Programmable Alarm 1 set over MDIO
B15	PRG_ALRM2	0	LVCMOS	Programmable Alarm 2 set over MDIO
	PRG_ALRM3 PM_SYNC		LVCMOS LVCMOS w/ PDR	Programmable Alarm 3 set over MDIO Performance monitoring sync: Rising edge synchronizes PM statistics counters
B12	GND			
	TX_DIS			Transmitter Disable. "1" or NC = transmitter disabled, "0" = transmitter enabled
	MOD_LOPWR MOD_R\$Tn			Module Low Power Mode. "1" or NC= module in low power (safe) mode, "0"= power-on enabled Module Reset. "0" resets the module, "1" or NC = module enabled.
B8	RX_LOS	0	LVCMOS	Receiver Loss of Optical Signal. "1'= low optical signal. "0"= normal condition
	GLB_ALRMn	0	LVCMOS / OD	Global Alarm. "0": Alarm condition, "1": no alarm condition, Open Drain, Pull Up Resistor on Host +12V Module Supply Voltage Return Ground, can be seperate or tied together with Signal Ground
	2V_GND			They measure suppry voltage result oround, can be seperate or sed together with Signal Ground
B4	12V_GND			1407 Martin Romanni Malanan
B3 B2	12V 12V			+12V Module Supply Voltage
	12V			

OIF OPTICAL INTERNETWORKING FORUM

Table 12: MSA-100GLH Electrical Connector - Row A Pin Description (Note: Pins for future use (FFU) should be left unconnected on both the host board and the module)

	100G	I/O	Logic	Description
A84	12V			+12V Module Supply Voltage
A83	12V			
A82	12V			
	12V_GND			+12V Module Supply Voltage Return Ground, can be seperate or tied together with Signal Grour
A80 A79	12V_GND 12V_GND			
	MOD_ABS	0	GND	Module Absent. "1" or NC = module absent, "0" = module present, Pull Up Resistor on Host
A77	GND	-		Ground
A76	RXMCLKn	0	CML	Receive Monitor Clock, negative leg
A75	GND	-		
	RXMCLKp GND	0	CML	Receive Monitor Clock, positive leg
	RX0n	0	CML	Receive Data 0, negative leg
	GND			
	RX0p	0	CML	Receive Data 0, positive leg
	GND DX4a	_	<u></u>	Dessity Data 4, association for
	RX1n GND	0	CML	Receive Data 1, negative leg
	RX1p	0	CML	Receive Data 1, positive leg
	GND			
	RX2n GND	0	CML	Receive Data 2, negative leg
	RX2p	0	CML	Receive Data 2, positive leg
	GND			
A60	RX3n	0	CML	Receive Data 3, negative leg
	GND RX3n	0	CML	Receive Data 3, positive leg
	RX3p GND		OML	rveceive Data 3, positive leg
	RX4n	0	CML	Receive Data 4, negative leg
	GND			
	RX4p GND	0	CML	Receive Data 4, positive leg
	RX5n	0	CML	Receive Data 5, negative leg
	GND			
	RX5p	0	CML	Receive Data 5, positive leg
	GND RX6n	0	CML	Receive Data 6, negative leg
	GND	-	OWE	Nebelve Data 0, negative reg
A46	RX6p	0	CML	Receive Data 6, positive leg
	GND	_		
	RX7n GND	0	CML	Receive Data 7, negative leg
	RX7p	0	CML	Receive Data 7, positive leg
	GND			
	RX8n GND	0	CML	Receive Data 8, negative leg
	RX8p	0	CML	Receive Data 8, positive leg
	GND			
	RX9n	0	CML	Receive Data 9, negative leg
	GND RX9p	0	CML	Receive Data 9, positive leg
	GND	-	0.112	reserve servers, positive reg
	RXDSCn	0	CML	Receive Deskew Channel, negative leg (SFI-S only, otherwise no connect)
	GND BXDSCp	0	CML	Reneive Deskew Channel, positive log /SELS only, otherwise an accord)
	RXDSCp GND		OWL	Receive Deskew Channel, positive leg (SFI-S only, otherwise no connect)
	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data
	MDC	Т	1.2V CMOS	Management Data Clock
A26 A25	GND VND_IO_A	I/O	LVCMOS	Vendor I/O A
A25	VND_IO_B		LVCMOS	Vendor I/O A Vendor I/O B
A23	VND_IO_C	I/O	LVCMOS	Vendor I/O C
	VND_IO_D	I/O	LVCMOS	Vendor I/O D
	GND VND_IO_E	1/0	LVCMOS	Vendor I/O E
	VND_IO_F		LVCMOS	Vendor I/O F
A18	VND_IO_G	I/O	LVCMOS	Vendor I/O G
		I/O	LVCMOS	Vendor I/O H
	gnd Vnd Io J	1/0	LVCMOS	Vendor I/O J
A14	VND_IO_K		LVCMOS	Vendor I/O K
A13	FFU			For Future Use
A12			LVCMOS LVCMOS	Receiver Alarm transfer input for Re-generator mode
	RX_ALRM_OUT FFU		2701000	Receiver Alarm transfer output for Re-generator mode For Future Use
A9	FFU			For Future Use
	FFU			For Future Use
A7 A6	FFU 12V_GND			For Future Use +12V Module Supply Voltage Return Ground, can be seperate or tied together with Signal Grour
	12V_GND 12V_GND			
A4	12V_GND			
A3	12V			+12V Module Supply Voltage
A2 A1	12V 12V			
				1



10.1 Normative references

[N1] IEEE 802.3ba[™] -2010 "Amendment: Media Access Control Parameters, Physical Layers and Management Parameters for 40Gb/s and 100Gb/s Operation", Clause 45 – MDIO (March, 2010)

[N2] <u>OIF-CEI-02.0 - Common Electrical I/O (CEI) - Electrical and Jitter Interoperability</u> agreements for 6G+ bps and 11G+ bps I/O (*February 2005*)

[N3] Hirose FX10 Datasheets: <u>http://www.hiroseusa.com/Special_downloads18.asp</u>

10.2 Informative references

[I1] <u>OIF-FD-100G-DWDM-01.0 - 100G Ultra Long Haul DWDM Framework Document</u> (*June 2009*)

[I2] ITU-T Rec. G.709/Y.1331 (v4.2 – Feb. 2012) Interfaces for the Optical Transport Network (OTN)

[I3] OIF-SFI-S-01.0 – Scalable Serdes Framer Interface (SFI-S): Implementation for Interfaces Beyond 40G for Physical Layer Devices (Nov. 2008)

[I4] Hirose FX10 PCB Routing Guideline:

http://www.hiroseusa.com/FX10_PCB_routing_guideline_v1.2.pdf

[I5] CFP MSA Management Interface Specification V2.2, r06a (July 1, 2013)

11 Appendix A: Glossary

ADC	Analog Digital Converter
CDR	Clock and Data Recovery
CN	Connector
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
DEC	Decoder
DSP	Digital Signal Processor
DWDM	Dense Wavelength Division Multiplex
ENC	Encoder
FEC	Forward Error Correction
FFU	For Future Use
Gbaud	10 ⁹ Symbols Per Second
GH	Guide pin Hole
GND	Ground
GP	Guide Pin
IA	Implementation Agreement
LVCMOS	Low Voltage CMOS
MDC	Management Data Clock
MDIO	Management Data Input/Output
NC	No Connect
OIF	Optical Internetworking Forum
OTL	Optical channel Transport Lane
PCB	Printed Circuit Board
PM-QPSK	Polarization Multiplexed Quaternary Phase Shift Keying
RX	Receiver



12 Appendix B: Open Issues / current work items

None.



13 <u>Appendix C: List of companies belonging to OIF when</u> <u>document is approved</u>

Kaiam

Acacia Communications ADVA Optical Networking Alcatel-Lucent Altera AMCC Amphenol Corp. Analog Devices Anritsu Applied Communication Sciences Avago Technologies Inc. Broadcom Brocade **BRPhotonics BTI Systems** China Telecom **Ciena** Corporation Cisco Systems **ClariPhy Communications** Coriant R&G GmbH CPaD Deutsche Telekom Dove Networking Solutions **EMC** Corp Emcore Ericsson ETRI FCI USA LLC Fiberhome Technologies Group **Finisar** Corporation Fujikura Fujitsu Furukawa Electric Japan Google Hewlett Packard Hitachi Huawei Technologies **IBM** Corporation

Kandou **KDDI R&D Laboratories** Keysight Technologies, Inc. LeCroy Luxtera M/A-COM Technology Solutions Mellanox Technologies Microsemi Inc. Microsoft Corporation Mitsubishi Electric Corporation Molex MoSys, Inc. MultiPhy Ltd NEC **NeoPhotonics** NTT Corporation Oclaro Orange **PacketPhotonics** PETRA **Picometrix** PMC Sierra **QLogic Corporation** Oorvo Ranovus **Rockley Photonics** Samtec Inc. Semtech Spirent Communications Sumitomo Electric Industries Sumitomo Osaka Cement **TE Connectivity** Tektronix **TELUS** Communications, Inc. TeraXion **Texas Instruments**



Infinera Inphi Intel Ixia JDSU Juniper Networks Time Warner Cable US Conec Verizon Xilinx Yamaichi Electronics Ltd. ZTE Corporation

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