OIF Marketwatch: SI to the forefront

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Overview

- > System requirements drive diversity
- > ASIC requirement drive commonality

>Solutions

- 50G PAM with FEC
- NRZ with FFE, CTLE, DFE
- ENRZ



25G and 50G Interfaces



25G and 50G VSR channel (Best solution is NRZ)



2m 26AWG passive copper cable



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ASICs promote commonality

Constraints on switch ASICs

- Single SERDES design reduces R&D costs.
- Ability to 'turn' ASIC promotes multiple use parts
- 2.5G/10G/25G: First designs supported chip to module, 2nd Generation supports all: (chip to module, chip to chip, backplane, copper cable)
- 50G: More applications but still one SERDES
 - First design supports all applications



Diversity vs commonality



Diversity vs commonality chart



IL

R	1.5dB@14GHz 3dB@28GHz	Bump-to-bump Inside MCM or 3D Stack
२ २।	4dB@14GHz 8dB@28GHz	Ball-to-ball Across PCB
R M	10dB@14GHz 20dB@28GHz	Ball-to-ball
R C	20dB@14GHz 40dB@28GHz	Ball-to-ball
F	35dB@14GHz	Ball-to-ball

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Where did we end up?

> Ethernet will use PAM for all 50G electrical interfaces

- Solved the PAM 9dB noise penalty problem thru the use of strong FEC
- Low latency applications will use NRZ (i.e. HPC/InfiniBand)
- >Not clear what will happen with memory interface



Challenges with 50G NRZ designs

>Requires best input sensitivity

- To reduce the impact of higher losses
- > Requires advanced materials
 - Would benefit from reduced Meg7 pricing

> Requires better signal integrity of designs

- Surface roughness
- Control of via stubs
- Reduce trace impedance (85 ohms?)



Improved PCB material

Approx. 20% improvement in loss could be achieved for 50G NRZ designs



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Lee Ritchey Source Designcon 2015

Surface Roughness

Improvements in surface roughness could reduce channel loss by 1dB for 50G NRZ VSR designs 2.2



Challenges with 50G PAM4 designs

> Requires Low crosstalk

To reduce the impact of reduced SNR

Requires equalization for ISI (nonlinearity)

– DFE, FFE, CTLE

> Requires FEC

To reduce the impact of reduced SNR



Crosstalk measurements



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FEC coding

Performance of various block codes



