Implementation Agreement for Integrated Dual Polarization Intradyne Coherent Receivers

IA # OIF-DPC-RX-01.1

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Working Group: **Physical and Link Layer (PLL) Working Group**

TITLE: **Implementation Agreement for Intradyne Coherent Receivers**
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ABSTRACT: This contribution reflects the results from the first maintenance cycle of IA# OIF-DPC-RX-01.0 Implementation Agreement for Intradyne Coherent Receivers.

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4 Document Revision History

Version	Date	Description
OIF-DPC-RX-01.0 Initial release	16 April 2010	Initial release
OIF-DPC-RX-01.1	TBD	Various editorial corrections. Various additions to the descriptive text. Addition of table of operating characteristics to section 9 specifying several parameters. Addition of table of fiber characteristics to section 10 specifying several parameters. Update or addition of several mechanical dimensions of package including reduction of body length from 60mm to 50mm. Designation of DC pins 5&6 for connecting internal monitor photodiode. Removal of subscripts distinguishing PD bias pins to accommodate multiple versions already in use. Removal from appendix of items now specified in IA body.

5 Introduction

This document details an implementation agreement for an integrated intradyne coherent receiver initially targeting 100G PM-QPSK applications with nominal symbol rates up to 32 GBaud. While specifically addressing 100G PM-QPSK applications, this Implementation Agreement strives to remain modulation format and data rate agnostic whenever practical to maximize applicability to future market requirements. This document is not a multi-source agreement, but is expected to be the foundation of future MSAs.

100G DWDM represents a significant development expense for component and system suppliers. Currently available photonics components addressing the market are discrete and varied. A need for integration has been identified in order to meet cost and size objectives. This implementation agreement aims to reduce risk to component suppliers and users by identifying and specifying common features and properties of the devices that will enable them to broadly meet the needs of this emerging market.

This Implementation Agreement originates from the “100G long-distance DWDM integrated photonics” project, undertaken in the Physical Link Layer working group. This Implementation Agreement defines: (1) Required functionality. (2) High speed electrical interfaces. (3) Low speed electrical interfaces. (4) Mechanical requirements. (5) Environmental requirements. Also included are informative specifications for (6) opto-electronic interfaces. This Implementation Agreement does not define the type of technology used in photonics sub-components, nor expected optical transmission performance of systems using receivers conforming to this Implementation Agreement. This Implementation Agreement is intentionally structured not to preclude differentiation of product or system performance.

This Implementation Agreement has the following relationships to other projects undertaken in the PLL Working Group: (1) “100G long-distance DWDM Transmission Framework”. (2) “Forward Error Correction for 100G PM-QPSK Long Distance Communication”. (3) “100G Long-Haul DWDM Transmission Module – Electromechanical”. It has a relationship to the IEEE 802.3 and ITU-T Standards Bodies.

6 Functionality

The required functionality for the integrated coherent receiver is shown within the dashed line in Figure 1. A single component containing the described functionality is not required to meet the objectives of this implementation agreement.

As indicated in Figure 1, the coherent receiver requires the following basic functionality:

- Eight (8) photo-detectors, comprised of 4 sets of balanced detectors
- Four (4) linear amplifiers with differential output
- Two (2) ninety degree hybrid mixers with differential outputs
- A polarization splitting element, separating the input signal into two orthogonal polarizations, with each polarization delivered to a hybrid mixer
- A polarization maintaining power splitter or polarization splitting element, splitting the local oscillator power equally to the two hybrid mixers.

At a minimum, the first 3 of the above functions must be contained in single photonics component to meet the objectives of this implementation agreement.

The polarization channels are indicated in Figure 1 as 'X-Pol' and 'Y-Pol' and the phase channels for each labeled XI, XQ and YI,YQ respectively. The complementary outputs for each channel are labeled 'p' and 'n'. X and Y indicate a pair of mutually orthogonal polarizations of any orientation. I and Q are mutually orthogonal phase channels in each polarization. I and Q are established relative to the phase of the Local Oscillator where the relationship of the phase of the Signal in the Q channel to the Local Oscillator is either advanced or delayed by nominally 90 degrees as compared to the relationship in the I channel. The relative advance or delay of the Q channel in the Y polarization channel should correspond to that in the X polarization channel. Outputs 'p' and 'n' are the complementary outputs for each polarization-phase channel and are such that the output voltage for 'p' increases as the Signal and Local Oscillator approach the in-phase condition to form constructive interference, and the output voltage for 'n' decreases under the same conditions.

Additional required functionality for the integrated coherent receiver includes:

- Automatic Gain Control (AGC) and/or Manual Gain Control (MGC)
- User settable output voltage swing
- Independent output swing adjustment for each of the four outputs
- Peak indicators for each output

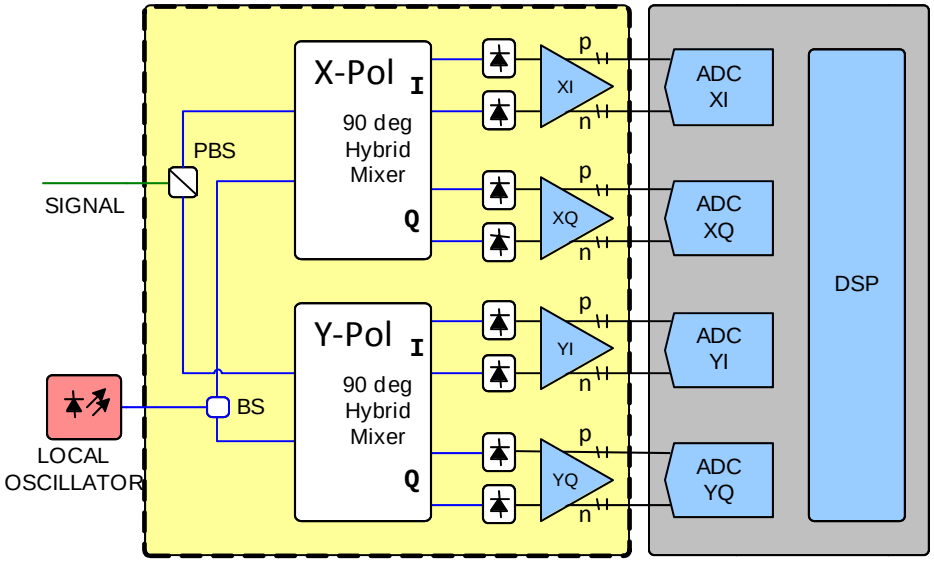


Figure 1: Functional diagram of a dual polarization intradyne coherent receiver. The yellow area enclosed by the dashed line indicates the functionality specified in this implementation agreement.

7 High Speed Electrical Interface

The high speed electrical interface is co-planar waveguide, consistent with the pitch and pin definition detailed in Table 1, Table 2, and Figure 2. It is noted for the channel pin-out shown in Figure 2 that X, Y, I, Q, p, and n are consistent with the descriptions in Section 6. It is also noted that alternate polarities for the differential signals specified in Figure 2 are acceptable.

Table 1: High-speed electrical interface description.

Parameter	Value	Notes
Interface Type	Differential	
Channel Number	4	
Channel Configuration	G-S-G-S-G	per Figure 2
Signal Line Coupling	AC	
Signal Line Impedance	50 Ohm to ground	
Channel Pin-out	XI XQ YI YQ	per Figure 2
Differential Signal Pin-out	Signal Complementary Signal	p n

Table 2: High-speed electrical interface dimensions.

Parameter	Symbol	Min	Typ	Max	Units
Lead Pitch	A		1		mm
Lead Length (referenced from outside wall of package, as defined by dimension LP2 in Section 11)	B	2.00		3.00	mm
Signal Lead Width	C	0.10		0.30	mm
Ground Lead Width	D	0.10		0.50	mm
Channel Pitch	E		5		mm
Signal to Complimentary Signal Pitch	F		2		mm

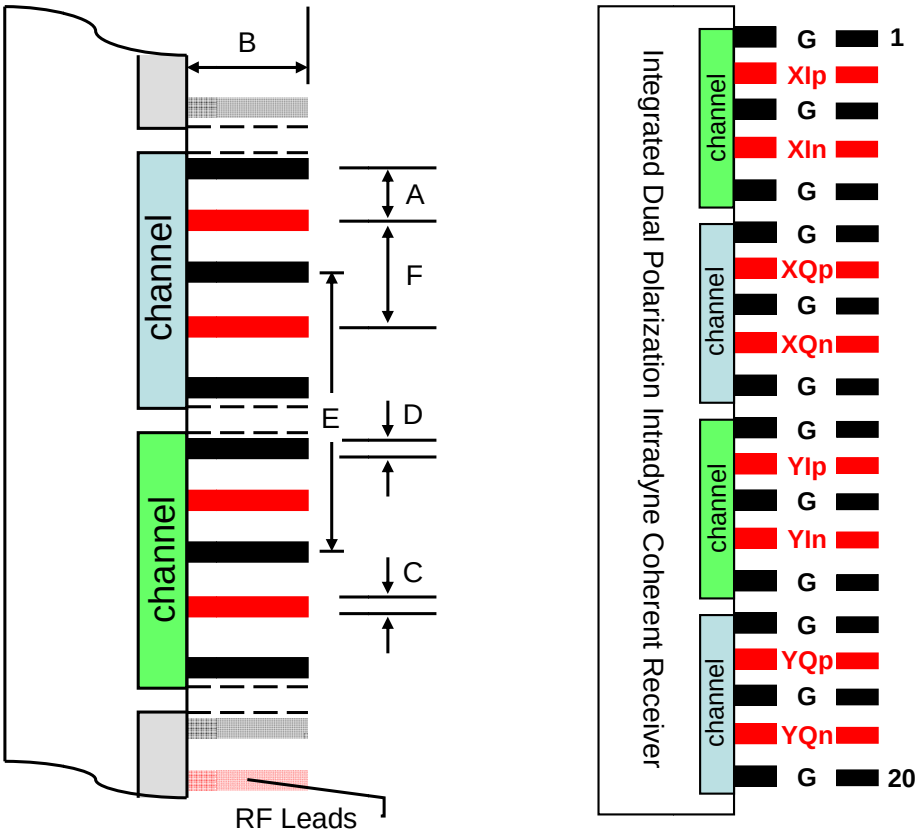


Figure 2: High-speed electrical interface definition.

8 Low Speed Electrical Interface

The low speed electrical connections are provided through 40 pins, located and numbered as shown in Figure 3. Unused pins are not required to be present.

The photocurrent of each photodiode, or a representative equivalent quantity, shall be measurable.

The pin pitch is specified to be 1.27 mm.

The pin definition for the low speed electrical interface is provided in Table 3.

Table 3: Low speed electrical interface pin definition.

Pin #	Symbol	Description	Pin #	Symbol	Description
1	SD-Y	Shutdown Y (optional)	40	RFU	Reserved for future use
2	PI-YI	Peak indicator YI	39	PI-XQ	Peak indicator XQ
3	GA-YI	Gain adjust YI	38	GA-XQ	Gain adjust XQ
4	OA-YI	Output amplitude adjust YI	37	OA-XQ	Output amplitude adjust XQ
5	MPD+	Monitor photodiode cathode (optional)	36	RFU	Reserved for future use
6	MPD-	Monitor photodiode anode (optional)	35	MC/AGC-X	MC/AGC selection X (optional)
7	VCC-YI	Supply-voltage amplifier YI	34	VCC-XQ	Supply-voltage amplifier XQ
8	GND	Ground reference	33	GND	Ground reference
9	PD-YI	Photodiode bias voltage YI [1]	32	PD-XQ	Photodiode bias voltage XQ [1]
10	PD-YI	Photodiode bias voltage YI [1]	31	PD-XQ	Photodiode bias voltage XQ [1]
11	PD-YQ	Photodiode bias voltage YQ [1]	30	PD-XI	Photodiode bias voltage XI [1]
12	PD-YQ	Photodiode bias voltage YQ [1]	29	PD-XI	Photodiode bias voltage XI [1]
13	GND	Ground reference	28	GND	Ground reference
14	VCC-YQ	Supply-voltage amplifier YQ	27	VCC-XI	Supply-voltage amplifier XI
15	MC/AGC-Y	MC/AGC selection Y (optional)	26	RFU	Reserved for future use
16	RFU	Reserved for future use	25	RFU	Reserved for future use
17	OA-YQ	Output amplitude adjust YQ	24	OA-XI	Output amplitude adjust XI
18	GA-YQ	Gain adjust YQ	23	GA-XI	Gain adjust XI
19	PI-YQ	Peak indicator YQ	22	PI-XI	Peak indicator XI
20	RFU	Reserved for future use	21	SD-X	Shutdown X (optional)

[1] *PD-YI, PD-YQ, PD-XI, PD-XQ each represent 2 pins wherein each one of the two pins independently supplies the bias voltage to correspondingly each one of the two photodiodes for the labeled Polarization / Phase channel.*

9 Environmental and Operating Characteristics

Basic operating characteristics are listed in Table 4.

Table 4: Operating Characteristics

Parameter		Unit	Min	Typ	Max	Note
Symbol Rate		GBaud			32	
Operating Frequency	C-Band	THz	191.35		196.20	#1
	L-Band		186.00		191.50	
Amplifier Supply Voltage Pins 7,14,27,34		V		3.3		
Photodiode Bias Voltage Pins 9-12, 29-32	Option 3.3	V	3.135	3.3	3.465	#2
	Option 5.0		4.75	5.0	5.25	
	Option 6.0		5.75	6.0	6.25	
Monitor Photodiode Bias Voltage - Pins 5&6	Option 3.3	V	3.135	3.3	3.465	#2
	Option 5.0		4.75	5.0	5.25	
Operating Temperature	Standard	Deg C	-5		75	#3
	Preferred		-5		80	
Operating Humidity		%RH	5		85	#4

#1 Minimum supported range. On 50GHz grid, as defined in G694.1. At least one of the two frequency bands to be supported.

#2 Vendor to state which Bias Voltage option or options are allowed both for signal Photodiodes and Monitor Photodiodes.

#3 Max temperature is the outside surface temperature of the photonic module and is to be measured in "hot zone" of case.

#4 non-condensing

10 Mechanical

The mechanical requirements for the integrated coherent receiver are detailed in Figure 3, Table 5: Fiber Characteristics and Table 6. The requirements include:

- Fiber input and high speed electrical output located on opposite sides
- Signal input fiber to be Single Mode Fiber (SMF)
- Local oscillator fiber to be Polarization Maintaining Single Mode Fiber (PM SMF)
- DC supply and control voltages applied from remaining sides
- DC pins shall provide suitable strain relief (e.g. utilizing omega bends)
- The thermal transfer path shall be through the PCB side of the device
- The devices hot region shall be within the area indicated in Figure 3.
- Use of appropriate strain relief in high speed electrical pins

For implementations with BS and/or PBS functions located external to the main photonics component, the maximum envelope shall pertain only to the main photonics component. In implementations without integrated BS and/or PBS, the main photonics component contains the optical hybrids, photo-diodes, and linear amplifiers.

Table 5: Fiber Characteristics

Parameter		Unit	Min	Typ	Max	Note
Fiber Bend Radius: SM-PMF on Local Oscillator Input	Standard	mm	20			#1, #2, #3
	Preferred		15			
Fiber Bend Radius: SMF on Signal Input		mm	15			

#1 The polarization state in any PM fiber shall be aligned to the slow axis of the PM fiber.

#2 The slow axis of any PM fibers shall be aligned to the connector key.

#3 All fibers to be uniquely identified.

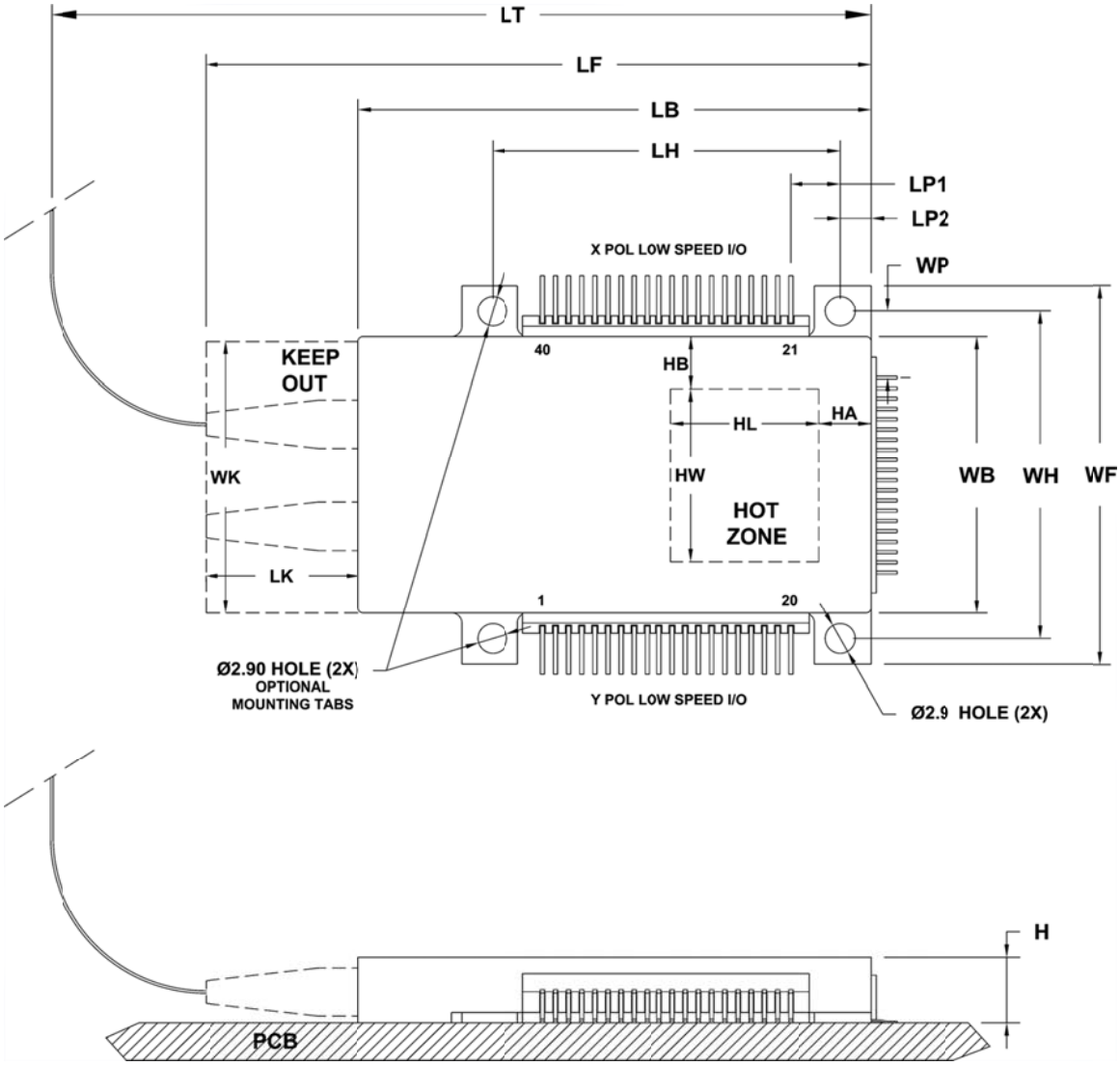


Figure 3: Mechanical diagram.

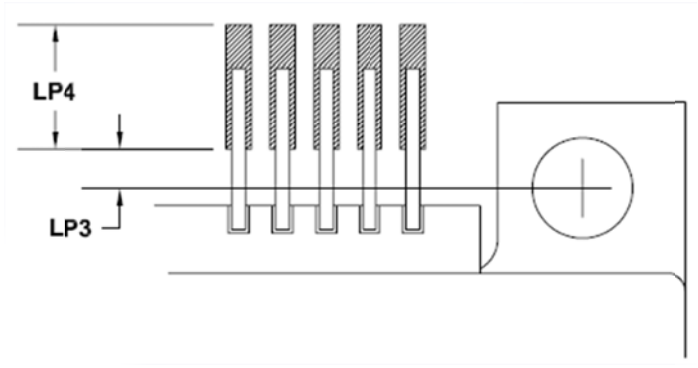


Figure 4: DC/control pin landing pad location.

Table 6: Mechanical dimensions

Parameter	Description	Value	Note	Units
H	Package height	9	Maximum	mm
LT	Total length, including 90 degree fiber bend	90	Maximum	mm
LF	Full length of package, including fiber boots	70	Maximum	mm
LB	Length of package body	50	Maximum	mm
LH	Distance between mounting holes (optional)	34	Nominal	mm
LP1	Distance between mounting hole center and pin 21 center	4.935	Nominal	mm
LP2	Distance between mounting hole center and RF end of package	3	Nominal	mm
LP3	DC/Control pin landing pad location relative to mounting hole center	1.5	Maximum	mm
LP4	DC/Control pin landing pad length	2.5	Minimum	mm
WF	Width of package, including mounting flanges and DC pins	41	Maximum	mm
WH	Distance between mounting holes	32	Nominal	mm
WB	Width of package body	27	Nominal	mm
WP	Distance between mounting hole center and first RF pin center	6.5	Nominal	mm
HA	Location of hot region relative to package edge	3 4	Minimum Maximum	mm mm
HB	Location of hot region relative to package edge	HW to be centered in package	Minimum	mm
HW	Width of hot region	WB	Maximum	mm
HL	Length of hot region	25	Maximum	mm
WK	Width of boot area Keep-Out region	22	Maximum, Centered To Package	mm
LK	Length of boot area Keep-Out region	(Max LF) - LB	Maximum	mm

11 References

11.1 Normative references
11.2 Informative references

12 Appendix A: Glossary

ADC	Analog to Digital Converter
AGC	Automatic Gain Control
BS	Beam Splitter
CMRR	Common Mode Rejection Ratio
DSP	Digital Signal Processor
GBaud	10^9 Symbols per second
IA	Implementation Agreement
LO	Local Oscillator
MGC	Manual Gain Control
MSA	Multi-Source Agreement
OIF	Optical Internetworking Forum
PBS	Polarization Beam Splitter
PCB	Printed Circuit Board
PM-QPSK	Polarization Multiplexed Quaternary Phase Shift Keying
THD	Total Harmonic Distortion

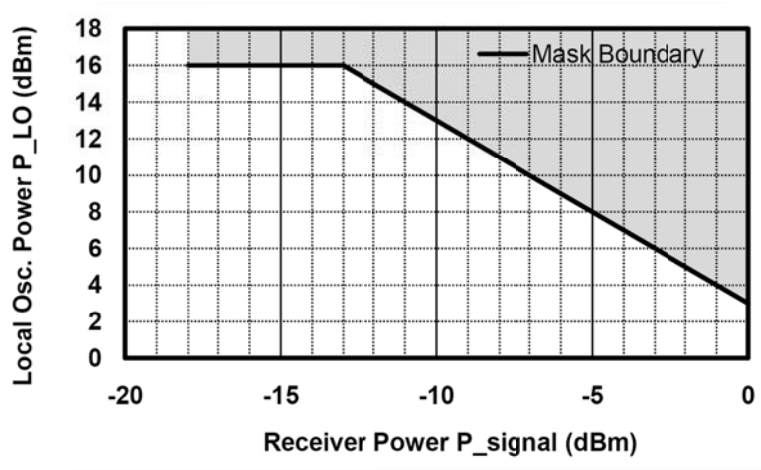
13 Appendix B: Opto-Electrical Properties (informative)

Opto-electrical properties consistent with the application and objectives described in the 100G framework document are provided in Table 7: Opto-electrical properties
. As this release of the implementation agreement comes very early in the development cycle, these values are to be interpreted as target values. It is expected that values will be updated as necessary and become normative and moved to the main body of this document as the technology matures.

Table 7: Opto-electrical properties

Parameter	Units	Min	Typ	Max	Comments
Symbol Rate	GBaud			32	
Operating Signal Power	dBm	-18	-10	0	Average optical power
Local Oscillator Power	dBm				See Figure 5 for recommended operating conditions.
Linear output swing adjustment range Standard Extended	 mVppd mVppd	 300 400	 500	 700 900	Peak to peak, differential, AC coupled
Maximum Gain Control Bandwidth	MHz		5		Settable via external control. Measured by applying step at gain control node such that output changes 5%. BW is estimated by 0.22/Tr where Tr is 20-80% rise/fall of the output envelope step.
Total Harmonic Distortion (THD) DC current = 1.3 mA AC = 0.36mApp in to each PD $V_{OUT\|DIFF}$ = 500mVpp F_{IN} = 1GHz ± 10%	%			5	Assumptions: P(SIG) = -10dBm P(LO) = 13dBm Excess loss = 2dB, PD Responsivity = 0.8A/W
Common Mode Rejection Ratio ($CMRR_{DC}$) Signal to I & Q LO to I & Q	 dBe dBe			 -20 -12	See Figure 6 for definition
Common Mode Rejection Ratio ($CMRR_{22GHz}$) Signal to I & Q LO to I & Q	 dBe dBe			 -16 -10	See Figure 6 for definition

Small Signal Bandwidth (3dB)	GHz		22		
Low Frequency Cutoff	kHz			100	AC coupling
Phase Error	±deg			5	Between XI and XQ and between YI and YQ
Optical Reflectance	dB			-27	Signal and LO ports. Per ITU-T G.959.1
Output Electrical Return Loss (S22): f < 16 GHz 16 GHz < f < 24 GHz 24 GHz < f < 32 GHz	 dB dB dB	 10 8 6			
Skew: p, n	ps			2	
Channel skew	ps			10	Time difference between earliest and latest channel. Includes channel skew variation.
Channel skew variation	ps			5	Temporal variation in the skew between any 2 channels due to case temperature, wavelength, input optical power, amplifier gain, and aging. Time for channel defined as mean of p and n.



P_signal (dBm)	P_LO (dBm)	I_diff_pp (mA)
0	3	0.715
-3	6	0.715
-6	9	0.715
-10	13	0.715
-13	16	0.715
-16	16	0.506
-18	16	0.402

Figure 5: Recommended maximum allowable local oscillator power mask as a function of signal power to the integrated receiver for linear operation. A photodiode responsivity of 0.8A/W, NRZ coding, back to back operation, 0.715mA peak to peak differential linear input dynamic range, and an excess loss of 2dB are assumed . P_LO power level is as applied prior to the splitter equally dividing LO between X and Y partitions.

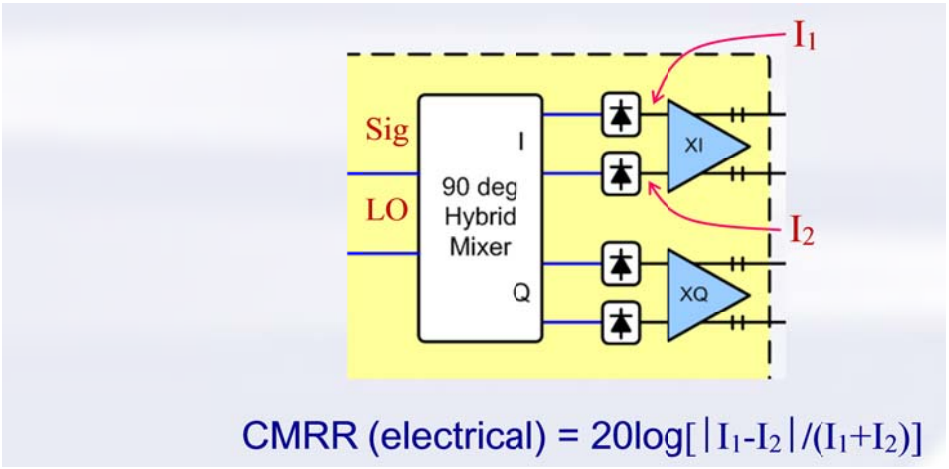


Figure 6: CMRR definition.

14 Appendix C: FPC Interfaces (informative)

It is recognized that it may be possible to design FPC (flexible printed circuit) interfaces that maintain compatibility with the electro-mechanical specifications in the normative sections of this IA. This release of the IA does not preclude FPC (flexible printed circuit) solutions that maintain electro-mechanical compatibility at the host board level

15 Appendix D: Open Issues / current work items

16 Appendix E: List of companies belonging to OIF when document is approved

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