OPTICAL INTERNETWORKING FORUM

White Paper: Multi-Vendor Interoperability Testing of CFP4, QSFP28, and backplanes with CEI-28G-VSR and CEI-25G-LR Interface During ECOC 2014 Exhibition

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1. Executive Summary

The Optical Interworking Forum (OIF) has developed a set of Interoperability Agreements focused on new common electrical interfaces (CEI) applicable to higher speed optical systems requiring interconnect baud rates of 19.60 Gbaud to 28.10 Gbaud using NRZ coding. The OIF is also investigating the standardization and common understanding of thermal performance using a common set of definition metrics in the future. The OIF membership, consisting of semiconductor, connector, optical module suppliers, system suppliers, test equipment providers, allows a unique perspective for developing industry requirements, and a comprehensive understanding of the technology trade-offs necessary to enable the development and support for these requirements.

A multi-vendor interoperability event to demonstrate applications and industry ecosystem using CEI-28G-VSR, CEI-25G-LR interfaces and work supporting thermal characterization and standardization was successfully demonstrated during ECOC 2014 Exhibition by several members of the OIF Physical and Link Layer (PLL) Working Group. The demonstrations were broad in scope ranging from Optical and active copper interoperability of the emerging CFP4 MSA using the OIF CEI-28G-VSR electrical specification, to long reach backplane and QSFP28 passive copper cable using the OIF CEI-25G-LR electrical specification.

At this event, multiple interoperability tests with the CFP4 optical module form factor successfully demonstrated support for CEI-28G-VSR interfaces used with this new MSA form factor. This new demonstration at ECOC 2014 builds on the previous interoperability events that took place at the OFC 2012, OFC 2013, OFC 2014, ECOC 2012 and ECOC 2013 Exhibitions.

Also demonstrated was a QSFP28 passive copper cable and three interoperability demonstrations that support 25Gb/s over backplane per CEI-25G-LR. The QSFP28 demonstration showed various lengths and gauges of passive copper cables. The three backplane demonstrations used back plane connector systems over various lengths of PCB material driven by a daughter card with common quad retimer or FPGA to show industry support of the interface. These demonstrations were an extension of similar ones shown at ECOC 2013 and were subsequently documented in a previous white paper.

In addition, OIF members also demonstrated some of the work in thermal modeling, in determining some of the key metrics that can potentially be used to support a future standard.

In all, the ECOC 2014 PLL interoperability builds on the previous interoperability events and consisted of nine individual demonstrations with 13 participating vendors. The nine demos were assembled as examples that the ecosystem for 100Gb/s electrical and optical interfaces is viable and interoperable from multiple

sources. It also demonstrated industry cooperation to promote key issues and metrics for successful implementation of next generation communication systems and networks.

1.1. CEI-28G-VSR Interoperability Testing

The first four demonstrations exemplified the interoperability of pluggable optics, their electrical interfaces and connectors, retimers and gearbox IC's that performed error free over IEEE 802.3ba 100GBASE-LR4 optical links, supporting OTU4 data rates and 100GBASE-SR10 from a variety of manufacturers. The four demonstrations were:

Demo 1: CFP4 100GBASE-LR4/ER4f Interoperability using CEI-28G-VSR

A Xilinx FPGA using a Serial IO Analyzer IBERT design driving CEI-28G-VSR to a host card with a Finisar CFP4 ER4f module plugged into it. At the far side of the link was a JDSU CFP4 100GBASE-LR4 module. In this direction the modules were interoperating at 100GBASE-LR4 over 10km of single mode fiber. The JDSU CFP4 module, utilizing a CFP4 connector from Yamaichi was driving OIF-28G-VSR into an Inphi 100 GbE CDR which checks the fidelity of the PRBS-31 data pattern. Independently, the Inphi 100GbE CDR drove OIF-28G-VSR to the JDSU CFP4 module which in turn drives 40km of single mode fiber. The data was received by the Finisar CFP4 ER4f module with a bit error rate that surpassed the specification of 1e-6. The Finisar CFP4 ER4f module drove CEI-28G-VSR to the Xilinx FPGA that checked the PRBS-31 data pattern.

Demo 2: CFP4 100GBASE-LR4 Interoperabiity using CEI-28G-VSR

A MoSys evaluation board with MoSys LineSpeed™ 100G low power full duplex retimer driving CEI-28G-VSR to a host breakout card with a Yamaichi CFP4 host connector is connected to a Finisar CFP4 100GBASE-LR4 module with integrated Semtech retimer. At the far side of the 10km, 100GE (4x25.78G) optical link was a Fujitsu CFP4 100GBASE-LR4 module. The Fujitsu CFP4 module was plugged into an Inphi breakout board with a Yamaichi CFP4 host connector and was driving CEI-28G-VSR to 100G retime ICs. The traffic is generated in each direction across the link to generate full duplex 100GE traffic.

Demo 3: CFP4 Active Copper Cable Interoperability using CEI-28G-VSR

A Yamaichi CFP4 5m Active Copper Cable is driven by an Inphi iKON™ Retimer and a MoSys LineSpeed™ Retimer, sending and receiving 112Gbps OTU4 rate data. The CFP4 module form factor includes a Semtech GN2504 Backplane Re-timer and Yamaichi connectors and will support up to 10m AWG26 cabling, enabling a cost and power effective short reach alternative to optical modules with the same interoperability with the host linecard system.

Demo 4: CEI-28G-VSR compliance demonstration

This demonstration successfully addressed CEI-28G-VSR/CAUI-4 compliance testing from the perspective of a QSFP28 module. The input module stressed test, used to verify compliance at the TP1a test point, was based upon a

QSFP28 channel which included Semtech MCB/HCB PCBs, a module PCB based upon a Semtech GN2104 quad re-timer and a TE Connectivity QSFP28 connector. The PPG3204 data pattern generator, BertScope jitter sources and DSA8300 oscilloscope were provided by Tektronix and the the PAN-X VNA by Agilent. The output eye requirements were based upon a similar channel to that used for the input test but the QSFP28 connector was provided by Molex. The TP4 output eye test was enabled by an Agilent 86100D oscilloscope.

The demonstrations above outline the use of the OIF CEI-28G-VSR specification to successfully support a wide range of the new CFP4 applications for both optical and active copper solutions. Further, the standards have been built to ensure interoperability between multiple vendors to ensure a robust ecosystem.

1.2. CEI-25G-LR Interoperability Testing

The OIF has been at the forefront of the industry with the development of common electrical interface (CEI) implementation agreements (IA) that support 25 Gb/s over backplane architectures (CEI-25G-LR). This development work is important in enabling the industry to re-use conventional chassis, line card, backplane and cabling architectures as they develop equipment that is able to meet the evolving and challenging bandwidth demands of the communications industry. The next 4 demonstrations are examples of continuing industry support of the standards by developing new products.

The demonstrations were:

Demo 5: QSFP28 passive copper cable interoperability using CEI-25G-LR

The demonstration consists of 2 to 4 meters of QSFP28 passive copper cable from multiple vendors successfully passing full duplex 100G traffic between MoSys PHY devices. In the demonstration, MoSys LineSpeed™ 100G Multi-Mode Gearbox evaluation boards are connected with breakout cards and QSFP28 passive copper cables of various lengths and gauges (2m/30Gauge, 3m/28Gauge, and 4m/26Gauge) from four vendors (Amphenol, Molex, TE Connectivity, and Yamaichi). Four lanes of PRBS traffic at 25.78 Gbps was generated by the MoSys Gearbox devices in each direction to generate a full duplex link across a variety of Amphenol, Molex, TE Connectivity and Yamaichi breakout card and QSFP28 passive cables and verified error free. The reference channel target was the CEI-25G-LR channel.

Demo 6: Backplane Demonstration using CEI-25G-LR

This demonstration consists of a Semtech GN2504 quad re-timer board driving four lanes of CEI-25G-LR through an Amphenol supplied reference backplane system including two XcededPlus connectors terminated by a Semtech GN2504

quad re-timer board operating error free at 25.78125 Gb/s error free with a PRBS31 data pattern.

Demo 7: Backplane demonstration using CEI-25G-LR

The demonstration consists of a Xilinx Virtex® UltraScale™ FPGA driving four lanes of OIF CEI 25G LR to generate100G operation across a Molex reference backplane link with end-to-end loss of >25dB at 12.9GHz. Each lane carries a PRBS-31 pattern running at a 25.78125 Gb/s data rate. PRBS generation and checking is performed on-chip.

Demo 8: Backplane demonstration using CEI-25G-LR

This demonstration consists of a Xilinx Virtex® UltraScale™ FPGA driving four lanes of CEI-25G-LR through a TE Connectivity supplied reference backplane system including two STRADA Whisper connectors terminated by a Semtech GN2504 quad re-timer board operating error free at 25.78125 Gb/s error free with a PRBS31 data pattern.

1.3. Thermal Modeling

For next generation systems, the density and data rate of interconnects will be some of the critical factors that will determine the success in the marketplace. As such, system designers will continue to push the limits of the technology to drive capacity and density higher. This, in turn, will also increase the density of components to the limits of thermal management. Thermal management can limit the performance and reliability of a component or subsystem and affect the overall integrity of the system itself. The intent of the OIF is to develop a document that will provide a degree of standardization and common understanding across the Networking Industry to enable optimized thermal performance using a common set of definitions in the future. The next demonstration highlights the effect of these factor's on thermal management.

Demo 9: Thermal Modeling Demonstration

Molex and TE Connectivity built a thermal emulator test vehicle, a line card thermal emulator test platform that consists of a simulated line card supporting 8 positions of the proposed CDFP style 2 400Gb/s optical modules. Module heat dissipation and airflow were controlled and temperature was measured at various points to detect the effect of the surface flatness. Thermal efficiency was improved with flatter surfaces as anticipated by thermal models.

2. OIF PLL Multi-Vendor Interoperability Testing Objectives

Interoperability is one of the keys to the success of any standard or implementation agreement. In order to promote the acceptance and demonstrate the viability of CEI-28G-VSR and CEI-25G-LR, the OIF sponsored a private, closed door interoperability Plugfest in August 2014. This Plugfest reiterated that

CEI-28G-VSR and CEI-25G-LR are widely supported by an increasing number of companies across the industry with participants including four semiconductor manufacturers (Inphi, MoSys, Semtech, and Xilinx), four connector and copper cable subsystem vendors (Amphenol, Molex, TE Connectivity, Yamaichi), three manufacturers of optical modules (Finisar, JDSU and Fujitsu Optical Components) and two test equipment manufacturers (Agilent and Tektronix). Cooperation between semiconductor, connector, optical module, optical component and test equipment suppliers is crucial to enable implementation and integration of high-speed signaling by system and operator vendors. ECOC 2014 showcased working demonstrations of the CEI-28G-VSR electrical interface implemented on CFP4 100GBASE-LR and Active Copper Cable. In addition, passive copper cable and several backplane demonstrations using CEI-25G-LR highlighted interoperability with multiple cables and connector systems.

2.1. CEI-28G-VSR, CEI-25G-LR Background Information and Applications

The communications and networking industries' data rates have been increasing along with the demands for higher levels of traffic aggregation. Additionally, the industry desires interoperable interfaces that support these next generation data rates. The OIF has been at the forefront of this demand, leading the industry with the development of CEI implementation agreements (IA) that support up to 28.10 GBd in chip-to-module electrical interface applications and 25 GBd line card to line card “long reach” electrical interface applications.

This development work is unique and timely in enabling the industry to re-use conventional chassis and line-cards as they develop equipment that is able to meet the evolving and challenging bandwidth demands of the communications industry. The CEI-28G-VSR Clause and the CEI-25G-LR Clause are ratified and available for industry use.

The use of pluggable optical transceivers and direct attach copper cables is a common practice in equipment developed for the communications market. Developing interoperable pluggable solutions that keeps up with the demanding bandwidth needs of industry is critical to enabling next generation equipment that supports the communications service providers.

2.2. CEI-28G-VSR Specification Channel Requirement

The CEI-28G-VSR application reference diagram is shown in Figure 1. It consists of 100Ω differential PCB traces, vias, one connector and AC coupling capacitors. The CEI-28G-VSR IA is intended to be used for “Very Short Reach” channels, with length up to 150 mm, and loss up to 10.0 dB loss at Nyquist rate. The model that is being initially targeted for the next generation of optical modules is retimed interfaces operating at 25.78 – 28.10 GBd. The overall CEI-28G-VSR link needs to operate with a bit error ratio (BER) of 1e-15 or less. VSR interface supports multiple lanes and is hot pluggable.

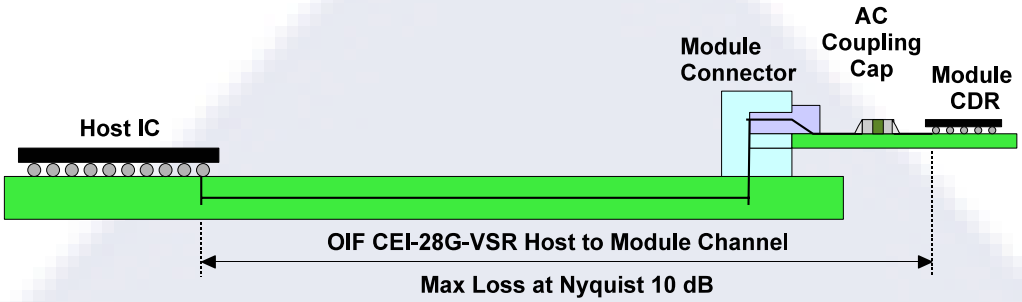

Figure 1: CEI-28-VSR Reference Model

A VSR link supports a maximum loss of 10 dB at Nyquist for operation from 19.60 to 28.10 GBd with NRZ modulation. The link loss budget is divided into a maximum host PCB loss of 7.3 dB, a connector loss of 1.2 dB and a module PCB loss of 1.5 dB, Figure 2 shows a diagram of the loss breakdown. TP1a and TP4a are respectively the host electrical output and input measurement points measured with Host Compliance Board (HCB) with PCB loss of 2.0 dB. TP1 and TP4 are respectively the module electrical input and output measurement points measured with module compliance board (MCB) with PCB loss of 1.25 dB.

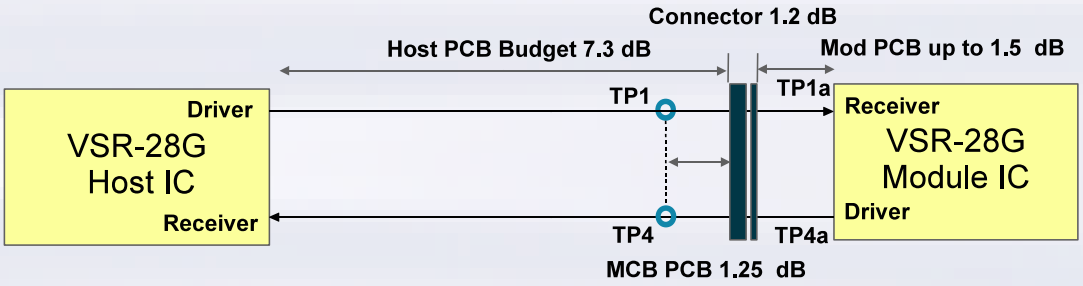

Figure 2: CEI-28G-VSR Reference Model

Figure 3, shows the CEI-28G-VSR channel response scaled for operation at 28 GBd with loss of 10 dB at Nyquist frequency of 14 GHz.

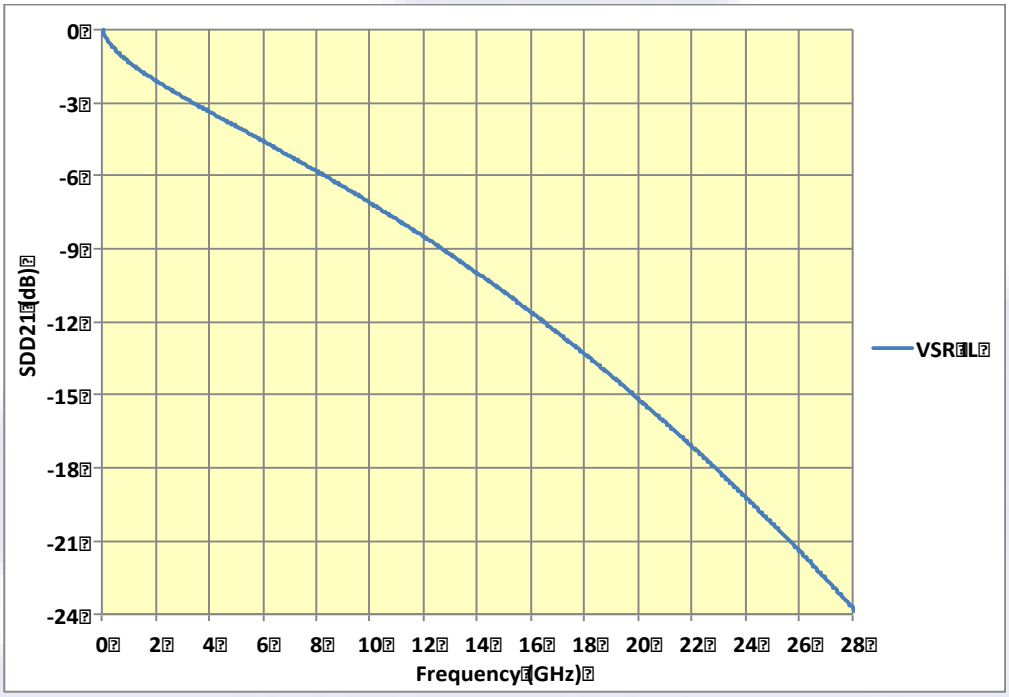

Figure 3: CEI-28G-VSR Channel Response

2.3. CEI-25G-LR Background Information and Applications

As the demands on industry data rates have increased along with the demands for higher levels of traffic aggregation, the communications and networking industries have need of interoperable interfaces that support these next generation data rates. The OIF has been at the forefront of this demand by leading the industry with the development of common electrical interface (CEI) implementation agreements (IA) that support 25 Gb/s over backplane architectures, 28 Gb/s in chip-to-chip applications and 28 Gb/s in chip-to-module applications. This development work is important in enabling the industry to re-use conventional chassis, line card and cabling architectures as they develop equipment that is able to meet the evolving and challenging bandwidth demands of the communications industry.

CEI-25G-LR is an OIF Clause which address the needs of 25 Gb/s Long Reach backplane applications. The CEI-25G-LR Clause was ratified along with CEI-28G-VSR and CEI-28G-SR as part of the Common Electrical I/O (CEI) 3.0 Implementation Agreement.

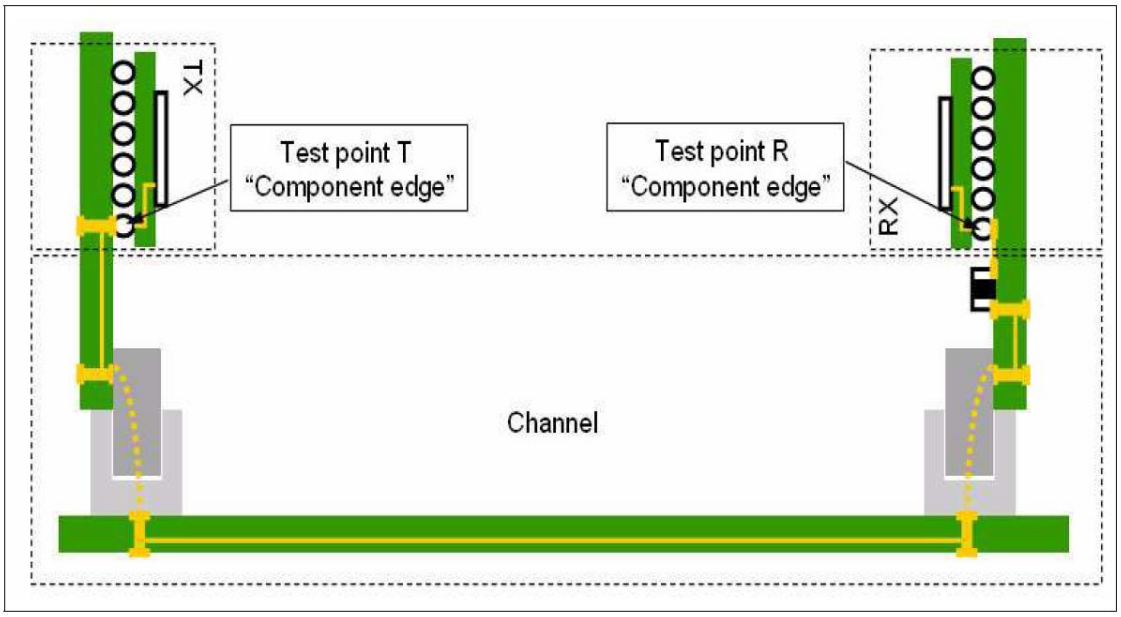

Figure 4: CEI-25G-LR Reference Model

As shown in

Figure 4, backplane architectures are commonly used in communications equipment. Developing 25 Gb/s backplane channel specifications is important to enable the industry to continue use of this architecture in switches, routers, transport and data center equipment. The CEI-25G-LR channel consists of 100Ω differential PCB traces, vias and up to two connectors. As this IA is targeted to longer reach backplane applications total allowable channel loss can be up to 25 dB at Nyquist rate and the transmitter is able to generate a maximum swing of 1200 mVppd and is required to have an FIR equalizer. The receiver implementation is not mandated and can be vendor specific.

3. Demonstrations

3.1. Demonstration 1: CEI-28G-VSR CFP4 100GBASE-LR4/ER4f Modules

Finisar, Inphi, JDSU, Semtech, Yamaichi and Xilinx

Component Overview

Finisar CFP4 ER4f Module: Finisar is demonstrating the feasibility of a 40 km error-free 100G link using 4x28G DML and 4x28G APD technologies in the CFP4 module form factor. This so-called "ER4f" approach requires the use of FEC in

the data path (similarly to 100GBASE-SR4) and is expected to be standardized by the ITU-T, enabling low-power and high-density 40 km 100G optical transceiver modules such as CFP4 and QSFP28.

Inphi IN112525 iKON™ CDR: Enabling today's 2-Terabit line cards, the iKON™ Clock and Data Recovery (CDR) Retimer ICs bring advanced transmit and robust and fully adaptive receive equalization for 25 to 28Gbps line card applications. Targeting CFP4 and QSFP28 systems for 100G client side solutions, the low power CMOS architecture deployed in the retimer will accelerate deployment for data center and enterprise networks by using state of the art signal performance monitoring, including Inphi's iScan™, the industry's highest resolution data agnostic margin indicator.

JDSU CFP4 100GBASE-LR4 Module: The JDSU CFP4 100GBASE-LR4 module is a full duplex, photonic-integrated optical transceiver operating at either 103.125 Gbps or 111.81 Gbps. The module complies with the CFP MSA CFP4 Hardware Specification, IEEE802.3-2012 Clause 88 and ITU-T G.959.1-2012-02. The JDSU module uses a 4x28G integrated EML based TOSA and 4x28G integrated PIN ROSA achieving exceptional eye performance with low power consumption.

Semtech Module Re-Timer: Leveraging a generation of innovation in 10G module CDRs, Semtech's quad-lane auto-adaptive GN2104 family of low-power re-timers are optimized for reference-free 25-28Gbps operation in next-generation optical modules and active cables. By resetting the jitter budgets within the module in both directions, Semtech's CDRs are perfect for new applications such as CFP2 / 4 and QSFP28 optical modules. The GN2104 family features best-in-class receive sensitivity, input jitter tolerance and output jitter, allowing for reliable signal recovery and clean, wide-open transmit eyes.

Yamaichi CFP4 connector and the mechanical parts are fully compliant with CFP MSA specification and have signal loss performance better than -1dB at 14GHz and better than -1.2dB at 16GHz, which indicates its capability even at 32Gbps per lane usage. The connector system is available with single and quad port cages as standards. Custom design cage and heat sink support is also available.

Xilinx VU095 Virtex® UltraScale™: The Xilinx Virtex® UltraScale™ family of FPGAs is implemented on the latest 20nm SOC process. The FPGA contains 940,800 logic cells, 768 DSP slices, 62,208Kbits of block RAM (BRAM), four 100G Ethernet blocks, six 150GBd Interlaken blocks, 32x 16.3 GBd GTH transceivers and 32x 32.75 GBd GTY transceivers. The GTY transceivers are designed to exceed the OIF-28G-VSR and OIF-25G-LR electrical specifications and are targeted to interoperate with the latest CFP4 optical modules and 28 GBd backplanes. For the demonstration, the device has been configured with an IBERT IP example design that is simultaneously transmitting and receiving

PRBS-31 and checking the received data for errors. Performance is reported via the Vivado® Serial IO Analyzer.

Demo 1 Description

This demonstration system consists of the following blocks: Xilinx FPGA evaluation board, Finisar CFP4 evaluation board, a Finisar CFP4 100GBASE-ER4f module with integrated retimer IC, a JDSU 100GBASE-LR4 module with integrated retimer IC, a JDSU CFP4 evaluation board utilizing a Yamaichi CFP4 connector, and Inphi CDR evaluation board. A PRBS-31 pattern is generated from the Xilinx FPGA across 4 lanes at 25.78GBd per 100G Ethernet requirements. The Xilinx FPGA is connected to a Semtech retimer inside the Finisar CFP4 ER4f module via the OIF-28G-VSR interface comprised of the Xilinx evaluation board, a length of cable and the Finisar CFP4 evaluation board. The equalization in the Semtech retimer is sufficient to recover the data pattern and provide a clean signal to the Finisar optics for transmission over up to 40km of single mode fiber. The JDSU CFP4 100GBASE-LR4 module receives the data pattern, retimes the data and retransmits the data over an OIF-28G-VSR channel comprised of a JDSU CFP4 evaluation board populated with a Yamaichi CFP4 connector, cables and an InPhi evaluation board where the data is recovered by the InPhi CDR device which is running on an independent and asynchronous clock. The InPhi CDR checks the PRBS-31 data to ensure error free performance. In the return direction, the InPhi CDR generates PRBS-31 data which it transmits across an OIF-28G-VSR channel to the JSDU CFP4 optical module. The JDSU optical module transmits at 100GBASE-LR4 output levels over 40km of single mode fiber. The Finisar CFP2 ER4f module receives data at a better than 1e-6 BER, a BER under the threshold recoverable by the 802.3bj RS-FEC. The recovered data is retimed by a Semtech retimer and retransmit over an OIF-28G-VSR channel to be received by the Xilinx FPGA without introducing additional errors. Data is fidelity is checked by the Xilinx FPGA where the BER is confirmed to be better than 1e-6. The combination of Xilinx UltraScale FPGA, Finisar CFP4 ER4f optics, Semtech retimers, JDSU CFP4 100GBASE-LR4 optics and InPhi retimers show extensive industry interoperability across both electrical and optical interfaces.

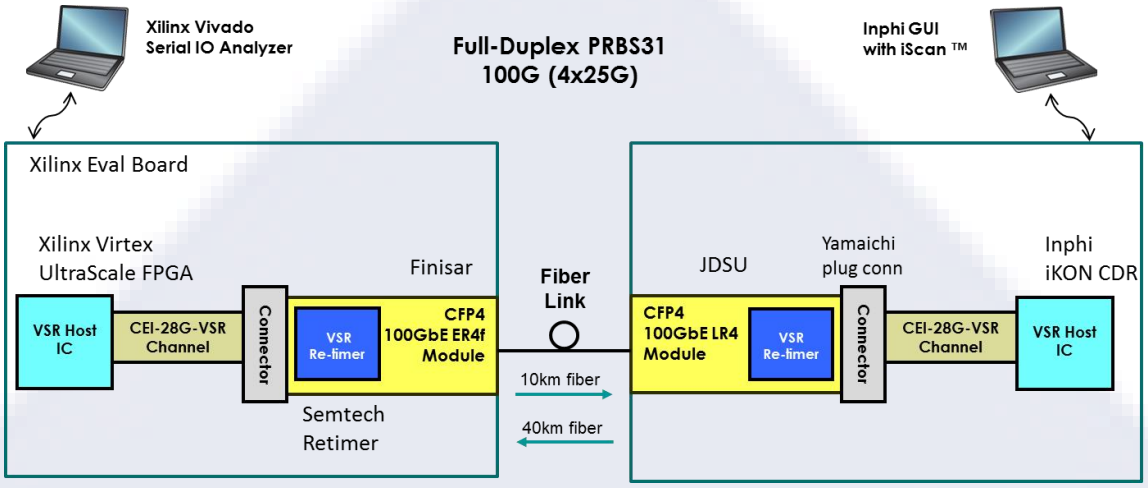

Figure 5: Demo 1 Block Diagram

3.2. Demonstration 2: CEI-28G-VSR CFP4 100GBASE-LR4 Module

Inphi, Finisar, Fujitsu, MoSys, Semtech, Yamaichi

Component Overview

Inphi IN112525 iKON™ CDR: Enabling today's 2-Terabit line cards, the iKON™ Clock and Data Recovery (CDR) Retimer ICs bring advanced transmit and robust and fully adaptive receive equalization for 25 to 28Gbps line card applications. Targeting CFP4 and QSFP28 systems for 100G client side solutions, the low power CMOS architecture deployed in the retimer will accelerate deployment for data center and enterprise networks by using state of the art signal performance monitoring, including Inphi's iScan™, the industry's highest resolution data agnostic margin indicator.

Finisar CFP4 LR4 module: Finisar's FTLC1141 100GBASE-LR4 CFP4 optical transceiver module uses 4x28G DML technology, which enables a lower power dissipation than EML-based solutions. It provides a retimed 4x25G/28G electrical interface to the host board, meets IEEE 802.3, OIF and OTN standards, and interoperates with existing 100GBASE-LR4 CFP, CFP2 and CPAK modules. It is expected to be production-released in 2015.

Fujitsu CFP4 Module: The FOC (Fujitsu Optical Components) CFP4 100GBASE LR4 module applied 4ch 28G integrated DML TOSA and 4ch 28G integrated ROSA. The module realizes transmitter good eye performance and receiver high sensitivity and low consumption power.

MoSys LineSpeed™ MSH110 Retimer: The MoSys LineSpeed™ 100G Low Power Full Duplex Retimer IC (MSH110) is a single-chip, low-power CMOS device optimized for low power retiming/CDR applications inside optical or copper modules or on the line card to support full duplex 100GE or OTN operation. The device supports CFP2, CFP4 and QSFP28 module interfaces with a strong self-adapting equalizer for ease of connection and improved signal integrity up to 20dB of insertion loss. The device features the industry's lowest power dissipation, small full duplex footprint, reference-free operation, system and line side integrated loopbacks, and on-chip PRBS generation, error checking and diagnostic capabilities using the MoSys Spotlight™ Analyzer.

Semtech Retimers: Leveraging a generation of innovation in 10G module CDRs, Semtech's GN2425 and GN2426 are low-power retimers optimized for reference-free 25-28Gbps operation in next-generation optical modules and active cables. By resetting the jitter budgets within the module in both directions, Semtech's CDRs are perfect for challenging new applications such as 100GBASE-LR4/ER4 and OTU4 CFP2 optical modules. The GN2425 and GN2426 feature best-in-class receive sensitivity, input jitter tolerance and output jitter, allowing for reliable signal recovery and clean, wide-open transmit eyes.

Yamaichi CFP4 Connector / CFP4 Module Compliance Board: Yamaichi CFP4 connector and the mechanical parts are fully compliant with CFP MSA spec, and has signal loss performance better than -1dB at 14GHz and better than -1.2dB at 16GHz, which indicates its capability even at 32Gbps per lane usage. The connector system is available with single and quad port cages as standards. Custom design cage and heat sink support is also available. The Yamaichi CFP4 module compliance board has been designed to adhere to OIF CEI-28G-VSR IA and work very well as a module and chip performance evaluation tool.

Demo 2 Description

This demonstration system consists of the following blocks: an Inphi 100G retimer, evaluation board and Yamaichi connector based CFP4 breakout board, a Fujitsu CFP4 LR4 module, a Finisar CFP4 LR4 module with a semtech retimer inside of it, and a MoSys 100G retimer, evaluation board and CFP4 breakout board with CFP4 connector. A PRBS31 data pattern is generated from the Inphi retimer devices across four lanes at 27.95Gb/s per lane to meet OTN requirements or four lanes at 25.78 Gb/s to support the 100G Ethernet rates. The Inphi VSR Host IC is connected to an integrated retimer IC inside the Fujitsu CFP4 module via an evaluation board, Yamaichi connector, and CFP4 breakout card representing approximately 8-10dB of loss. The Tx and Rx inputs on the Inphi retimer and CFP4 module retimer are sufficient to ensure error free operation in both directions to the CEI-28G-VSR electrical requirement. The Fujitsu CFP4 LR4 optical module transmits and receives the data to the Finisar CFP4 LR4 optical module over 10km of single mode fiber. The Finisar module with its integrated retimer is then connected electrically through a CFP4 breakout

card, connector, and evaluation board connector to a MoSys low power retimer IC. The total electrical channel represents approximately 8-10dB of insertion loss – representing CEI-25G-VSR grade channel. Similarly, PRBS 31 traffic is generated in the other direction from the MoSys retimer IC following the return path of 10km of fiber between the Finisar CFP4 and Fujitsu CFP4 LR4 modules and terminating at the Inphi Host IC. Data integrity is monitored by both retimer devices to ensure error free operation and data integrity over extended time (>8 Hours) to conform to the IEEE and OIF standards. The combination of CFP4 LR4 modules from Finisar and Fujitsu and electrical components from Inphi and MoSys, show extensive industry interoperability across both optical and electrical interfaces required to meet both Ethernet and OTN standards.

Demo 2:
CEI-28G-VSR CFP4 Optical Module Demo
(Inphi, Finisar, Fujitsu, MoSys, Yamaichi)

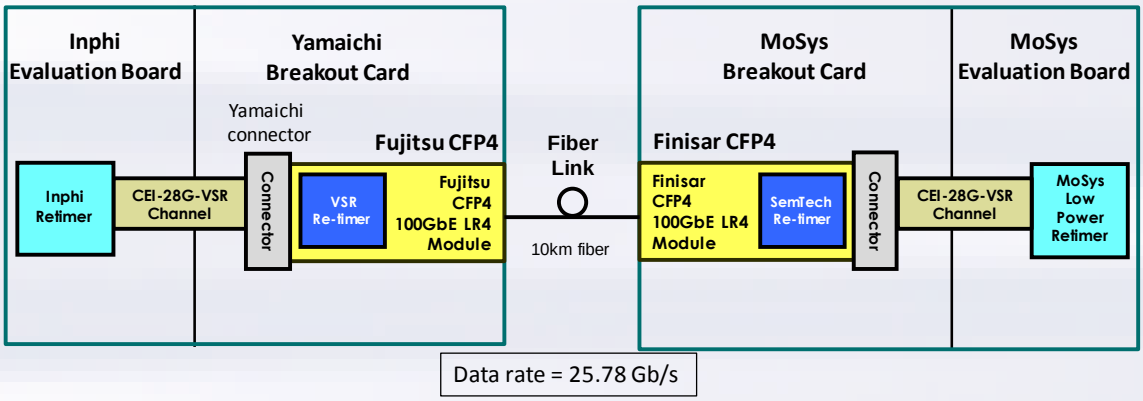

Figure 6: Demo 2 Block Diagram

3.3. Demonstration 3: 4 x 28Gbps over 5m Active Copper Cable

Inphi, MoSys, Semtech and Yamaichi

Component Overview

Inphi IN112525 iKON™ CDR: Enabling today's 2-Terabit line cards, the iKON™ Clock and Data Recovery (CDR) Retimer ICs bring advanced transmit and robust and fully adaptive receive equalization for 25 to 28Gbps line card applications. Targeting CFP4 and QSFP28 systems for 100G client side solutions, the low power CMOS architecture deployed in the retimer will accelerate deployment for data center and enterprise networks by using state of the art signal performance monitoring, including Inphi's iScan™, the industry's highest resolution data agnostic margin indicator.

The MoSys LineSpeed™ 100G Quad Retimer (MSH210) is a single chip low power CMOS IC designed to support full duplex 100 Gigabit links for optical transceivers, active and passive copper cable, extended line card or backplane applications. All SerDes on the PHY IC are equipped with Tx equalization and a strong self-adapting Rx equalizer to support a wide range of IEEE and OIF standards ranging from very short reach (CEI-25G-VSR) to extended reach (CEI-25G-LR) and data rates up to 28 Gbps. The device includes on chip pattern generators, error checking and monitoring capabilities.

The Yamaichi CFP4-Active Copper Cable drives 4 lanes of 28Gbps signals more than 5m length implementing a Semtech retimer chip, with plans to support up to 10m with AWG26 copper cable. The cable module also supports the CFP MSA memory map and MDIO (Clause 45) control interface for compatibility with CFP4 optical transceivers. These features allow the CFP4-ACC as an alternative to optical fiber connections for short reach applications. The internal electrical signal path has been designed to adhere to CEI-28G-VSR IA, and shows great performance together with the Yamaichi CFP4 Connector.

Semtech GN2504 Backplane Re-timer: Building upon the successful GN2104 module re-timer family of parts, Semtech's new GN2504 quad-lane reference-free backplane re-timers is specifically designed for higher loss applications having greater than 30 dB of loss at 25-28Gbps rates including backplane, line-card and copper cable. These backplane re-timers are specifically designed as a high performance, low power solution providing required configurability and robustness including adjustable output de-emphasis and swing and a fully adaptive input equalizer with sophisticated eye monitoring capability.

The Yamaichi CFP4 connector and the mechanical parts are fully compliant with the CFP MSA spec, and has signal loss performance better than -1dB at 14GHz and better than -1.2dB at 16GHz, which gives a capability to 32Gbps per lane. The connector system is available with single and quad port cages as standards. Custom design cage and heat sink support is also available.

The Yamaichi CFP4 Module Compliance Board has been designed to adhere to OIF CEI-28G-VSR IA and enables module and chip performance evaluations.

Demo 3 Description

This demonstration system consists of 4 bidirectional lanes of 28Gbps, resulting in a data aggregation of 112Gbps for OTU4 systems and conforming to CEI-28G-VSR electrical specifications.

A MoSys LineSpeed™ Retimer sends and receives 4x28Gbps prbs31 streams of data through a Yamaichi CFP4 connector/Compliance Board, and into a Yamaichi CFP4-ACC 5m Active Copper Cable module. Inside the CFP4 module

a Semtech GN2504 Retimer includes transmit and fully adaptive receive equalization to compensate for the 5m AWG26 cable loss.

At the far end module the data stream is fed to an Inphi iKON™ Retimer and prbs31 pattern verification and BER are measured, as well as the reverse data stream generated and sent back across the system.

This demonstration shows that CFP4 form factor modules adhering to the OIF CEI-28G-VSR IA can be implemented with Copper Cables in the range of 5m length. This gives a cost effective alternative to optical modules for short reach applications.

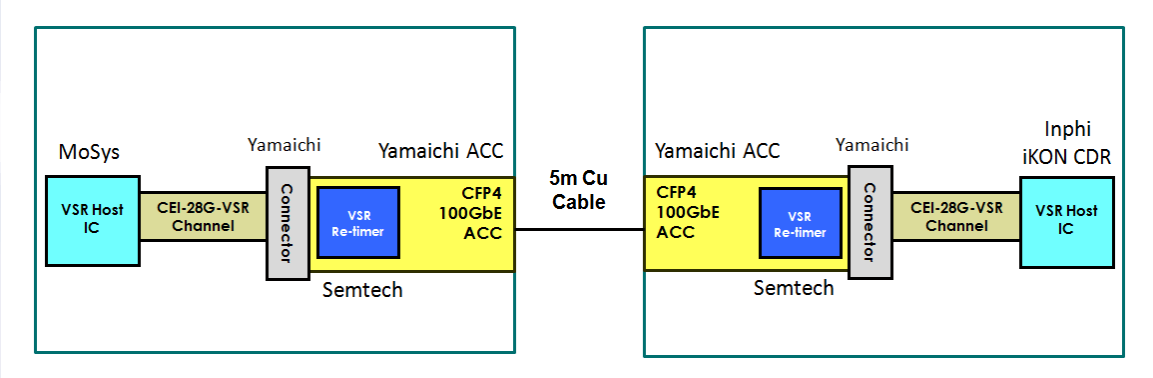

Figure 7: Demo 3 Block Diagram

3.4. Demonstration 4: CEI-28G-VSR QSFP28 Module Compliance Demo

Agilent, Molex, Semtech, TE Connectivity, Tektronix

Component Overview

Agilent 86100D DCA-X Oscilloscope and N5225A Network Analyzer: The 86100D DCA-X Oscilloscope is a modular platform that accommodates up to 4 measurement modules and 16 measurement channels. Includes 86108B 50 GHz module, Option 200 Enhanced Jitter Analysis, Option 201 Advanced Waveform Analysis software and the N1012A OIF CEI 3.1 Compliance and Debug Software. The N5225A Network Analyzer is a four port 50 GHz analyzer with extensive device characterization for single-ended and differential parameters

Molex zQSFP+™ connectors are used on the MCB boards. The zQSFP+ system from Molex supports next-generation CEI-28G-VSR, 100 Gbps Ethernet and InfiniBand Enhanced Data Rate (EDR) applications with excellent cooling, improved signal integrity (SI), superior electromagnetic interference (EMI) protection and low power consumption. The preferential coupling design uses a

narrow-edge coupled, blanked- and formed-contact geometry and insert molding to optimize electrical performance.

Semtech GN2104 Module Re-Timer: Leveraging a generation of innovation in 10G module CDRs, Semtech's quad-lane auto-adaptive GN2104 family of low-power re-timers are optimized for reference-free 25-28Gbps operation in next-generation optical modules and active cables. By resetting the jitter budgets within the module in both directions, Semtech's CDRs are perfect for new applications such as CFP2/4 and QSFP28 optical modules. The GN2104 family features best-in-class receive sensitivity, input jitter tolerance and output jitter, allowing for reliable signal recovery and clean, wide-open transmit eyes.

TE Connectivity's zQSFP+ connector is a new high speed, high density interconnect that supports data rates from 28 Gbps per lane over the connector's 4 channels, providing an aggregate bandwidth of 100Gbps. TE's zQSFP+ connector is used on the TP1a Module Stressed Input Test MCB in the demo. The connector interface is fully backwards compatible to the existing QSFP+ modules and cable assemblies. Through a coupled, narrow-edged, blanked- and formed- contact geometry and insert molding design, the zQSFP+ interconnect exhibits robust industry compliant signal integrity, as well as mechanical and electrical performance. The zQSFP+ cage offers excellent thermal performance and enhanced EMI protection and is available in single ports, ganged ports and stacked ports.

Tektronix DSA8300 Sampling Oscilloscope: The DSA8300 Series is a modular oscilloscope system that allows for electrical and optical sampling modules. For the OIF Interop, Tektronix provides the 80E10B Electrical Module. When used with the DSA8300 Series, this new module provides sub-100 femtosecond intrinsic jitter, low vertical noise, >45GHz bandwidth performance to enable high fidelity measurements of OIF 28G-VSR system.

Tektronix BERTScope BSA286CL: The BERTScope provides Pattern Generation and Error Analysis, High-speed BER Measurements up to 28.6 Gb/s. The latest "CL" model provides fast input rise time / high input bandwidth error detector for accurate signal integrity analysis on OIF-CEI designs.

Tektronix PPG3204 Pattern Generator: The Tektronix PatternPro® series programmable pattern generators provide up to four channels of stressed pattern generation for high-speed datacom testing and crosstalk generation.

Demo 4 Description

The goal of the demonstration is to verify that the Semtech module re-timer is able to meet all of the CEI-28G-VSR requirements over a QSFP28 based chip-to-module channel at an operating data rate of 28.0Gb/s. Two important module

tests include the host-to-module stressed input test at the module TP1a test point and that the module-to-host output eye measurement at the TP4 test point as shown in the Figure below. Other important tests include minimum requirements for input differential and differential to common mode return loss as documented in the VSR IA specification. As well, the VSR test philosophy is predicated upon a minimum set of performance parameters for the MCB (module compliance board) and HCB (host compliance board) boards. For this demonstration Semtech manufactured both MCB and HCB boards as well as module PCB boards. The mated MCB/HCB system was required to meet several S-parameter requirements as outlined in the VSR Implementation Agreement.

The QSFP28 channel for the TP1a test was based upon a VSR MCB which was assembled with a TE Connectivity connector as well as a module PCB based upon GN2104 CDRs. An important part of setting up the TP1a test is to ensure that the required eye height and widths are properly calibrated at TP1a using a mated MCB/HCB system along with a source which is able to inject the necessary sinusoidal and Gaussian jitter for this test. This portion of the test is configured using the Tektronix BertScope unit and the Freq Dependent attenuator PCB at the TP1 test point. Also, the crosstalk aggressors from the neighboring channels are required to be injected into the system, also at TP1 which was carried out by the Tektronix PPG3204 generator. During the calibration phase the eye height and width requirements were verified using the S/W CTLE function which was provided within the Tektronix DSA8300 Sampling Oscilloscope. Once the TP1a channel was calibrated then the HCB was swapped with the actual module PCB and the system was verified to be able to tolerate its stressed input which includes varying sinusoidal jitter using the Tektronix BertScope. Another crucial requirement for the module input is that it meets its various TP1 input S-parameter measurements which were carried out by the Agilent PNA-X VNA for this demonstration.

The QSFP28 channel for the TP4 test was also based upon a VSR MCB, but in this case it was instead assembled with a Molex connector, and the module PCB was based upon GN2104 CDRs as was the case for the TP1a stressed test. The output eye requirements were verified using the module PCB connected to the MCB along with the necessary aggressors injected into the system at the TP4 test point. The TP4 eye width and eye height requirements were verified using the built-in S/W CTLE function within the Agilent 86100D sampling oscilloscope.

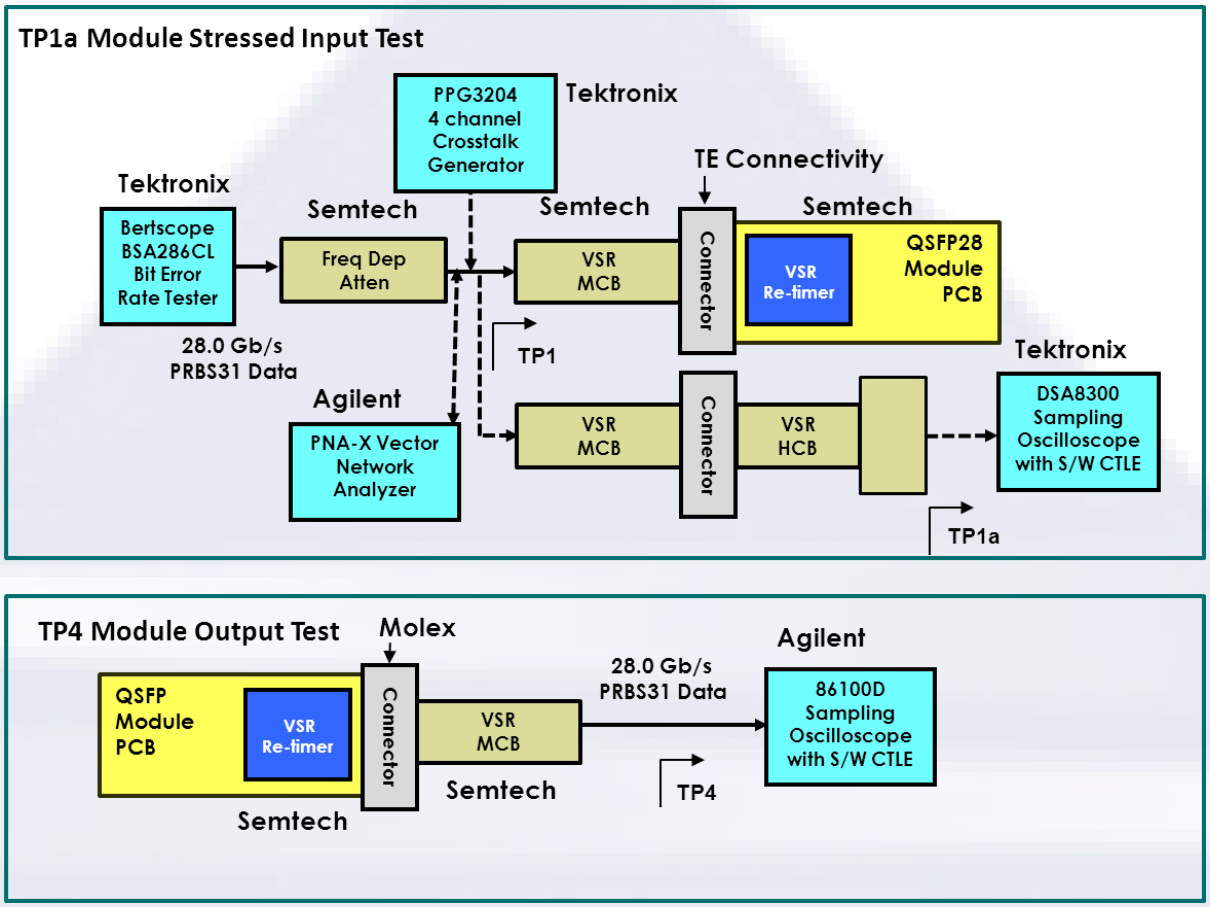

Figure 8: Demo 4 Block Diagram

3.5. Demonstration 5: CEI-25G-LR QSFP28 Passive Cu Cable Demo

Amphenol, Molex, MoSys, TE Connectivity, Yamaichi

Component Overview

Amphenol QSFP28 Passive Copper Cables / QSFP Connector: Amphenol, in demo 5, will be demonstrating their ExpressPort QSFP+ 28Gb/s/lane, 100Gb+ capable connector system. Along with the connector and breakout boards, various lengths and gauges of passive copper cables will also be demonstrated. The Amphenol cables employ the SpectraStrip SkewClear EXD copper cable for greater link distances."

Molex QSFP28 Passive Copper Cables / QSFP28 Connector: zQSFP+ cables provided by Molex are constructed of a very low loss, 100 ohm, eight pair bundled twinax. The twinax is terminated to a passive, low loss PCB providing a final 28G passive cable assembly in 2m, 3m and 4m lengths

Molex zQSFP+TM connectors compatible with QSFP28 are used on the MCB boards. The zQSFP+ system from Molex supports next-generation CEI-28G-VSR, 100 Gbps Ethernet and InfiniBand Enhanced Data Rate (EDR) applications with excellent cooling, improved signal integrity (SI), superior electromagnetic interference (EMI) protection and low power consumption.

MoSys Gearbox: The MoSys LineSpeed™ 100G Multi-Mode Gearbox IC (MSH310) is a single-chip, low-power CMOS device designed to support 10:4 gearbox or 10:10 retiming applications for 10G, 40G and 100G Ethernet and OTU4 line cards and optical modules. The device features a strong self-adapting equalizer for extended reach on both the 10G and 25G lanes and supports standards ranging from CEI-28G-VSR to CEI-25G-LR. The device includes on-chip PRBS generation, error checking and diagnostic capabilities.

TE Connectivity QSFP28 Passive Copper Cable / QSFP28 Connector: TE Connectivity has supplied a number of 100G (4x25G) QSFP28 passive direct attach copper cable assemblies for use in Demo 5. These cable assemblies feature TE's own Madison Cable brand TurboTwin parallel pair bulk cable with optimized construction which minimizes insertion loss and cross talk and a unique drainless bulk cable construction. The assemblies range from 24AWG through 33AWG with eight differential copper pairs, providing four data transmission channels. Various market applications demand a wide range of cable lengths and diameters (wire gauges), which can be met with TE's cables. The contributed samples range from 0.5 meters to 6 meters. These next generation cables share the same mating interface with QSFP+ form factors, making them backward compatible with existing QSFP ports.

TE Connectivity's zQSFP+ connector is a new high speed, high density interconnect that supports data rates from 28 Gbps per lane over the connector's 4 channels, providing an aggregate bandwidth of 100Gbps. The connector interface is fully backwards compatible to the existing QSFP+ modules and cable assemblies. Through a coupled, narrow-edged, blanked- and formed- contact geometry and insert molding design, the zQSFP+ interconnect exhibits robust industry compliant signal integrity, as well as mechanical and electrical performance. The zQSFP+ cage offers excellent thermal performance and enhanced EMI protection. Connectors are available in cages with individual, ganged and stacked ports to meet a wide range of equipment density and packaging options.

Yamaichi QSFP28 Passive Copper Cable / QSFP28 Connector:
Yamaichi QSFP28 Passive Copper Cable works at 100GBASE-CR4 channels up to 5m length with variation of AWG30 to AWG24 cable size. This QSFP28 Passive Copper Cable also support InfiniBand EDR channel as well.

The Yamaichi QSFP28 connector complies to SFF-8672 standard which has full compatibility with existing generation of 10Gbps QSFP+ connector footprints and cages. This feature allows using common mechanical parts between 40GbE QSFP+ and 100GbE QSFP28, which generates purchasing volume advantage. Even having this mechanical compatibility feature, Yamaichi QSFP28 connector still has good signal performance, and performing -1.65dB loss at 28GHz which is potentially capable at 56Gbps per lane usage as well.

Demo 5 Description

This demonstration system consists of the following blocks: a MoSys 100G Gearbox and evaluation board, a MoSys 100G retimer and evaluation board connected with QSFP28 breakout cards, connectors and various length and gauge QSFP28 passive copper cable assemblies from Amphenol, Molex, TE Connectivity and Yamaichi.

In this demonstration, the MoSys Gearbox device generates 4 lanes of PRBS 31 traffic at 25.78Gb/s from the evaluation board. The evaluation board is then connected to a breakout card and connector from Amphenol, Molex, TE Connectivity and Yamaichi. A QSFP28 passive copper cable of various lengths and widths with examples being 2 meters of 30 AWG, 3 meters of 28 AWG or 4 meters of 26 AWG, are connected to second connector and breakout card on the other side of the link. The four lanes are connected and error checking is performed on the 100Gb/s link in the MoSys retimer device. In order to create and verify a full duplex 100Gb/s link, 4 lanes of 25.78Gb/s traffic is generated and checked across in the opposite direction across the QSFP28 cable, connectors and breakout boards. The electrical channel was represented by OIF CEI-25G-LR with insertion loss from end to end up to approximately 27-28dB (depending on setup and cable length/type). The QSFP28 breakout cards, connectors and passive copper cables are interchanged in the setup between different vendors. The performance is measured and monitored to be error free using MoSys IC Spotlight™ Analyzer.

Demo 5 operated error free across all four lanes at 25.78Gb/s with a PRBS31 data pattern in both directions.

Demo 5:
CEI-25G-LR QSFP28 Passive Cu Demo
(Amphenol, Molex,Mosys , TE Connecttivity, MoSys, Yamaichi)

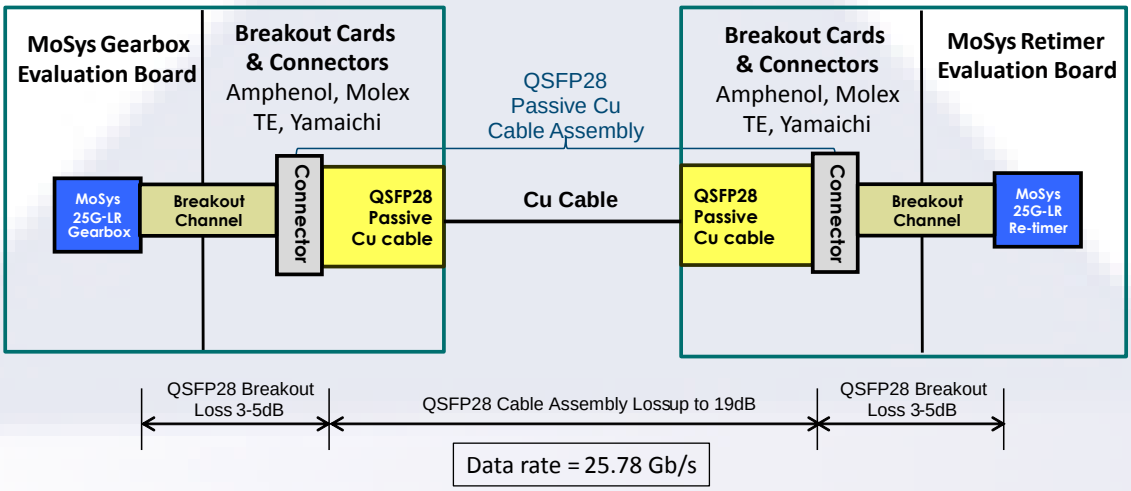

Figure 9: Demo 5 Block Diagram

3.6. Demonstration 6: CEI-25G-LR Application

Amphenol and Semtech

Component Overview

Amphenol Connector: Amphenol Xcede connector family of connectors provide superior signal integrity performance up to 28Gb/s, The Xcede2 coming out in 2014 will provide performance to 56Gb/s. The Xcede plus used in this back plane demonstration has dedicated tooling for 85 or 100 Ohm impedance, lower insertion loss and supports embedded capacitor technology.

Amphenol Backplane: The Amphenol supplied reference backplane channel consists of two daughter cards, a backplane, and two XcedePlus connectors. The XcedePlus connector is ideal for the 25Gb/s per lane we demonstrating here. It is backward compatible with legacy Excede connectors so new daughter cards can be used in existing systems. The Semtech SerDes connects to the Amphenol daughter cards through 2.4mm connectors.

The daughter cards are a 20 layer PCB with Megtron6 for the high sped signal layers. There are various breakout layers and with a total etch length of 7”.

The backplane is also a 20 layer PCB employing Megtron6 in the high speed signal layers. The total etch length used in the demo is 12 inches. The 85 Ohm differential pairs are made up of a 7.0 / 5.0 / 7.0 geometry.

Semtech GN2504 Backplane Re-timer: Building upon the successful GN2104 module re-timer family of parts, Semtech's new GN2504 quad-lane reference-free backplane re-timers is specifically designed for higher loss applications having greater than 30 dB of loss at 25-28Gbps rates including backplane, line-card and copper cable. These backplane re-timers are specifically designed as a high performance, low power solution providing required configurability and robustness including adjustable output de-emphasis and swing and a fully adaptive input equalizer with sophisticated eye monitoring capability.

Demo 6 Description

The goal of the demonstration is to exhibit the OIF CEI-25G-LR Implementation Agreement (IA) with 4-lane 100G operation across a backplane link with end-to-end loss greater than 25dB at 12.9GHz. Each lane carries a PRBS31 pattern running at a 25.78125Gb/s data rate. PRBS generation and checking is performed on-chip.

The demonstration includes a Semtech backplane re-timer operating over a Amphenol-supplied reference backplane. The total insertion loss of the backplane is 31db and includes the 30 inch backplane trace and the paddle cards to the coaxial connectors.

The entire channel loss including the coaxial interconnect and the evaluation board PCB traces is approximately 34dB. The demonstration ran 4 lanes of bidirectional traffic at 25.78Gbps resulting in 4 NEXT (near end cross talk) lanes, in row and in column, and 3 FEXT (far end cross talk) lanes, in row and in column acting on victim pairs in order to increase the amount of crosstalk.

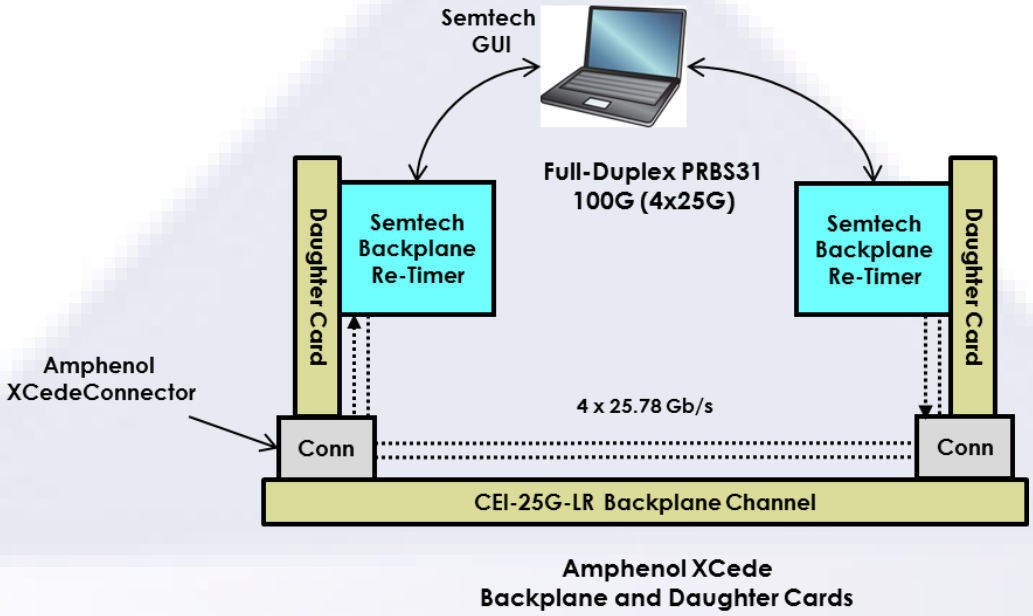

Figure 10: Demo 6 Block Diagram

3.7. Demonstration 7: CEI-25G-LR Application

Xilinx and Molex

Component Overview

Molex Connector: The Impel™ Backplane Connector System provides a scalable price-for-performance solution enabling customers to secure a high-speed 25Gbps – 56Gbps connector with industry leading density. The Impel™ Connector System provides the footprint and interface that will enable customers to migrate to faster data rates 56Gbps, through an optimized electrical structure that leverages tightly coupled differential pairs with improved pair-to-pair isolation. The Impel™ backplane connector family is a 92ohm solution providing low cross-talk and high signal bandwidth while minimizing channel performance variation across every differential pair within the system.

Molex Backplane: The Impel Backplane system consists of a Reference Backplane (BP), and 2 Reference Daughter Cards (DC), using the 4-pair Impel™ Backplane Connector solution (BP = 171315-1807 and DC = 171320-1038).

The reference backplane uses Megtron 6 material, is 6.35mm thick with trace width and spacing of 7mils/8mils/7mils and controlled to a nominal impedance of 90ohms. There are 4 different trace lengths are available on Impel™ Reference BP: 0.166 meter, 0.286 meter, 0.516 meter, and 0.746 meter. The Reference Backplane is designed for 90ohm differential impedance to reduce impedance

discontinuity between Impel™ backplane connector, backplane connector via, and differential traces.

There are 2 Daughter-card boards used in conjunction with the Reference Backplane. The Reference Backplane Daughter-card boards are made with Megtron 6 material with a provided total thickness of 3.05mm. The Reference Backplane Daughter-card boards utilize 5.9mils/4.1mils/5.9mils for trace width and spacing, are controlled to a nominal impedance of 90ohms, and contribute to a total of 5-inches, (0.127m), of trace length. Each DC board utilizes the Impel™ part number 171320-1038 in conjunction with 2.92mm RF connectors. The total channel lengths in the mated condition of DC to BP are as follows: 0.42 meter, 0.54 meter, 0.77 meter and 1 meter.

The Xilinx Virtex® UltraScale™ family of FPGAs is implemented on the latest 20nm SOC process. The FPGA contains 940,800 logic cells, 768 DSP slices, 62,208Kbits of block RAM (BRAM), four 100G Ethernet blocks, six 150GBd Interlaken blocks, 32x 16.3 GBd GTH transceivers and 32x 32.75 GBd GTY transceivers. The GTY transceivers are designed to exceed the OIF-28G-VSR and OIF-25G-LR electrical specifications and are targeted to interoperate with the latest CFP4 optical modules and 28 GBd backplanes. For the demonstration, the device has been configured with an IBERT IP example design that is simultaneously transmitting and receiving PRBS-31 and checking the received data for errors. Performance is reported via the Vivado® Serial IO Analyzer.

Demo 7 Description

The goal of the demonstration is to exhibit the OIF CEI 25G LR Implementation Agreement (IA) with 4-lane 100G operation across a backplane link with end-to-end loss of >25dB at 12.9GHz. Each lane carries a PRBS-31 pattern running at a 25.78125Gb/s data rate. PRBS generation and checking is performed on-chip.

The demonstration contains a Xilinx Virtex UltraScale FPGA chipset operating over a Molex-supplied reference backplane. The 0.516 meter backplane channel and two 0.127 meter line cards, which are used in this demonstration, contains approximately 27dB of loss from the 2.94 mm connector on one daughter card to the 2.94 connector on the other daughter card. An additional 6 dB of loss is on the Xilinx Virtex UltraScale FPGA Retimer Evaluation Board for a total channel loss of 33dB. The demonstration runs 4 lanes of bidirectional traffic at 25.78Gbps resulting in 4 NEXT (near end cross talk) lanes, in row and in column, and 3 FEXT (far end cross talk) lanes, in row and in column acting on victim pairs in order to increase the amount of crosstalk.

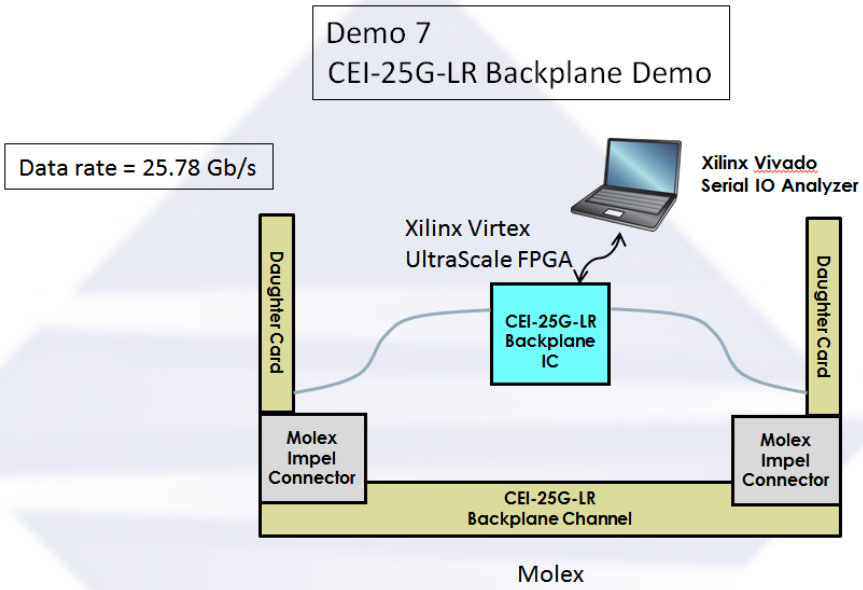

Figure 11: Demo 7 Block Diagram

3.8. Demonstration 8: CEI-25G-LR Application

Semtech, TE Connectivity and Xilinx

Component Overview

Semtech GN2504 Backplane Re-timer: Building upon the successful GN2104 module re-timer family of parts, Semtech's new GN2504 quad-lane reference-free backplane re-timer is specifically designed for higher loss applications having greater than 30 dB of loss at 25-28Gbps rates including backplane, line-card and copper cable. These backplane re-timers are specifically designed as a high performance, low power solution providing required configurability and robustness including adjustable output de-emphasis and swing and a fully adaptive input equalizer with sophisticated eye monitoring capability.

TE Connectivity Connector: TE's STRADA Whisper backplane connector is designed to support data rates per differential pair up to 56Gbps. The connector's individually shielded pairs results in noise performance that is less than 1% @ 20 ps signal edge rates and insertion loss of less than 1db and flat past 15GHz. STRADA Whisper connectors are available in both 100 ohm and 85 ohm versions and can be supplied with embedded capacitors. The in-row "horizontal" pair orientation results in zero skew. Since PCB interfaces are a critical element of over-all connector performance, the STRADA Whisper connector footprint has been engineered to optimize the technical tradeoffs of impedance, cross talk and route-ability.

Xilinx FPGA: Xilinx VU095 Virtex® UltraScale™: The Xilinx Virtex® UltraScale™ family of FPGAs is implemented on the latest 20nm SOC process. The FPGA contains 940,800 logic cells, 768 DSP slices, 62,208Kbits of block RAM (BRAM), four 100G Ethernet blocks, six 150GBd Interlaken blocks, 32x 16.3 GBd GTH transceivers and 32x 32.75 GBd GTY transceivers. The GTY transceivers are designed to exceed the OIF-28G-VSR and OIF-25G-LR electrical specifications and are targeted to interoperate with the latest CFP4 optical modules and 28 GBd backplanes. For the demonstration, the device has been configured with an IBERT IP example design that is simultaneously transmitting and receiving PRBS-31 and checking the received data for errors. Performance is reported via the Vivado® Serial IO Analyzer.

The TE supplied daughter cards are 110mils thick using Megtron 6 material encompassing 14 layers each.[1] All of the differential traces routed from the 2.4mm test points to the skew-less STRADA Whisper connector footprint are 5 inches in length in a 6-9-6 mil trace width configuration. The traces and other copper in the boards utilize Megtron 6 VLP foil finishes. The signal vias in both the STRADA Whisper connector and 2.4mm test points are counter-bored to within 10 mils of the signal layer. The daughter card contains the STRADA Whisper receptacle.

The TE supplied backplane, which contains the STRADA Whisper connector header, is 200mils thick using Megtron 6 material encompassing 20 layers. All of the differential traces routed on the backplane are in a 7-9-7 mil trace width configuration. The traces and other copper in the board utilize a Megtron 6 H-VLP foil finish. The signal vias in the STRADA Whisper connector footprint are counter-bored to within 10mils of the signal layer. The backplane demonstrates lengths of 4, 8, 17, and 30". When combined with a daughter card on each end the total trace length demonstrated in the channel is extended to 14, 18, 27, and 40 inches.

Demo 8 Description

The goal of the demonstration is to exhibit the OIF CEI-25G-LR Implementation Agreement (IA) with 4-lane 100G operation across a backplane link with end-to-end loss of >25dB at 12.9GHz. Each lane carries a PRBS-31 pattern running at a 25.78125 Gb/s data rate. PRBS generation and checking is performed on-chip.

The demonstration includes a Xilinx FPGA interoperating with the Semtech backplane re-timer over a TE Connectivity-supplied reference backplane. The TE Connectivity channel is built with Megtron6 material and implements TE's STRADA Whisper backplane connector product.

[1] Megtron is a registered trademark of Panasonic.

The 30 inch backplane channel and two 5 inch line cards, which are used in this demonstration, contain approximately 27dB of loss from the 2.4mm connector on one daughter card to the 2.4mm connector on the other daughter card. Several dB of additional loss takes place on the Xilinx and Semtech evaluation cards and coaxial interconnect so that total channel loss exceeds 30 dB. The demonstration runs 4 lanes of bidirectional traffic at 25.78Gbps resulting in 4 NEXT (near end cross talk) lanes, and 3 FEXT (far end cross talk) lanes, acting on victim pairs in order to increase the amount of crosstalk.

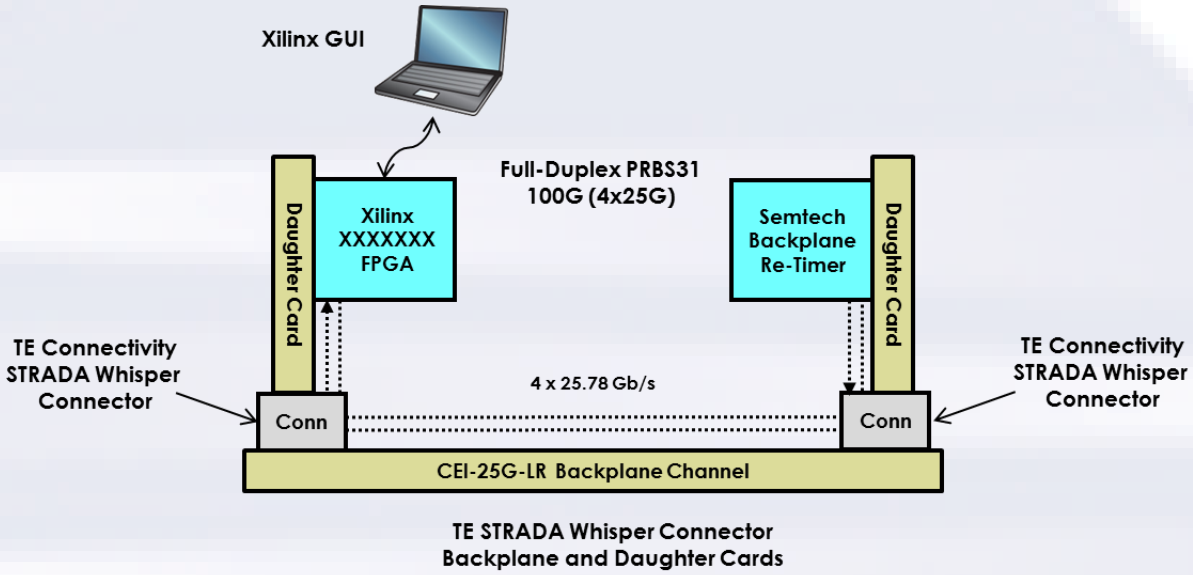

Figure 12: Demo 8 Block Diagram

3.9. Demonstration 9: Module to Host Thermal Interface Modeling

Molex, TE Connectivity

Demonstration 9

Thermal Interface Background Information and Applications

The Module to Host Thermal Interface application reference diagram is shown in Figure 13. It consists of a pluggable optical transceiver that is dissipating power mounted in a cage on the host board (line card) and the cage has a heat sink to aid in transferring the thermal energy from the optical module into the airflow provided by the host line card for the purpose of managing the system's thermal environment. Insufficient thermal conduction between the optical module and heat sink will increase the temperature of the internal components. High

operating temperatures may reduce system performance, reduce product reliability and possibly cause the product to shut down. A representative graph of the effect of different fin geometry on the case temperature of seven horizontally mounted optical modules under three different air flow rates is shown in Figure 14. This illustrates the effect that a heat sink variation can have on a pluggable optical transceiver case temperature. Historically, as data rates increase the power dissipation of the optical module increases resulting in increased power densities and a requirement for more tightly controlled thermal interfaces. The intent of the OIF's effort in this case is to develop a document that will provide a degree of standardization and common understanding across the Networking Industry. For additional information, see the OIF's white paper on this subject.

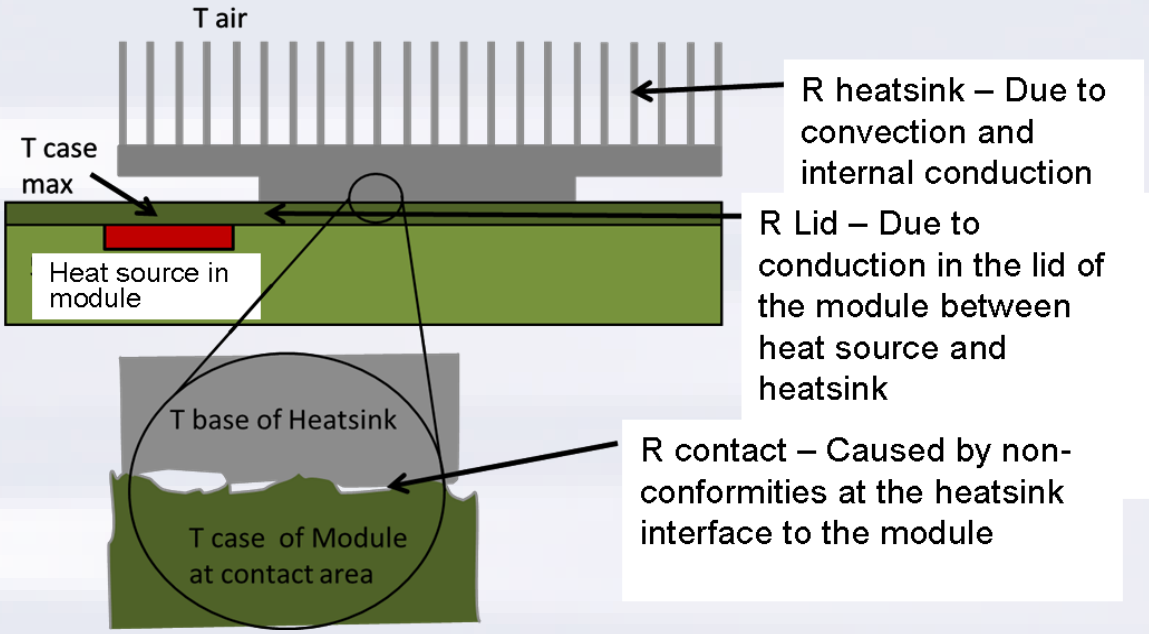

Figure 13: Module to Host Thermal Interface

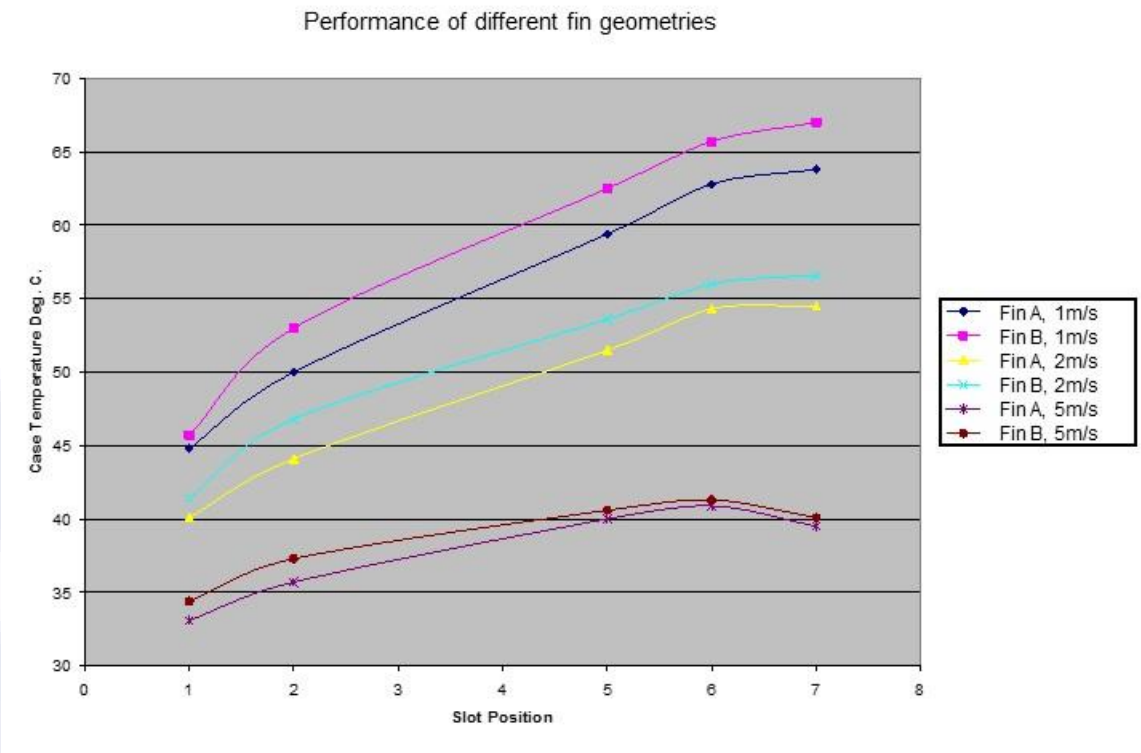

Figure 14: Performance of Different Heat Sink Fin Geometry

Thermal Interface of Pluggable Modules

Participating companies in Demo 9 were Molex and TE Connectivity with a thermal emulator test vehicle, simulating a line card with thermally programmable pluggable modules, and various heat sink solutions in support of the OIF's active project to develop an Implementation Agreement defining standardized thermal interfaces between pluggable modules and hosts.

Thermal Interface Overview

Currently there is no standardized thermal interface definition between a pluggable module and a host. This is because pluggable modules are developed by various independent MSAs, as well as individual contributors with no wide-spread standardization. The OIF has a current project in process to develop an Implementation Agreement that plans to provide a standardized methodology of defining thermal interfaces on optical modules that can be shared across industry. To support that project Molex and TE Connectivity have teamed up to demonstrate the effects of some of the variables that must be considered in a module to host thermal interface.

Component Overview

CDFP Connector/Cage: Supporting next-generation 400 Gbps applications, the CDFP Interconnect System will transmit 400 Gbps data rates (25 Gbps per-serial-lane) with excellent signal integrity (SI), electromagnetic interference (EMI) protection and thermal cooling. The CDFP connector will offer a dense, fast interconnect to the market and is currently being defined by the new CDFP multi source agreement (MSA). The 120 circuit connector is a double paddle card receptacle design integrated into a metal cage. The connector will be offered in two styles: style 1 (short body) for passive or active copper cables; style 2 (long body) for optics such as active optical cables (AOCs) or pluggable transceivers. The zCD passive copper cable assemblies will offer the densest 25 Gbps copper solution in the market when used with the zCD style 1 connector. The small and highly flexible assembly will use proven individual twinax and braid construction for short-reach 400 Gbps Ethernet (GbE) or legacy and proprietary applications.

CDFP Active Optical Cables (AOC): The CDFP AOCs deliver 16-by-28 Gbps, or 400 Gbps of bandwidth, in a compact CDFP MSA standard interface. The units used in the demo are VCSEL based, but single mode lasers can also be accommodated for longer reach solutions.

In this demo the Style 2 (long body) connector and cage are used along with actual Active Optical Cable assembly ends (fiber's have been cut off). The power dissipation of each plug is managed by turning on various functions inside the module via the 2 wire control interface.

Demo 9 Description

This demonstration consists of a line card thermal emulator test platform that consists of a simulated line card supporting 8 positions of the CDFP 400Gb/s optical module that is in process of being defined by the CDFP MSA (see Figure 3). This emulator allows the 8 pluggable positions to be powered to various levels of power dissipation, monitors the heat sink temperatures, is able to vary the flow rate of the cooling air passing over the modules/heat sinks and monitors air pressure. Using such a test platform enables an investigation of single variable and multiple variable scenarios in a controlled setting. In the demonstration that was completed in August 2014, Molex and TE considered three different heat sink flatness's on the CDFP modules and also looked at two heat sink fin geometries. It has been demonstrated that flatter surfaces do enhance the thermal transfer efficiency but not to a great degree. Based on this result, secondary data was captured looking at heat sink fin geometry.

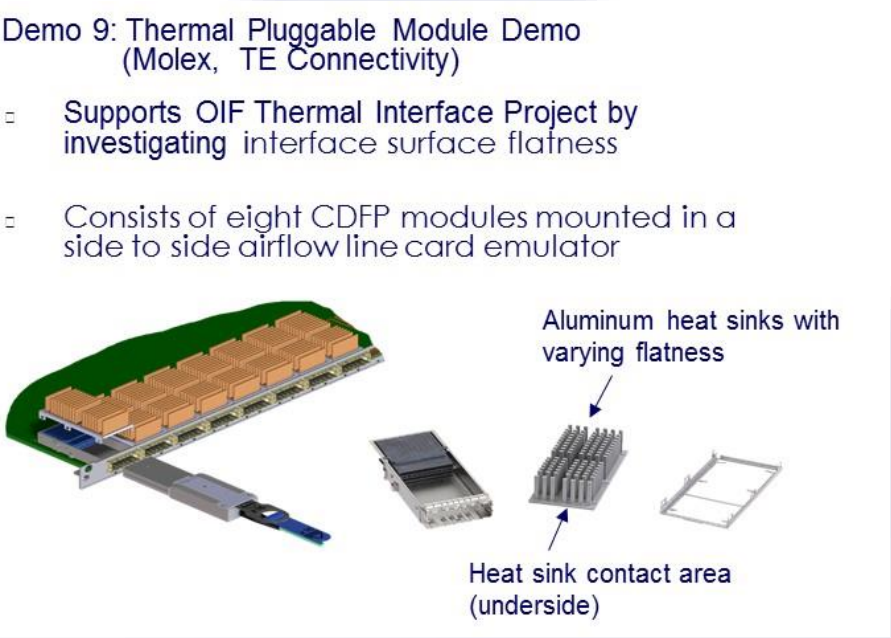

Figure 15: Demo 9 - Thermal Pluggable Module

4. Conclusions

Leveraging OIF developed standards, the demonstrations build on previous interoperability events by showing the breadth and robustness of these industry standards in establishing a strong ecosystem. The nine demonstrations highlight the latest in emerging technology and how the OIF standards bring semiconductor, connector, optical module, active copper cable, passive copper cables, backplane and test equipment vendors together using a common interface.

OIF CEI-28G-VSR is the key building block for next generation 100 GbE, OTN, 32 GFC (Fibre Channel), and IB EDR (InfinBand) retimed optical modules. The interoperability demonstrations of CFP4 modules supporting various optical standards such as LR4 and ER4 and active copper cables, successfully highlighted use of the OIF CEI-28G-VSR specification. This OIF standard is widely accepted and the IEEE 802.3bm CAUI-4 specification is being developed largely based on OIF CEI-28G-VSR specification.

The demonstrations of the OIF CEI-25G-LR show the industry interoperability for long reach applications with channels at or in excess of 25dB. Several industry backplanes and passive copper cables using the QSFP28 form factor were demonstrated successfully interoperating using the electrical standard.

The thermal interface demonstration represents the OIF work that is in process to develop a thermal interface implementation agreement.