

Collaboration and Innovation. At Light Speed.



Market Drivers for Physical Layer Electrical Interoperability at 25-28 Gbaud

Market Trend/Needs

Next generation architectures capable of supporting industry growth rates To enable economical adoption of 100Gb/s, definition of signals was required for board-to-board, chip-to-chip and chip-to-module

Broad deployment through interoperable chips, connectors, and optical modules

Interconnect Challenges

Ensure robust electrical interfaces able to meet system Bit Error Rate (BER) targets Multi-vendor Interoperability Defined parameters meeting industry







PLL Demo Overview

PLL Demo includes five individual Interop Demo's made up of ten participating companies and one test equipment vendor Three demos focused on Very Short Reach chip-to-module applications based upon CEI-28G-VSR

Two demos focused on Long Reach backplane applications using CEI-25G-LR

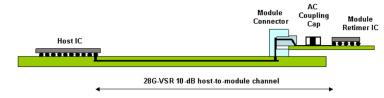
Plugfests completed in January 2012



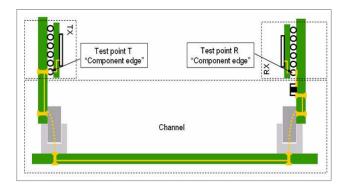


CEI-28G-VSR and CEI-25G-LR Application Overview

28G-VSR targeted to chip-tomodule channels of up to 10 dB loss



25G-LR targeted to backplane channels of up to 25 dB loss

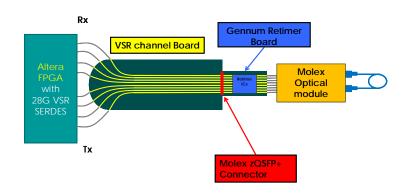




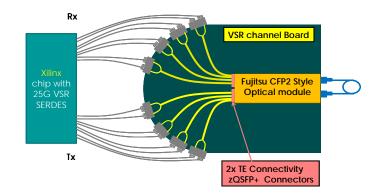


Three CEI-28G-VSR demos

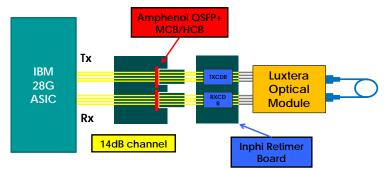
Demo No. 1 Altera - Gennum - Molex



Demo No. 2 Xilinx - TE Connectivity -Fujitsu Optical Components



Demo No. 3 IBM - Amphenol – Inphi - Luxtera

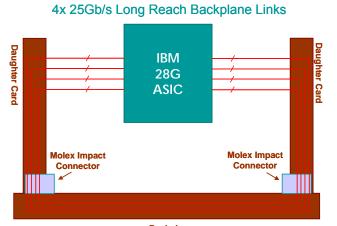




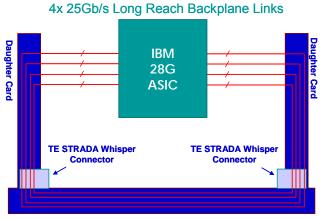
Two CEI-25G-LR demos

Demo No. 4 IBM - Molex

Demo No. 5 IBM – TE Connectivity



Backplane



Backplane



Benefits of PLL Interoperability Demo

Demonstration of viability of next generation 25 – 28 Gb/s electrical system interfaces for switches, routers, transport and data center equipment

- Validation of interface architectures and constraints as defined in the Implementation Agreement
- Demonstration that an Ecosystem is now in place to deliver the next generation of data rates to System OEM vendors and manufacturers

