Panel: Enabling Next Generation Co-Packaging Solutions

Panelists

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OIF Physical & Link Layer Working Group CO-Packaging Vice Chair

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Panelists

Nathan Tracy

Technologist, System Architecture Team and Manager of Industry Standards at TE Connectivity

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OIF Market Awareness & Education Committee Co-Chair, Physical & Link Layer

AGENDA

- **Co-Packaging Framework Document**
- **External Laser for Co-packaging**
- **3.2T Module for Co-packaging**
- **Co-Packaging Electrical Interfaces**
- **Thoughts on Where to Go From Here**
- **Challenges for Next Generation Co-Packaging Solutions**
- **Panel Discussion**

Co-Packaging Framework Document

K.P. Jackson
March 9, 2023
Sumitomo Electric

Where the optical networking industry's interoperability work is done

PROJECT HIGHLIGHTS 2023

130+ member companies → Identifies Industry Needs and Gaps → Develops Implementation Agreements → Performs Interoperability Demonstrations

OPTICAL

Multivendor interoperability in client form factors

800ZR
- >80km Coherent DWDM

800LR
- <10km Coherent Point-to-Point

400ZR
- >80km Coherent DWDM
- >25km Coherent

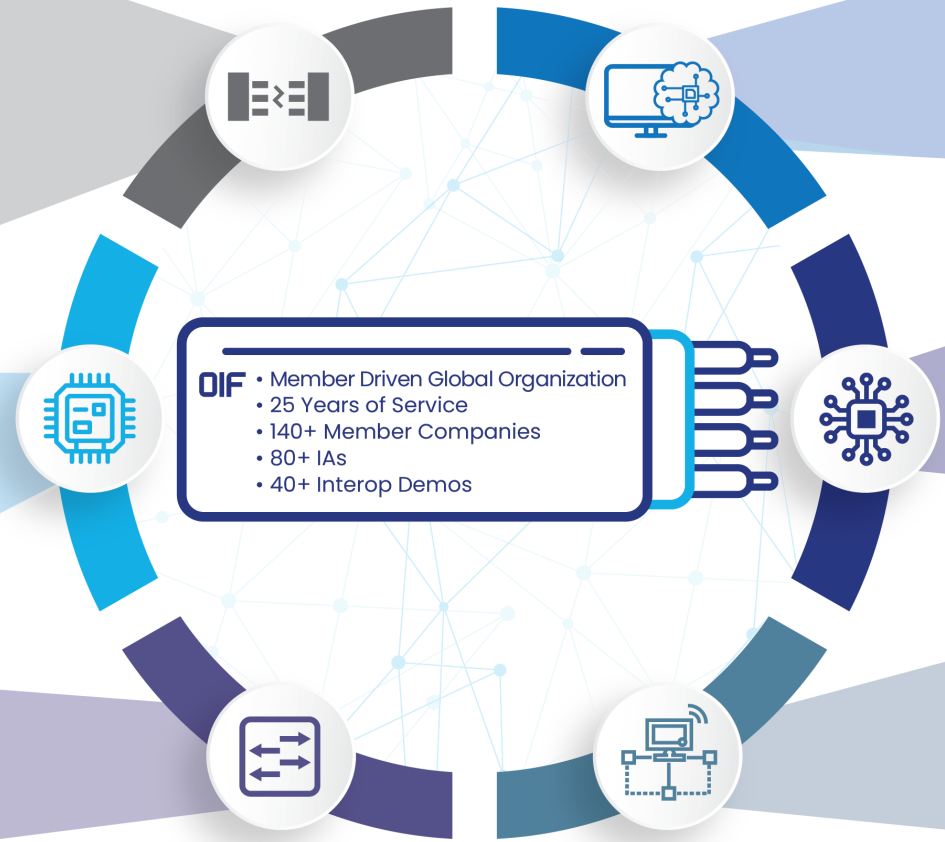
CO-PACKAGING

Co-Packaged Modules
- Densely Integrated Modules
- High Capacity, Energy Efficient

External Laser Sources
- Multivendor Interoperability

PROTOCOL

FlexE
- More Efficient
- Agile Networking



MANAGEMENT

CMIS and Coherent CMIS
- Common
- Flexible
- Extendable

ELECTRICAL

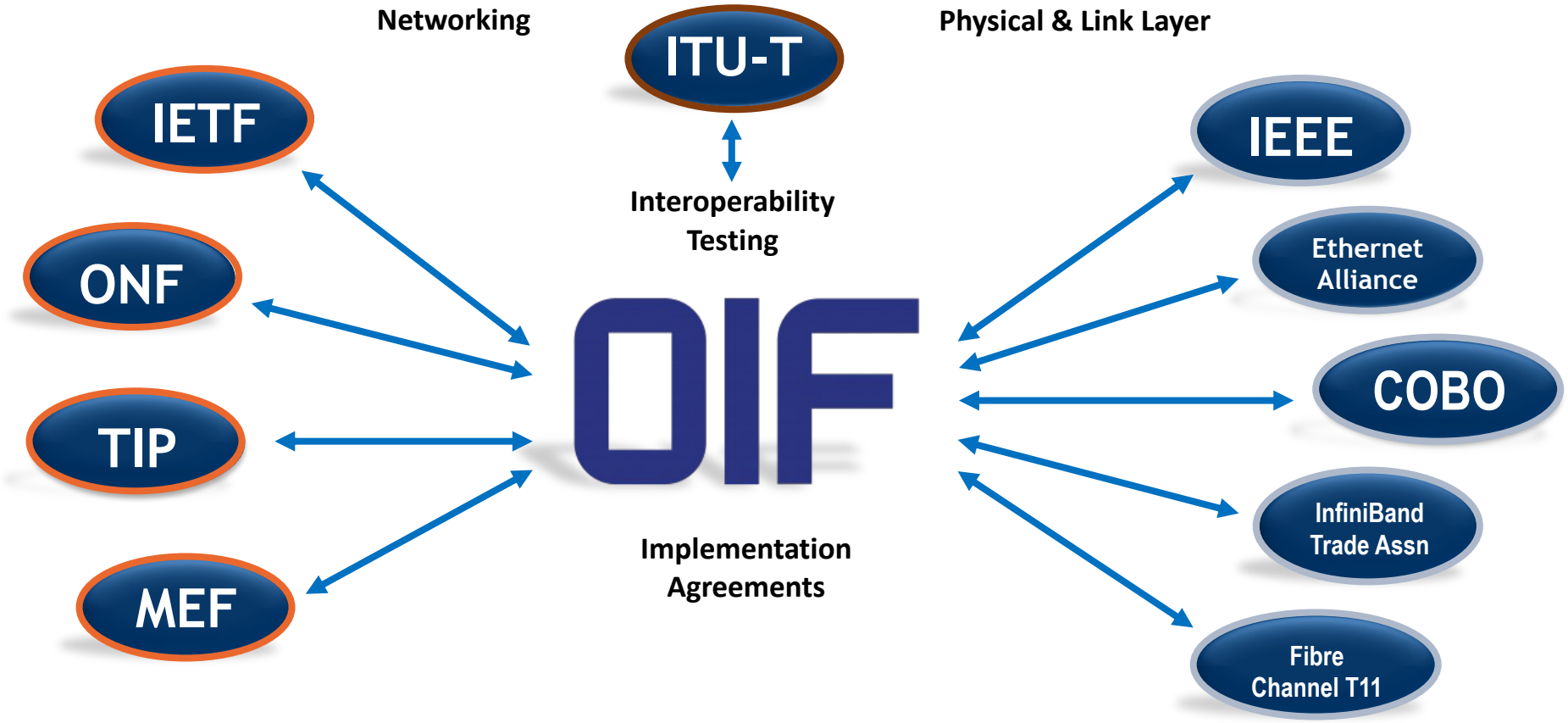
CEI
- High-Speed Building Blocks
- 224G, 112G, 56G, 28G

NETWORKING

Transport SDN APIs
- Automation
- Programmability
- Interoperability Testing

FOR MORE INFORMATION, VISIT WWW.OIFORUM.COM

Where OIF Fits



OIF is celebrating 25 years!

Come join us.

What is a Framework Document?

- A framework project has been a successful vehicle for the OIF.
- It enables the OIF membership to explore next generation industry needs and to forge an industry consensus, particularly with respect to interoperable solutions
  - Identify the various application needs (application spaces)
  - Identify points where interoperability is important
  - Identify what kinds of parameters should be interoperable
  - Identify additional projects which can nail down specifics for interoperability
- It results in a document (whitepaper) detailing how the OIF can address next generation industry needs through follow-on implementation agreements (IAs).

Note: OIF is contribution-driven by member companies.

Co-Packaging Framework Overview

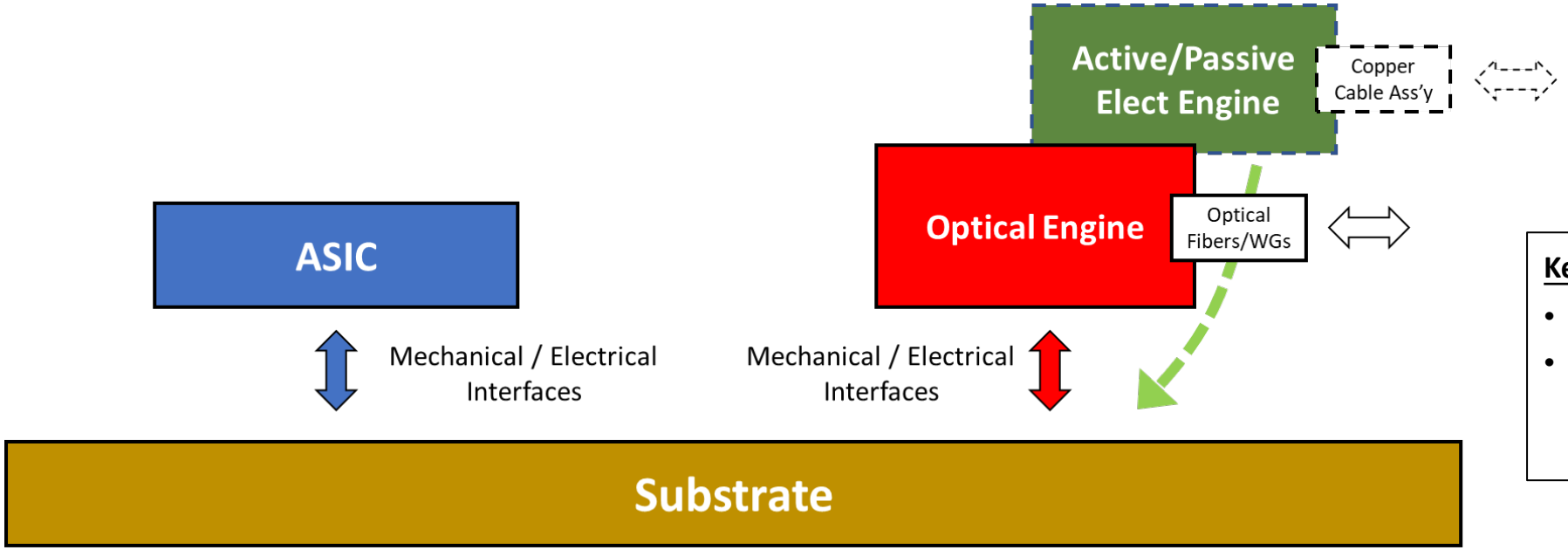
- Identified the key co-packaged applications and their requirements
- Identified and studied key issues associated with co-packaging
- Identified opportunities and developed industry consensus to pursue interoperability standards
- Documented the study in the Framework IA (a technical whitepaper)
- Launched follow-on standardization activities at the OIF
    - Descriptions of those activities to follow

This Framework Project:

- Enabled (and continues to enable) an industry conversation of co-packaging with ASICs
- Leveraged the industries' knowledge to appropriate interoperability solutions
- Helped the industry to achieve consensus (in certain areas)

Scope of the Co-Packaging Framework Project?

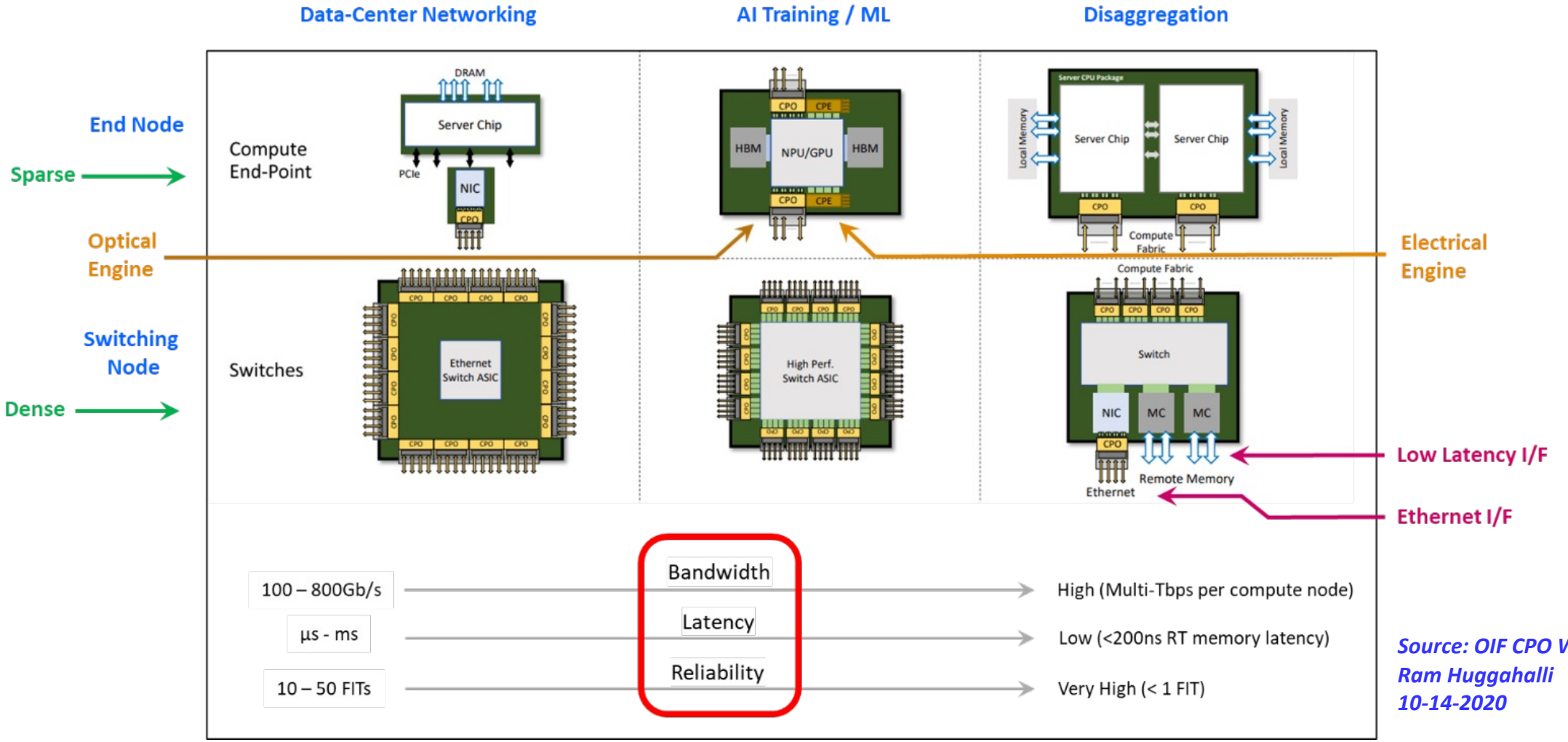
- **Applications:** System applications benefiting from co-packaging.
- **Interfaces:** optical and electrical interfaces, footprint and pin-out, power, signaling, safety, thermal interfaces, MIS, etc., as well as internally facing electrical and corresponding mechanical interfaces.



Key advantages:

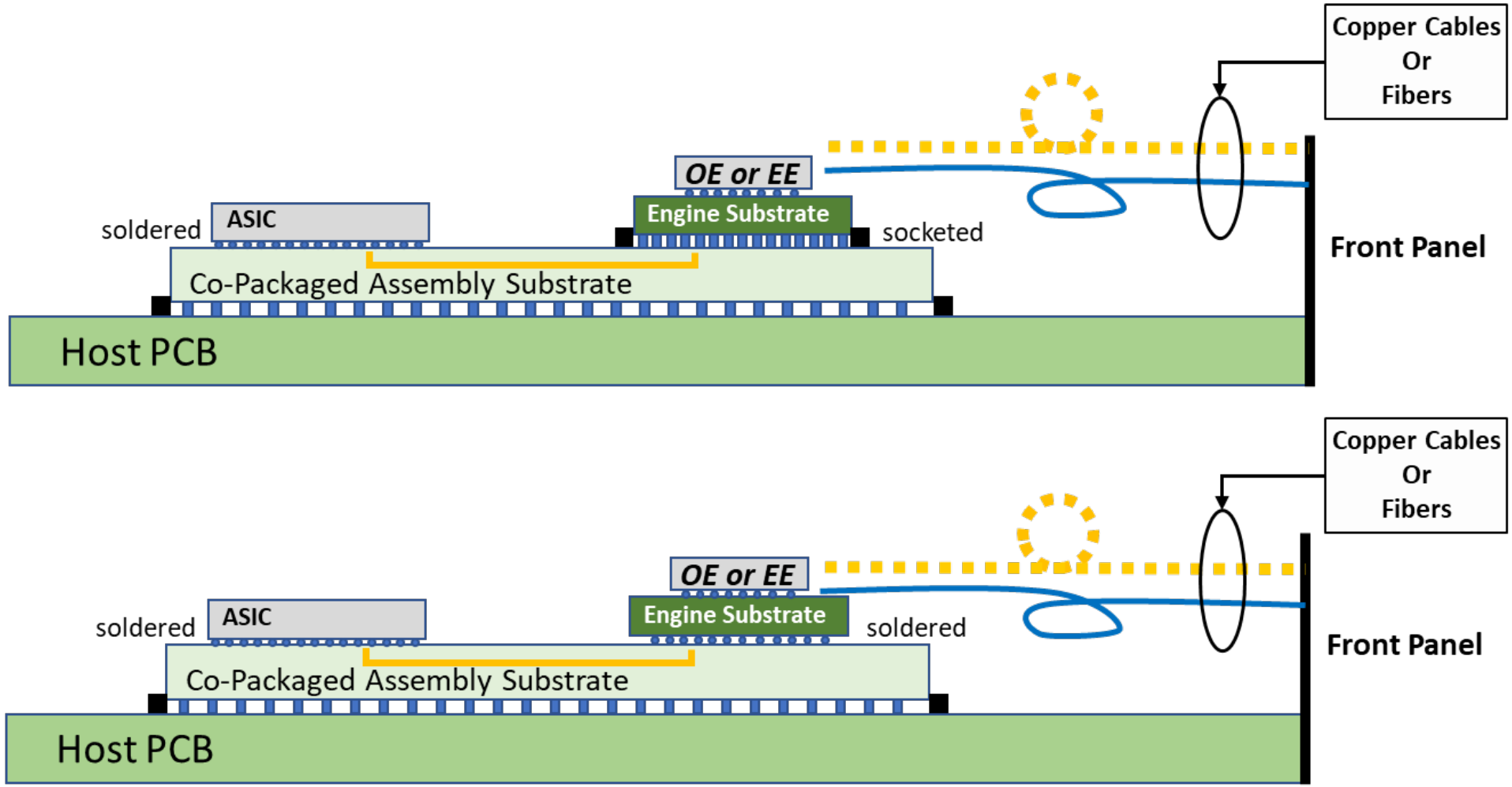
- Higher interconnect bandwidth density
- Lower overall system power consumption due to close proximity of engines to host ASIC

Co-packaging Applications

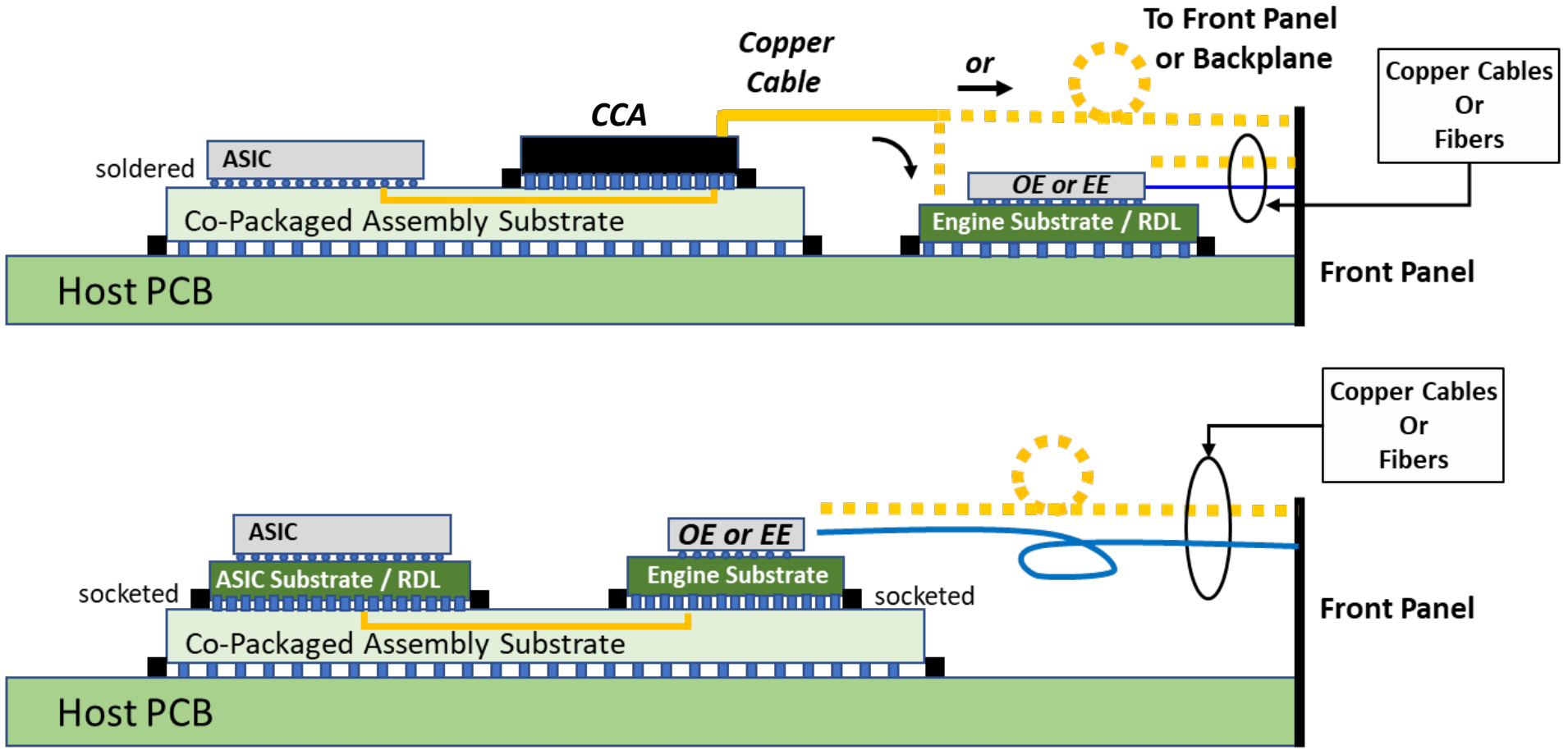


Source: OIF CPO Webinar, Ram Huggahalli 10-14-2020

Use-Cases (1)


Copper Cables
Or
Fibers
OE or EE
Engine Substrate
soldered
ASIC
socketed
Front Panel
Co-Packaged Assembly Substrate
Host PCB
Copper Cables
Or
Fibers
OE or EE
Engine Substrate
soldered
ASIC
soldered
Front Panel
Co-Packaged Assembly Substrate
Host PCB

Use-Cases (2)


To Front Panel
or Backplane
Copper
Cable
or
CCA
Copper Cables
Or
Fibers
soldered
ASIC
OE or EE
Co-Packaged Assembly Substrate
Engine Substrate / RDL
Host PCB
Front Panel
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Or
Fibers
ASIC
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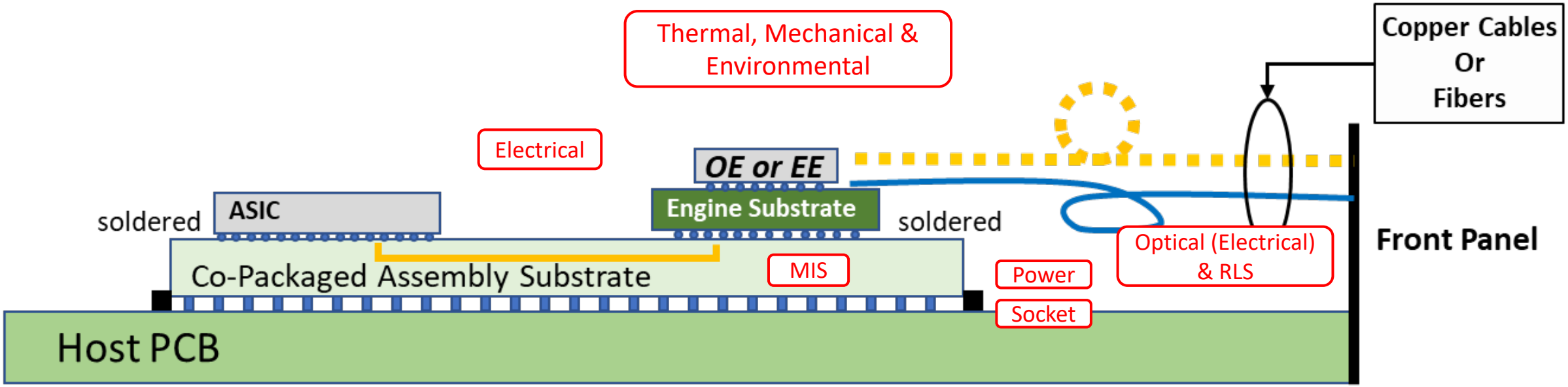
socketed
ASIC Substrate / RDL
Engine Substrate
socketed
Co-Packaged Assembly Substrate
Host PCB
Front Panel

Potential Interfaces for Study and Interoperability *(red)*



Application Example

- **Switch Generation:** 51.2Tb/s or higher
- **Lane Speed:** 106 Gb/s
- **Interface Architecture:** XSR (or XSR+) based AUI, 400G-FR4 PMD
- **Motivation:** System power reduction, ecosystem & operational readiness

Reliability and Repairability

Summary

- The OIF Co-Packaging Framework document was published 1Q22:

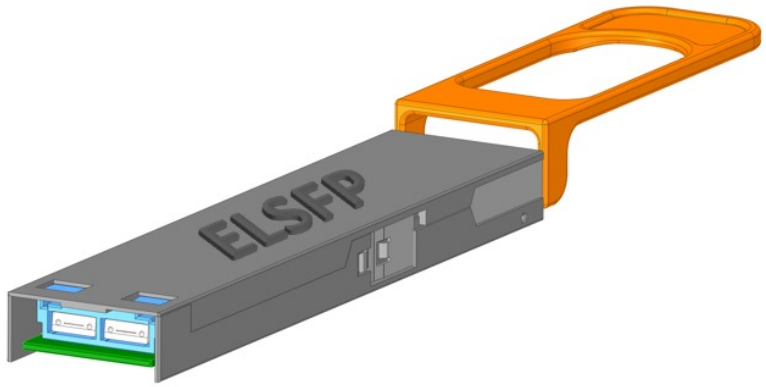
  https://www.oiforum.com/wp-content/uploads/OIF-Co-Packaging-FD-01.0.pdf

- This study resulted in other OIF projects, e.g. External Laser Source, Co-Packaged Optical Transceiver and XSR+ electrical interface (connecting host ASIC to engine (or transceiver module)

- Framework Document “Maintenance Cycle” in-progress
  - Updates to document to reflect recent developments (thinking)
  - Typos, clarifications

External Laser Source Implementation Agreement Project

External Laser Small Form-factor Pluggable (ELSFP)



Laser challenges in a CPO :

- Require lower temp than Si and SiPho
- Reliability (Temp, Current, Facet power)
- May require complex package (i.e. TEC)
- Not commoditized/Custom/Expensive

Features provided by pluggables:

- Located in the coolest part of the system
- Field Replaceable
- Large physical volume for diverse packaging options
- Standardized by the ELSFP IA in the OIF/Multi-Source

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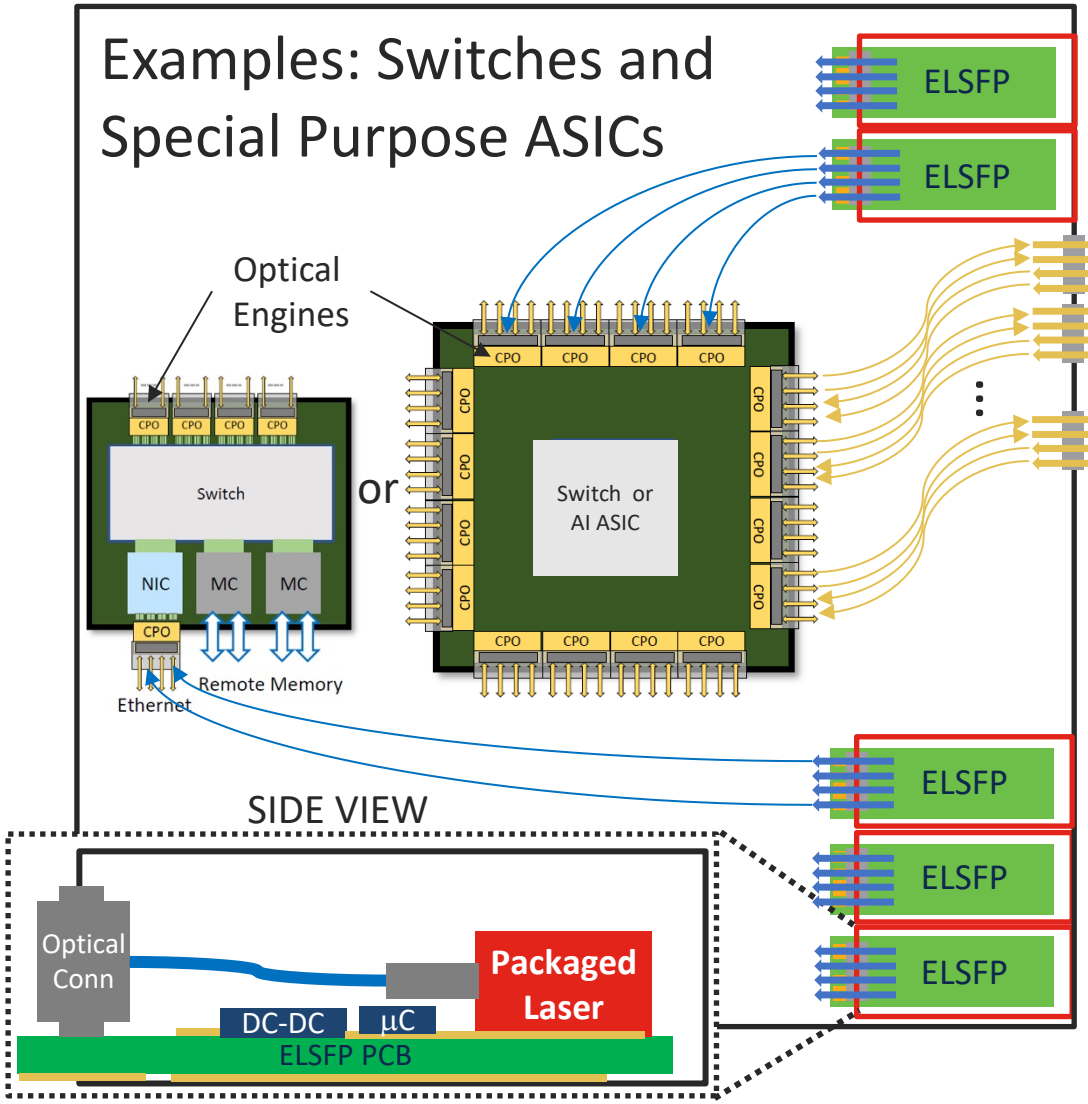

- ELSFPs provide CW laser power for optical engines (OEs).
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- CPO systems will likely need multiple (i.e. 4, 8, or 16) ELSFPs (*Compared to 32 or 64 Pluggable Transceivers*)
- The light from a given ELSFP can feed more than a single OE.
- A pluggable form factor helps to ensure total system reliability and a "hot swap" replacement if a single laser or ELSFP module fails.
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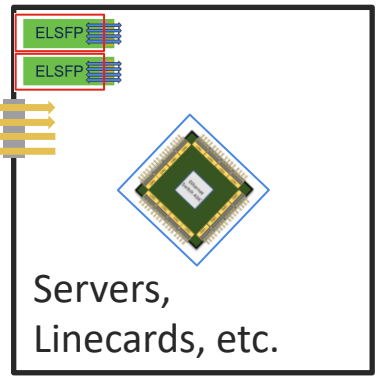


Initial Technical Concept

Faceplate Density

- Width similar to OSFP (16 modules across a standard faceplate)
- Blind mate pluggable
- Optimize system faceplate for MAX airflow to cool the CPO chip complex

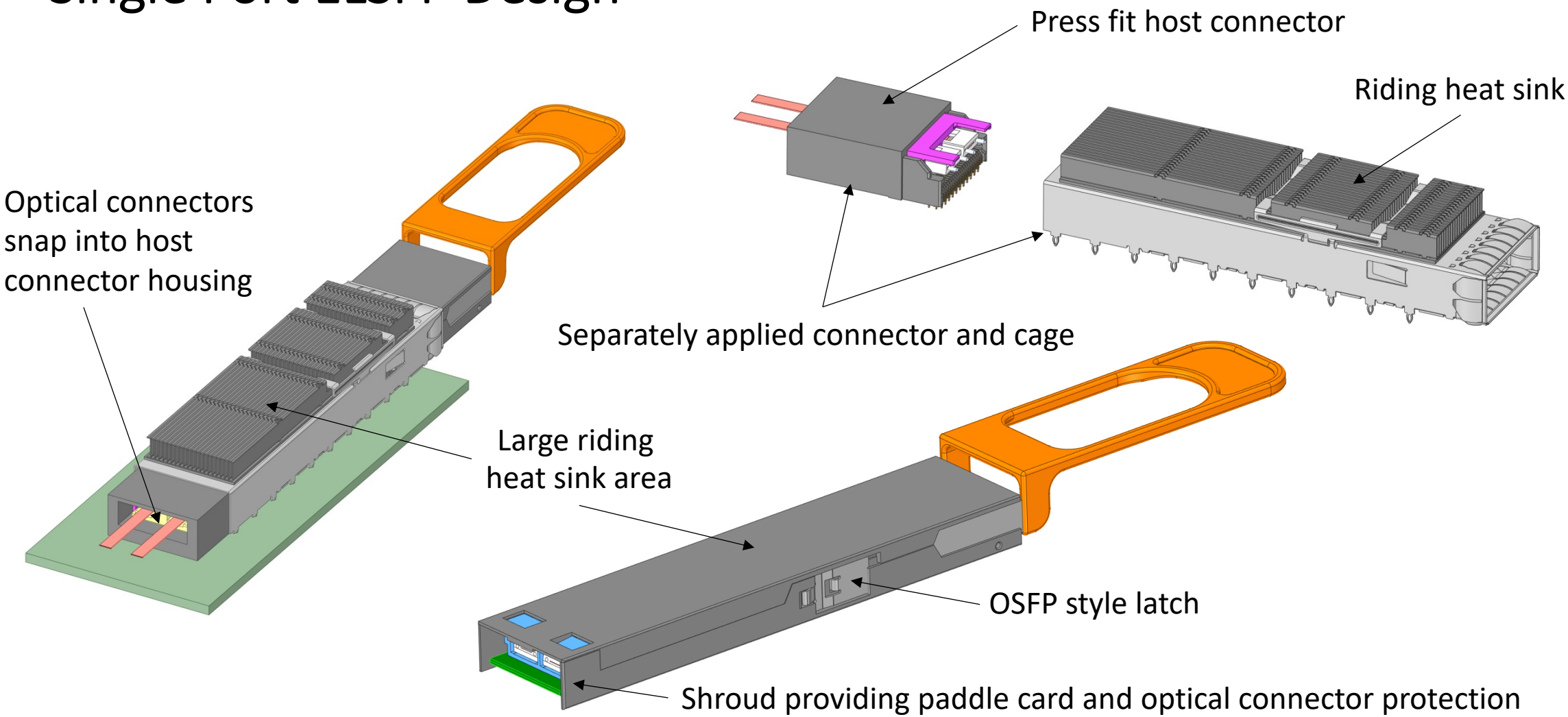
Commonality

- Industry standard 3.3V Supply
- CMIS (Common Management Interface Specification)
- Share form-factor among applications

Scaling

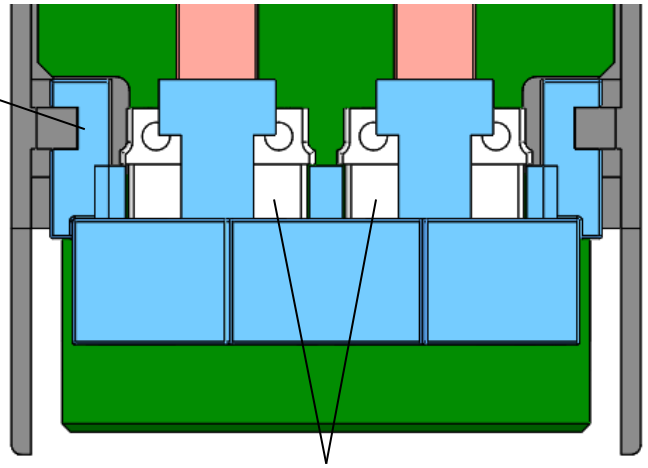
- Optical Power Classes
- Thermal Power Classes
- Belly-to-belly configurations
- Riding heat sink for system flexibility
- 1 or 2 “MT like” ferrules for future proofing
  - Support for 8 PM fibers per MT
  - Support for multiple OE modules

Single Port ELSFP Design



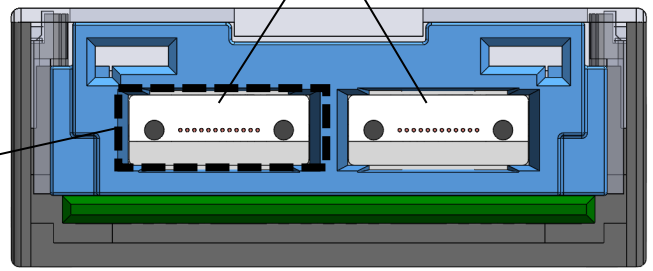
Module-Side Optical Connector

Connector-to-Module Attachment (Optional)

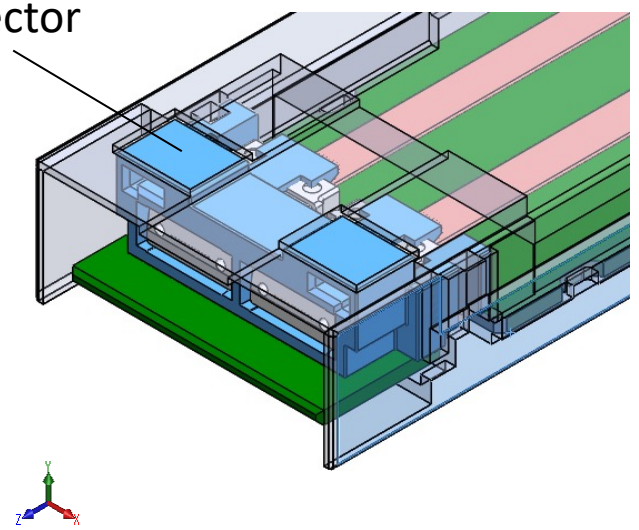


1 or 2 MT-like Ferrules

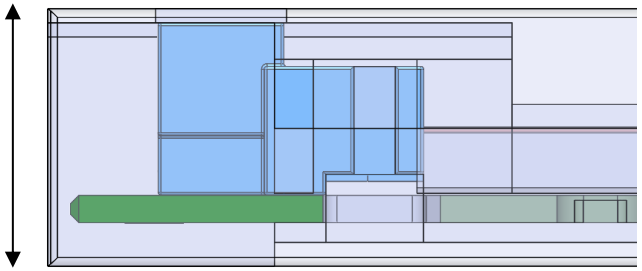
Optional 2nd MT-like Ferrule



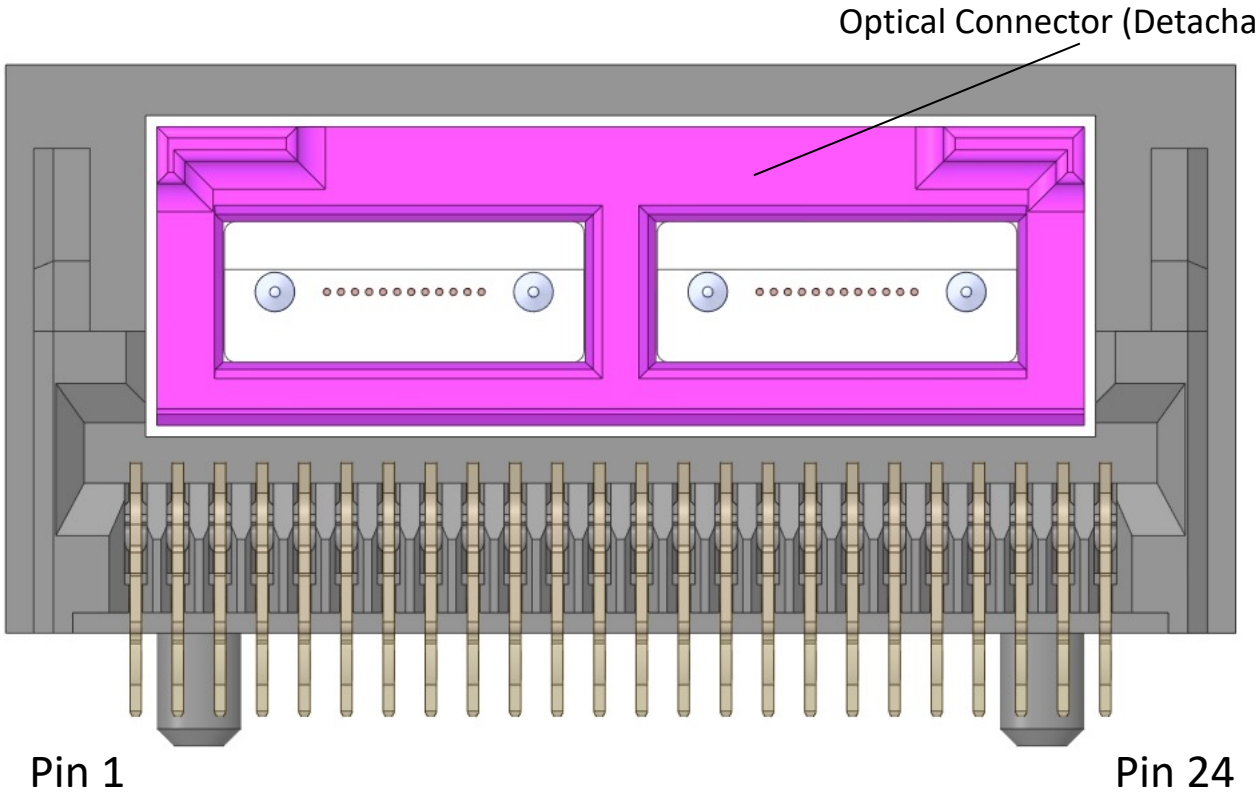
Robust anchoring for optical connector



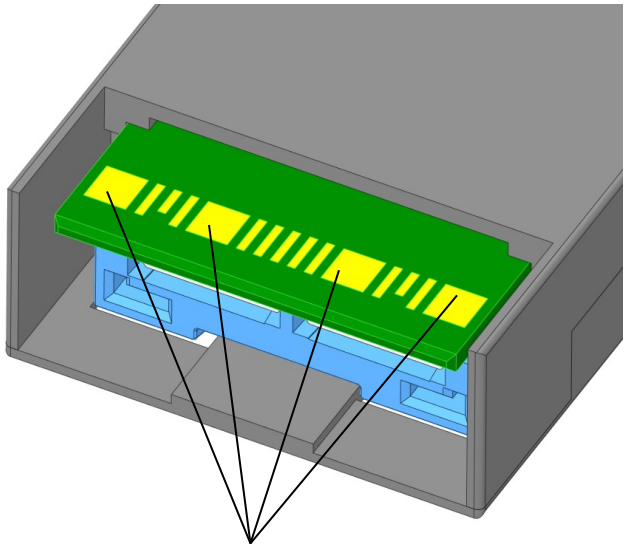
Low profile for maximum system airflow



Host-side Electro-Optical Connector



Module Bottom side Electrical Contacts



Sufficient power and ground to support **30W**

Additional pins for control/management, laser safety (i.e. presence pin), and spares for future proofing
Optical connector sub-assembly (pink) is separable from the board mounted electrical connector sub assembly

ELSFP Longevity *(future-proofing)*

- Switch bandwidth doubles every 2 years.
- Laser output power requirements are expected to increase ~1.5-2dB every switch generation.
- Typical laser die and packaging development and qualification cycle exceeds 2 years.
- ELSFP module temperature increases proportionally with the total laser power in order to reduce system fan power consumption which scales cubically.
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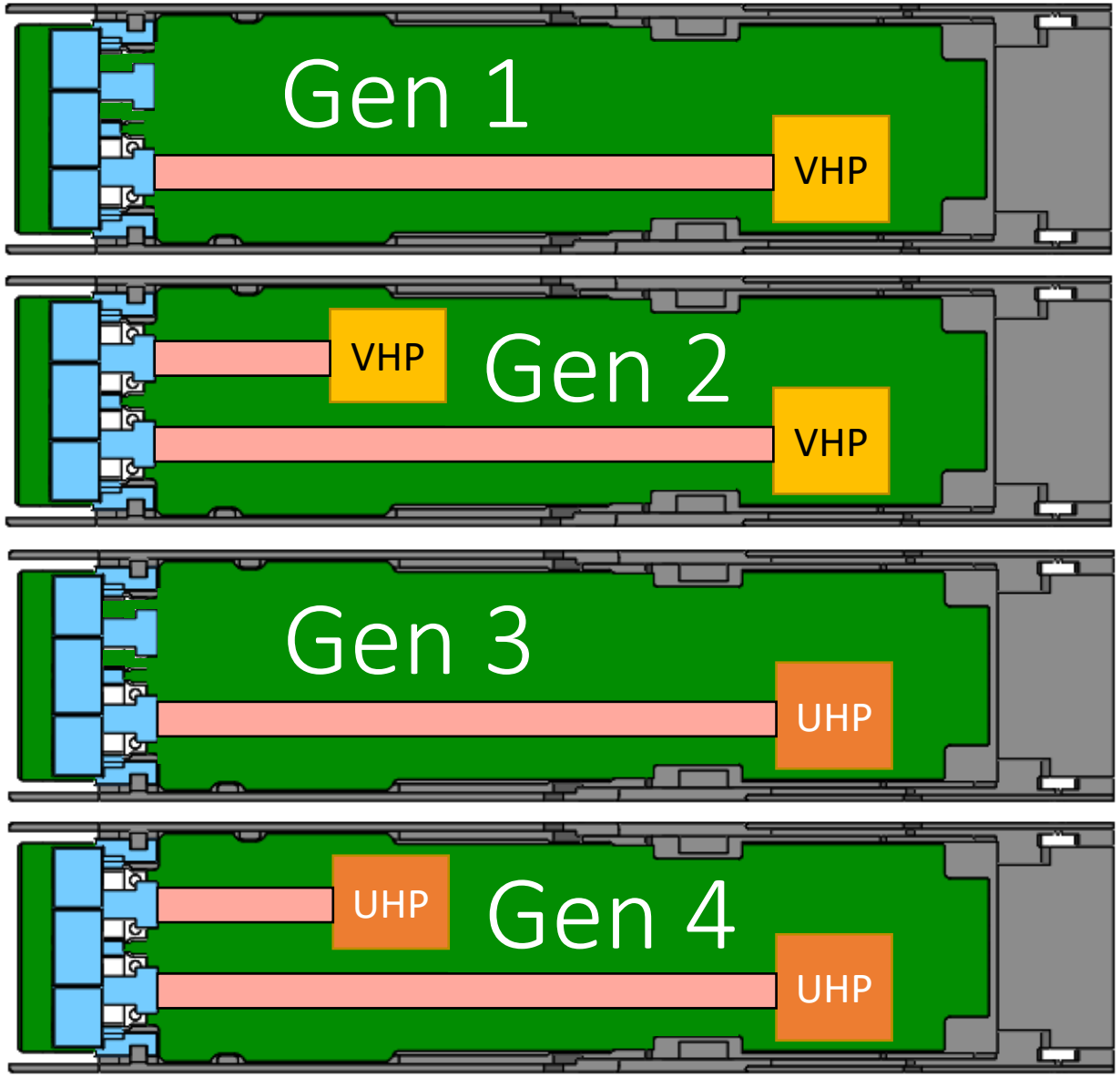
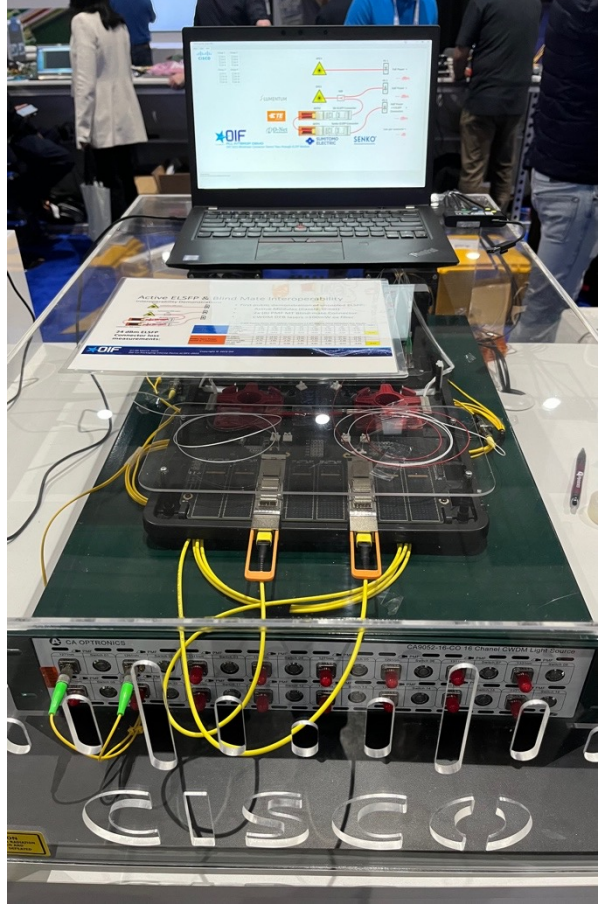
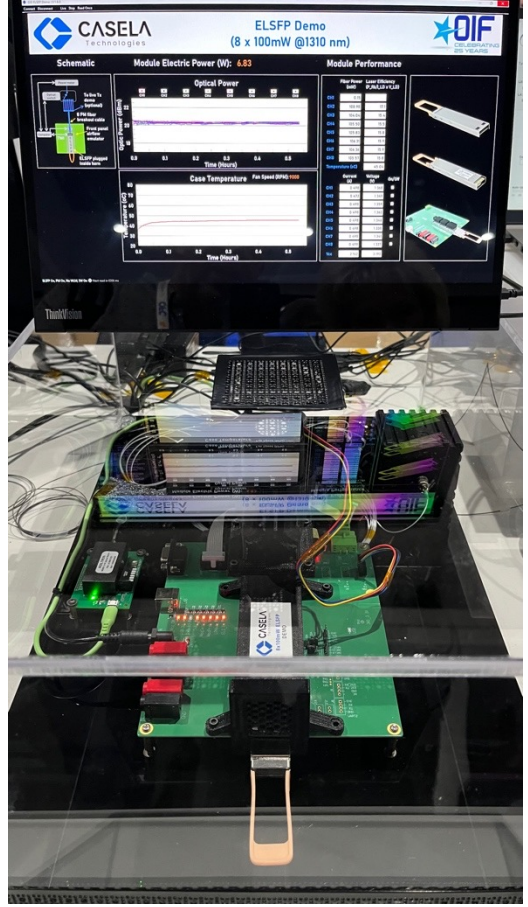




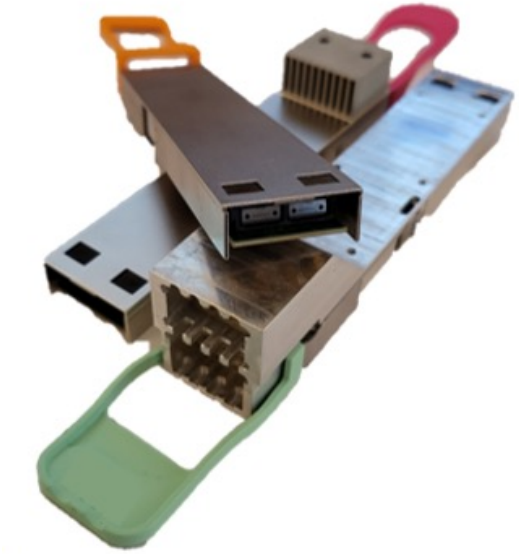


OFC 2023 Live Demos: 1310nm ELSFPs, each with 8 lasers, >100mW/fiber at 55C case, 6-7W. Blind-mate optical connector loss demonstration. ELSFP=> Powering live optical engine link.

The ELSFP is a fundamental building block that will enable the industry to transition to CPO. By specifying this in the OIF we include nearly all market participants in this form-factor definition promoting a robust multi-vendor eco-system.

Thank-you

ELSFP



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External Laser Source Implementation Agreement

K.P. Jackson

March 09, 2023

Sumitomo Electric

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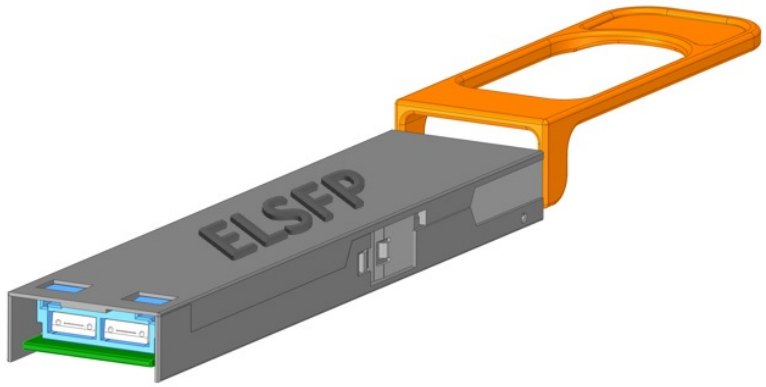

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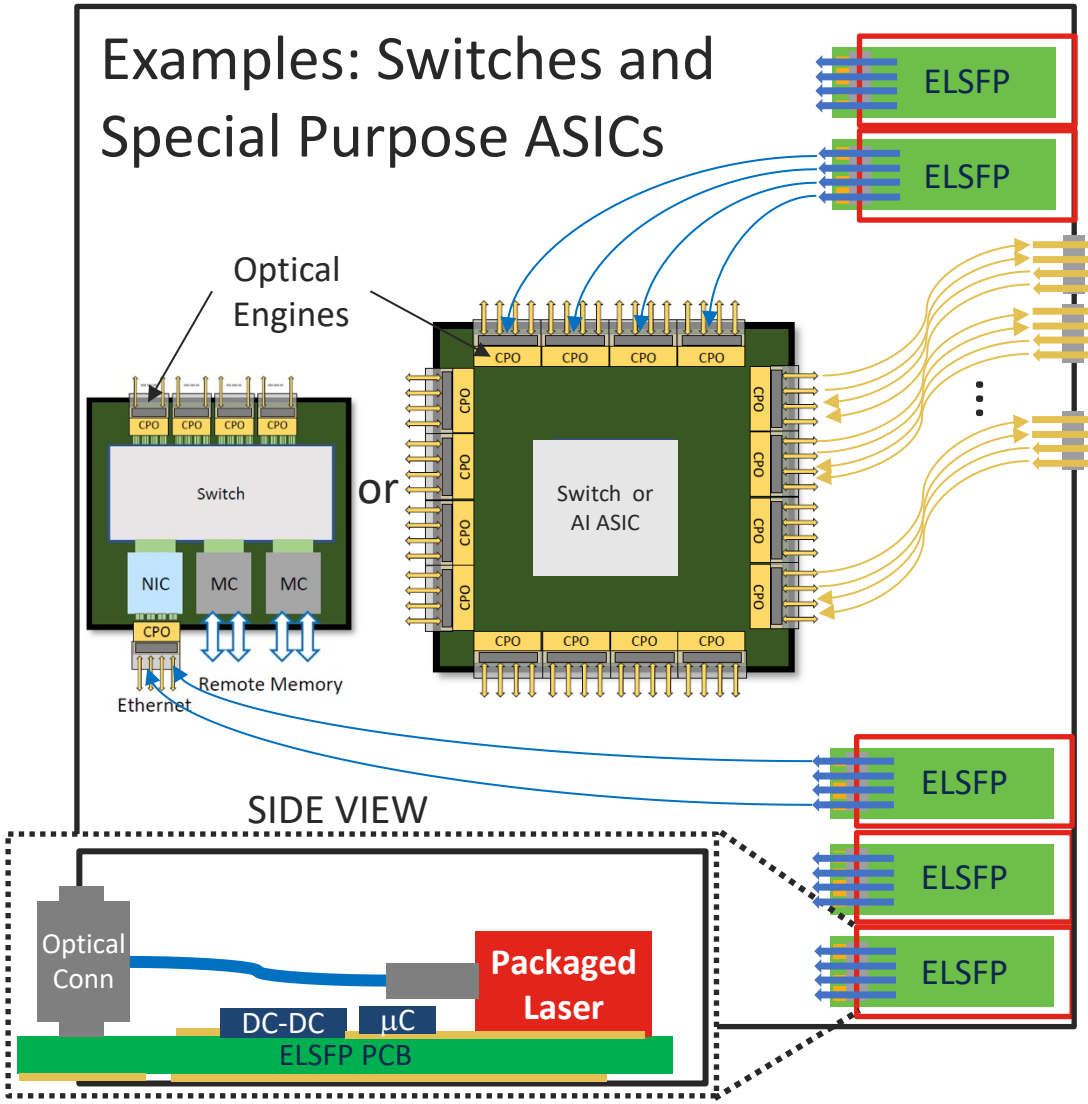

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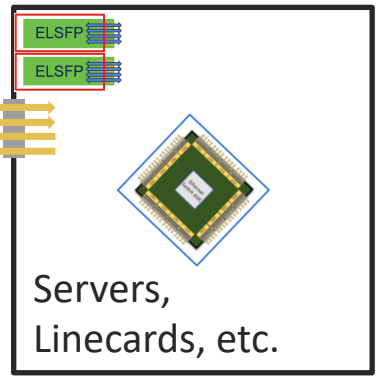

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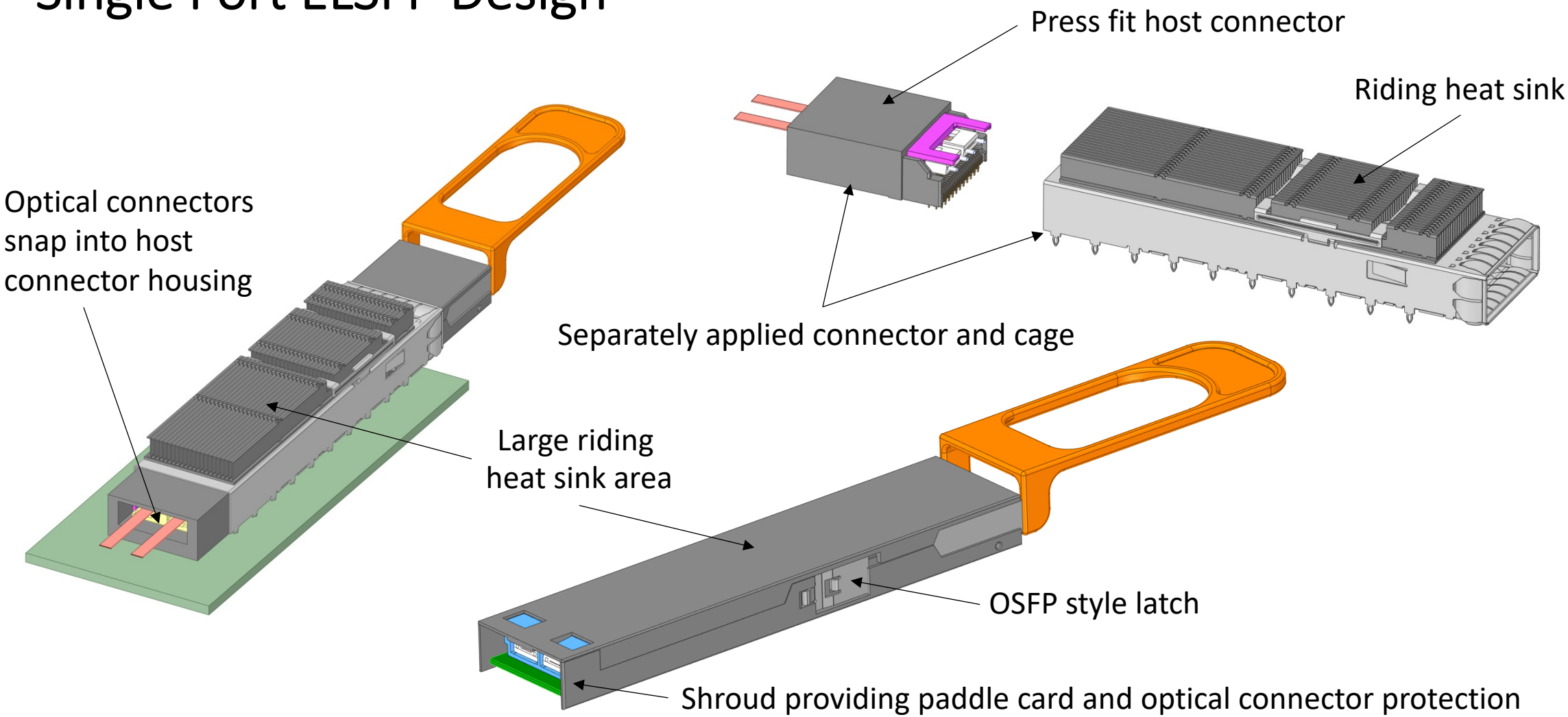

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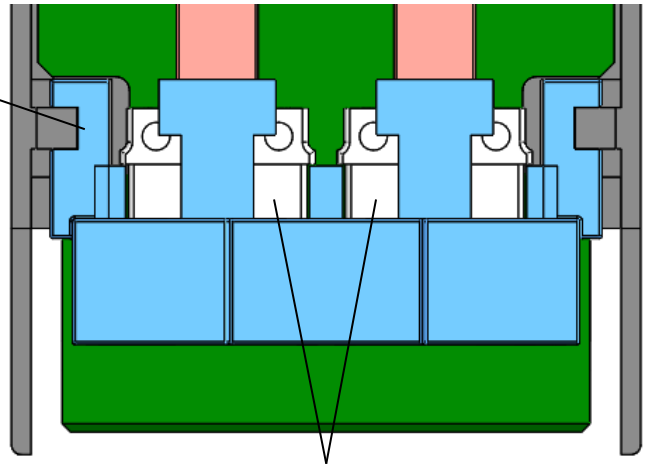

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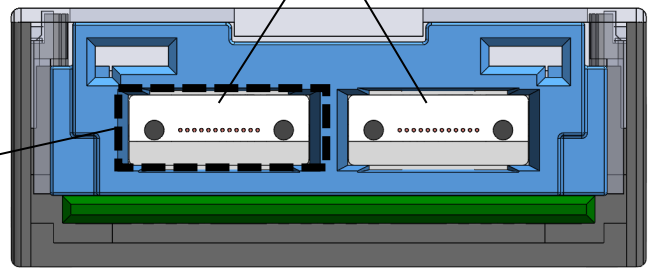

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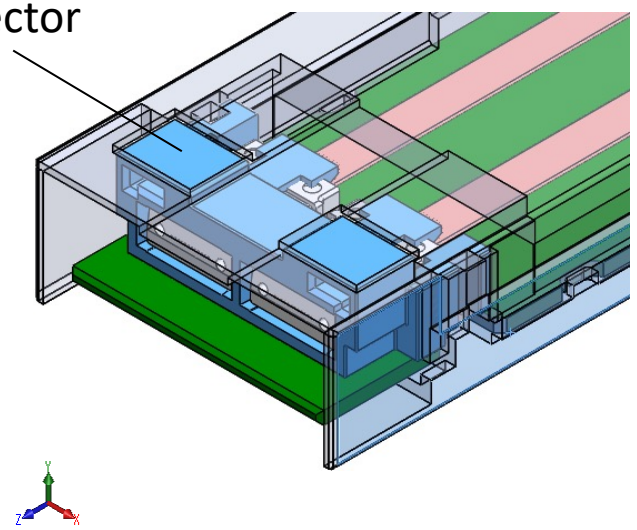

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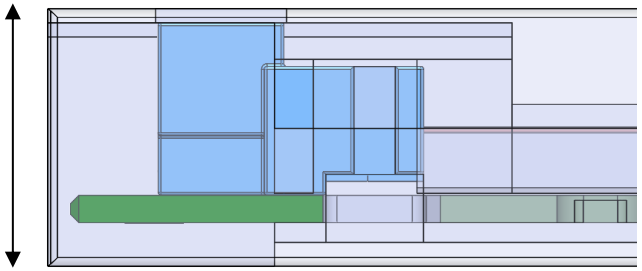
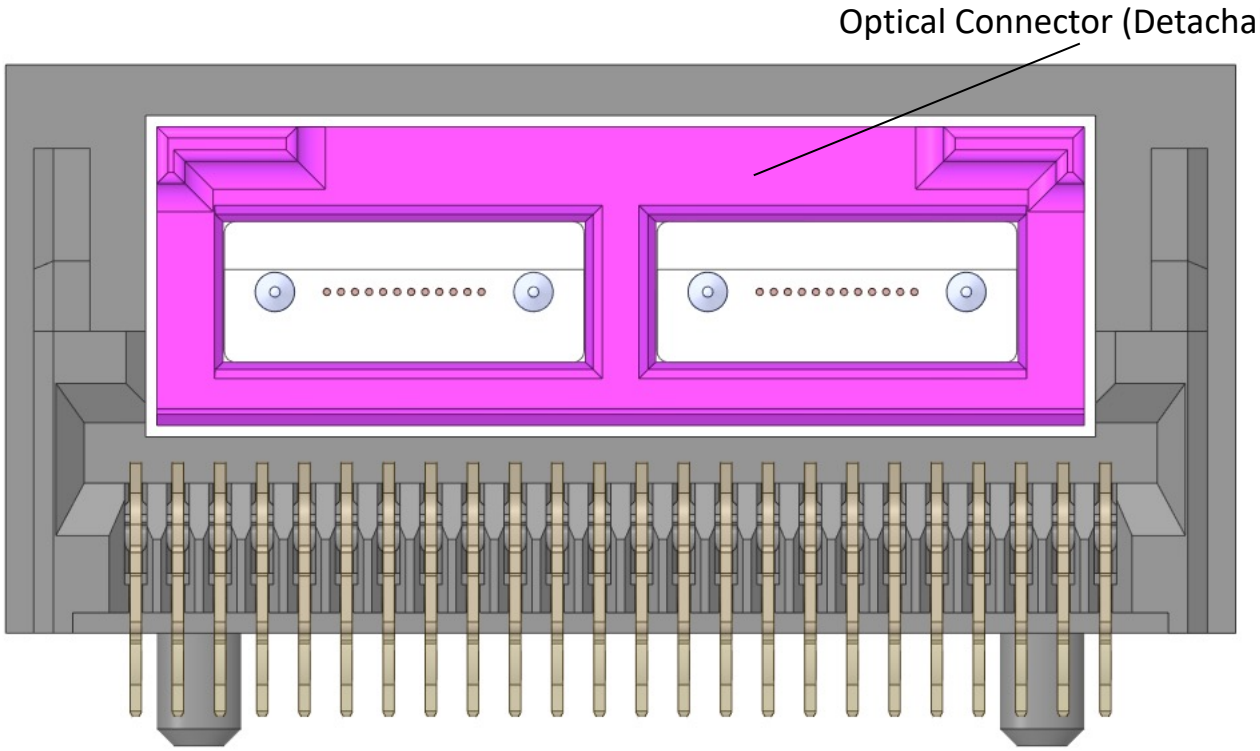


Electro-Optical Connector



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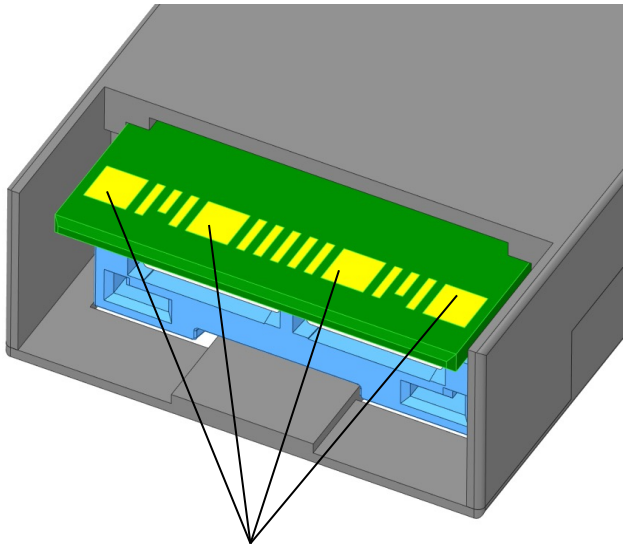

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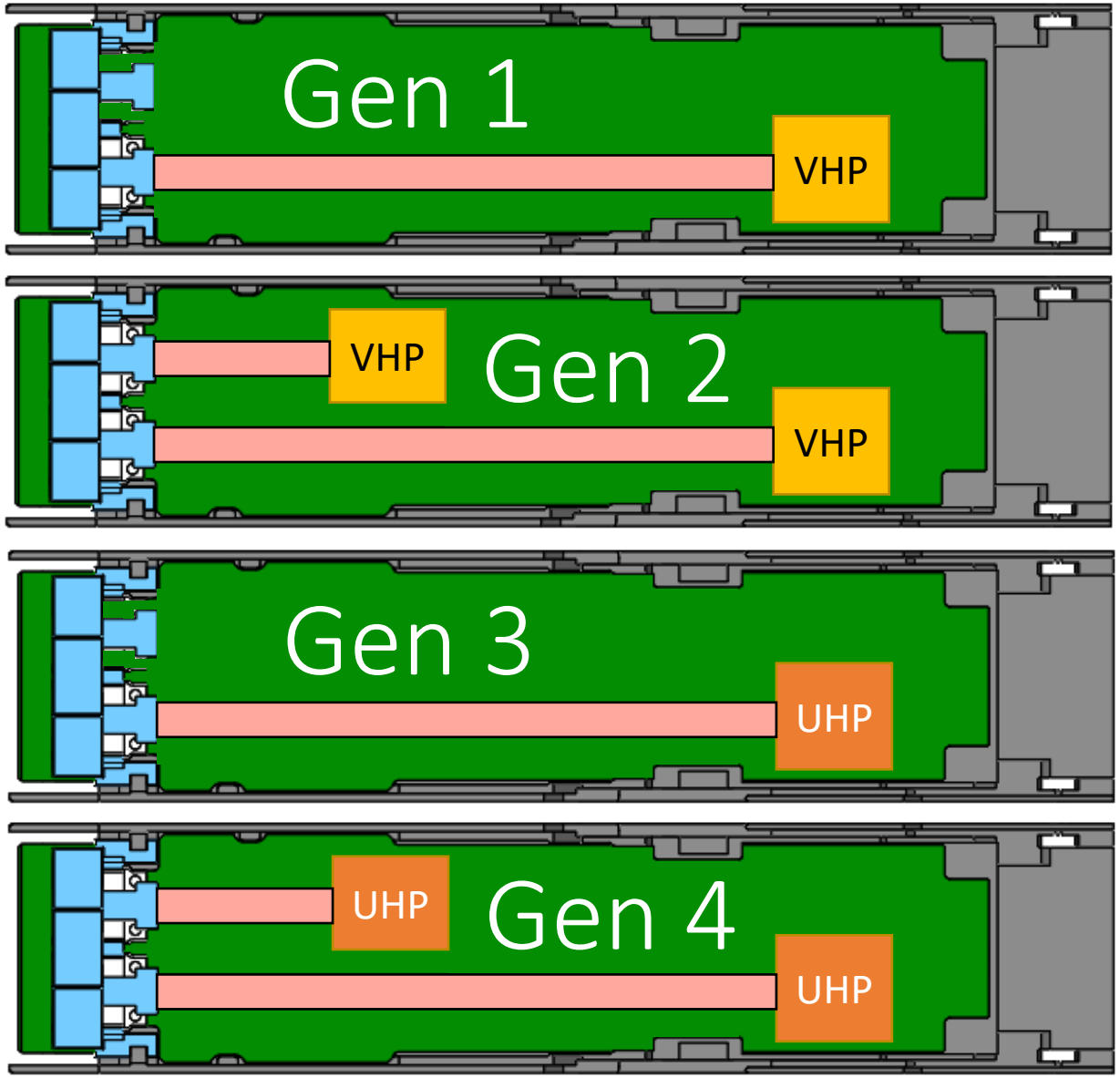

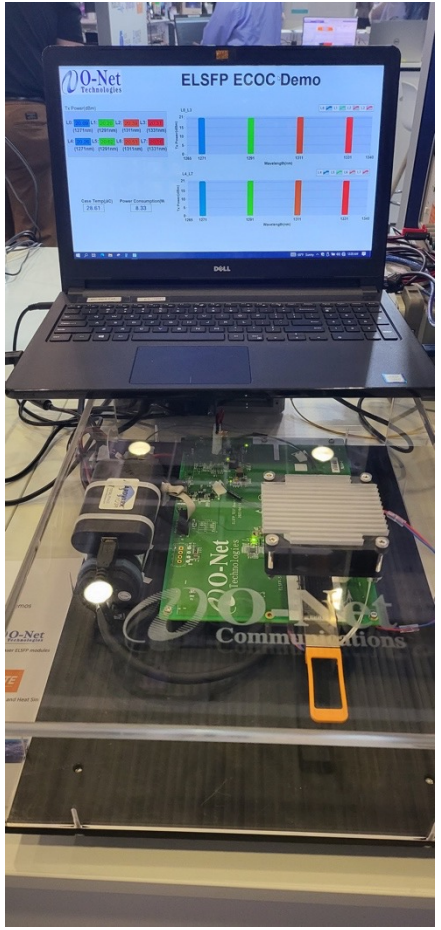

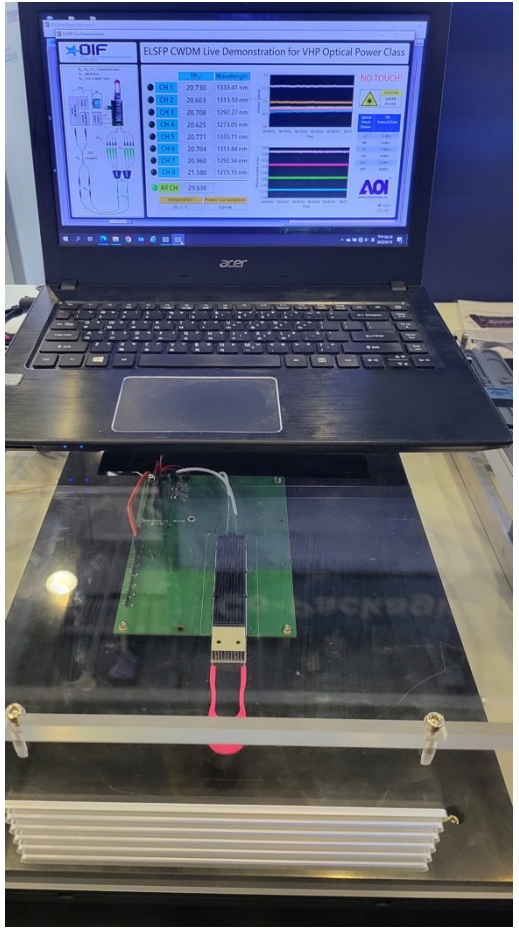

Live 1311nm and CWDM ELSFPs, demos at OFC'22 and ECOC'22 with each with 8 lasers, >100mW/fiber at 55C case, 8-9W. CWDM DFB lasers up to 500mW/fiber cooled to 50C and 100mW/fiber at 95C

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CPO 3.2T Module Update

Richard J R B Ward
OIF 3.2T Module Editor
Chief Technologist Data Connectivity, Astera Labs

Overview

- The OIF started the 3.2T Module Project Feb 2021
  - Project proposed by Facebook/Meta, Microsoft, Ranovus, Intel, with a large industry supporter backing

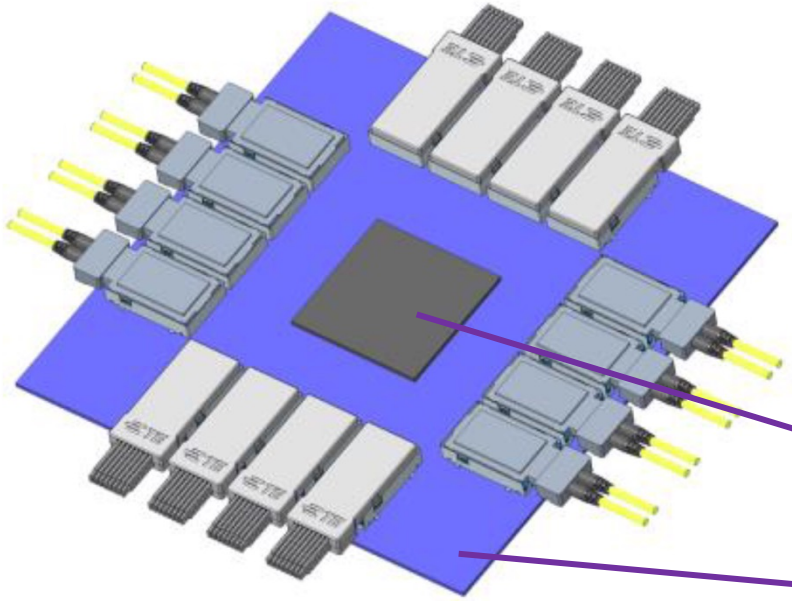
- The goal was to create an Implementation Agreement (IA) for:
  - A 3.2T Optical Co-Packaged Module for 51T data-center switch applications

Overview of the 3.2T IA Scope

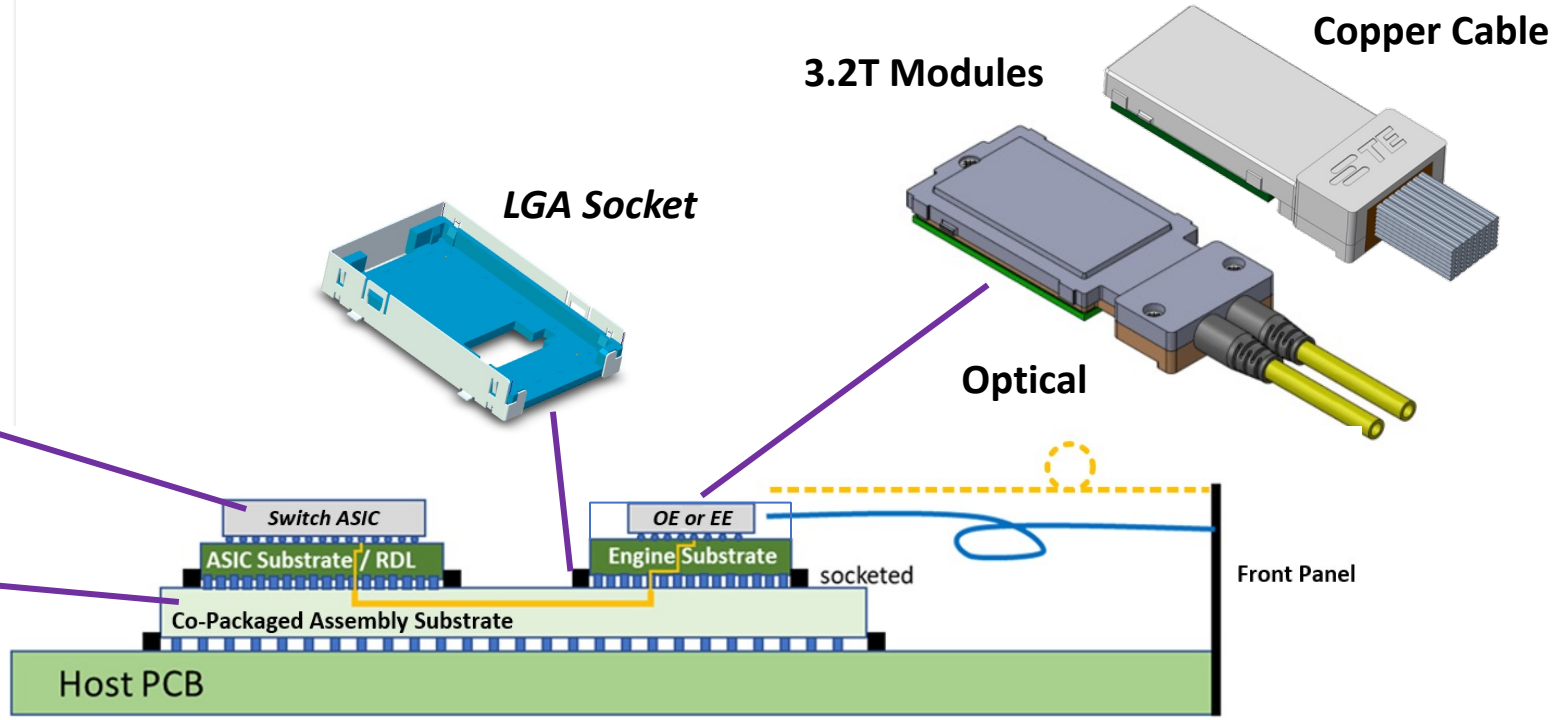
- Define Electrical (RF, DC, low-speed), Optical, Mechanical, and Control
- As a “replacement” component in the data center
- 8 x 400Gb/s channels implemented as
  - 32 x CEI-112G-XSR electrical host-side channels (retimed)
  - 8 x 400GBASE-FR4 optics, or
  - 8 x 400GBASE-DR4 optics
- Internal and External Laser options

Example System Attachment

- 16 x 3.2T Modules for 51.2T Switch Capacity



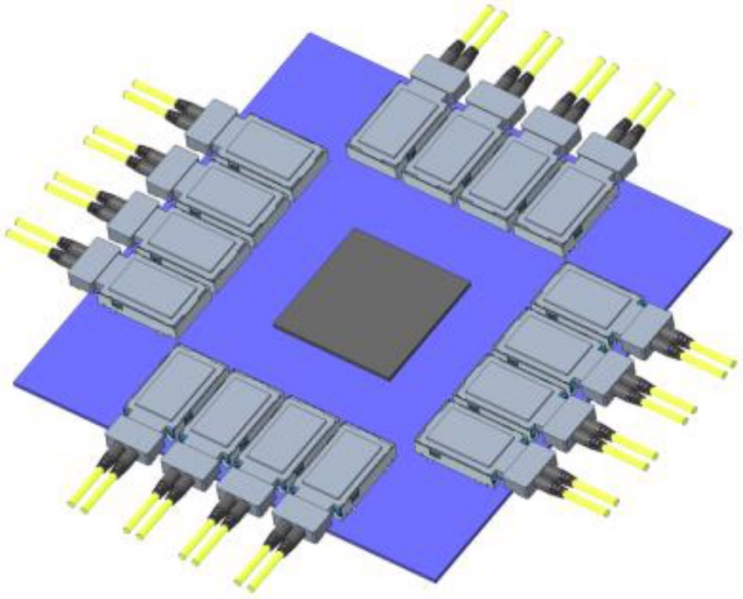
Co-Packaged Assembly Substrate (Interposer)



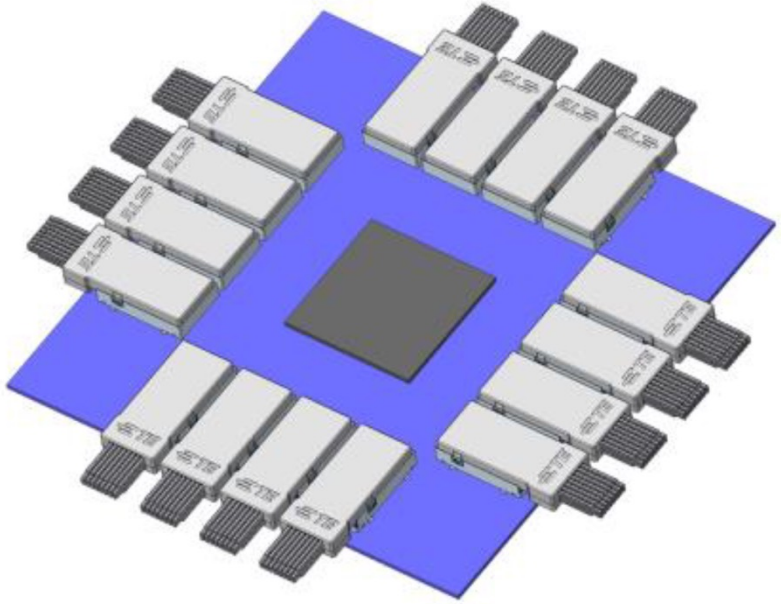
Channel components cross-section

Flexibility at Build Time

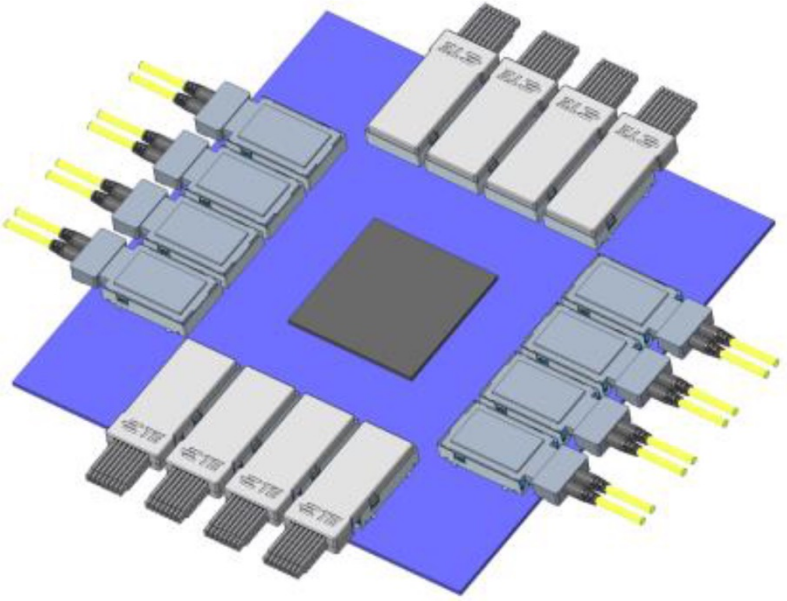
- Mix and match of Optical and Copper Attach Modules



100% Optics



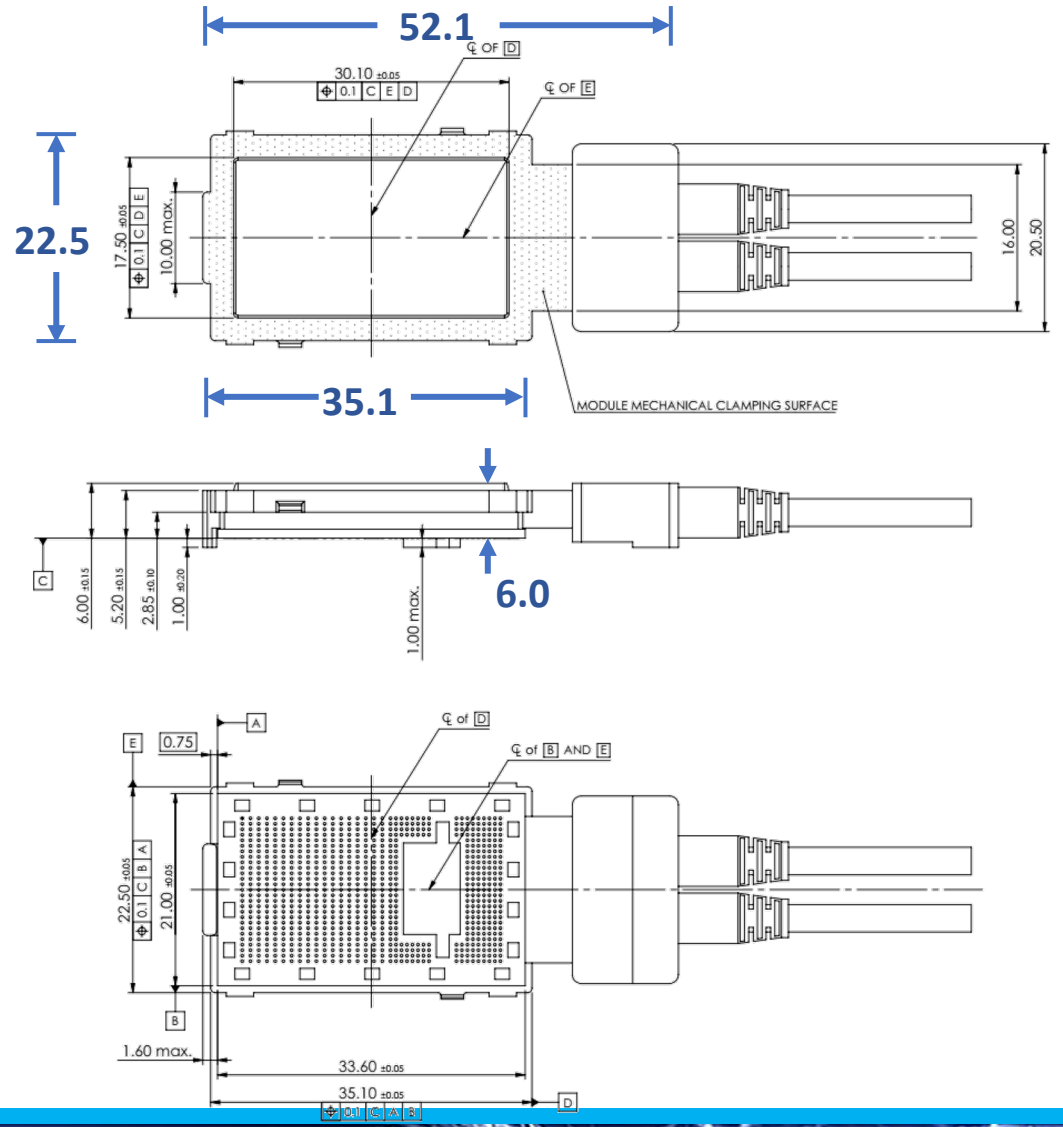
100% Copper



50% Optics / 50% Copper

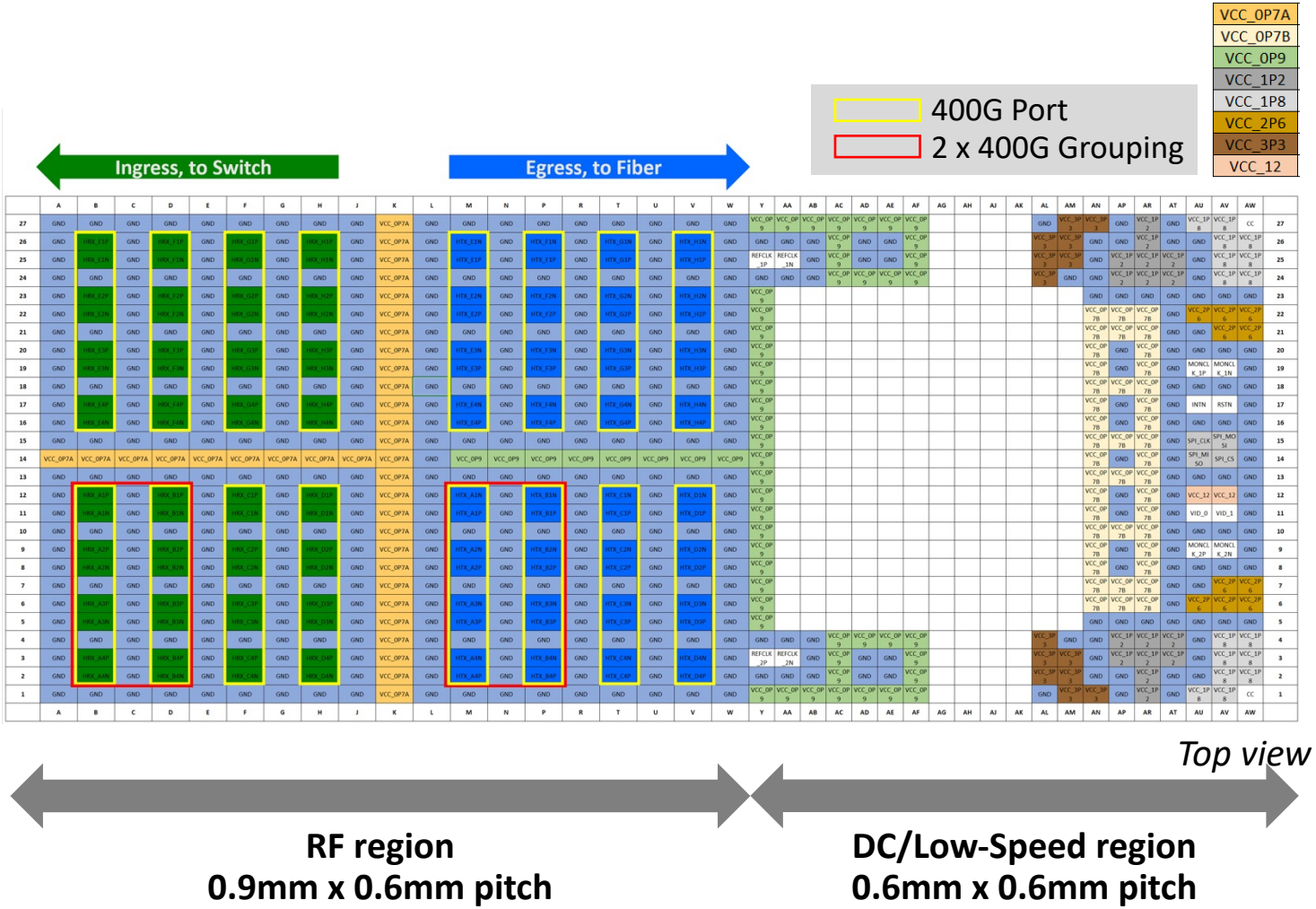
3.2T Module Dimensions

- Highly integrated EO Solution
- The 3.2T Optical module is 1/5th the volume of the OSFP (Type 3)
- Power capability:
  - 56W (Internal Laser option)
  - 48W (External Laser option)



LGA Pin Map

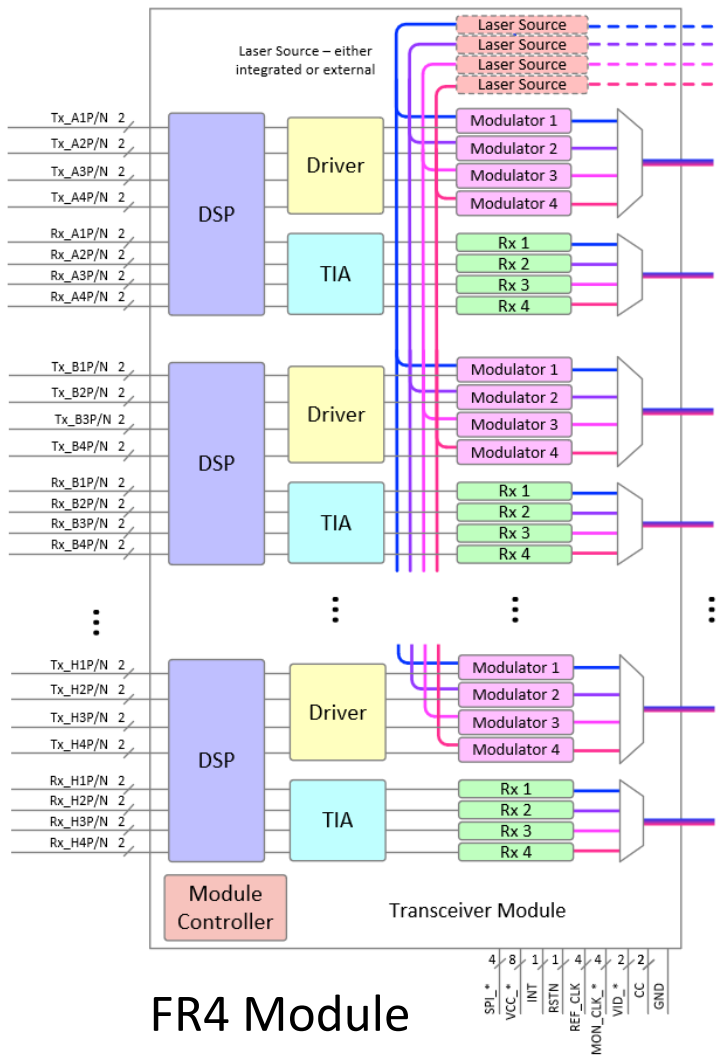
- Split pin-field pitches
- Defined supply rails:
  12V, 3.3V, 2.6V, 1.8V, 0.9V,
  0.7V (adjustable);
  1.2V (fixed)
- Comms Electrical: 1.2V SPI
- Comms protocol: CMIS 5.3
- 400G and 800G (2x400G) port grouping defined



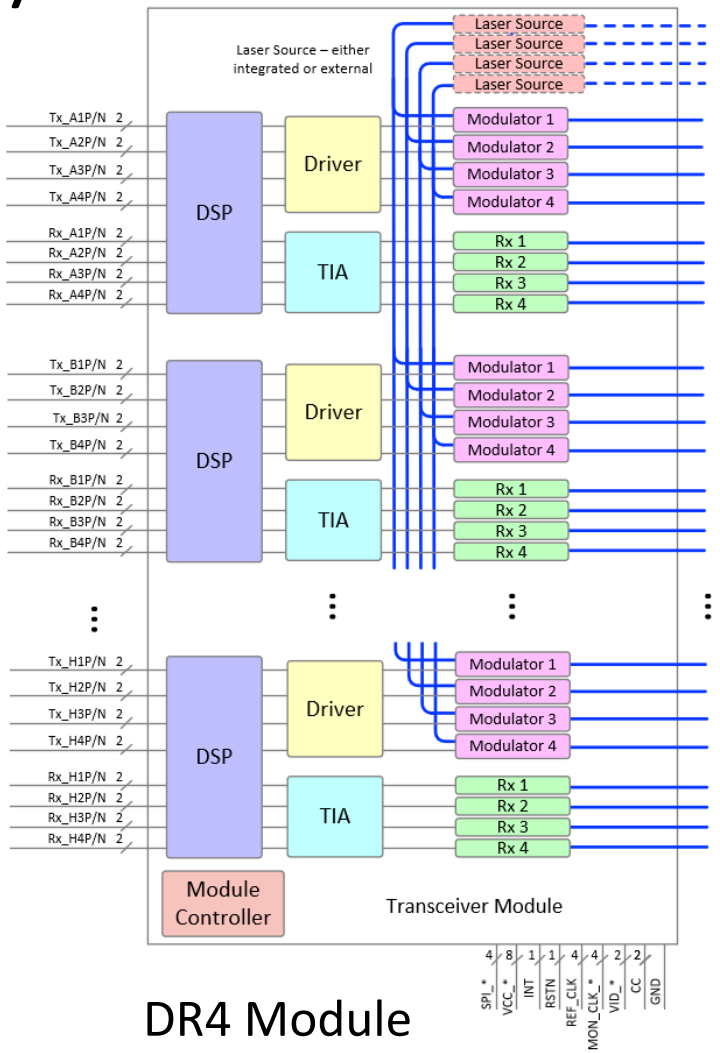
3.2T Optical Module Functionality

To fit the functionality, requires a*dvanced 3D integration of:*

- *Optics (Laser + Modulator + PD)*
- *Electronics (Driver + TIA + Control)*



FR4 Module

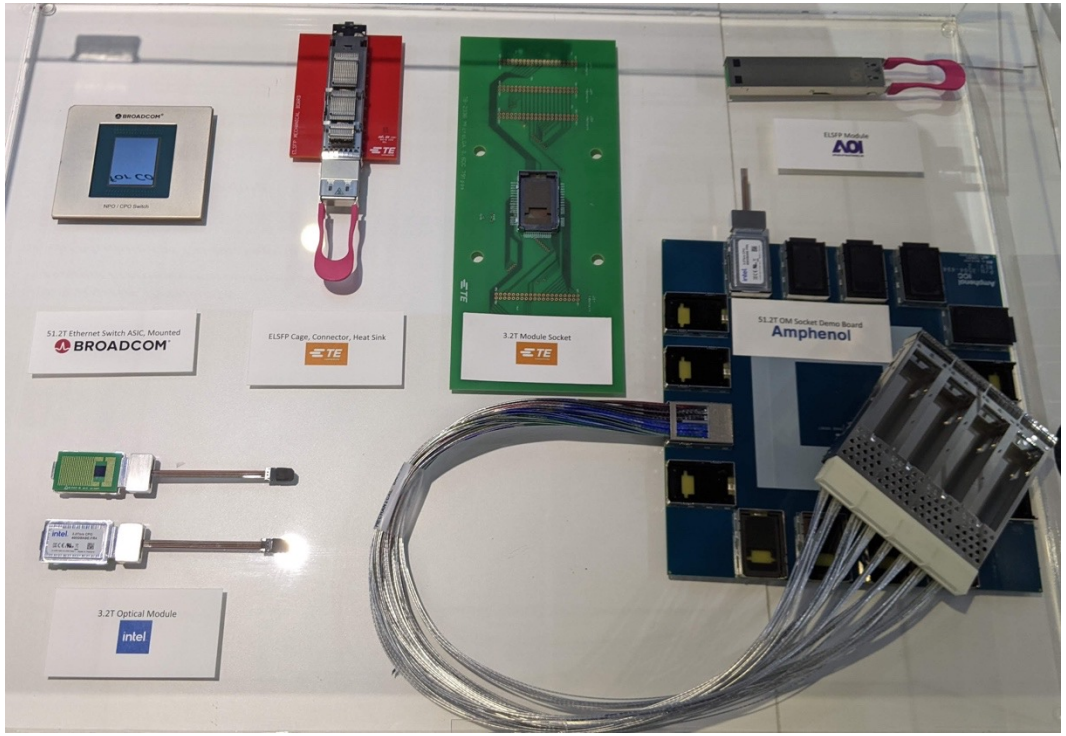


DR4 Module

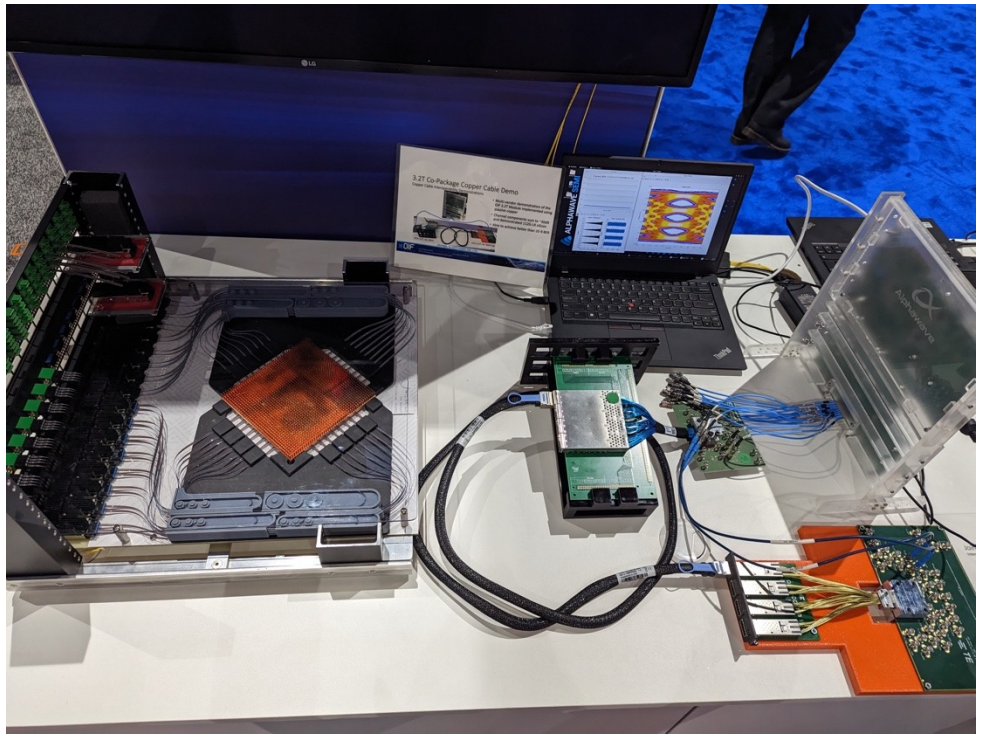
Ecosystem hardware coming together

From the OIF Interop Demonstrations and Showcases

OFC 2022



OFC 2023



Summary

- The OIF Co-Packaging Workgroup membership has defined a highly integrated Electro-Optical solution for Ethernet Applications
- Enabling Optical and Copper Attach flexibility at System Build
- The Implementation Agreement is in the final stages of review by the membership

AGENDA

- **Co-Packaging Framework Document**
- **External Laser for Co-packaging**
- **3.2T Module for Co-packaging**
- **Co-Packaging Electrical Interfaces**
- **Thoughts on Where to Go From Here**
- **Challenges for Next Generation Co-Packaging Solutions**
- **Panel Discussion**

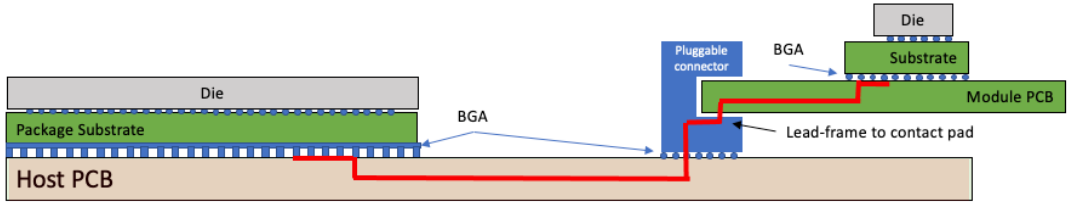
Co-Packaging Electrical Interfaces

Yi Tang
Cisco Systems, Inc.

03/09/2023

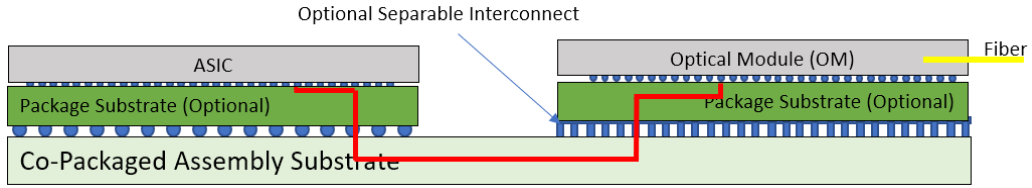
CEI – An Essential Building Block for Co-packaging

Pluggable Module Channel Example Illustration



- Channel loss: 16dB ball to ball (22-24dB bump to bump)
- Typical pluggable connectors: IL of ~1dB with RL of -10dB @26.5GHz

CPO/NPO Channel Example Illustration



- Channel loss: CPO – 10dB bump to bump; NPO – 13dB bump to bump
- Optional separable interconnect performance example: LGA socket: IL of ~0.05dB with RL of -40dB @26.5GHz (*oif2020.341.01, Nathan Tracy*)
- Avoids/reduces major discontinuities.
- Optical modules are not end-user pluggable.

- Significant power saving opportunity over VSR to be captured.
- A broad interoperable ecosystem is the key to success and can only be achieved through standardization.

CEI-112G-XSR-PAM4

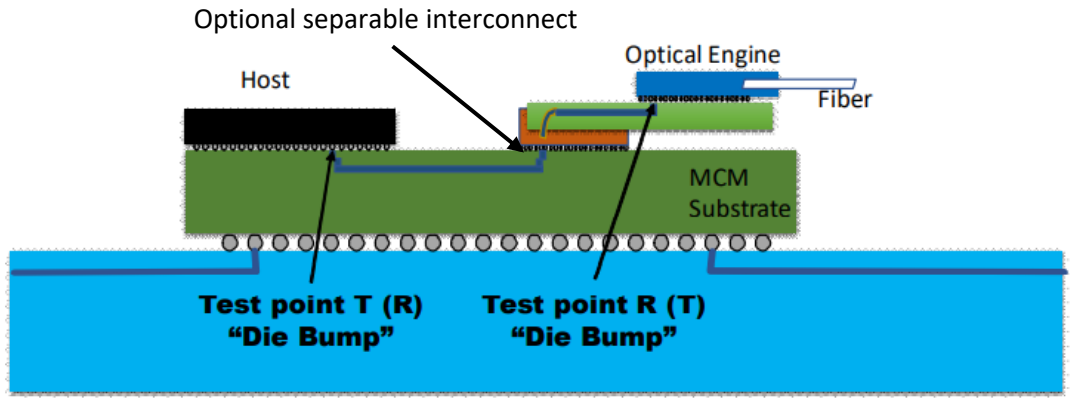


Diagram Source: OIF-CEI-05.0 – Common Electrical I/O (CEI) – Electrical and Jitter Interoperability Agreements for 6G+ bps, 11G+ bps, 25G+ bps, 56G+ bps and 112G+ bps I/O (May 2022)

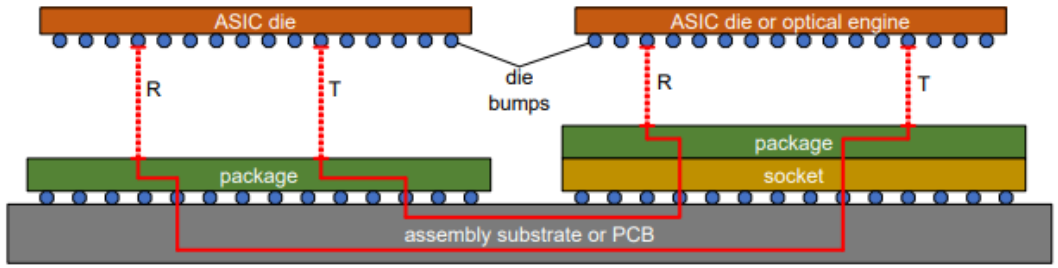
Category	IL at Nyquist (Max, dB)	BER (Max)
CAT1	10	1e-6
CAT2	10	1e-8
CAT3	8	1e-9

- Baud rates supported: 36 Gsym/s to 58 Gsym/s
- Based on loss and jitter budgets between TX and RX using copper signal traces in a SIP(System in a Package) to enable low power consumption
- Three channel categories are defined, allowing optimization for various applications.
- IA published in OIF-CEI-5.0 (clause 24) on May 5, 2022!

CEI-112G-XSR+ -PAM4

- Baud rates supported: 36 Gsym/s to 58 Gsym/s
  - Optimize for Ethernet rate @ 106.25Gbps – the key application for CPO/NPO
  - Insertion loss < 13dB @ 26.5625GHz Nyquist bump to bump with up to 1 separable interconnect.
- Enable the lowest practical energy consumption (pJ/b) implementation.
- Leverage specification methodology and other work from existing CEI 112 projects.

- Define compliance test methodology for output and input. Document constraints of the NPO applications used to derive the compliance specifications.
- Baseline document was adopted into IA draft on 11/01/2022. The working group addressed several key TBDs in the IA and the new revision oif2021.603.07 is uploaded to OIF.



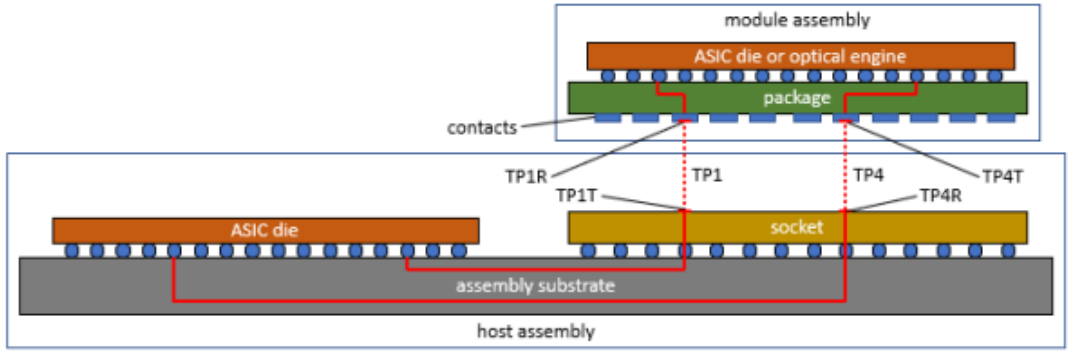


Diagram Source: oif2021.603.07 CEI-112G-XSR+-PAM4 Extended Extra Short Reach draft

What's Next

- OIF-FD-CEI-224G-01.0 – Next Generation CEI-224G Framework was published on 02/07/2022!
  - Challenges and possible solution space
  - Interconnect applications, including Co-packaging applications.
  - Points of Interoperability
  - Opportunities for future work
- The working group started CEI-224-XSR, CEI-224-VSR, CEI-224-MR, CEI-224-LR projects in Feb 2022.

"As has been demonstrated in the past, most recently at 112 Gbps, the OIF is proposing to play a key role in coordinating industry activity to identify and develop critical technical solutions that will enable next generation data rates to be cost effectively deployed in the development of next generation equipment and networks."

AGENDA

- **Co-Packaging Framework Document**
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- **Thoughts on Where to Go From Here**
- **Challenges for Next Generation Co-Packaging Solutions**
- **Panel Discussion**

Thoughts on Where to Go From Here

Nathan Tracy, TE Connectivity
OIF Market Awareness & Education
Committee Co-Chair, Physical & Link Layer

Current OIF 3.2 Tbps Formfactor
Size and Density Considerations

- The size of the co-package optics module combined with the required aggregate bandwidth (number of modules) determines the overall size of the Co-Package assembly or Near-Package assembly
- Size/density of the assembly is important
- Impacts substrate size and manufacturability

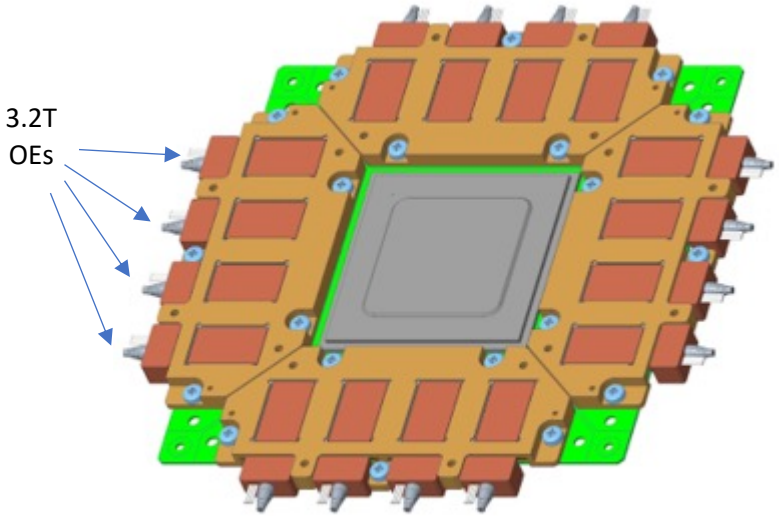


Figure 3 Example attachment system (51.2T)

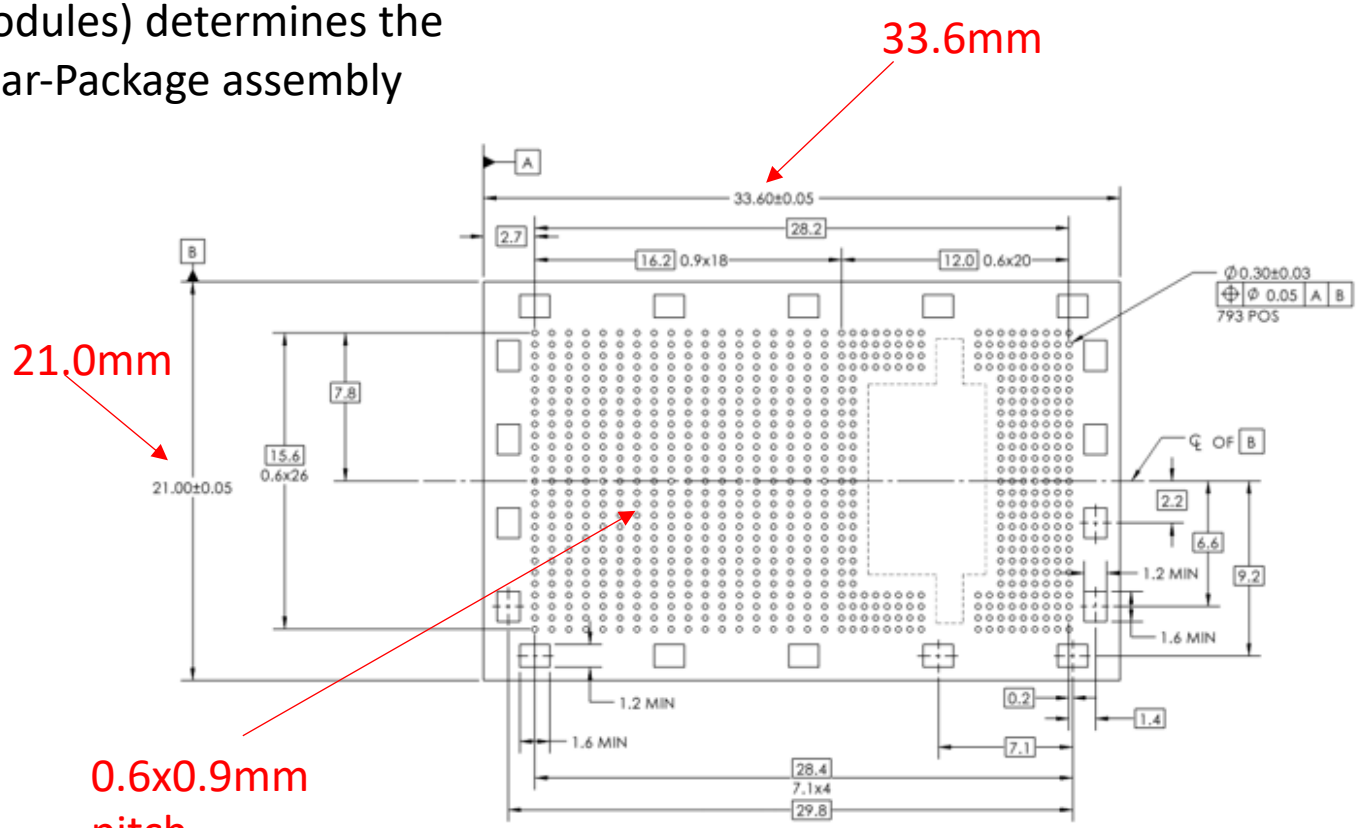
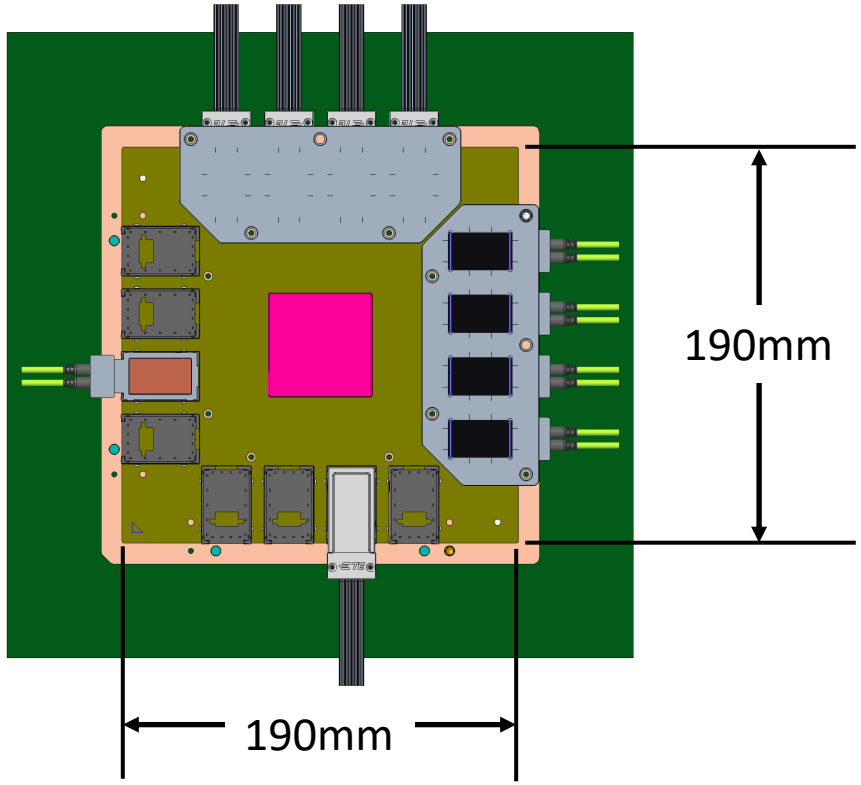


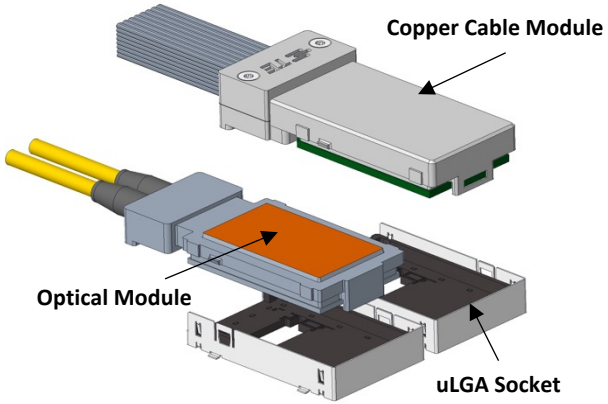
Figure 14 Module mechanical footprint (see notes below)

TE Reference Design

- Practical implementation of the current OIF Project in a 51.2T implementation

- Key Factors:
  - Socket size
  - Mechanical compression for flatness
  - Thermal compression and contact area
  - Electrical reliability

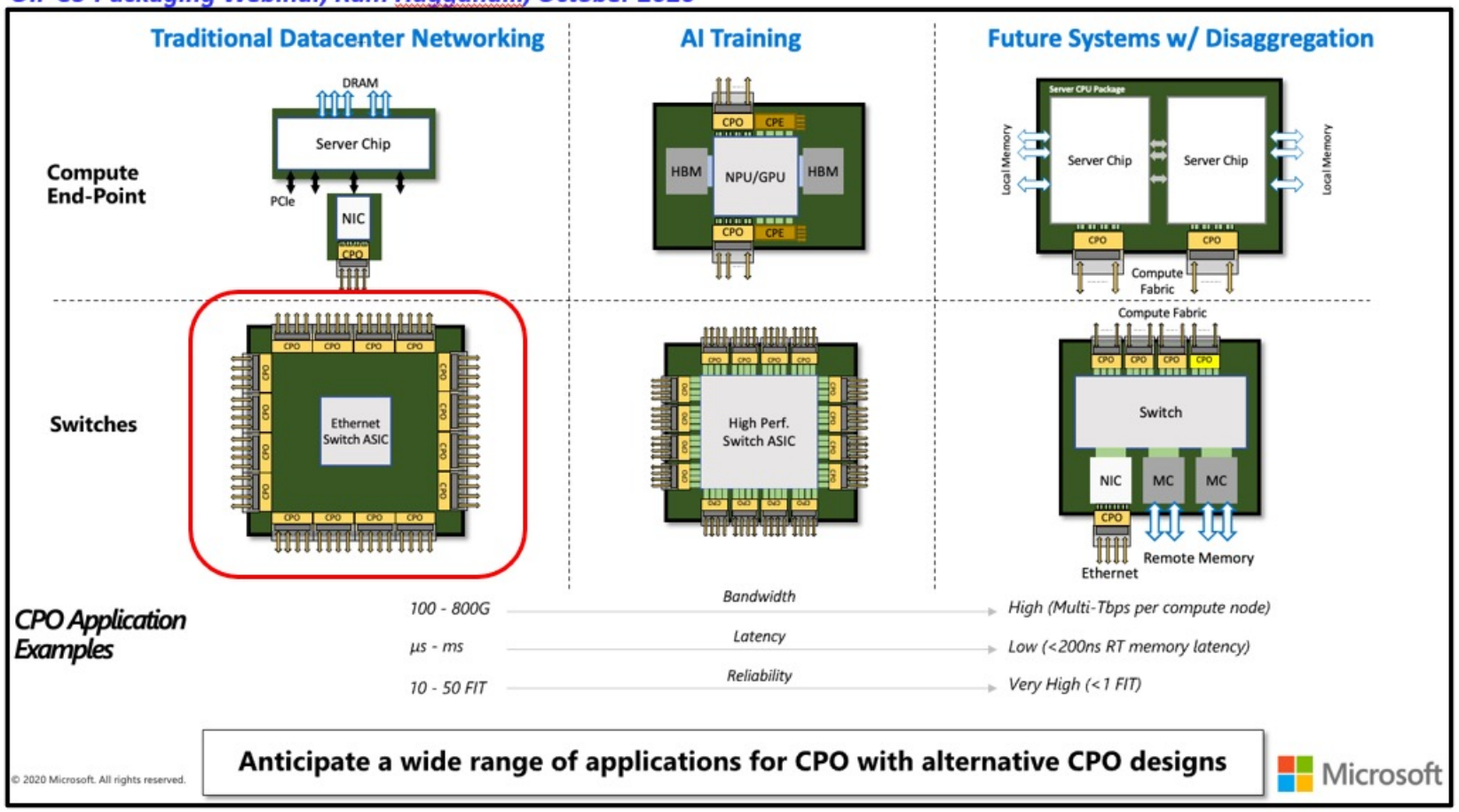




Current OIF Project is Optimized for One Application, Ethernet Switching

- Arguably the most challenging application from a size/density perspective
- Other applications bring their own challenging demands, but likely have a lower aggregate bandwidth to address
- Changes some of the mechanical constraints

OIF Co-Packaging Webinar, Ram Huggahalli, October 2020



Mechanical Factors Impacting Size/Density

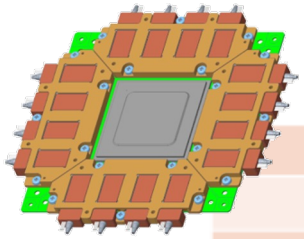
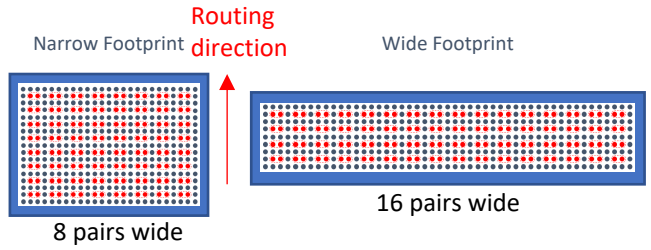


Figure 3 Example attachment system (51.2T)

	Scenario A	Scenario B	Scenario C	Scenario D	Scenario E	Scenario F	Scenario G	Scenario H
Module Bandwidth	3.2T	3.2T	3.2T	3.2T	6.4T	6.4T	6.4T	6.4T
# of Modules	16	16	16	16	8	8	8	8
Contact Pitch	0.40	0.40	0.60	0.80	0.40	0.60	0.80	0.80
Footprint	Narrow	Wide	Narrow	Narrow	Narrow	Narrow	Narrow	Wide
Socket Array	25 x 21 = 525	49 x 12 = 588	25 x 20 = 500	25 x 19 = 475	25 x 41 = 1025	25 x 40 = 1000	25 x 38 = 950	49 x 21 = 1029
Socket Size (W x D)	13.20 x 11.60	22.80 x 8.00	18.80 x 15.80	24.40 x 19.60	14.00 x 20.40	19.60 x 28.60	25.20 x 35.60	44.40 x 22.00
Substrate Size	97.80	129.00	128.00	157.40	88.80	115.80	140.40	151.60
Routing Distance (Manhattan)	52.20	84.20	81.80	109.80	42.40	67.60	90.40	103.60
Routing Distance (Crow Flies)	36.93	59.54	57.85	77.65	30.00	47.83	63.96	73.26
Ease of Routing								

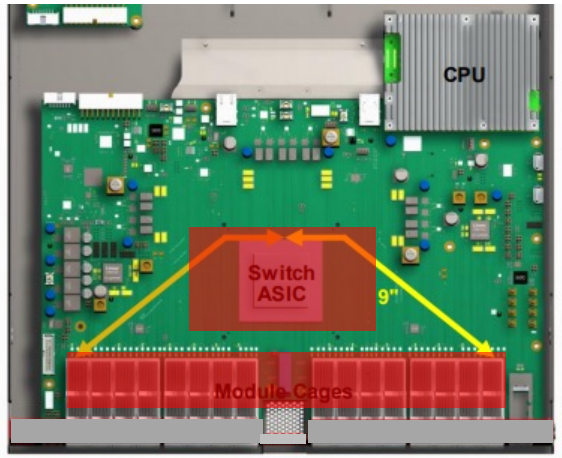
- There are a lot of “knobs” to adjust, but a significant change in size can be affected
- Socket contact pitch considerations can have a huge impact, both 0.4mm and 0.6mm are workable, 0.8mm has dire consequences
- Density of modules (aggregate bandwidth) is a huge factor, i.e. having modules on only two sides of the silicon changes everything (vs. 4 sides)



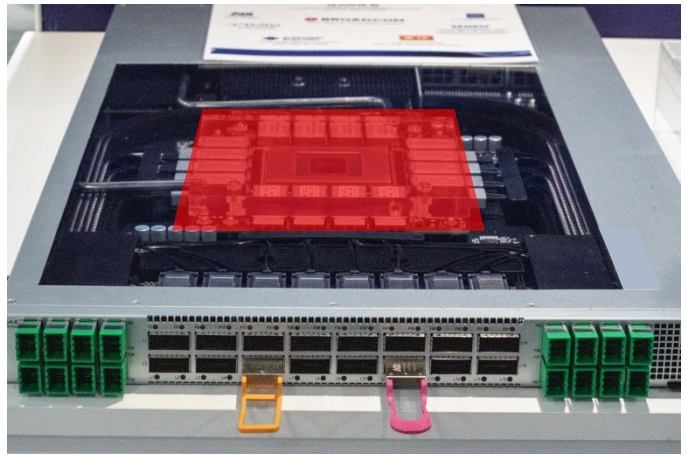
Thermal Considerations

- Co-Packaging moves all the modules next to the switch silicon
- Lower power but higher thermal density

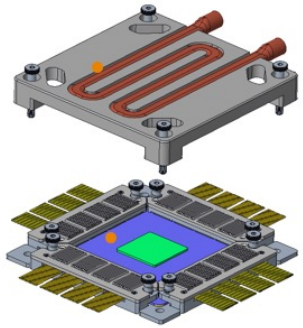
Conventional pluggable optics
Has heat sources distributed at the face plate & switch silicon



Co-Package optics
Has heat sources concentrated at the switch silicon area



Liquid cooling concept

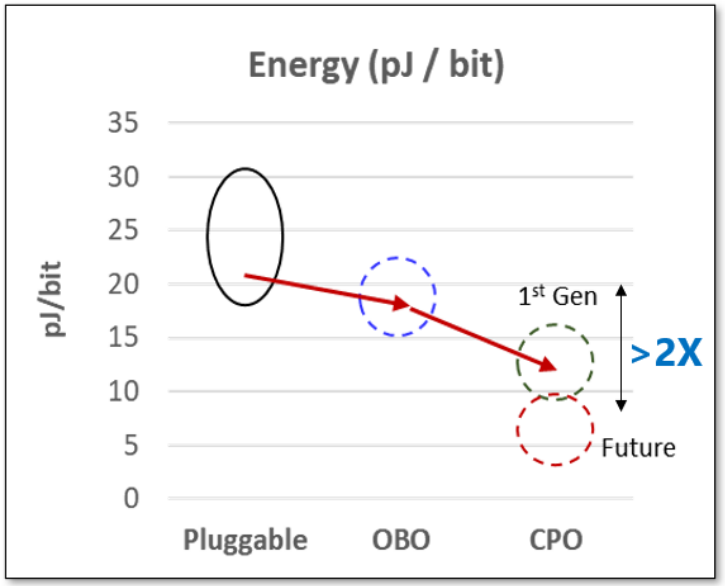


- Considering a “Linear” link, ie remove retimers from the optical modules

Linear (Unretimed) Further Reduces Power

OIF Co-Packaging Webinar, Ram Huggahalli, October 2020

CPO Benefits



Aggregate energy savings expected to be significant at a Datacenter level

	Interconnect Metric	Desired Characteristics
	Optical Reach	10-1000s of meters
HW Cost	Component Cost	<< $1 / Gbps
HW Cost	Bandwidth Density	100s of Gbps / mm
Oper. Cost	Reliability	< 10 FIT & *Minimize Cable Handling Errors!*
Oper. Cost	Energy Efficiency	< 10 pJ / bit
	Latency	Few ns + (prop. delay)

CPO

Multiple fundamental benefits can be enabled by Package-Level Optical Integration

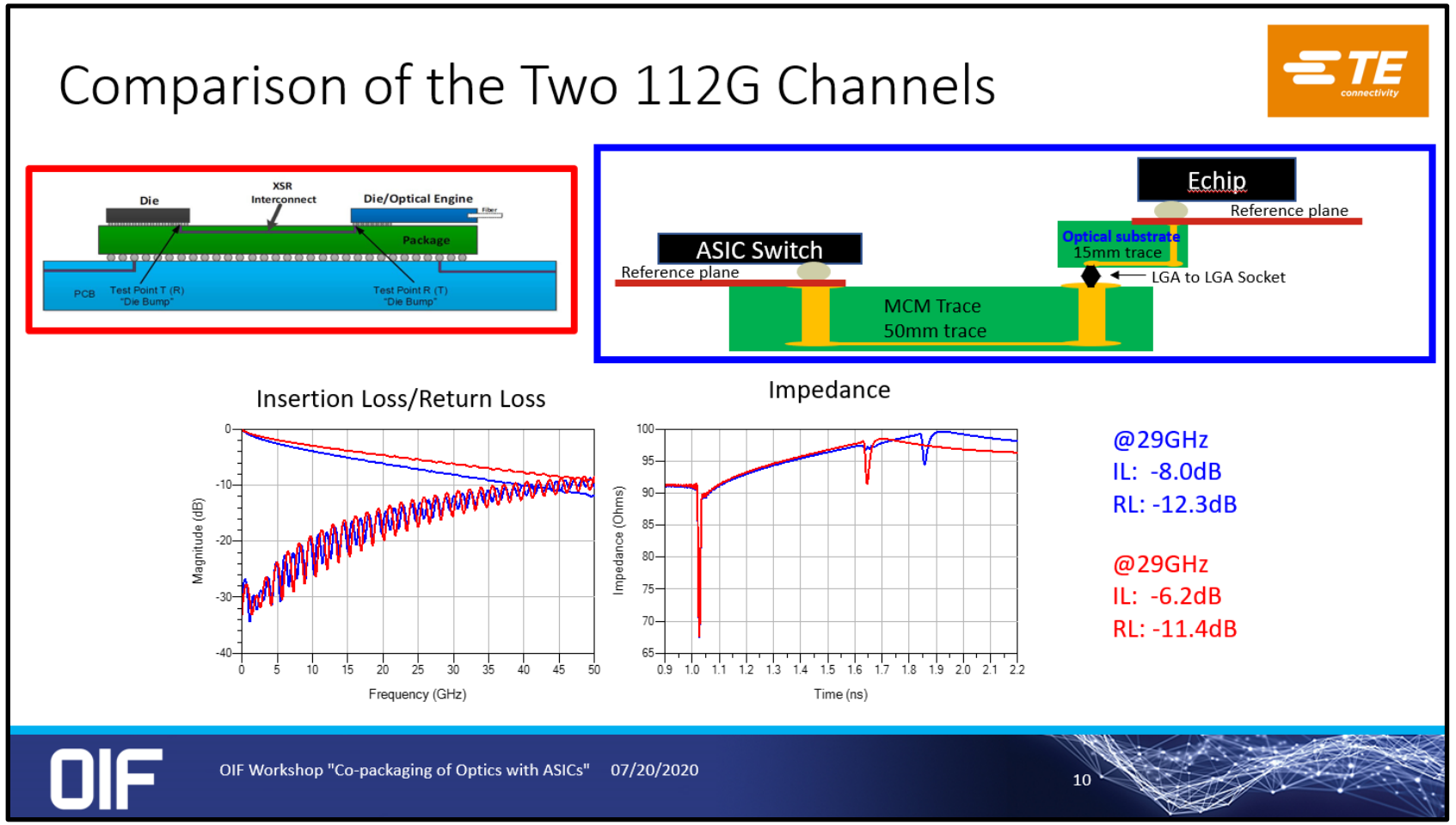
CPO is a Distinct Step Forward in Datacenter Communication Efficiency

(Energy / bit data includes module/chiplet-side electrical interface, DSP, PIC components, laser source. Excludes switch-side. Assume XSR for CPO.)

Microsoft

Linear Architectures Require Clean Channels

OIF Co-Packaging Webinar, Nathan Tracy, July 2020



Interconnect solutions are available for linear channels

Co-Packaging: Looking Forward

- Pluggables will continue to both evolve and meet needs. This is not about predicting the end
- Co-Packaging applications are much broader than high radix Ethernet switches. Will have unique needs, such as latency
- The electro-mechanical drivers are understood, size will decrease, and bandwidth density will increase
- 200 Gbps will bring conventional challenges and Co-Packaging opportunities
- Co-Package copper cables will deliver value
- Non-retimed architectures are being developed and will be valuable in Co-Packaging
- Thermal challenges will be addressed

OIF is a member driven, contribution led organization

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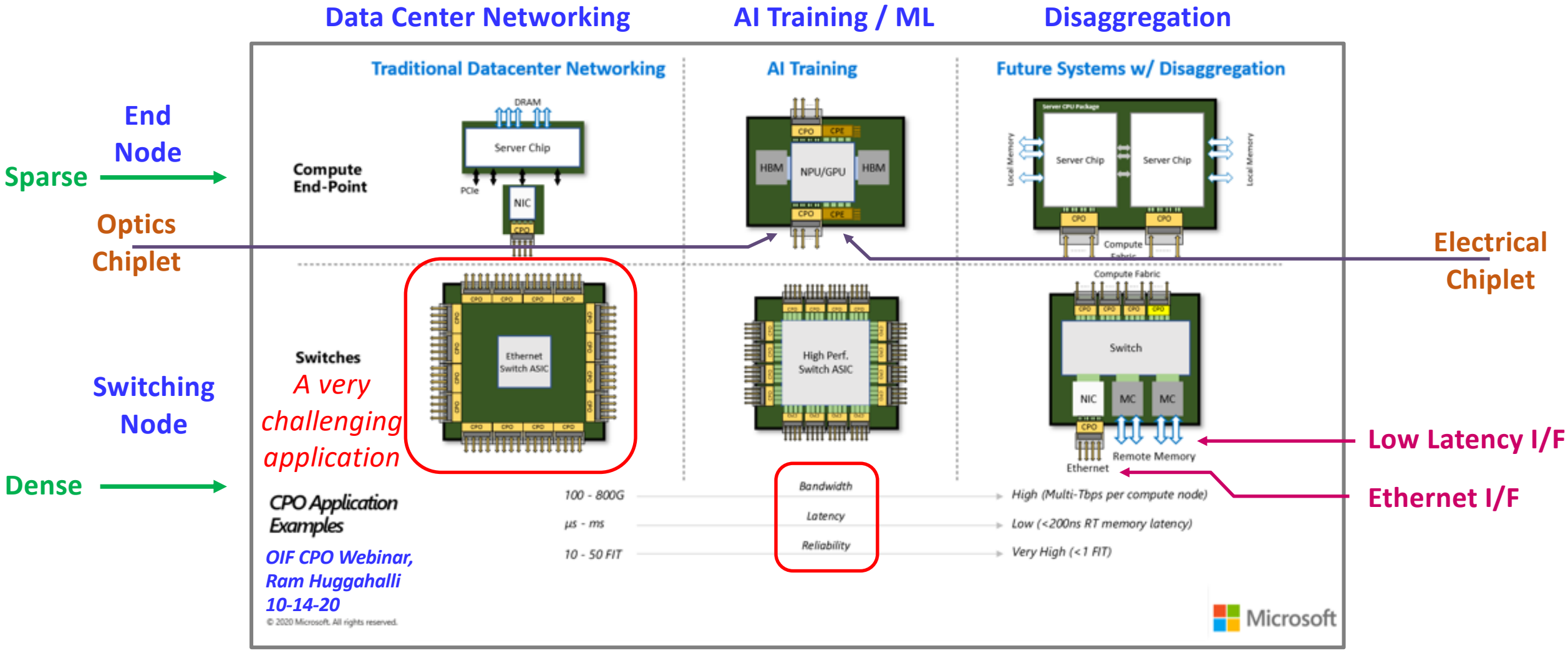
- **Panel Discussion**

Challenges for Next Generation Co-Packaging Solutions

Jeff Hutchins

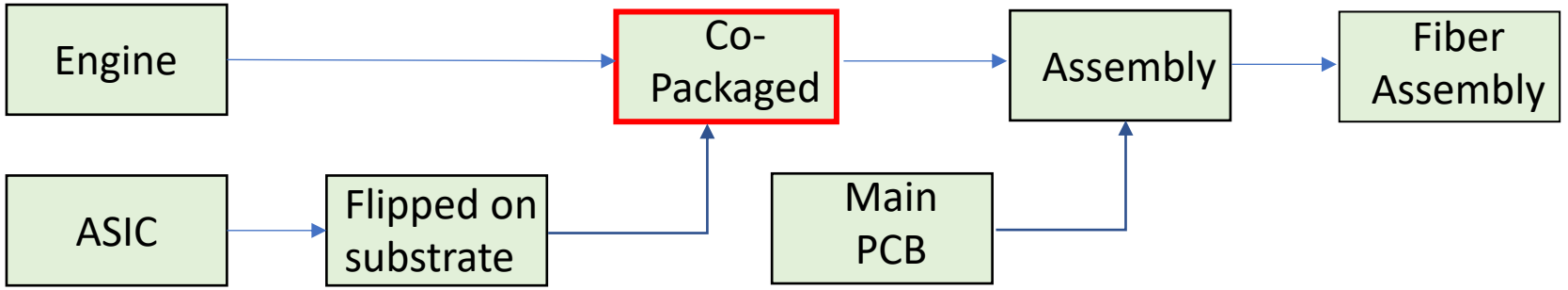
Ranovus

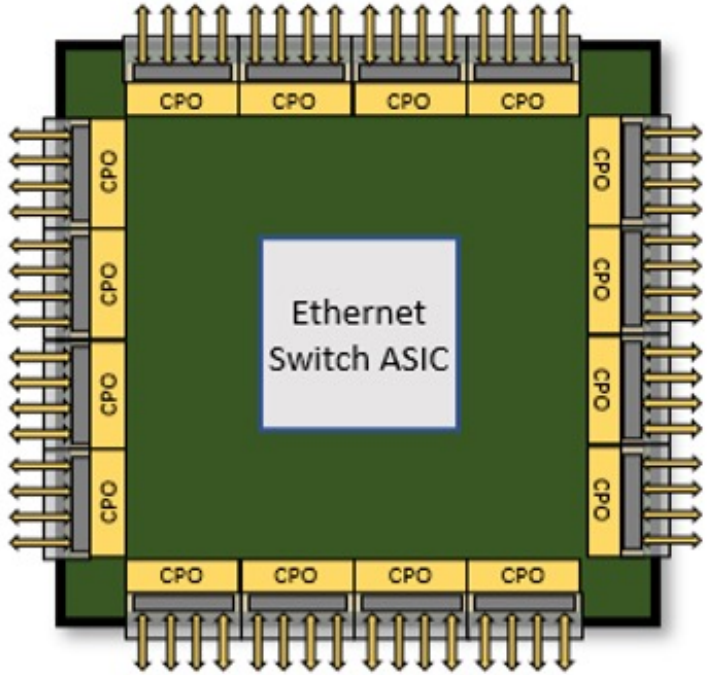
OIF Physical Link Layer Co-packaging Vice Chair



Applications requiring dense optical technologies, low latency, and reduced power will drive co-packaging

Yields are an important consideration (1)





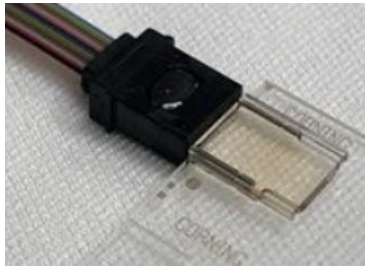
Co-Packaging Yield

$$Y_{package} = (Y_{engine})^{N}$$

First pass yield drops with increased engine count

- Optical engines require special consideration to survive reflow
- Sockets for the engine can make rework easier
- Fiber pigtails make it hard to automate handling co-packaged assemblies

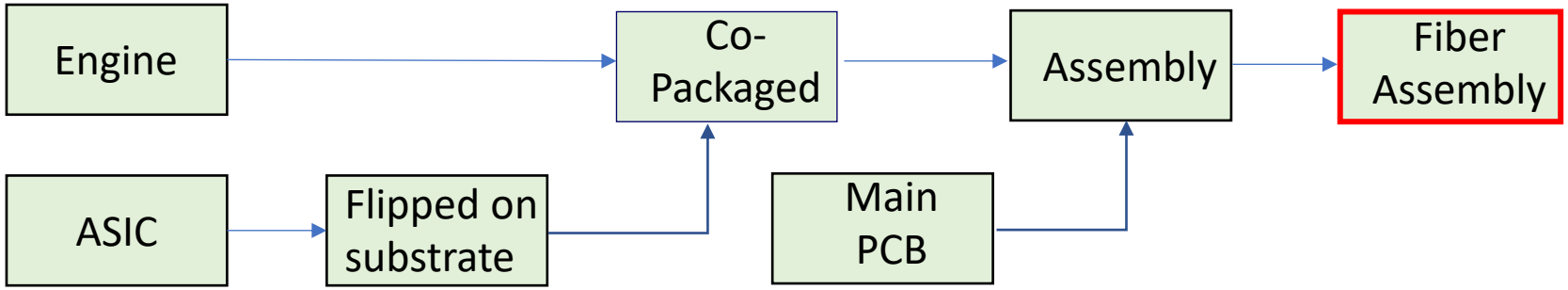
Optical connector at OE

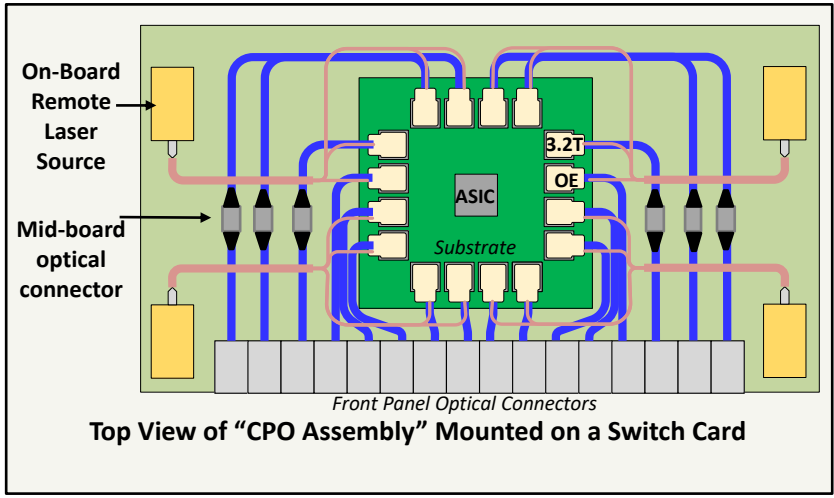


Glass Interposer for High-Density Photonic Packaging
Corning Research & Development Corporation
OFC2022 – Tu3A.3

Rework of co-packaging assembly can be facilitated with the use of engine sockets

Yields are an important consideration (2)





Top View of "CPO Assembly" Mounted on a Switch Card

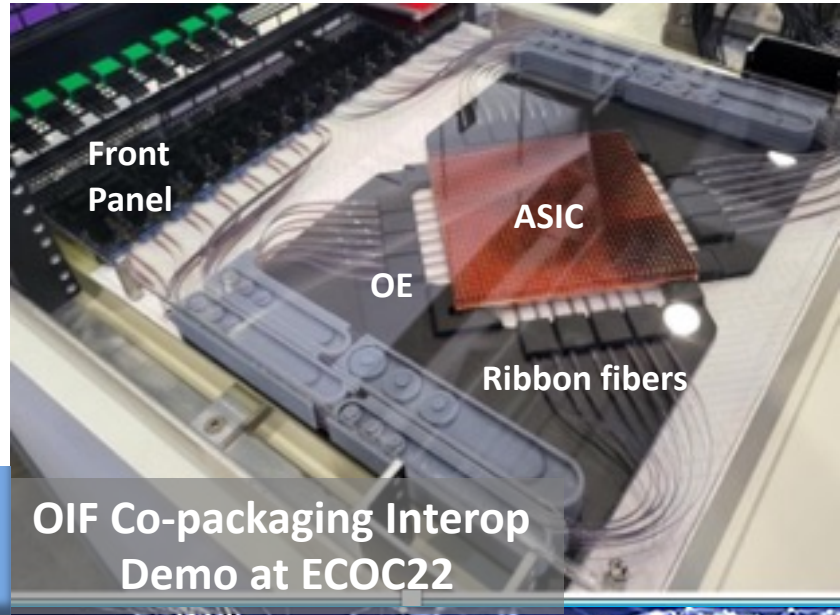
Fiber Assembly Yield

$$Y_{board} = (Y_{fiber})^{N}$$

First pass yield for mid-board optical connectors is an important factor

Number of Fibers for 51.2T Ethernet Switch Card with 100G Lanes

	DR (PSM)	FR4 (CWDM)
# Tx Fiber connections	512	128
# Rx Fiber connections	512	128
# Laser PM Fiber connections	64	32
Total Fiber Connections	**1088**	**288**
Assumed 3σ first pass fiber connection yield	99.865%	99.865%
First Pass Board Fiber Assembly Yield	**23.0%**	**67.8%**

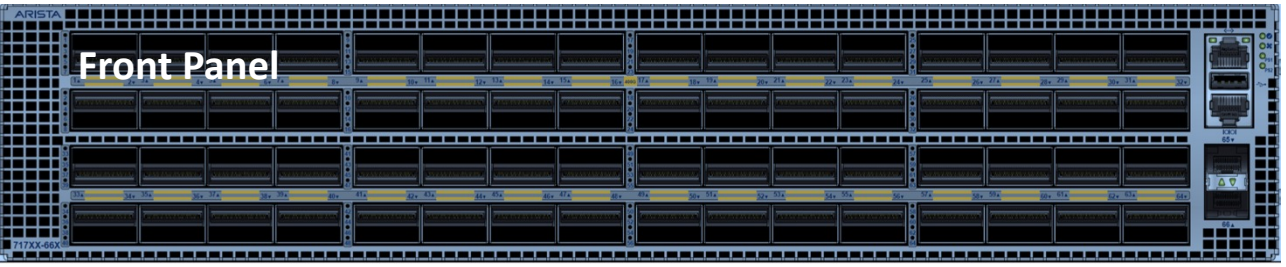


OIF Co-packaging Interop Demo at ECOC22

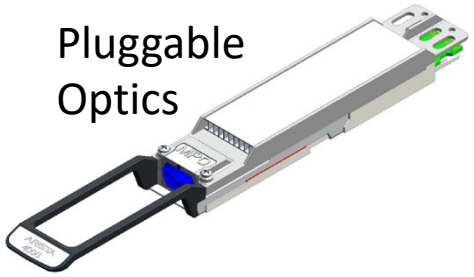
Manage tradeoff between optical link budget, coupling loss, and first pass yield!

Reliability

Front Panel Pluggables

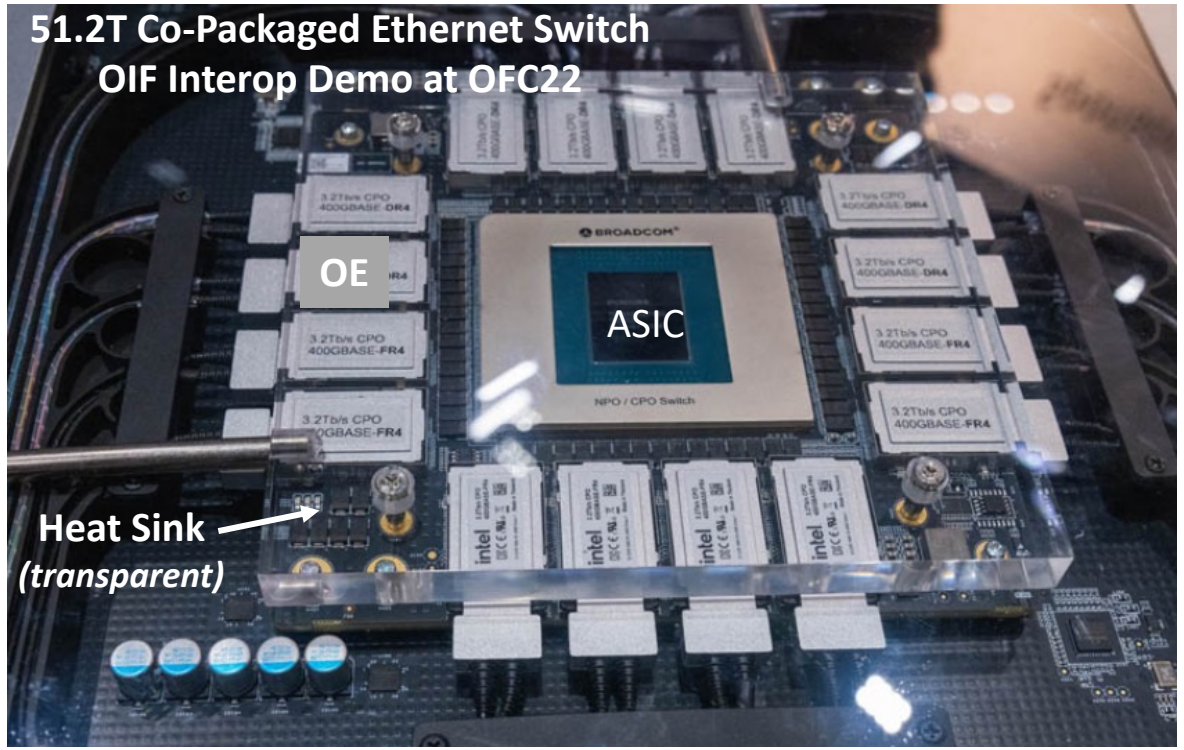


Pluggable Optics



Pluggables can be replaced if they fail without taking down the whole switch card

Co-Packaging with Optics



Co-packaged Engines are replaced by disassembling the co-packaged assembly

Ensuring excellent reliability is an important consideration for co-packaging

Laser Reliability

Laser External to Optical Engine	Laser Internal to Optical Engine
• Minimal impact to replace failed laser	• Whole switch card taken offline to repair
• Operates at higher optical powers to compensate for extra coupling losses	• Laser operates at co-packaged optics temperature
• Serves multiple channels	• Serves fewer channels
• Higher coupling losses	• Lower coupling losses

Laser reliability is a major contributor to overall optical engine reliability

Redundancy can improve reliability

Example:

Parameter	Laser Location: Front Panel	Laser Location: Optical Engine	Laser Location: Optical Engine 1:1 Redundancy
Laser Reliability at 40°C	2.0	2.0	2.0
Operating Temperature [°C]	45.0	70.0	70.0
# Lasers for per 8 channel block	2	4	4
Relative Laser Reliablity	1.0x	6.0x	~ 0x to 0.3x
Servicing impact	Minimal	Entire Switch	Entire Switch

Ea 0.35 eV, η = 1, assumed to be operated at similar current densities

Fiber Coupling Density

The number of lanes (λs) on a fiber depends on the application

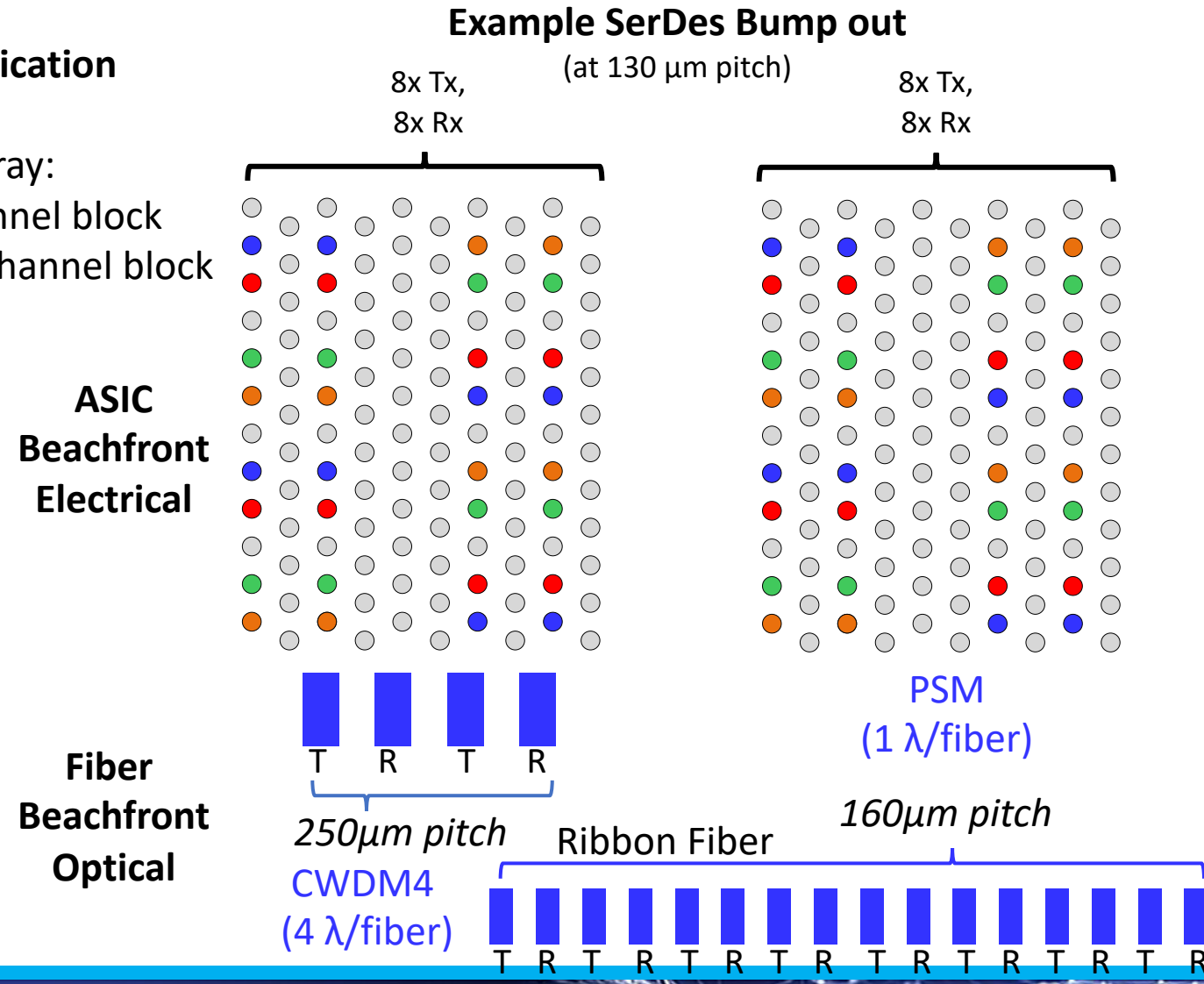
Two examples showing the ASIC bump-out & the fiber array:

- A 4λ per fiber scenario requiring four fibers per 8-channel block
- A 1λ per fiber scenario requiring sixteen fibers per 8-channel block

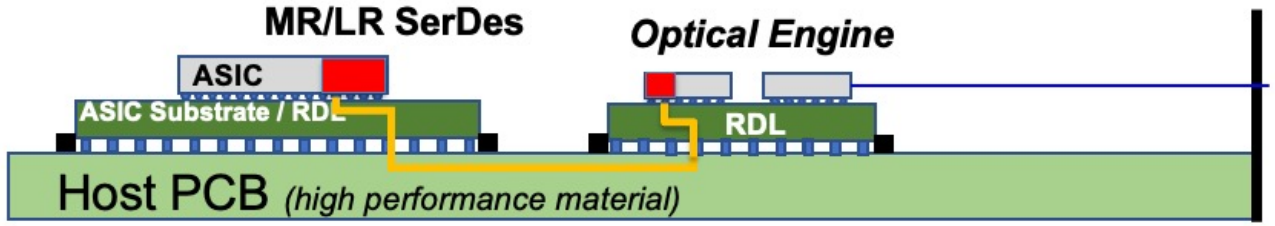
What is not included is this comparison is the optical connector overhead for alignment pins and housing

Fiber coupling density has been adequate for the current implementations

To achieve the desired increased co-packaging densities, denser fiber coupling and connector solutions will be needed

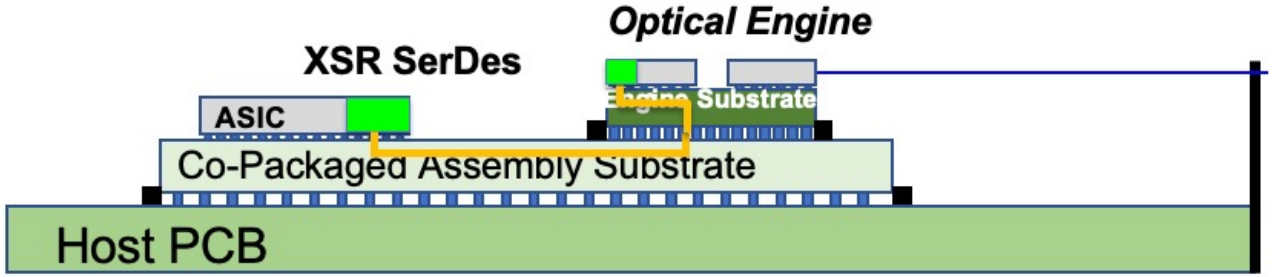


Improving latency with non-retimed Interfaces



On-Board or Pluggable Optics

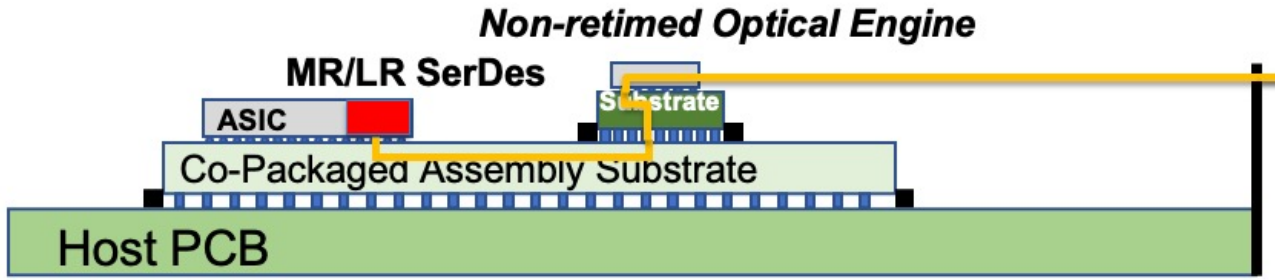
SerDes I/F can support pluggable or on-board optics

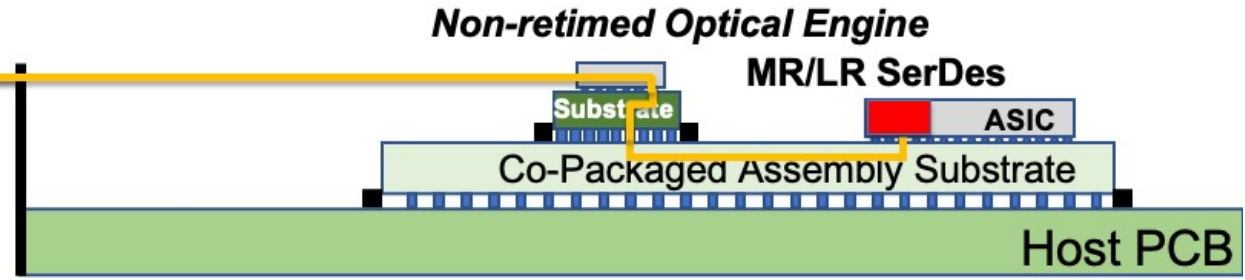


Co-packaging with low power XSR

XSR SerDes I/F supports ~50mm reach across substrate
Using a lower power SerDes could save up to ~40% reduction in switch card power

Co-packaging with non-retimed I/F





Future directions for high-speed interfaces

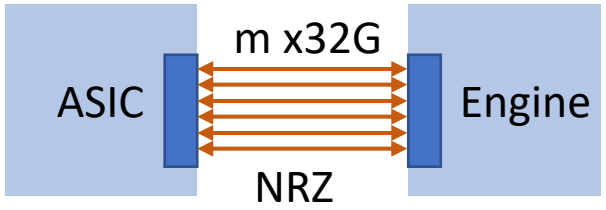
Next generation applications require bandwidth edge densities > 1T/mm

- Where latency is critical, interfaces would avoid time needed for forward error correction (FEC)
- Skipping FEC is easier at lower data rates which then requires more lanes to accommodate the same data transfer rate

Two examples:

For example: CEI- XSR/XSR+

- 130µm pitch, < 50mm electrical channel length
- Lite FEC

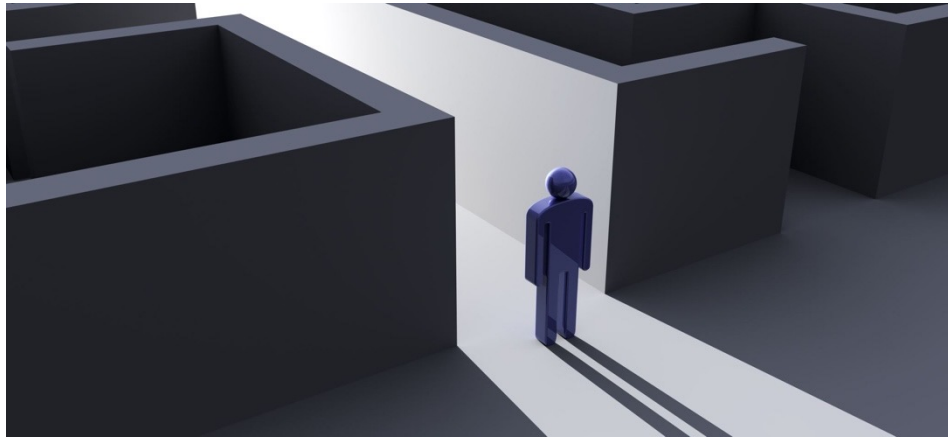


For example: UCIe, advanced package version

- 30µm pitch, ≤ 2mm channel length
- Utilizes cyclic redundancy check (CRC) and link level retry mechanism
- Very low latency

Next generation applications are driving higher data rates and increased edge densities

Challenges looking forward



Improve:

- Manufacturability and yields
- Reliability
- Beachfront optical density
  - Fiber coupling & connector density
- Beachfront electrical density [Gb/mm]
  - 200G electrical
  - Low latency “wide” interfaces
- Power efficiency [pJ/b]

AGENDA

- **Co-Packaging Framework Document**
- **External Laser for Co-packaging**
- **3.2T Module for Co-packaging**
- **Co-Packaging Electrical Interfaces**
- **Thoughts on Where to Go From Here**
- **Challenges for Next Generation Co-Packaging Solutions**
- **Panel Discussion**

Thank you for attending