CEI Interoperability Demo
ECOC 2023

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OIF's Common Electrical I/O (CEI) Work Has Been a Significant Industry Contributor

Name	Rate per pair	Year	Activities that Adopted, Adapted or were influenced by the OIF CEI
CEI-224G	224Gbps	202X	Several channel reach projects in progress, kicked off in 2022
CEI-112G	112Gbps	2022	Five channel projects are complete, two channel projects in progress, IEEE, InfiniBand, T11 (Fibre Channel), Interlaken, ITU.
CEI-56G	56Gbps	2017	IEEE, InfiniBand, T11 (Fibre Channel), Interlaken, ITU
CEI-28G	28 Gbps	2012	InfiniBand EDR, 32GFC, SATA 3.2, SAS-4,100GBASE-KR4, CR4, CAUI4, Interlaken, ITU
CEI-11G	11 Gbps	2008	InfiniBand QDR, 10GBASE-KR, 10GFC, 16GFC, SAS-3, RapidIO v3, Interlaken, ITU
CEI-6G	6 Gbps	2004	4GFC, 8GFC, InfiniBand DDR, SATA 3.0, SAS-2, RapidIO v2, HyperTransport 3.1, Interlaken, ITU
SxI5	3.125 Gbps	2002-3	Interlaken, FC 2G, InfiniBand SDR, XAUI, 10GBASE-KX4, 10GBASE-CX4, SATA 2.0, SAS-1, RapidIO v1, ITU
SPI4, SFI4	1.6 Gbps	2001-2	SPI-4.2, HyperTransport 1.03

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OIF CEI-112G Development Application Space

- PAM4 modulation scheme becomes dominant in OIF CEI-112 Gbps interface IA
- One SerDes core is not able to efficiently cover multiple applications from XSR to LR
- For short reach applications, simpler and lower power equalizations are desired

Interface	Application	Characteristics
CEI-112G-MCM	3D Stack; 2.5D Chip-to-Chiplet	CNRZ-5: up to 25mm package substrate No equalization/FEC Minimize power (pJ/bit)
CEI-112G-XSR	2.5D Chip-to-Chip; Chip to Co-Pkg Optics Engine (Chip ⇄ Optics)	PAM4: up to 50mm package substrate 6-10 dB at 28GHz Lite FEC, Rx CTLE
CEI-112G-XSR+	2.5D Chip-to-Chip; Chip to Near Pkg Optics Engine (Chip ⇄ Optics)	PAM4: up to 13dB at 26.5 GHz Power target per SerDes: 1.8pJ/bit Enables NPO implementations
CEI-112G-VSR	Chip to Module (Chip ⇄ Pluggable Optics)	PAM4: 12-16 dB at 28GHz FEC to relax BER to 1e-6 Multi-tap Tx FIR and Rx CTLE + multi-tap FFE or DFE
CEI-112G-MR	Chip-to-Chip & Midplane Applications (Chip ⇄ Chip)	PAM4: 20dB at 28GHz FEC to relax BER to 1e-6 Multi-tap Tx FIR and Rx CTLE + multi-tap FFE or DFE
CEI-112G-LR	Backplane or Passive Copper Cable (Chip ⇄ Chip)	PAM4: 28-30dB at 28GHz FEC to relax BER to 1e-4 Multi-tap Tx FIR and Rx CTLE + multi-tap FFE or DFE
CEI-112G-Linear	Chip ⇄ Pluggable Optics	PAM4: up to 11 dB at 28 GHz Without DSP/SERDES in Optical Module Lower power and cost targets

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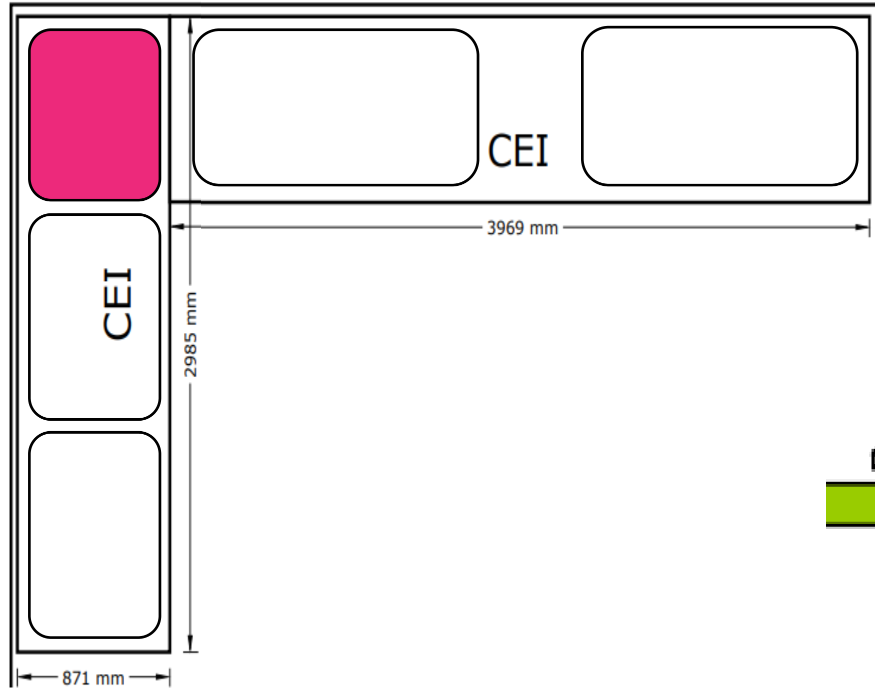
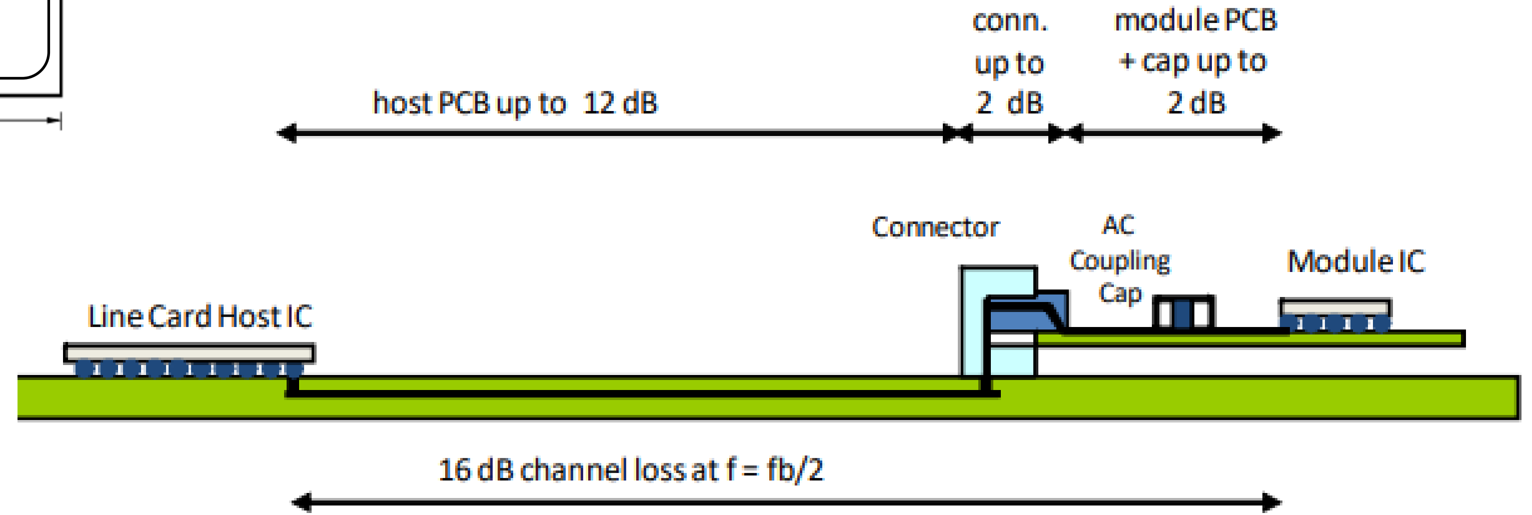
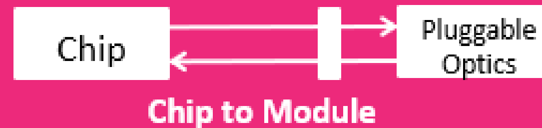
CEI-112G-VSR at ECOC 2023





CEI-112G-VSR



Chip to Module

PAM4: 12-16 dB at 28GHz
FEC to relax BER to 1e-6
Multi-tap Tx FIR and Rx CTLE + multi-tap FFE or DFE

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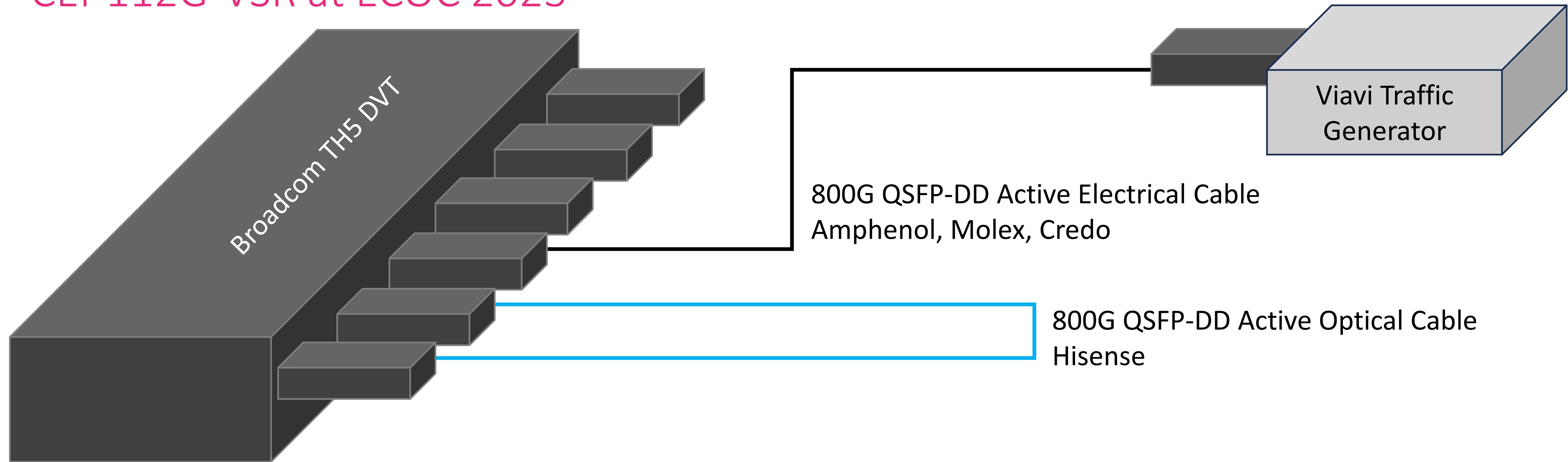

Re-timers are becoming more present in interconnects to extend their reach. This demonstration consists of an 800G port transmitting a 106.25Gbps PRBS31Q PAM4 signal to an 800Gbps QSFP-DD Active Electrical Cable (AEC) mated to a QSFP-DD module compliance board and terminated by an 800G Traffic Generator, extending the reach of copper cabling >2m while keeping BER low (1E-9). Active Optical Cables (AOC) is also used to extend the reach to up to 100m.

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CEI-112G-MR at ECOC 2023

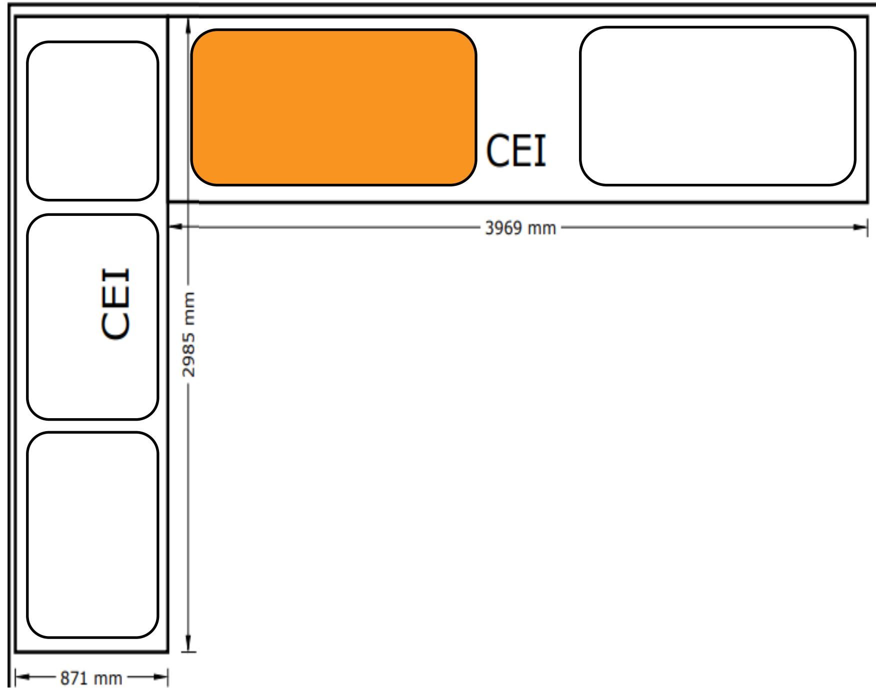
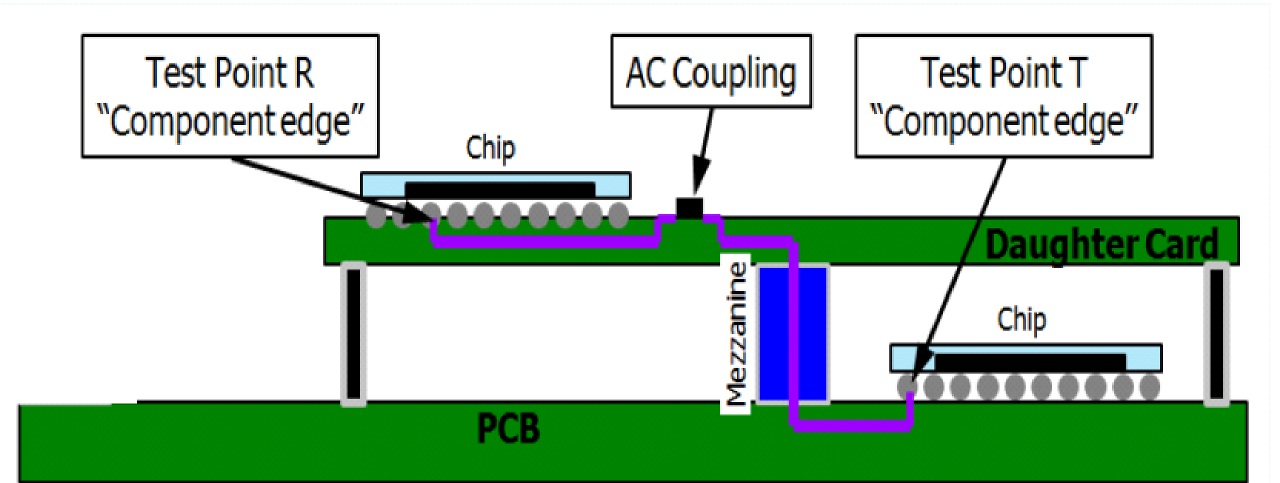


Figure 25-1.CEI-112G-MR-PAM4 Reference Model



CEI-112G-MR

Chip-to-Chip & Midplane Applications

PAM4: 20dB at 28GHz
FEC to relax BER to 1e-6
Multi-tap Tx FIR and Rx CTLE + multi-tap FFE or DFE

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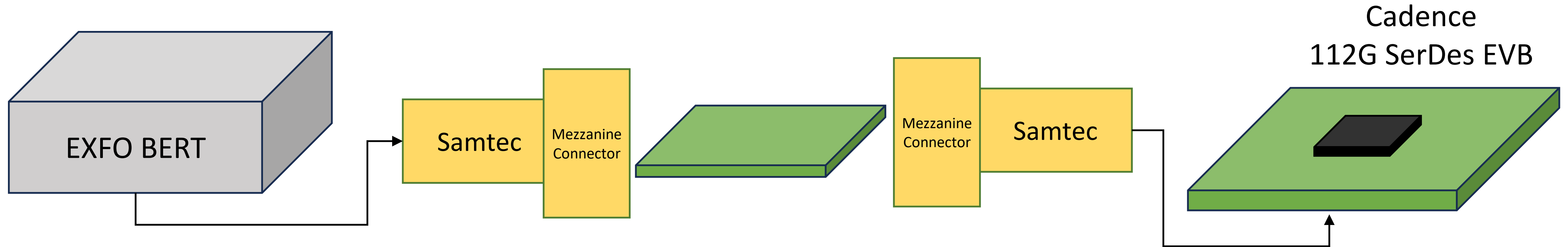

This medium reach interoperability demonstration consists of multivendor silicon transmitting 106.25 Gbps PRBS31Q PAM4 signals over a cabled host channel and ISI channel, simulating critical chip to chip connectivity in the datacenter.

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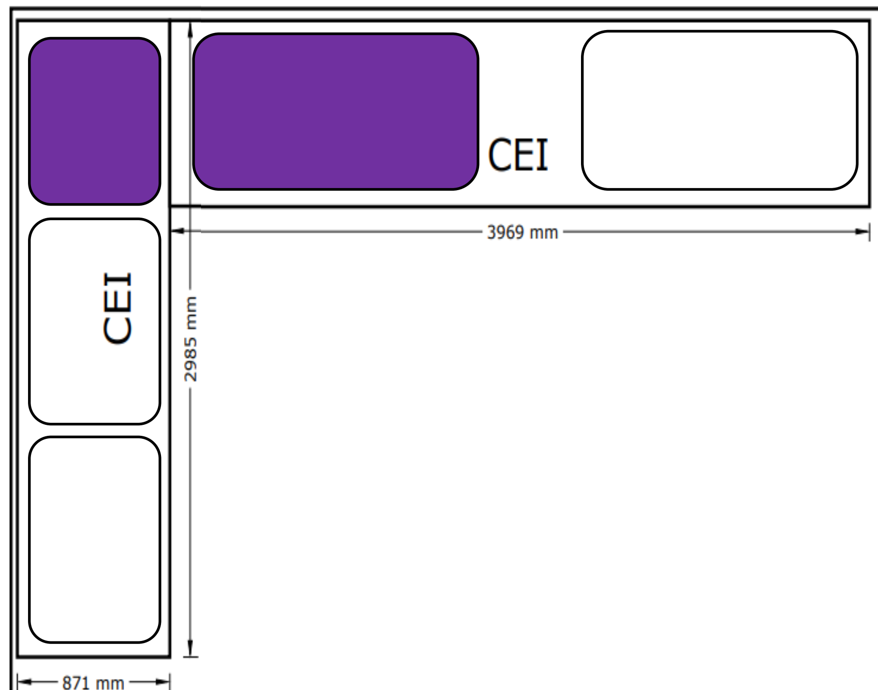
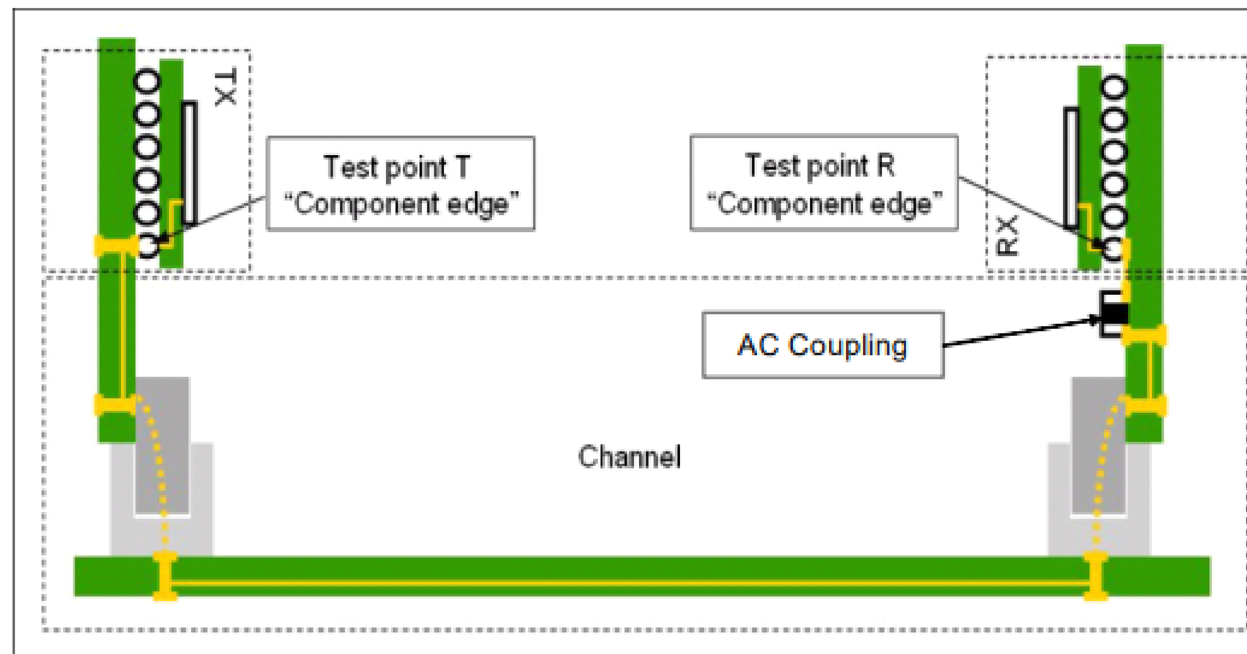
CEI-112G-LR at ECOC 2023





CEI-112G-LR

Backplane or Passive Copper Cable

PAM4: 28-30dB at 28GHz
FEC to relax BER to 1e-4
Multi-tap Tx FIR and Rx CTLE + multi-tap FFE or DFE

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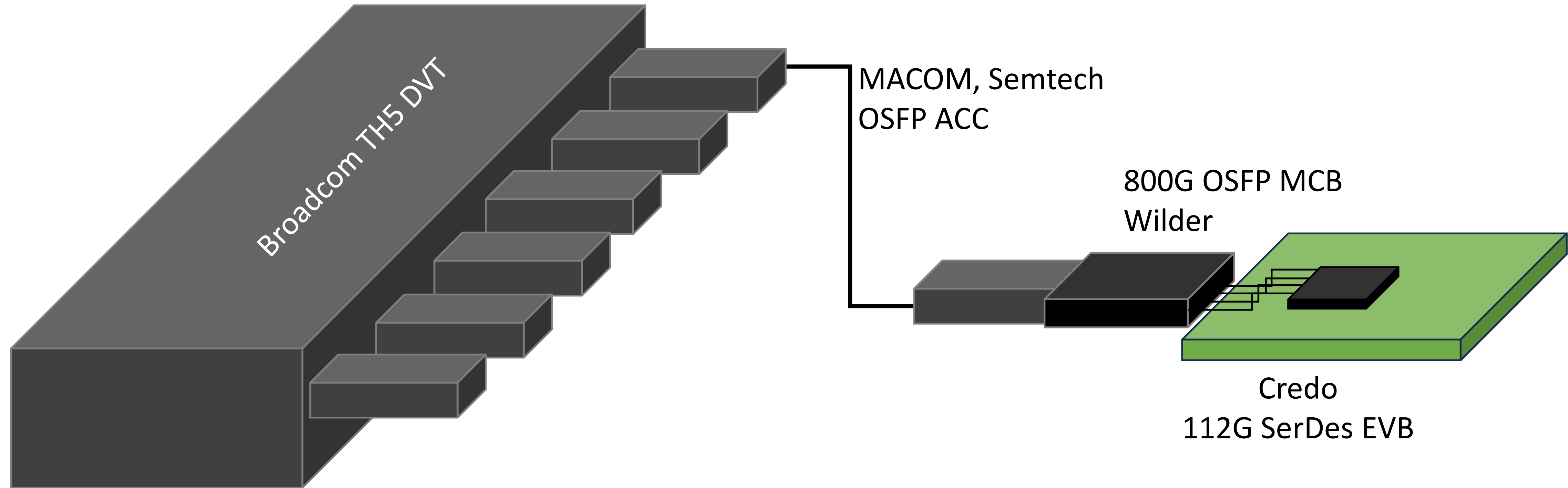
CEI-112G-LR at ECOC 2023



These long reach interoperability demonstrations consist of multivendor LR silicon sending bi-directional PRBS31Q PAM4 106.25 Gbps signals over passive Direct Attach Cables (DAC), Active Copper Cables (ACC), and Backplane connectors representing LR channels with insertion loss >36 dB. ACCs extend the reach compared to passive copper cables, while consuming lower power than retimed AECs. All links achieve a BER better than 1E-9, providing reasonable FEC margin to ensure no frame losses in deployment.

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CEI-112G-LR at ECOC 2023

Broadcom TH5 DVT

Amphenol, Molex
QSFP-DD DAC

800G QSFP-DD MCB
Wilder

Synopsys
112G SerDes EVB

These long reach interoperability demonstrations consist of multivendor LR silicon sending bi-directional PRBS31Q PAM4 106.25 Gbps signals over passive Direct Attach Cables (DAC), Active Copper Cables (ACC), and Backplane connectors representing LR channels with insertion loss >36 dB. ACCs extend the reach compared to passive copper cables, while consuming lower power than retimed AECs. All links achieve a BER better than 1E-9, providing reasonable FEC margin to ensure no frame losses in deployment.

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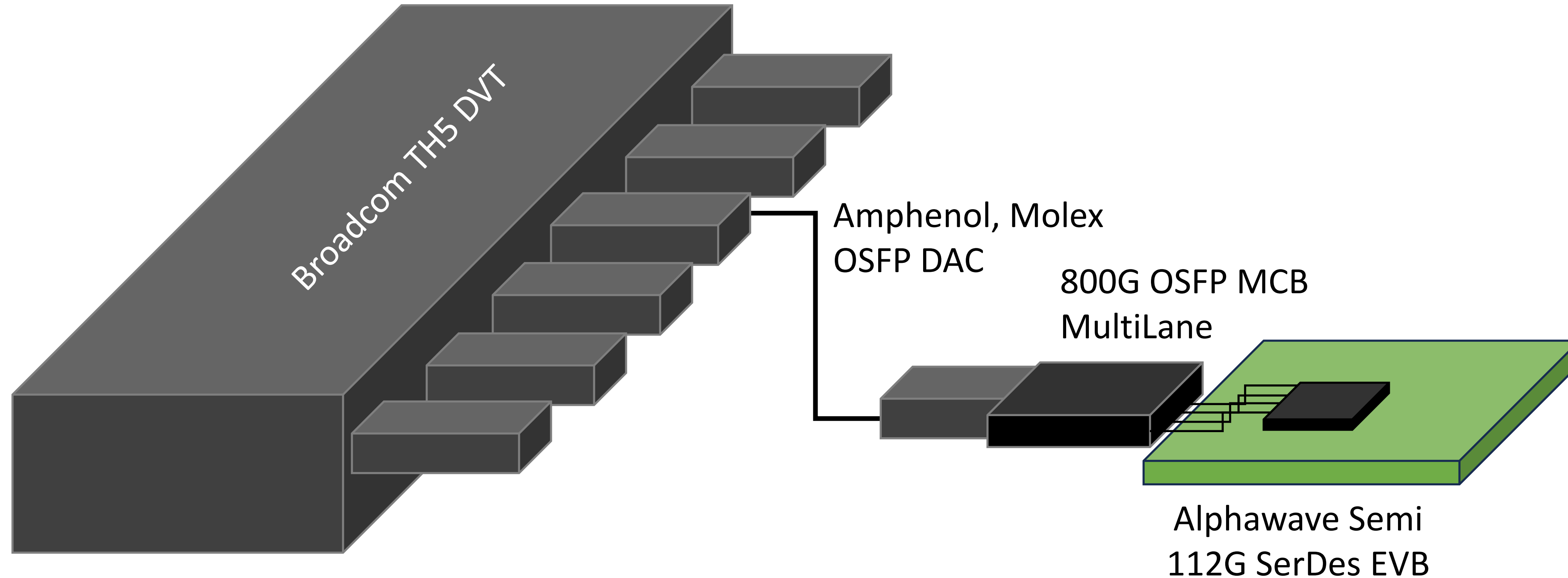

These long reach interoperability demonstrations consist of multivendor LR silicon sending bi-directional PRBS31Q PAM4 106.25 Gbps signals over passive Direct Attach Cables (DAC), Active Copper Cables (ACC), and Backplane connectors representing LR channels with insertion loss >36 dB. ACCs extend the reach compared to passive copper cables, while consuming lower power than retimed AECs. All links achieve a BER better than 1E-9, providing reasonable FEC margin to ensure no frame losses in deployment.

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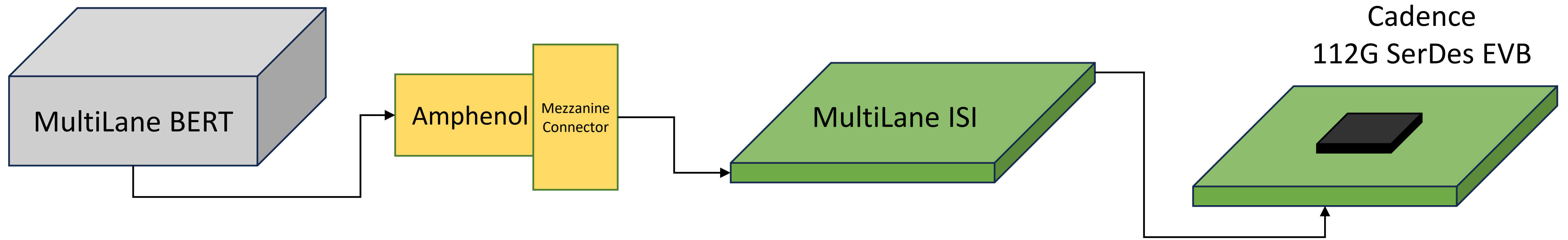
CEI-112G-LR at ECOC 2023



These long reach interoperability demonstrations consist of multivendor LR silicon sending bi-directional PRBS31Q PAM4 106.25 Gbps signals over passive Direct Attach Cables (DAC), Active Copper Cables (ACC), and Backplane connectors representing LR channels with insertion loss >36 dB. ACCs extend the reach compared to passive copper cables, while consuming lower power than retimed AECs. All links achieve a BER better than 1E-9, providing reasonable FEC margin to ensure no frame losses in deployment.

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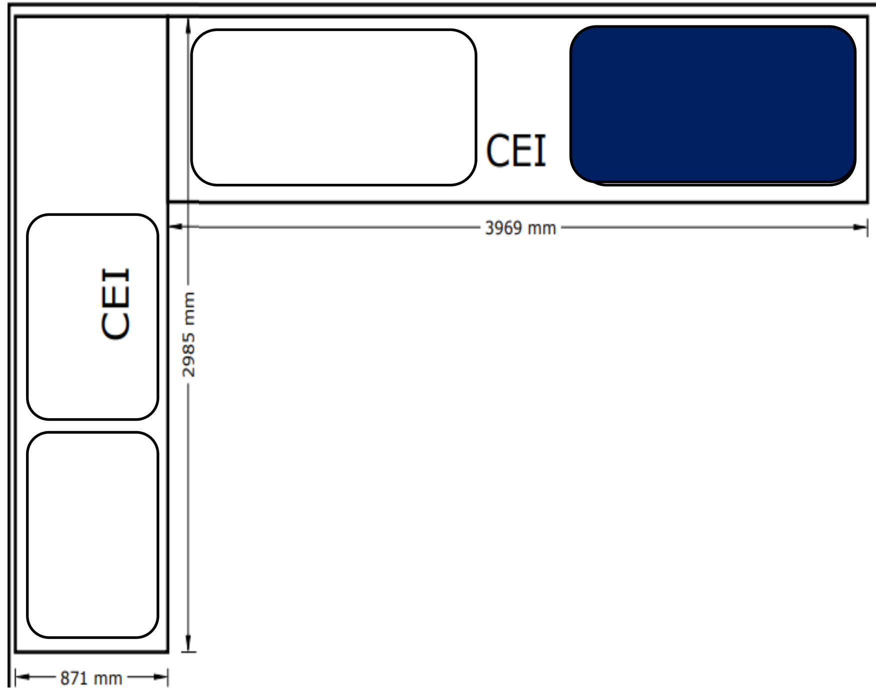
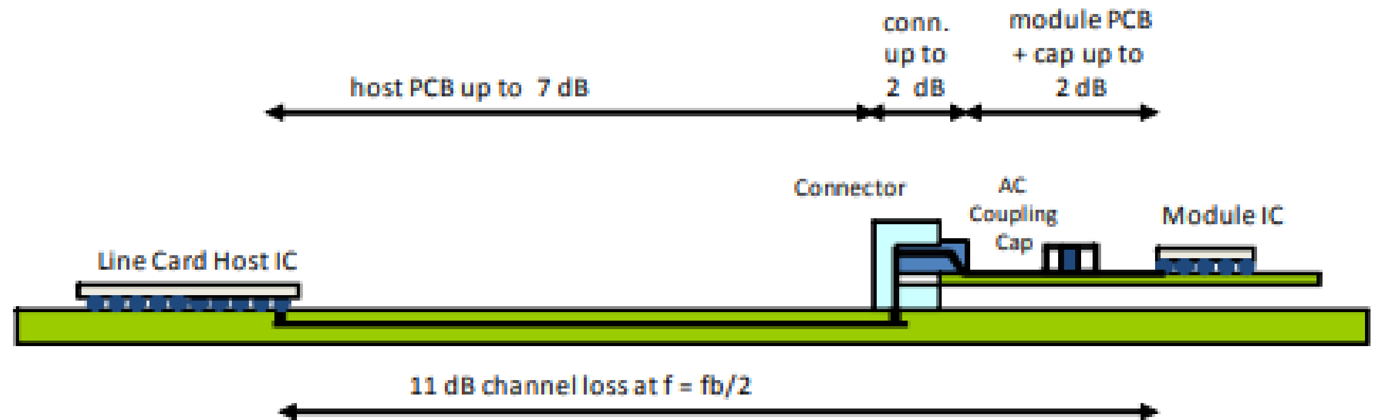
CEI-112G-Linear at ECOC 2023





CEI-112G-Linear

PAM4: up to 11 dB at 28 GHz
Without DSP/SERDES in Optical Module
Lower power and cost targets

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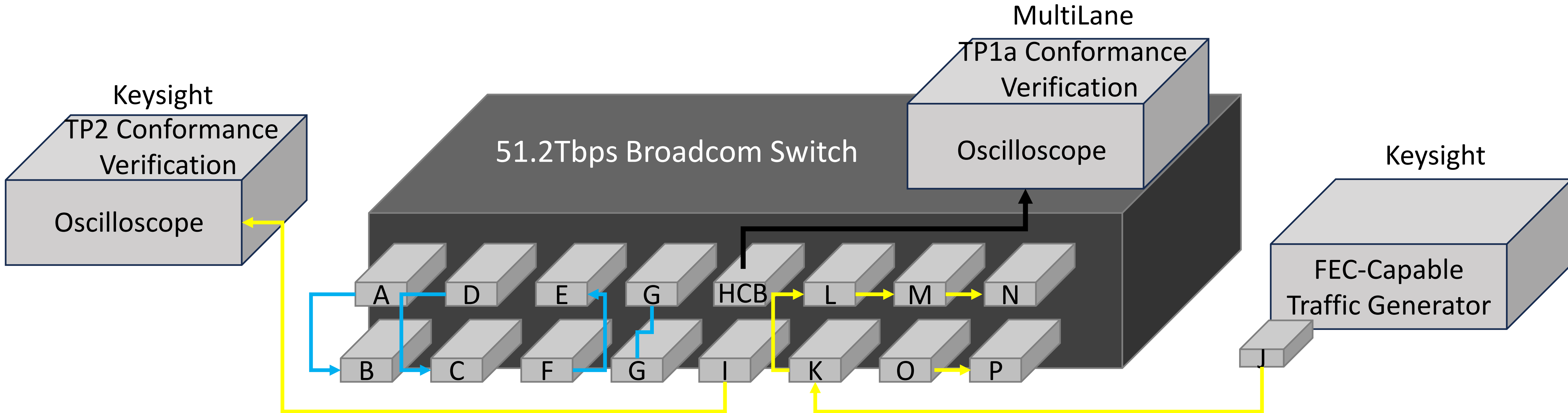
CEI-112G-Linear at ECOC 2023

Fiber Provided by Senko



800G OSFP LPO's: MACOM, EoptoLink, Semtech, Source Photonics, Hisense

This demonstration encompasses the entire ecosystem to enable multi-vendor CEI-Linear interoperability. A 51.2T capable switch drives single mode and multi-mode, multi-vendor Linear Pluggable Optics (LPO's) while demonstrating a quality BER and FEC tail margin, with minimal power consumption. Test and measurement equipment provide conformance verification and insight on compliance into each stage of the link. Interoperability between LPOs interfacing with retimed modules is also achieved showcasing compatibility between the two pluggable options.

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CEI-112G-Linear at ECOC 2023

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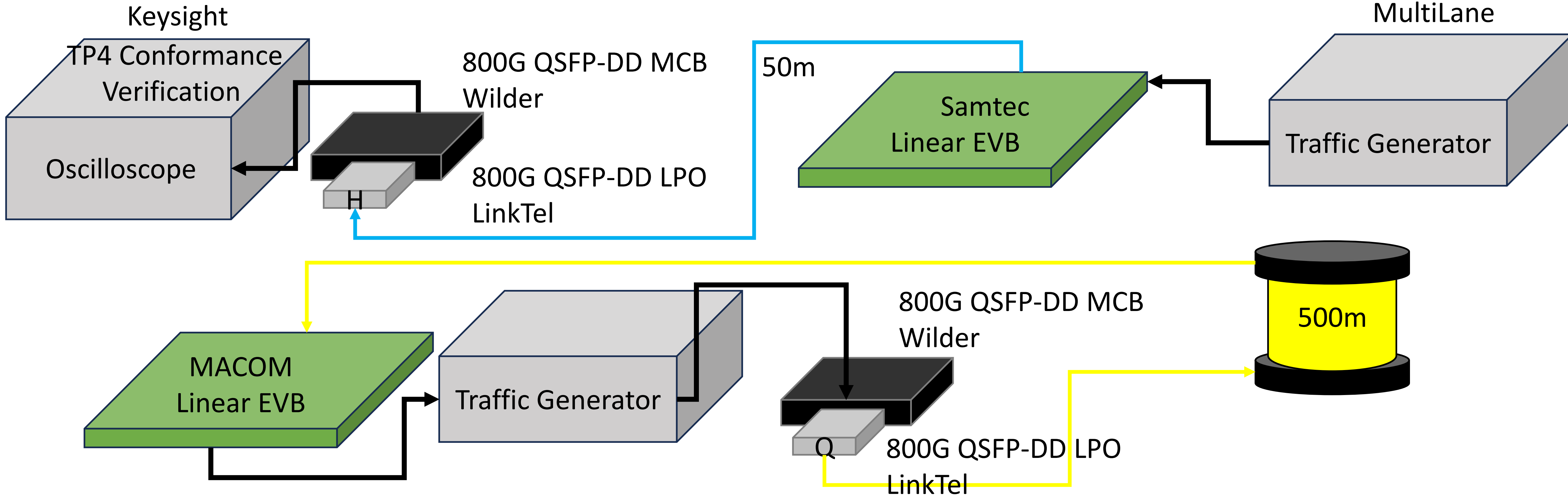

This demonstration complements the ecosystem build to show the capabilities of multi-vendor CEI-Linear interoperability across long reaches of single mode and multi mode Linear devices while demonstrating a quality BER and FEC tail margin, with minimal power consumption. Test and measurement equipment provide insight and compliance into each stage of the link.

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CEI-224G: Framework Document

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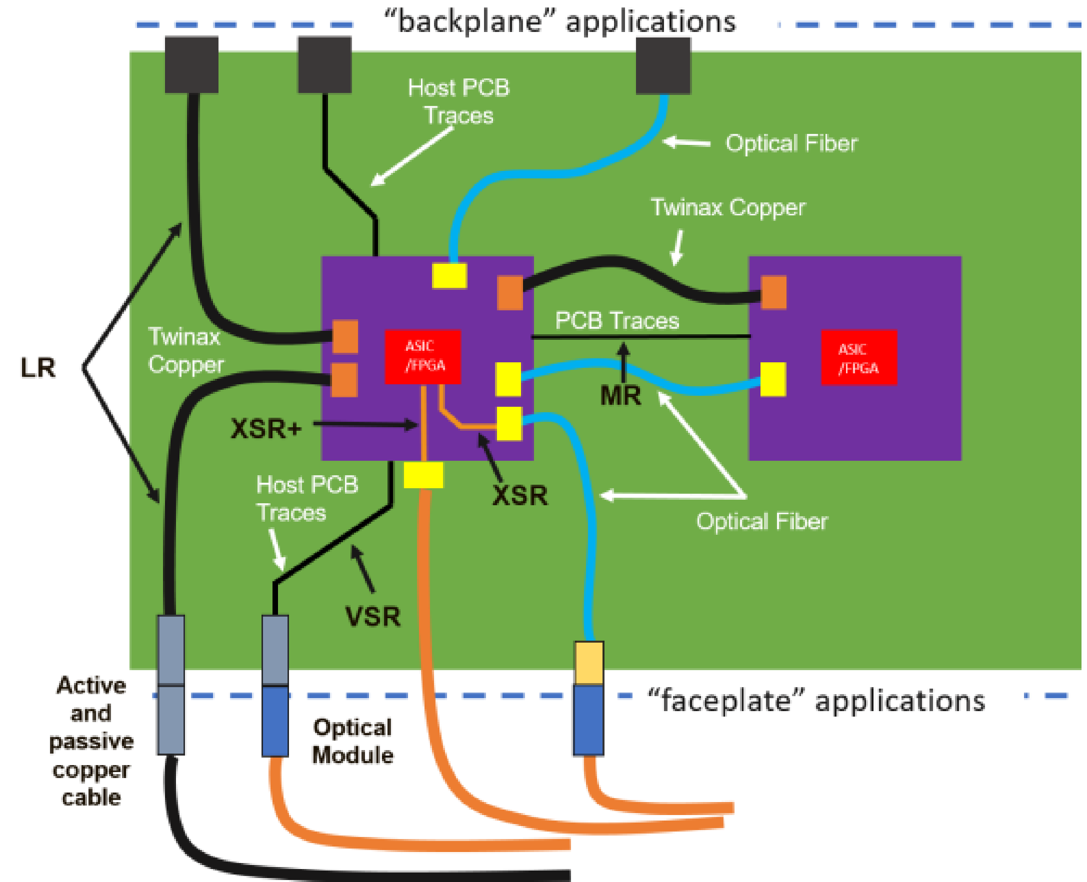
- Summarizes the consensus findings and guidance for new OIF CEI-224G projects
- Identifies key technical challenges for next generation systems
  - Power, density, performance, reach and cost
- Defines electrical interconnection applications and discusses some of the interoperability test challenges
- Establishes baseline materials that will enable 1.6/3.2 Tbps rate architectures and lower cost, lower complexity 800G and 400G architectures



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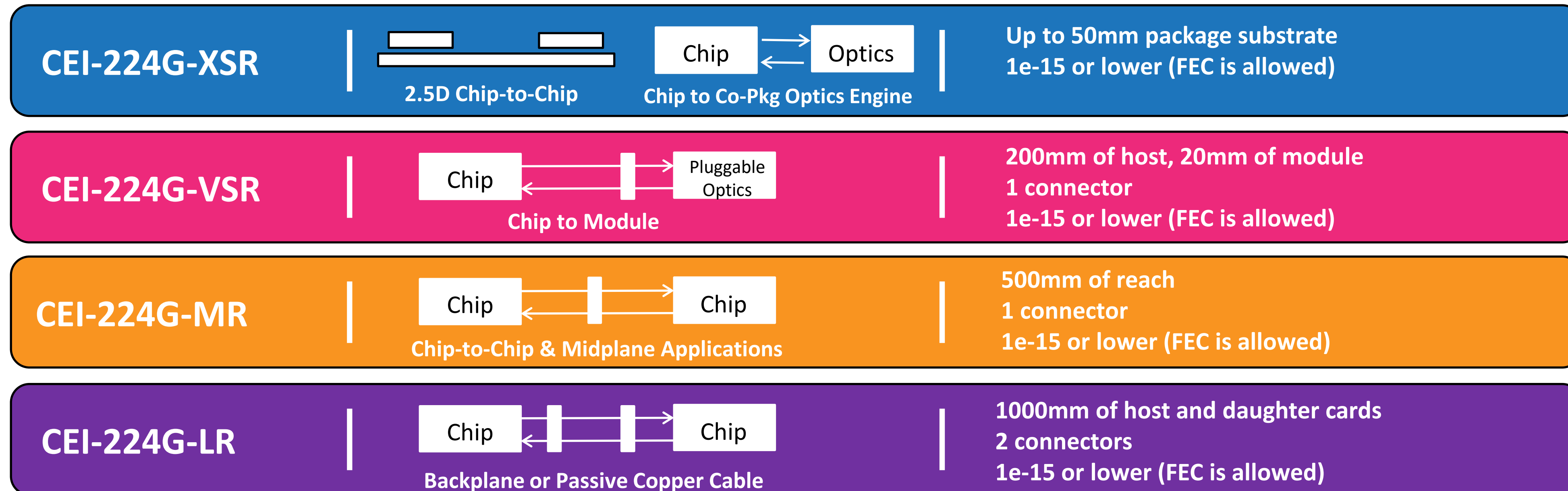
OIF CEI-224G New Project Starts



- New Projects started at OIF Q1 2022 meeting
- One SerDes core might not be able to cover multiple applications from XSR to LR
- For short reach applications, simpler and lower power equalizations are desired

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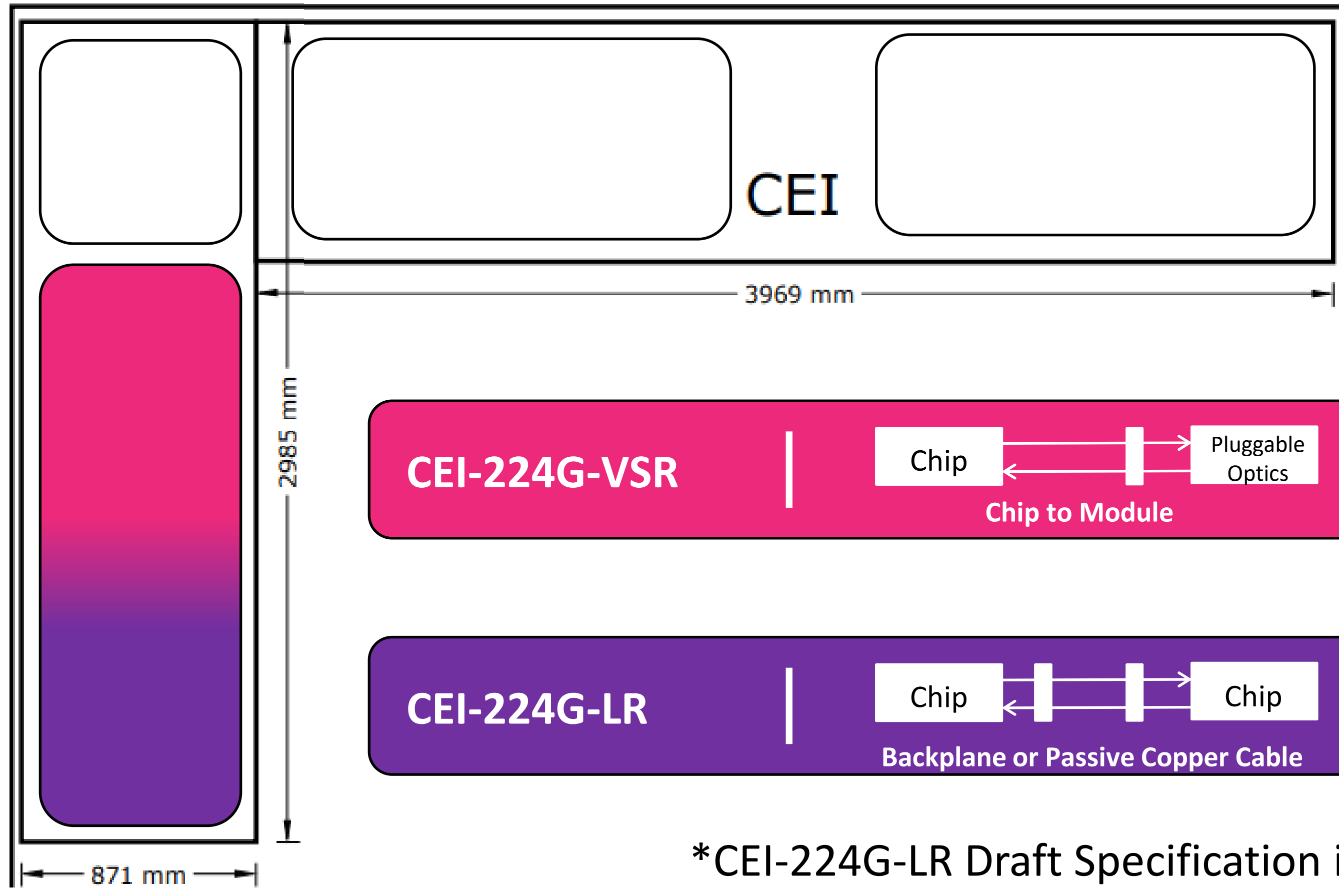
CEI-224G at ECOC 2023



CEI-224G-VSR

Chip → Pluggable Optics

Chip to Module

- 200mm of host, 20mm of module
- 1 connector
- 1e-15 or lower (FEC is allowed)

CEI-224G-LR

Chip → Chip

Backplane or Passive Copper Cable

- 1000mm of host and daughter cards
- 2 connectors
- 1e-15 or lower (FEC is allowed)

CEI-224G-LR Draft Specification is currently in review for OIF members

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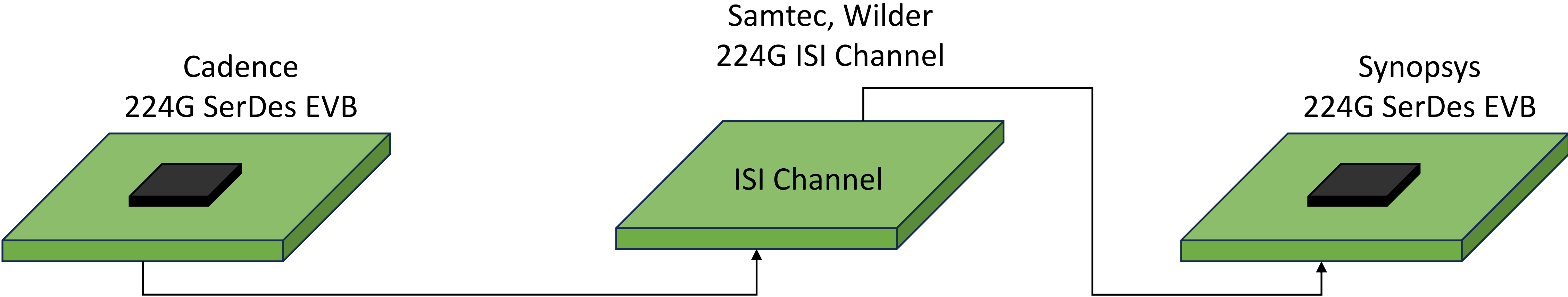
CEI-224G-VSR at ECOC 2023



This VSR interoperability demonstration consists of the first multivendor interoperability at 224G, with test chip silicon sending bi-directional PRBS31Q PAM4 212.5 Gbps signals over an ISI test board, with a die-to-die insertion loss of 29 dB. This is a building block for enabling Chip to Module channels, such as a switch ASIC to front panel pluggables, driving 1.6T connectivity.

CEI-224G-VSR | Chip → Pluggable Optics — **Chip to Module** | **200mm of host, 20mm of module**
1 connector
1e-15 or lower (FEC is allowed)

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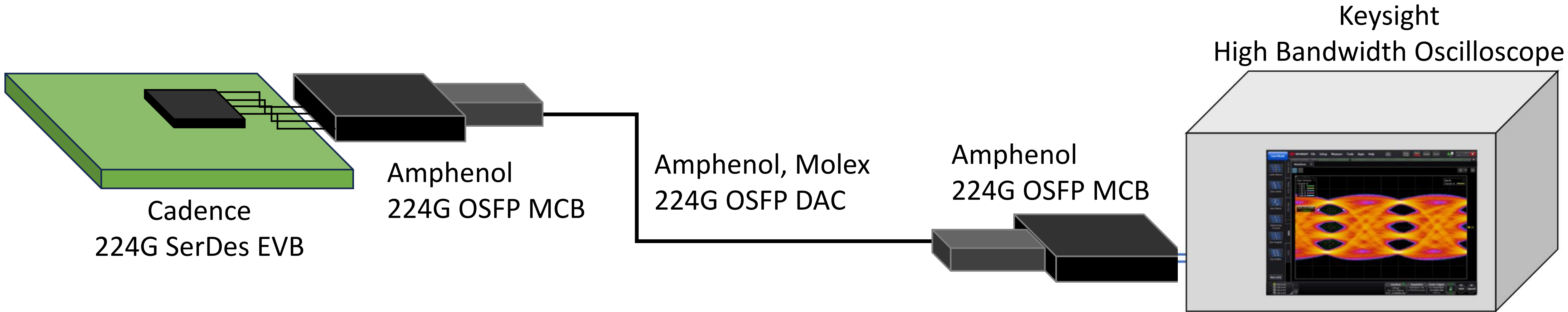
CEI-224G-LR at ECOC 2023



This LR demonstration is an operational showcase of test chip silicon sending a PRBS13Q PAM4 200 Gbps signal over a 1 meter OSFP DAC and break-out test fixturing, totaling 35 dB of insertion loss, ultimately terminated by an oscilloscope depicting a far-end recovered eye diagram. This is a building block for enabling system to system interoperability links, driving 1.6T connectivity.

CEI-224G-LR

Backplane or Passive Copper Cable

1000mm of host and daughter cards
2 connectors
1e-15 or lower (FEC is allowed)

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