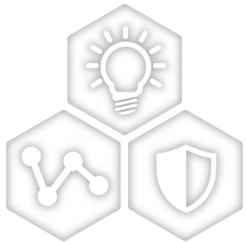




448G Modulation Proposal



A Leading Provider of Smart, Connected and Secure Embedded Control Solutions



Overview

- **Motivation**
- **PAM4m5 Modulation**
- **Alphabet Construction**
- **448G PAM6m8**
- **Summary**

Motivation

- **Channel loss for 448G channels over copper is challenging**
- **PAM6 at Nyquist=89.6 GHz and PAM8 at Nyquist=74.66 GHz are best current candidates**
 - Even here the proposed channels have difficult insertion loss
- **Maintain the following**
 - Continue using the standard Differential Pair wiring
 - No additional throughput loss (target 448G operation)
 - No changes to clocking or clock rates
 - Maintain current TX and RX architectures
 - DAC based TX
 - AFE + ADC + DSP based receiver
- **Add a Soft FEC as another DSP option**
 - DFE or MLSE or Soft FEC

Motivation: Soft FEC

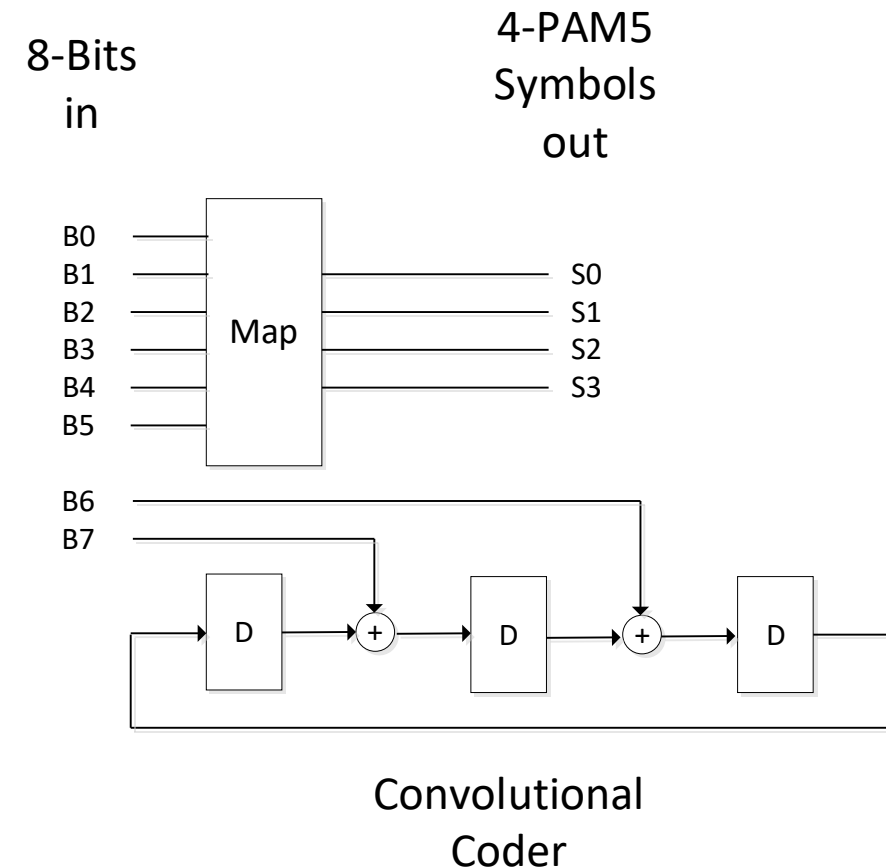
- Entangle the DFE channel with a Soft FEC
- Target to reduce the Pre-KP FEC Symbol Error Rate (SER) by 2 or more decades
- **Latency Target**
 - KP FEC is 5440 bits + t15 RS Decoding
 - Previous discussions permitted 2x and even 4x interleaving of KP FEC
 - Set soft FEC target latency at (0.25 to 1.0) x 5440 bits
- **Gates are efficient**
 - 3 nm or lower geometry
 - Gates/unit area continues to scale favorably
 - Try not to use SRAM as this does not scale well
- **Cooperates well with following KP FEC**
- **Follow Receiver Progression**
 - Analog Sampler Based DFE → ADC+DSP → ADC+DSP+SoftFEC

PAM4m5 Modulation

- **PAMXmY Modulation**
 - X represents the Baud rate PAM levels
 - Y represents the actual levels used
 - Baud rate is determined by PAM4 modulation with additional levels from PAM5 used by FEC
- **Signal Levels**
 - PAM4 $\{-3,-1,+1,+3\}$
 - PAM5 $\{-2,-1,0,+1,+2\}$
 - Power needs to be scaled appropriately so that average TX power matches PAM4
 - For discussion we keep these levels
- **Combine multiple PAM5 symbols to give us extra bit(s) for use by FEC**
 - 4 Symbols together provide 9 bits of information
 - 4 Symbols of PAM5 gives 625 possibilities
 - Use 512 of them to give us 9 bits of information
 - The extra bit can be used by a FEC (8/9 code rate)

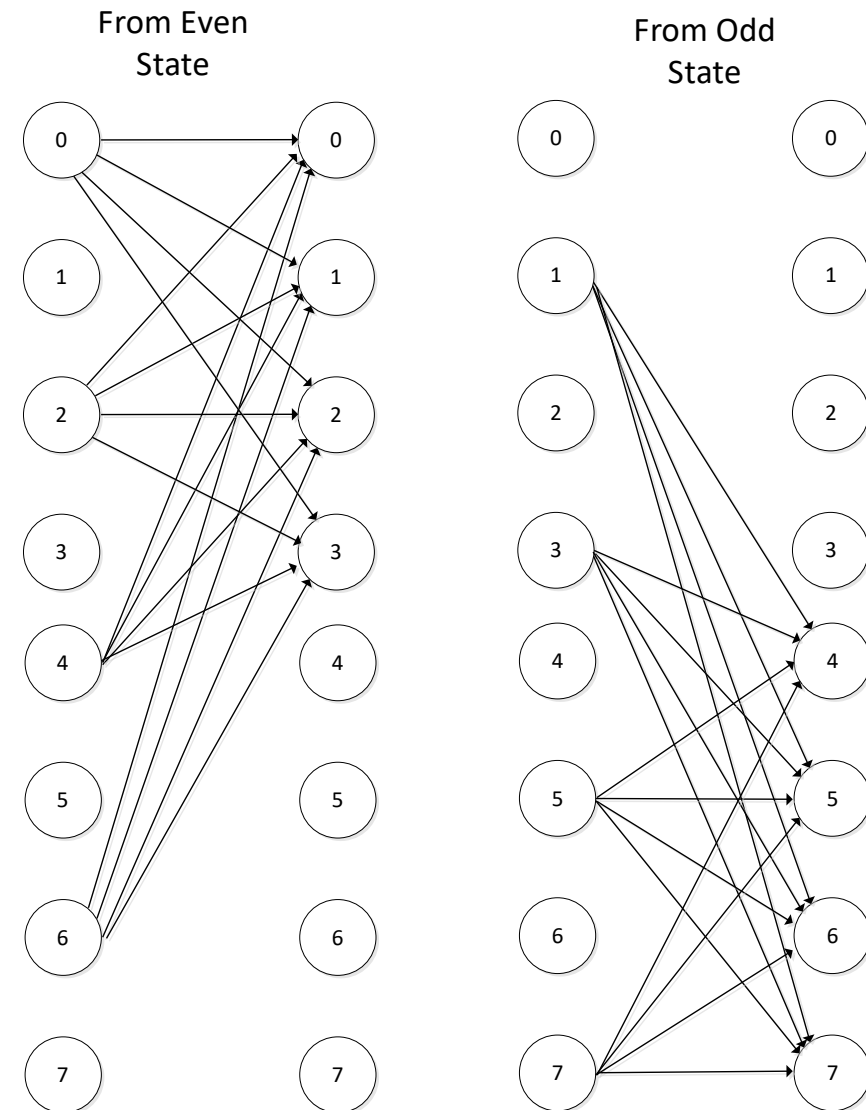
PAM4m5 Convolutional Coding (CC)

- 8-bits of information to generate 4 PAM5 symbols
- 2-bits to drive an encoding state
- 6-bits to drive the mapping of the PAM5 signals
- Define a Symbol Group (SG) as 4 consecutive PAM5 symbols conveying 9-bits of information
- Leads to an 8-state Encoder (8-state trellis)



Convolutional Coding: Trellis

- 8 state trellis
- Each state has 4 inputs
- Define a Transition Group (TG) as collection of 64 SGs that define an arc in the trellis
- Even numbered states are connected to states 0,1,2 and 3 (4 different TGs)
- Odd numbered states are connected to states 4,5,6 and 7 (4 different TGs)
- 8 different TGs are needed ($8*64=512$)
- Define the alphabet as the full set of 8 TGs



Alphabet Selection

- **Alphabet Optimization**

- Find the best Alphabet to give the lowest SER performance
- Several revisions of customized NP-Complete solver

- **Ideal Alphabet rules**

- DC Offset is 0 (DC)
 - Maintain DC balance without any other circuitry
- Nyquist transitions are minimized (-2 to 2 or 2 to -2) (NYQ)
 - Minimize the use of full BW transitions
- Minimize Average TX Power Consumption (PWR)
 - Lower Average TX power for best SNR

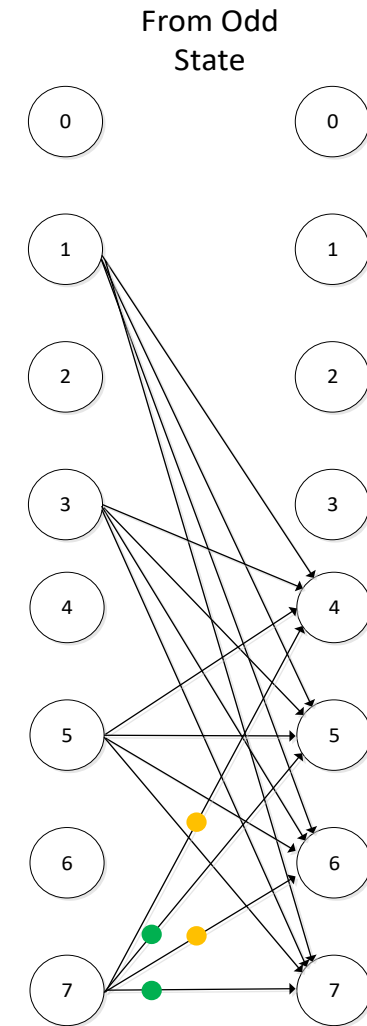
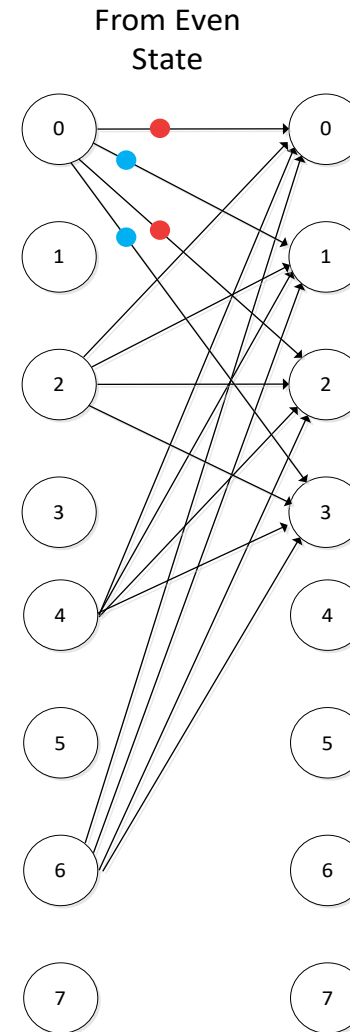
Alphabet Selection (cont)

- **Ideal Alphabet rules**

- Remove all full SG DFE propagation errors in one TG
 - DFE errors are known to propagate in an alternating pattern of +1,-1,+1,-1
 - Zig = (+1,-1,+1,-1)
 - Zag = (-1,+1,-1,+1)
 - No two elements within one TG can differ by a Zig or a Zag (ZZ)
- Remove all 3-symbol DFE propagation errors in one TG
 - (+1,-1,+1,x) or (-1,+1,-1,x) or (x,+1,-1,+1) or (x,-1,+1,-1)
- Squared distance of all elements within a TG is >2 (D)
 - Distance between SGA and SGB
 - $(S0A-S0B)^2 + (S1A-S1B)^2 + (S2A-S2B)^2 + (S3A-S3B)^2$
- Squared distance between alternate TG pairs is ≥ 2 (Alternate Distance (AD))

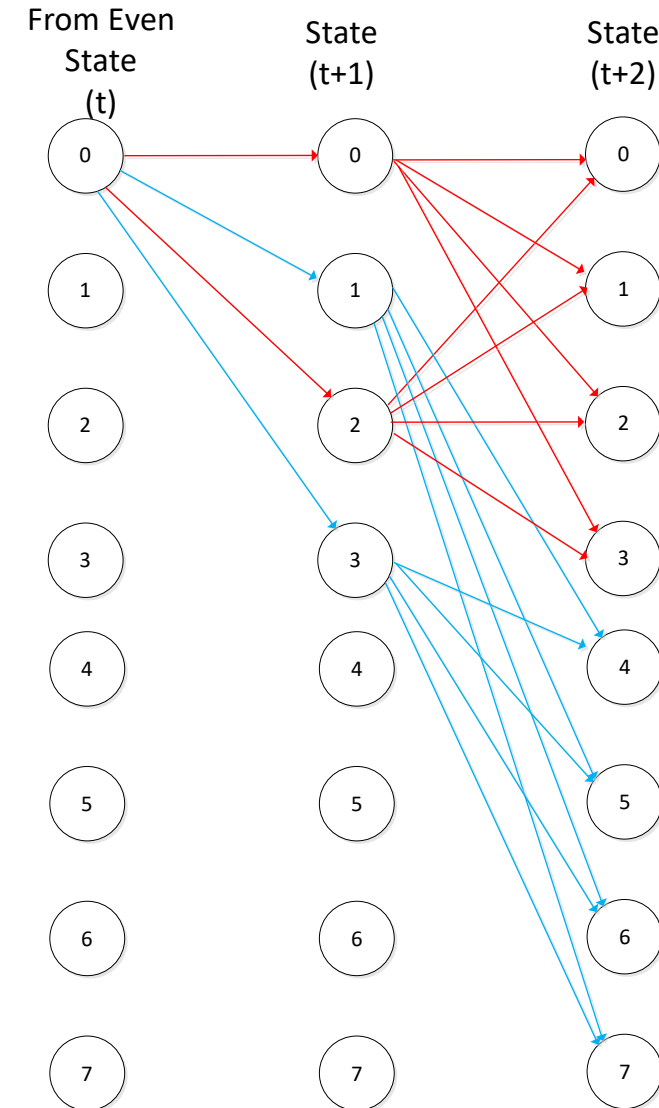
Alphabet Selection (cont)

- **Trellis Convergence gives us one more rule**
- **Squared distance between alternate TG pairs is ≥ 2 (AD)**
 - Ie. All elements of TG0 and TG2 have a minimum distance of at least 2
- **Divide the 8 TGs into 4 pairs as indicated by different colored pairs**
- **Note the 4 TGs entering each state will be different**
 - Same TGs used by even states but rotated in 4 different ways



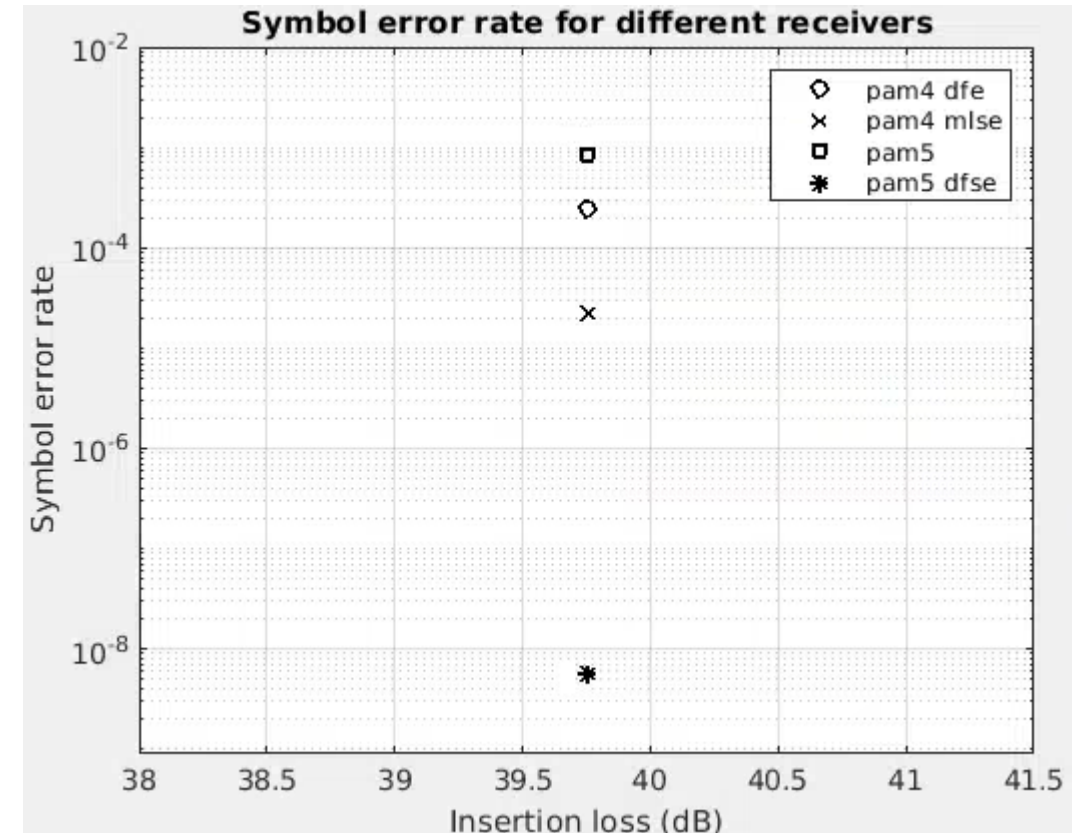
Alphabet Selection: Trellis Convergence

- **Why enforce AD rule?**
- **Red transitions from state 0 at time t can reconverge at time t+2**
 - States 0 through 3
- **Blue transition from state 0 at time t also compete at time t+2**
 - States 4 through 7
- **Red vs. Blue starting from time t cannot reconverge until at least time t+3**
 - Trellis itself will keep alternate colors apart longer



PAM4m5 Proof of Concept (POC) Performance

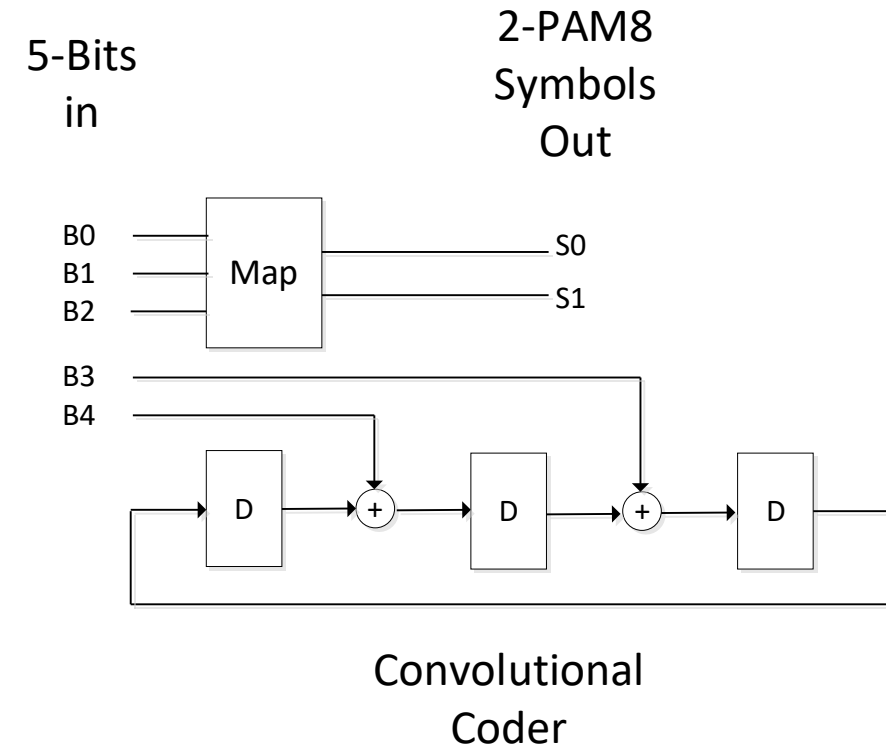
- **39.75 dB IL Channel, with standard AFE, ADC and DSP operation**
 - Same receiver used for each case with FFE and DFE taps adapted appropriately.
 - Tested at 128 Gbps
- **Native PAM5**
 - Nyquist scaled lower by 8/9 running classical DFE receiver
- **Native PAM4**
 - Receiver struggling to meet SER=1e-4
- **PAM4 MLSE receiver shows ~20x Ser improvement (~1.6 dB)**
- **PAM5 DFSE (Decision Feedback Sequence Estimation) receiver**
 - Alphabet “3a” shows good performance
 - Enhanced CC receiver operation



Operation at 448G

- **PAM6m8**

- Baud rate according to PAM6 (89.6 GHz Nyquist) modulation at PAM8
- SG is 2 symbols long
- Each TG has 8 elements (encode 3 bits)
- 8-state trellis requiring 8 TGs
 - 64 elements in the Alphabet
 - No free space in this case, all 64 possibilities for 2 PAM8 symbols will be used.
- Code Rate is 5/6 (5 bits in 6 bits out)



448G Alphabet

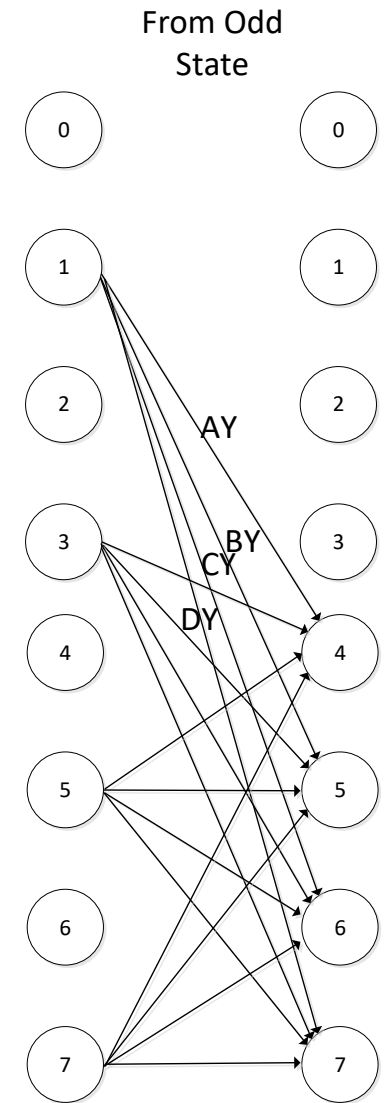
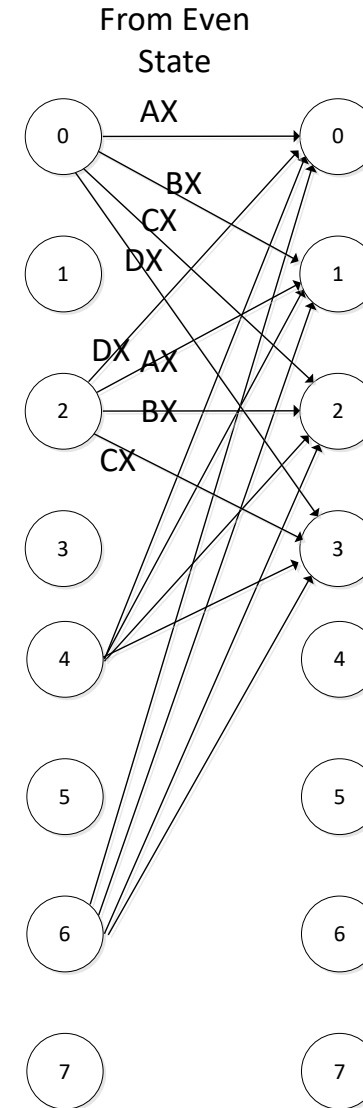
- **Some properties not available for optimization**
 - DC, PWR, NYQ (All available patterns used)
- **PAM8 levels**
 - $\{-7, -5, -3, -1, +1, +3, +5, +7\}$
- **Divide Symbols into two sets PAM2 and PAM4**
 - PAM2
 - Distance of 4 levels between alternates
 - $A=\{-7, +1\}$, $B=\{-5, +3\}$, $C=\{-3, +5\}$, $D=\{-1, +7\}$
 - Encodes 1 bit of information
 - PAM4
 - Distance of 2 levels between alternates
 - $X=\{-7, -3, +1, +5\}$, $Y=\{-5, -1, +3, +7\}$
 - Encodes 2 bits of information

448G Alphabet (cont)

- **Each 2 symbols must carry 3-bits of information**
 - One symbol is ABCD (1-bit)
 - One symbol is XY (2-bits)
- **For Alternate Distance we use the following pairs**
 - A with C and B with D
- **Full transition table is shown**
 - Use of TGs rotates for each even or odd pair
 - Make sure that all 4 TGs entering a state are different

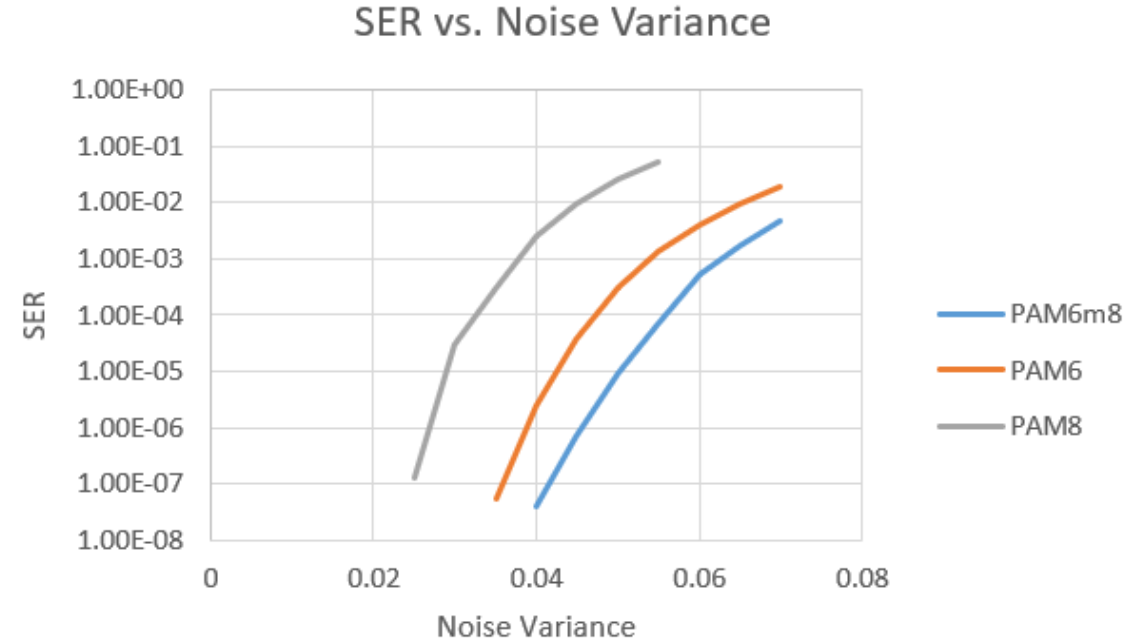
Transition Table

From	To	TG
0	0	AX
0	1	BX
0	2	CX
0	3	DX
1	4	AY
1	5	BY
1	6	CY
1	7	DY
2	0	DX
2	1	AX
2	2	BX
2	3	CX
3	4	DY
3	5	AY
3	6	BY
3	7	CY
4	0	CX
4	1	DX
4	2	AX
4	3	BX
4	4	CY
4	5	DY
5	6	AY
5	7	BY
6	0	BX
6	1	CX
6	2	DX
6	3	AX
6	4	BY
6	5	CY
6	6	DY
6	7	AY



PAM6m8 Results

- **Test with 1-tap DFE channel**
 - $1+D*0.875+\text{noise}$
- **Test Cases**
 - PAM8 DFE
 - PAM6 DFE
 - PAM6m8 DFSE
- **Standard CC implementation**
- **Preliminary Coding gain for PAM6m8 vs. PAM6 is 1.5 dB**



Summary

- **Motivation**

- Add a low latency softFEC to the standard DSP receiver to improve efficiently improve receiver margin
- Use higher modulation levels to provide parity bits for FEC operation

- **PAM4m5**

- Promising proof of concept results showing 3+ decades of SER improvement over standard MLSE PAM4 receiver

- **PAM6m8**

- Initial work for standard CC receiver at 448G presented

- **Future Work**

- 6m8 Alphabet Exploration
- Enhanced CC decoder to improve performance
- Operation at 74.66GHz

Thank You
