



Connector Study and Concept

SI performance and Routing Length of VLC-PCB for 448G

April 14, 2025 YAMAICHI ELECTRONICS CO., LTD. Toshiyasu Ito

OIF 448Gbps Signaling for AI Workshop April 15-16, 2025



Abstract:

Basically I will explain of the connector and high speed routing of PCB by the VLC(Vertical Line Card) structure for 448G.

VLC is a structure that uses a vertical line card. See page 13.

The OSFP connector and cage are mounted vertically on the front side of the board, and the ASIC package is mounted on the back side or other Vertical PCB.

This brings the connector and package closer together, allowing for a shorter distance for high-speed signal wiring.

We mainly studied the possibility of 448G by High speed routing of PCB.

Contributions of Touchstone: Included Documentation

- OIF2025.137.00 Touchstone of VLC-OSFP connector for 448G - it will be uploaded end of April
- OIF2025.138.00 Touchstone of 2D connector for 448G - it will be uploaded end of April
- OIF2025.139.00 Touchstone of VLC-OSFP-XD connector for 448G - it will be delayed

Supporters:

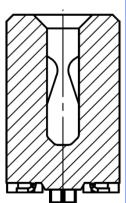
Chris Cole, Coherent Corp. Peter Winzer, Nubis Communications Toshiaki Sakai, Socionext OIF 448Gbps Signaling for AI Workshop April 15-16, 2025

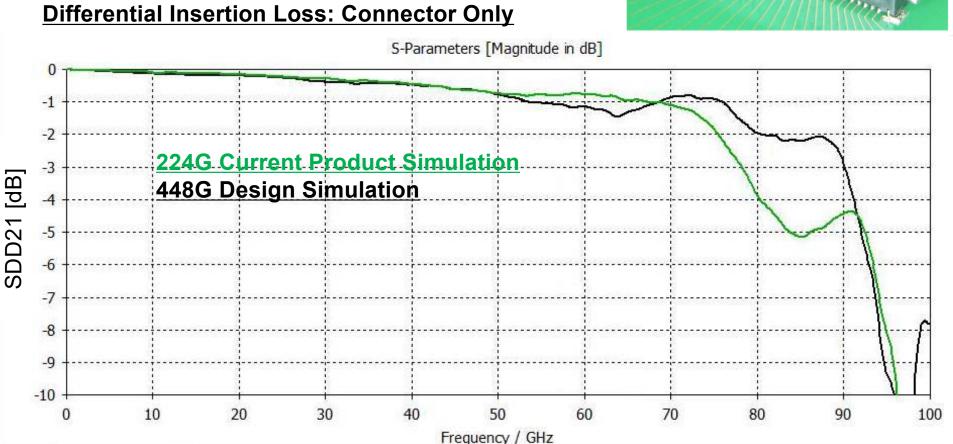
VLC-OSFP Connector for 448G

- Vertical Mounted OSFP Connector Simulation
- Connector have same pin mapping of OSFP.
- Connector Impedance is 92.5 ohm now.

Current OSFP-OSFP Connector

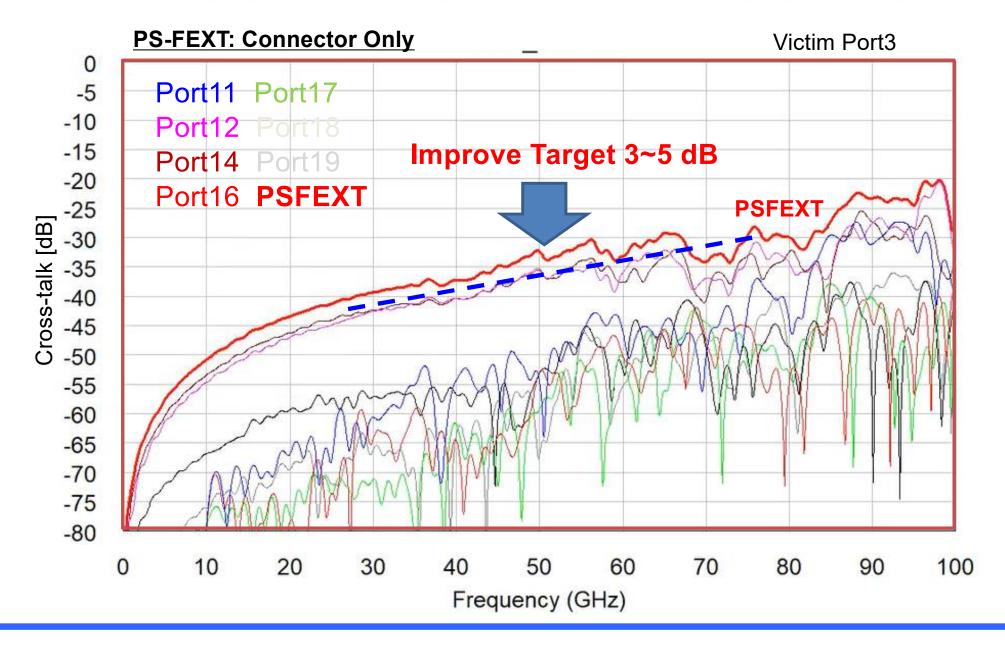








)		-			-		-							
GND		1	GND	2	GND	3	GND	4	GND	CNT	GND	5	GND	
GND	2	6	GND	7	GND	8	GND	9	GND	CNT	GND	10	GND	Victim
GND	2	11	GND	12	GND	13	GND	14	GND	CNT	GND	15	GND	Aggrossor
GND	D I	16	GND	17	GND	18	GND	19	GND	CNT	GND	20	GND	Aggressor

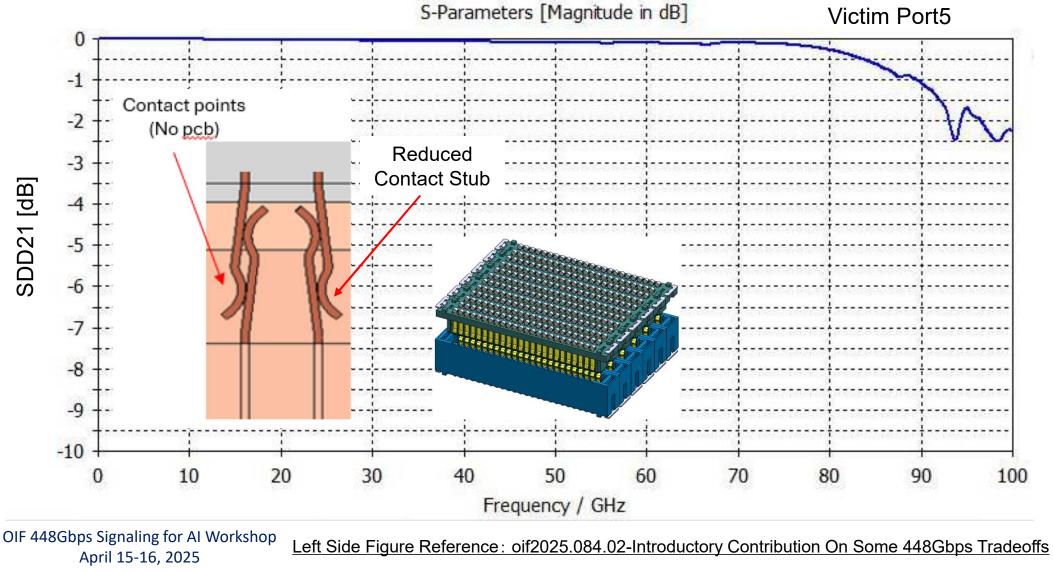




2D Connector for 448G

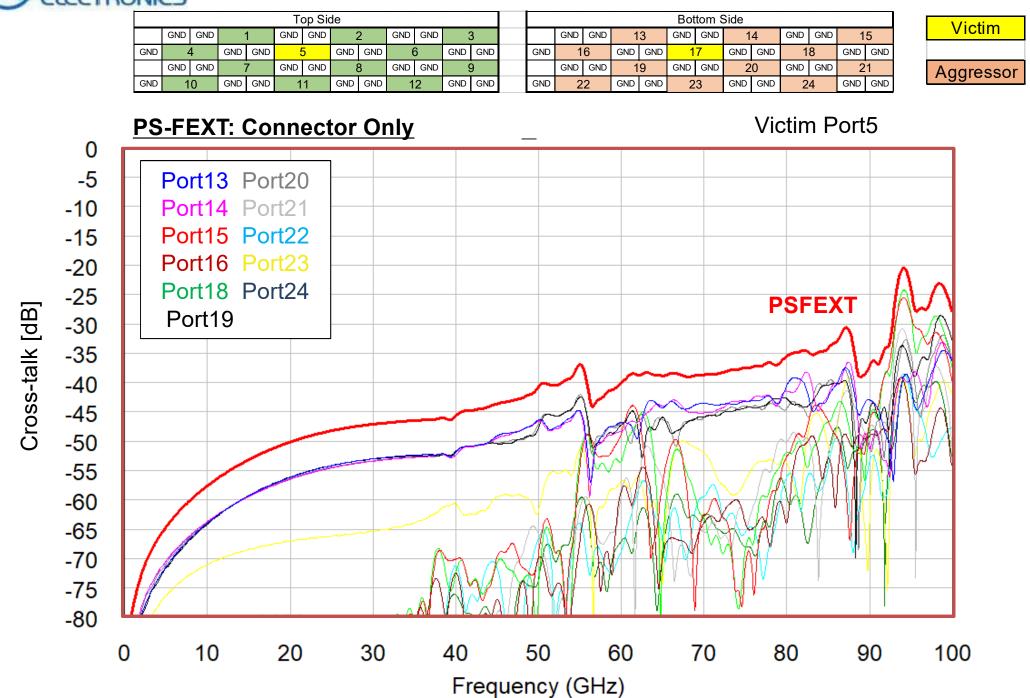
- Tuning of Yamaichi Original 2D Connector Simulation
- Connector Impedance is 92.5 ohm now.

Differential Insertion Loss: Connector Only



A YAMAICHI ELECTRONICS

Page 6



Reference: 224G-VSR Calculation Result

- This calculation is reference to check for Cross talk and other parameters by 224G specification.
- The COM default host and module PCB models were added to the connector stand-alone characteristics and calculated as a channel model.
- Connector model is simulation based.
- Channel model doesn't included the via model..

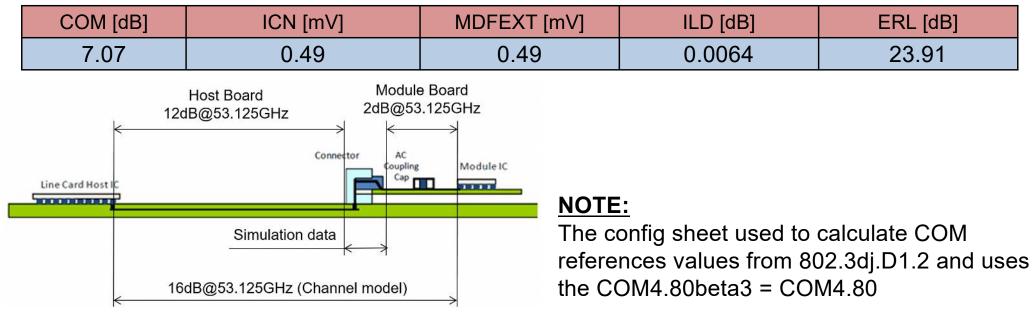
VLC-OSFP

Include 7FEXT and 2NEXT

COM [dB]	ICN [mV]	MDFEXT [mV]	MDNEXT [mV]	ILD [dB]	ERL [dB]
6.01	1.20	1.20	0.06	0.024	14.28

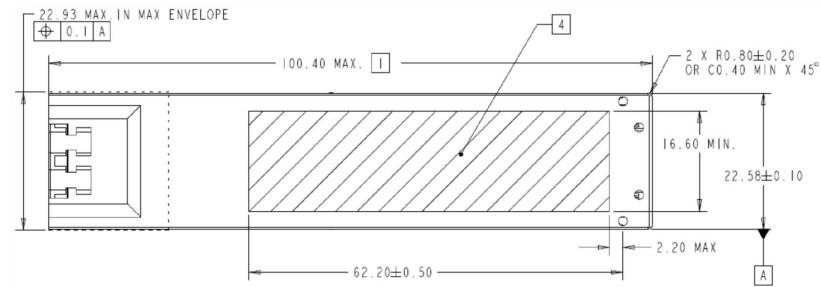
2D Connector

Include 11FEXT



Page 8 Standard Module: OSFP-RHS : 8 lanes (16 Differential Pairs/ DP)

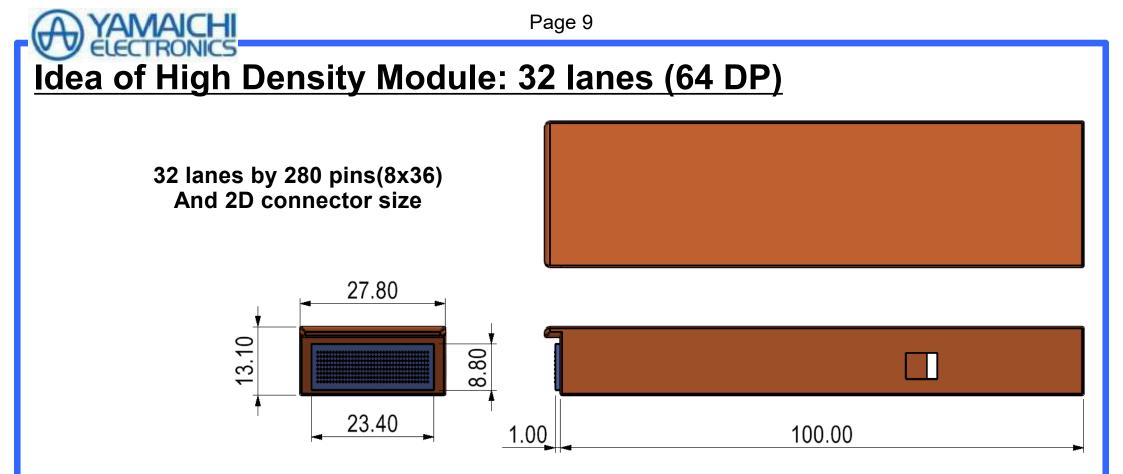
Reference: OSFP Module Specification Rev5



Standard Module: OSFP-XD-RHS : 16 lanes (32 DP)

- (|22.87) -- 22.98 MAX. FOR ENVELOPE || — 16.60 MIN. \oplus 0.1 A 2 X R0.80 OR CO.40 MIN X 45° Φ Θ θ 22.58 ± 0.10 ø O 2.20 MAX. ----**OIF 448Gbps Si** В -62.40 ± 0.50 Apri

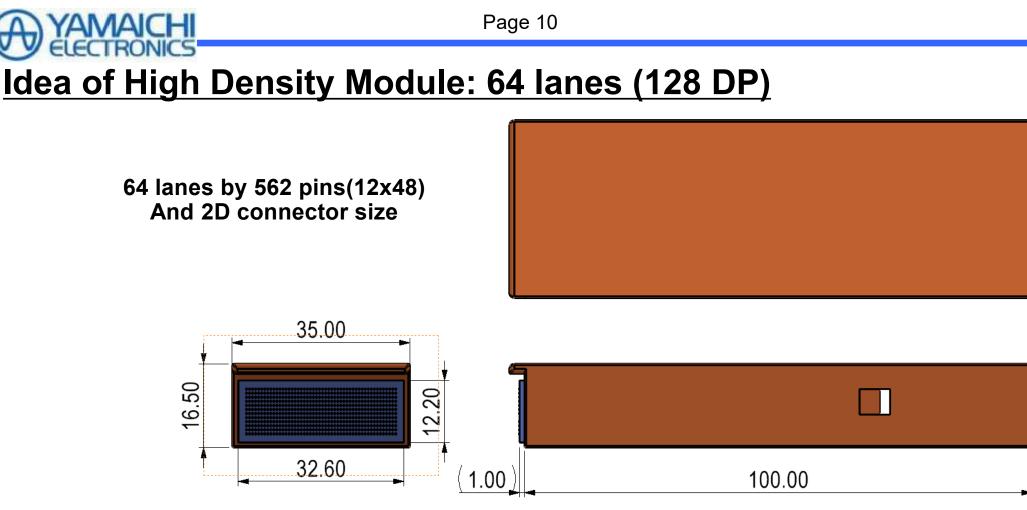
Reference: Specification for OSFP-XD Rev 1.07



- PWR=12 pins, Control=4 pins

	1	2 3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34 35	36
1		GND GND	-	Гх	GND	GND	1	Гх	GND	GND	T:	х	GND	GND	Т	x	GND	PWR	PWR	GND	GND	R	x	GND	GND	R	X	GND	GND	R	ĸ	GND	GND	Rx	GND
2	GND	Тx	GND	GND	Т	x	GND	GND	Tx	(GND	GND	T.	x	GND	GND	PWR	PWR	GND	F	Rx 🛛	GND	GND	R	х	GND	GND	R	x	GND	GND	R	x	GND GND)
3		GND GND	-	Гх	GND	GND	1	Гх	GND	GND	T:	х	GND	GND	Т	x	GND	Cnt	PWR	GND	GND	R	x	GND	GND	R	X	GND	GND	R	ĸ	GND	GND	Rx	GND
4	GND	Тx	GND	GND	T	x	GND	GND	Tx	(GND	GND	T	x	GND	GND	Cnt	Cnt	GND	F	8x	GND	GND	R	х	GND	GND	R	x	GND	GND	R	x	GND GND)
5		GND GND	-	Гх	GND	GND	1	Гх	GND	GND	T:	х	GND	GND	Т	x	GND	Cnt	PWR	GND	GND	R	x	GND	GND	R	X	GND	GND	R	ĸ	GND	GND	Rx	GND
6	GND	Тx	GND	GND	T	x	GND	GND	Tx	(GND	GND	Т	x	GND	GND	PWR	PWR	GND	F	8x	GND	GND	R	х	GND	GND	R	x	GND	GND	R	x	GND GND)
7		GND GND	-	Гx	GND	GND	٦	Гх	GND	GND	T:	x	GND	GND	Т	x	GND	PWR	PWR	GND	GND	R	x	GND	GND	R	x	GND	GND	R	ĸ	GND	GND	Rx	GND
8	GND	Tx	GND	GND	T	x	GND	GND	Тх	(GND	GND	T	x	GND	GND	PWR	PWR	GND	F	Rx	GND	GND	R	x	GND	GND	R	lx 🛛	GND	GND	R	x	GND GNE)

OIF 448Gbps Signaling for AI Workshop April 15-16, 2025



- PWR=17 pins, Control=7 pins

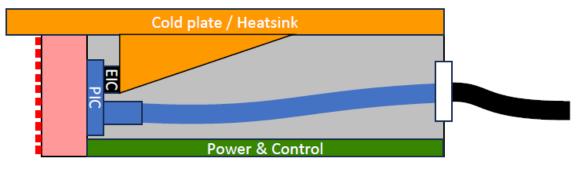
	1	2	3	4	5	6	7 8	9	10	11	12	13	14	15 1	6 17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34 35	36	37	38 39	40 41	42 43	44	45	46 47	48
1		GND	GND	Т	x	GND G	ND	Tx	GND	GND	Tx	0	GND (GND	Tx	GND	GND	T:	x	GND	PWR	PWR	PWR	PWR	PWR	GND	GND	Rx	(GND	GND	Rx	GND	GND	Rx	GND GND	Rx	GND	GND	Rx	GND
2	GND	-	Tx	GND	GND	Тx	GN	GND	T	x	GND (GND	Tx	G	ID GN	D '	Тx	GND	GND	PWR	PWR	PWR	PWR	PWR	GND	R	x	GND	GND	R	<	GND GNE) F	Rx	GND GND	Rx	GND GNE	R	x	GND GND	۲ ر
3		GND	GND	Т	x	GND G	ND	Tx	GND	GND	Tx	0	GND (GND	Tx	GND	GND	T	x	GND	GND	GND	GND	R	x	GND	GND	Rx	(GND	GND	Rx	GND	GND	Rx	GND GND	Rx	GND	GND	Rx	GND
4	GND	-	Тх	GND	GND	Тx	GNE	GND) T	x	GND (GND	Тx	G	ID GN	D .	Ťх	GND	GND	Т	x	GND	Cnt	GND	GND	R	x	GND	GND	R	(GND GNE) F	- Rx	GND GND	Rx	GND GNE	R	x	GND GND	ر د
5		GND	GND	Т	x	GND G	ND	Тх	GND	GND	Tx	0	GND (GND	Тx	GND	GND	T:	х	GND	GND	Cnt	GND	R	x	GND	GND	Rx	(GND	GND	Rx	GND	GND	Rx	GND GND	Rx	GND	GND	Rx	GND
6	GND	-	Tx	GND	GND	Тx	GNE	GND) T	x	GND (GND	Тx	G	ID GN	D	Тх	GND	GND	Т	x	GND	Cnt	GND	GND	R	x	GND	GND	R	(GND GND	P F	٦x	GND GND	Rx	GND GNE	R	x	GND GND	2 V
7		GND	GND	Т	x	GND G	ND	Тх	GND	GND	Tx	0	GND (GND	Tx	GND	GND	T:	x	GND	GND	Cnt	GND	R	x	GND	GND	Rx	(GND	GND	Rx	GND	GND	Rx	GND GND	Rx	GND	GND	Rx	GND
8	GND	-	Tx	GND	GND	Тx	GN) GND	D T	x	GND (GND	Tx	Gl	ID GN	D '	Тх	GND	GND	Т	x	GND	Cnt	GND	GND	R	x	GND	GND	R	(GND GND) F	Rx	GND GND	Rx	GND GND	R	x	GND GND	2
9		GND	GND	Т	x	GND G	ND	Тx	GND	GND	Tx	G	GND (GND	Tx	GND	GND	T:	x	GND	GND	Cnt	GND	R	x	GND	GND	Rx	(GND	GND	Rx	GND	GND	Rx	GND GND	Rx	GND	GND	Rx	GND
10	GND	-	Тх	GND	GND	Тx	GNE	GND	T	x	GND (GND	Tx	G	ID GN	D	Ťх	GND	GND	T	x	GND	Cnt	GND	GND	R	x	GND	GND	R	(GND GND) F	Ŕx	GND GND	Rx	GND GNE	R	x	GND GND	ر د
11		GND	GND	Т	x	GND G	ND	Tx	GND	GND	Tx	Ģ	GND (GND	Tx	GND	GND	T:	x	GND	GND	GND	GND	PWR	PWR	GND	GND	Rx	(GND	GND	Rx	GND	GND	Rx	GND GND	Rx	GND	GND	Rx	GND
12	GND	-	Tx	GND	GND	Тx	GNE	GND	T	x	GND (GND	Tx	G	ID GN	D	Тх	GND	GND	PWR	PWR	PWR	PWR	PWR	GND	R	x	GND	GND	R	<	GND GNE	F	٦x	GND GND	Rx	GND GNE	R	x	GND GND	ر د
C)IF	448	8Gb	bbs :	Sign	nalin	g for	' AI	Wo	rksł	nop																														

April 15-16, 2025

Inside Structure of High Density Module

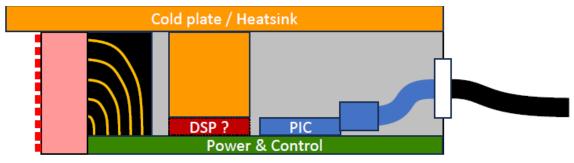
Vertically mounted chips with optical surface coupling:

- SI performance will be better.
- Is there enough space for mounting of PIC?
- Heat dissipation of PIC and EIC.



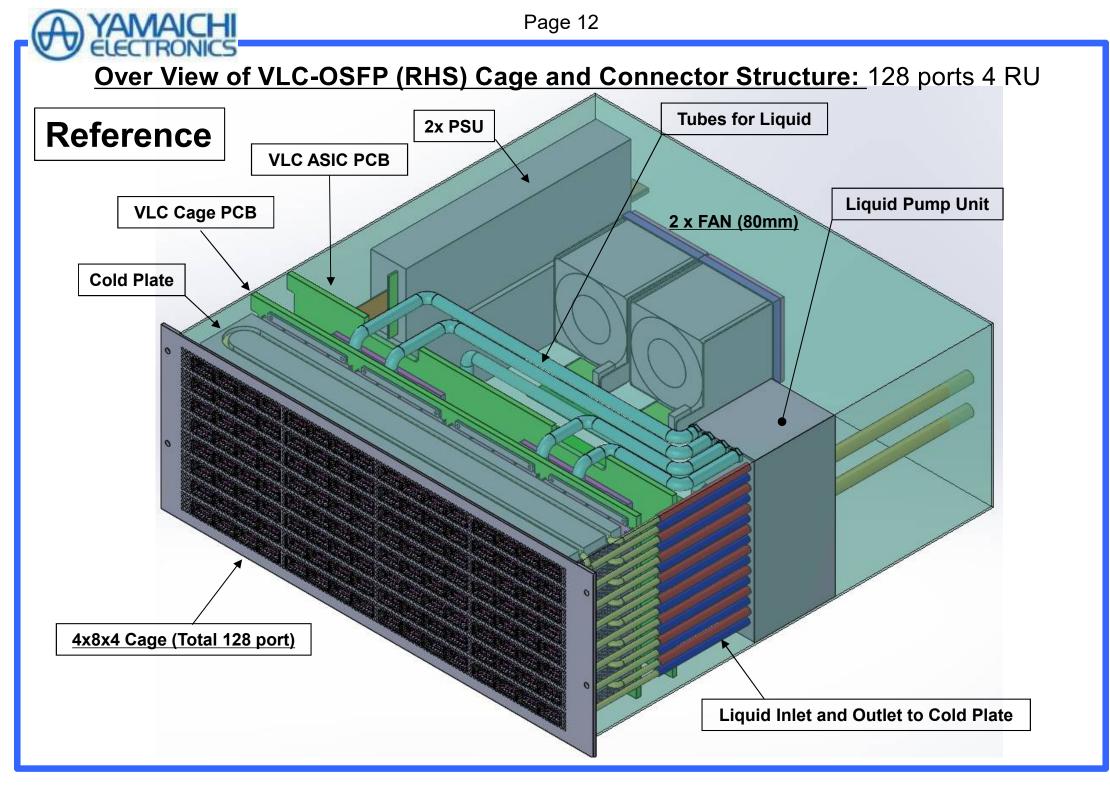
Horizontally mounted chips /Right angle terminal to module PCB:

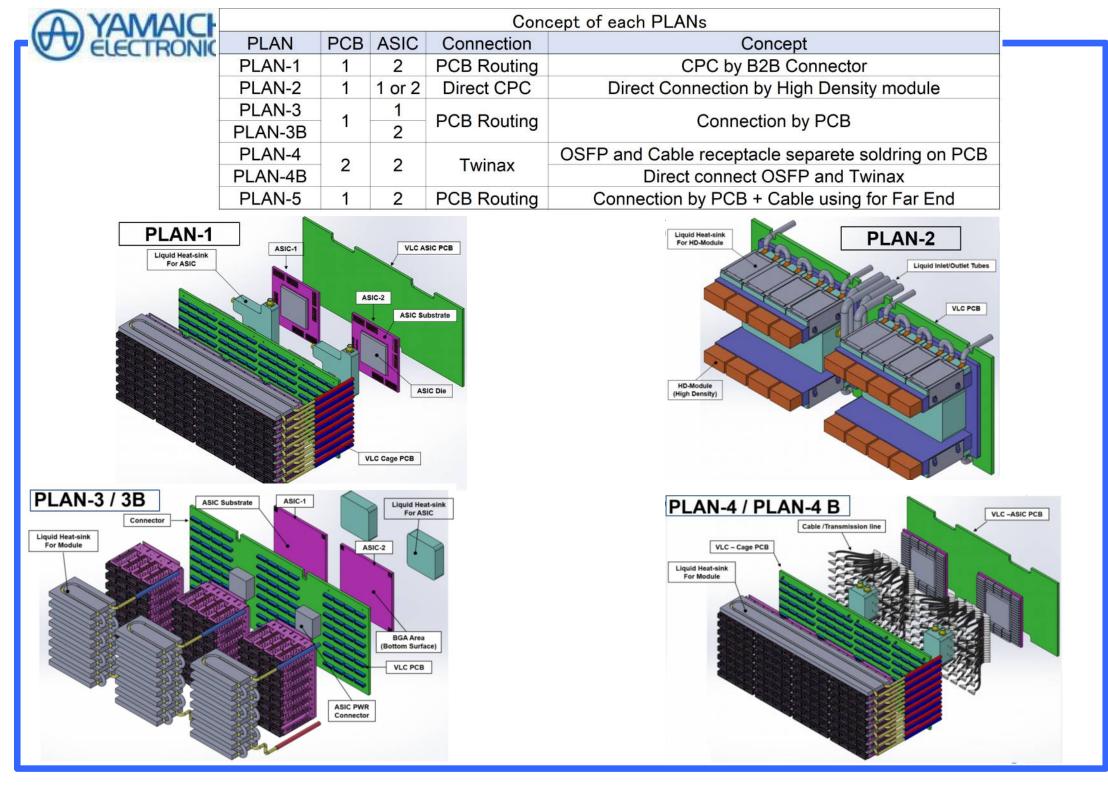
- Right angle terminal will be worse for Insertion loss and Cross-talk Probably Insertion loss will be plus 2~3dB.
- Is there enough Insertion loss of module PCB?



OIF 448Gbps Signaling for AI Workshop April 15-16, 2025

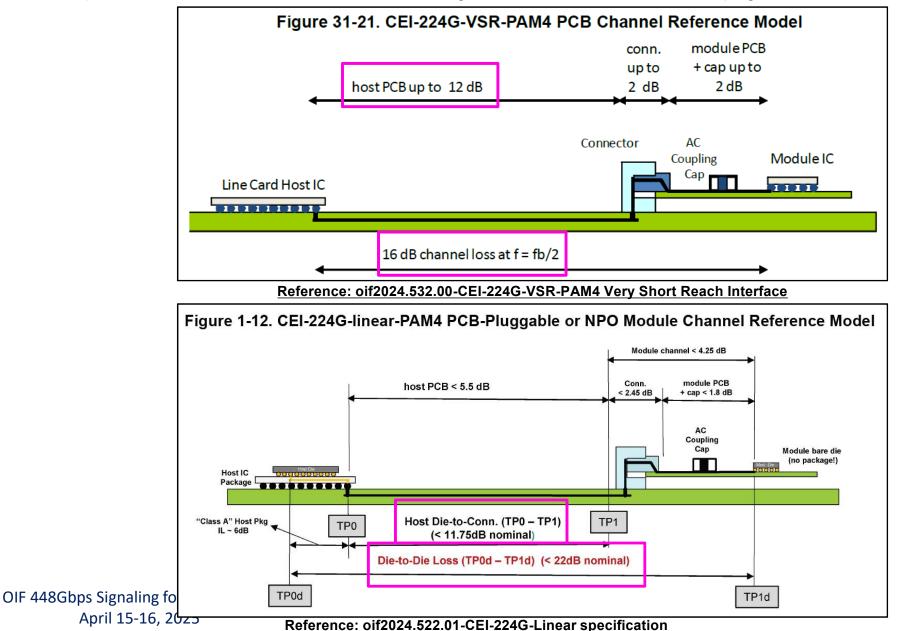
Reference: oif2025.010.02-High Density Connector - Sizing Considerations





Page 14 <u>Target Insertion loss of Host PCB Loss and Channel Loss for Reference</u>

- Target of maximum insertion loss of host PCB and channel loss was referred to CEI-224G-VSR and Linear.
- I compared Insertion loss and Transmission length as each PLANs after next page.





Comparison of PLANs vs Insertion loss (Upper Side is better)

- Table shows the host PCB and channel insertion loss of **longest line** for each PLAN at 74 GHz and 89 GHz.
- This includes PCB routing, connectors, vias, and module PCB+AC-CAP line lengths and insertion losses.
- Material insertion loss has a large effect.

		ト	J								~10 dE	8 10~12	dB 120	dB∼		~14 dB	14~16	6dB 1	6dB∼
	Trans.	Longe	st Line	Line Lo	oss [dB]	Via Lo:	ss [dB]	CPC-1	CONN	CPC-2	CONN	Host PCB	Loss[dB]	OSFP	CONN	Module P	CB+CAP	Channel	Loss[dB]
PLAN	Material	mm	inch	74GHz	89GHz	74GHz	89GHz	74GHz	89GHz	74GHz	89GHz	74GHz	89GHz	74GHz	89GHz	74GHz	89GHz	74GHz	89GHz
PLAN-2	Right Angle	0.0	0.00	0.00	0.00							0.0	0.0	4	4.5	2	2	6.0	6.5
PLAIN-2	Mezzanine	0.0	0.00	0.00	0.00							0.0	0.0	2	2.5	2	2	4.0	4.5
	Low Loss	80.4	3.17	8.50	10.22	1.40	1.60					9.9	11.8	2	2.5	2	2	13.9	16.3
PLAN-5	Ultra Low	00.4	5.17	5.31	6.39	1.40	1.00					6.7	8.0	2	2.5	2	2	10.7	12.5
		80.0	3.15	2.11	2.54	1.40	1.60	1	1.5	2	2.5	6.5	8.1	2	2.5	2	2	10.5	12.6
PLAN-4	Cable	150.0	5.91	3.96	4.77	1.40	1.60	1	1.5	2	2.5	8.4	10.4	2	2.5	2	2	12.4	14.9
PLAN-4 B		150.0	5.91	3.96	4.61			1	1.5			5.0	6.1	3	3.5	2	2	10.0	11.6
PLAN-3 B	Low Loss	91.7	3.61	9.69	11.66	1.40	1.60					11.1	13.3	2	2.5	2	2	15.1	17.8
FLAN-5 D	Ultra Low	91.7	5.01	6.06	7.29	1.40	1.00					7.5	8.9	2	2.5	2	2	11.5	13.4
PLAN-1	Low Loss	56.5	2.22	5.97	7.18	1.40	1.60	3	3.5			10.4	12.3	2	2.5	2	2	14.4	16.8
FLAN-I	Ultra Low	50.5	2.22	3.73	4.49	1.40	1.00	3	3.5			8.1	9.6	2	2.5	2	2	12.1	14.1
PLAN-3	Low Loss	145.5	5.73	15.38	18.50	1.40	1.60				-	16.8	20.1	2	2.5	2	2	20.8	24.6
FLAN-5	Ultra Low	145.5	5.75	9.61	11.56	1.40	1.00					11.0	13.2	2	2.5	2	2	15.0	17.7

Material Insertion loss

(Refer: oif2024.532.00)

Material	dB/mm	Los	s per Inch	[dB]
IVIALEITAI	ud/IIIII	56GHz	74GHz	89GHz
Low Loss PCB	0.080	2.03	2.69	3.23
Ultra Low Loss PCB	0.050	1.27	1.68	2.02
Twinax Cable	0.020	0.508	0.67	0.81

Concept of each PLANs

PLAN	PCB	ASIC	Connection	Concept
PLAN-1	1	2	PCB Routing	CPC by B2B Connector
PLAN-2	1	1 or 2	Direct CPC	Direct Connection by High Density module
PLAN-3	1	1	PCB Routing	Connection by BCB
PLAN-3B	1.	2	PCB Routing	Connection by PCB
PLAN-4	2	2	Twinax	OSFP and Cable receptacle separete soldring on PCB
PLAN-4B	2	2	TWINAX	Direct connect OSFP and Twinax
PLAN-5	1	2	PCB Routing	Connection by PCB + Cable using for Far End

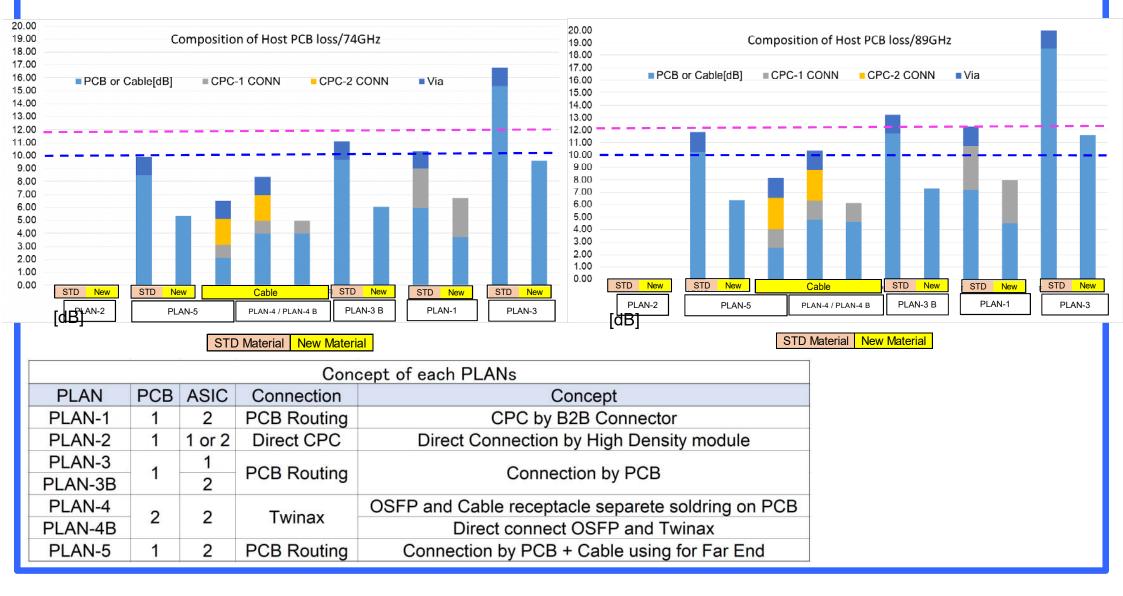
NOTE:

We will change the Host PCB Loss values by new materials of PCB and Cable at this Workshop and later.



PLAN Comparison of Host PCB loss (the plan on the left shows a low insertion loss)

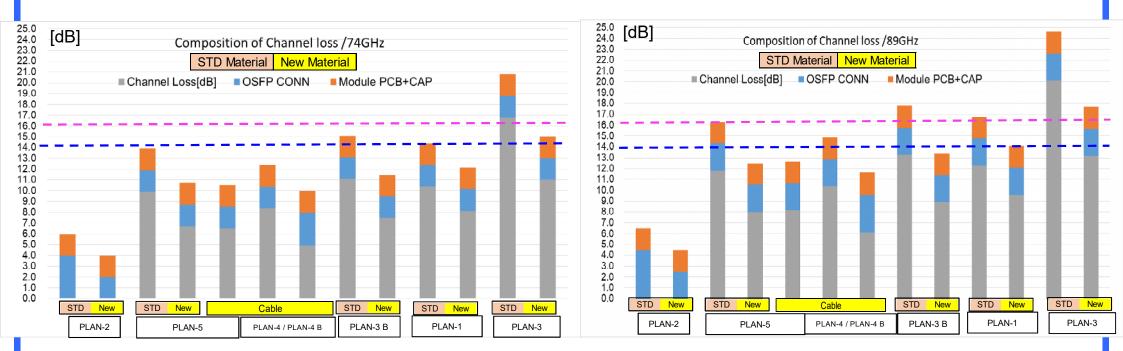
- This graph show Host PCB insertion loss at 74 GHz and 89 GHz.
- PLAN-2 (CPC with high-density modules) showed Zero lowest insertion loss.
- At 74 GHz, almost PLANs of the Host PCB are less than 12dB.
- The ultra-low loss PCBs except for PLAN-3 have a host PCB loss of 10 dB or less at 74GHz and 89 GHz.



(A) YAMAICHI

PLAN Comparison of Channel loss (the plan on the left shows a low insertion loss)

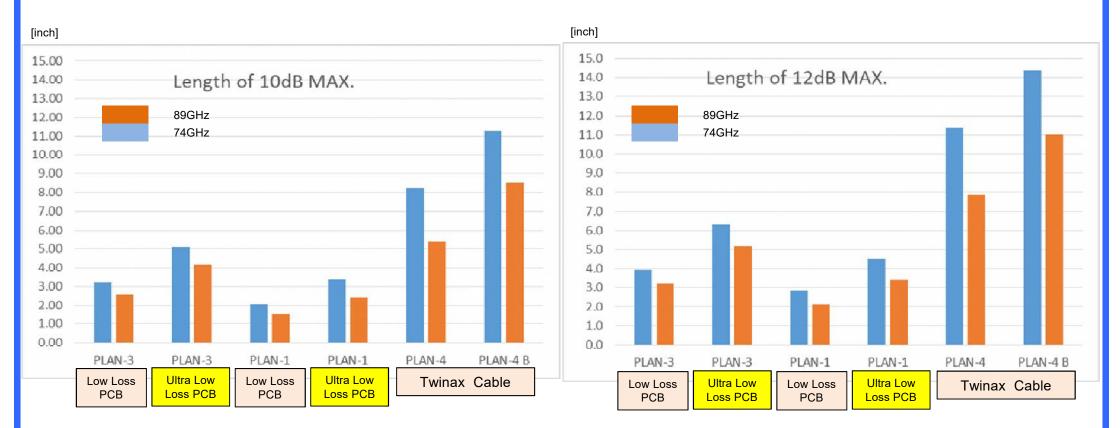
- This graphs show the Channel insertion loss at 74 GHz and 89 GHz.
- PLAN-2 (CPC with high-density modules) showed the lowest insertion loss.
- At 74 GHz, almost PLAN of the Channel insertion loss were less than 14dB.
- The ultra-low loss PCBs except for PLAN-3 have a Channel insertion loss of 12 dB or less at 89GHz.



			Cond	cept of each PLANs
PLAN	PCB	ASIC	Connection	Concept
PLAN-1	1	2	PCB Routing	CPC by B2B Connector
PLAN-2	1	1 or 2	Direct CPC	Direct Connection by High Density module
PLAN-3	1	1	PCB Routing	Connection by PCB
PLAN-3B		2	PCB Routing	Connection by PCB
PLAN-4	2	2	Twinax	OSFP and Cable receptacle separete soldring on PCB
PLAN-4B	Z	2	TWINAX	Direct connect OSFP and Twinax
PLAN-5	1	2	PCB Routing	Connection by PCB + Cable using for Far End

Host PCB/Cable Length of each plan at 10dB and 12dB of Host PCB Loss

- This graphs show PCB/Cable length at 10 dB and 12dB of Host PCB loss with each PLAN.



			Cond	cept of each PLANs
PLAN	PCB	ASIC	Connection	Concept
PLAN-1	1	2	PCB Routing	CPC by B2B Connector
PLAN-2	1	1 or 2	Direct CPC	Direct Connection by High Density module
PLAN-3	4	1	DCP Douting	Connection by DCP
PLAN-3B		2	PCB Routing	Connection by PCB
PLAN-4	2	2	Twinax	OSFP and Cable receptacle separete soldring on PCB
PLAN-4B	2	2	Twinax	Direct connect OSFP and Twinax
PLAN-5	1	2	PCB Routing	Connection by PCB + Cable using for Far End



<u>Summary</u>

SI performance simulation of 448G connector

- In this presentation, we report the SI performance of tuned vertical mount OSFP and 2D connectors. The 2D connector showed good performance, but the VLC-OSFP connector can also achieve satisfactory insertion loss.
- For study of Cross-talk, ICN of COM parameter of 448G is not specified.
 Then ICN of 224G-PAM4 was used as a reference. And the results were excellent.
- We provide these touchstone files.

As a result, we hope that committee members will utilize the 448G verification in advance.

Insertion Loss and Line Length for 448G

- We verified whether the VLC structure could achieve the insertion loss necessary for 448G transmission.
 The routing length are calculated of longest length in PCB and Cable.
- In this study, almost PLANs will be able to do 448G transmission.
 And it was found that by better setting the distance from the ASIC, an insertion loss of -10~12 dB of Host PCB loss can be achieved with 448G-PAM8 (74 GHz) or 448G-PAM6 (89 GHz).
- And PCB material is very important.

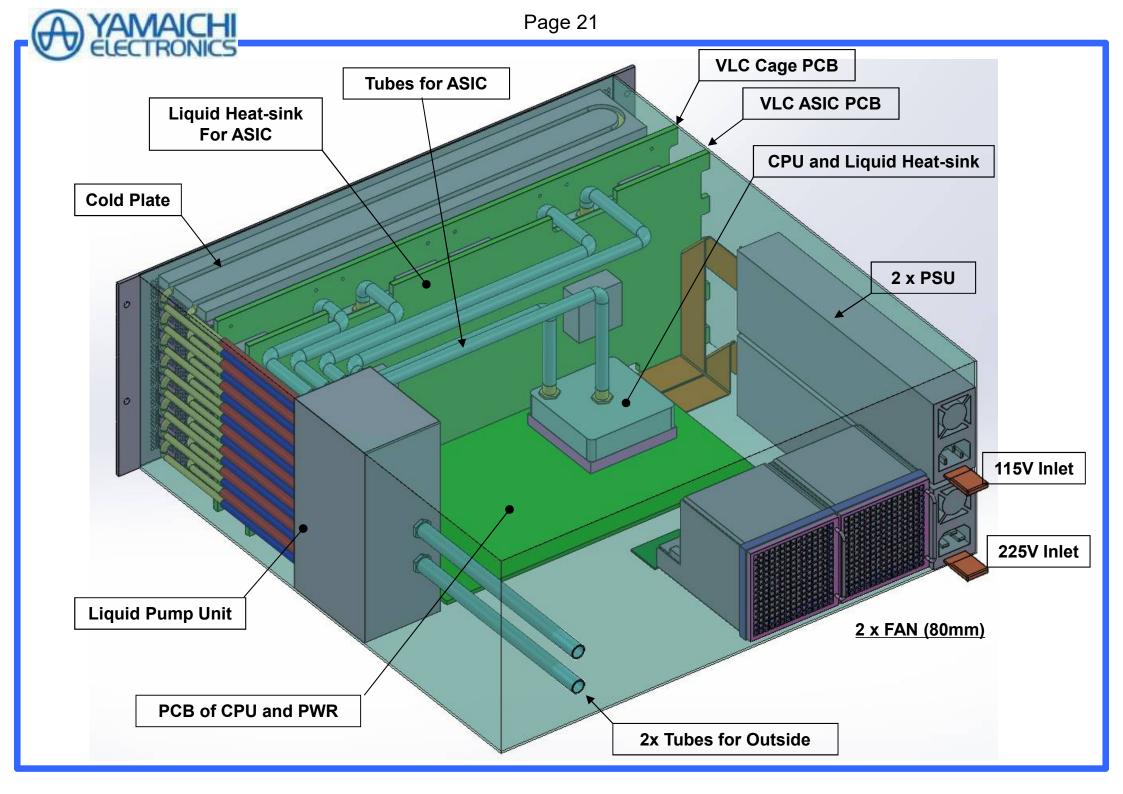
<u>Next Step</u>

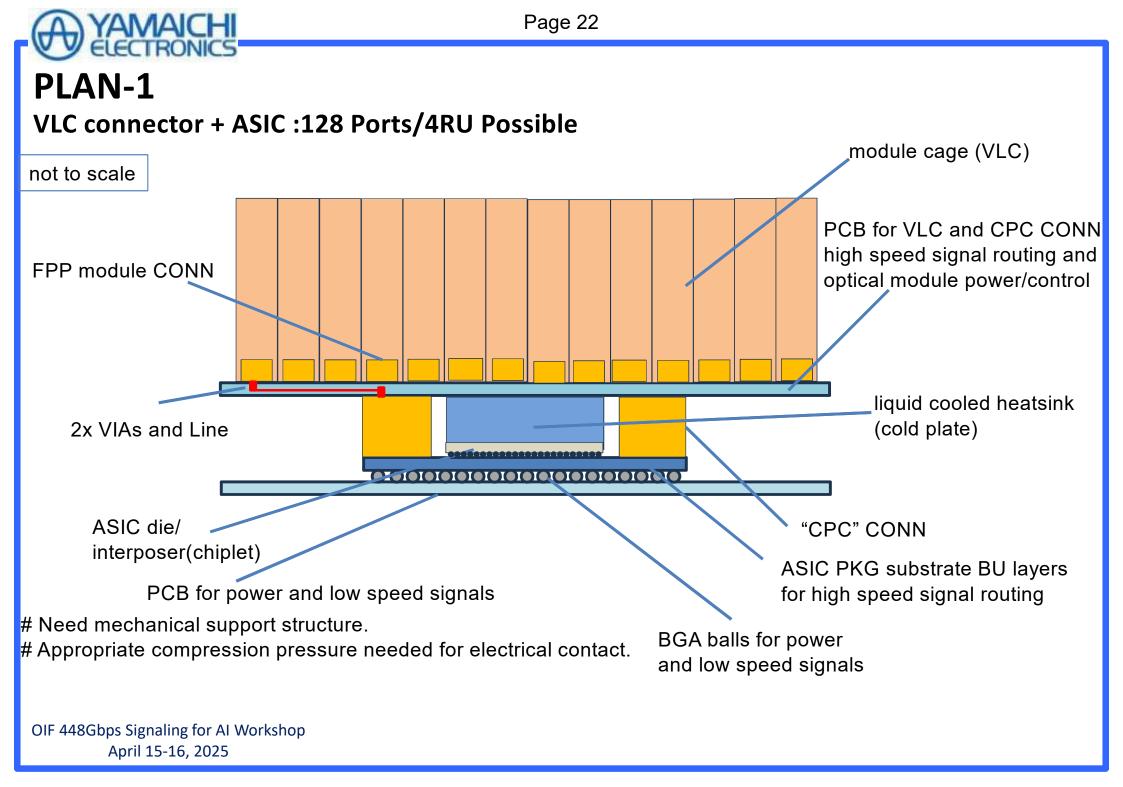
- Further improvement of connector and others after discussion at this 448G workshop.
- SI performance improvement and S-parameters (Touchstone) of 448G compatible OSFP-XD connector.
- OSFP and new high density module heat dissipation structure and simulation over 50 ~ 100 watts.
- The structure of VLC still has several points needed to improvement for actual use cases.

So we will improve these points for customers' actual use cases.



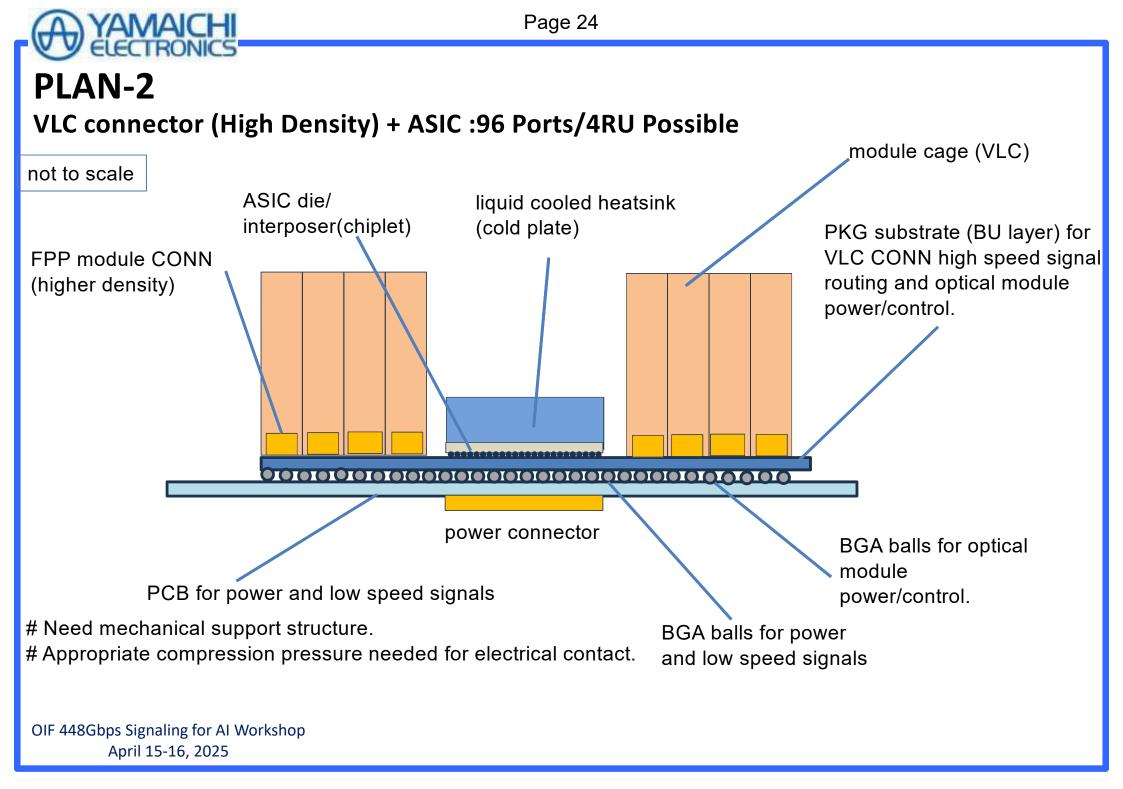
Backup Pages





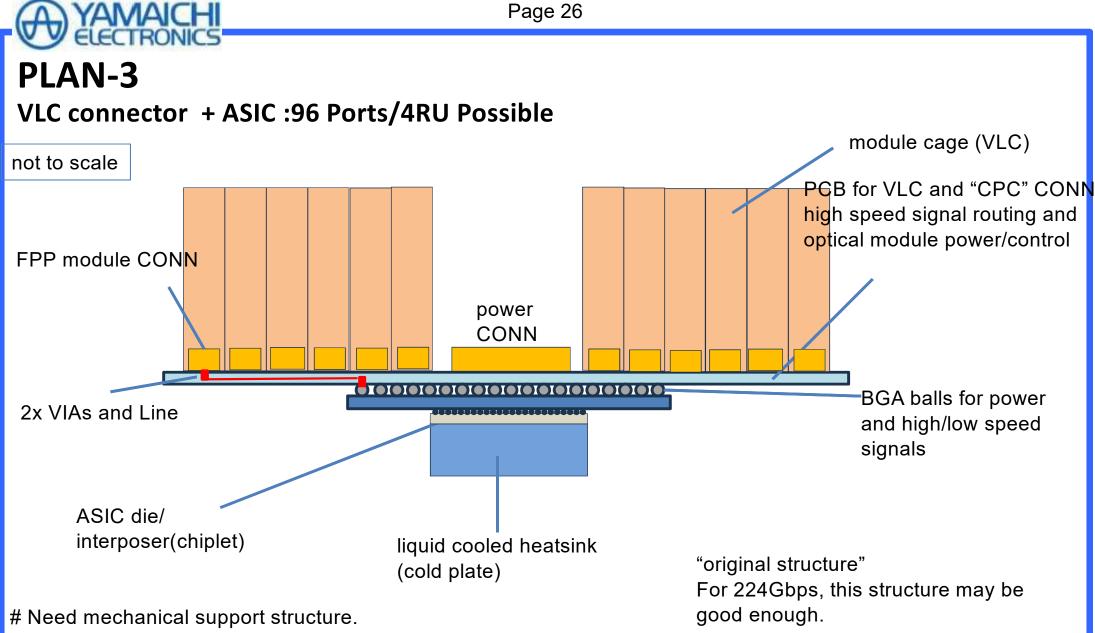


PLAN-2

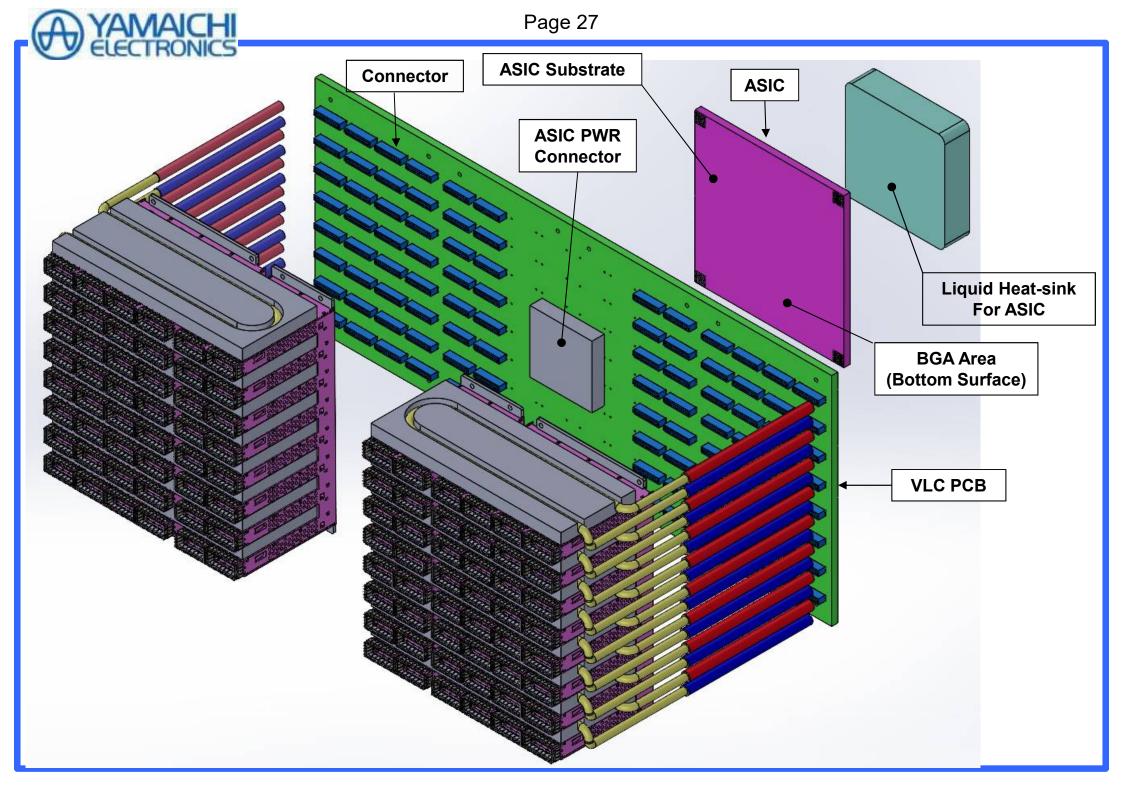


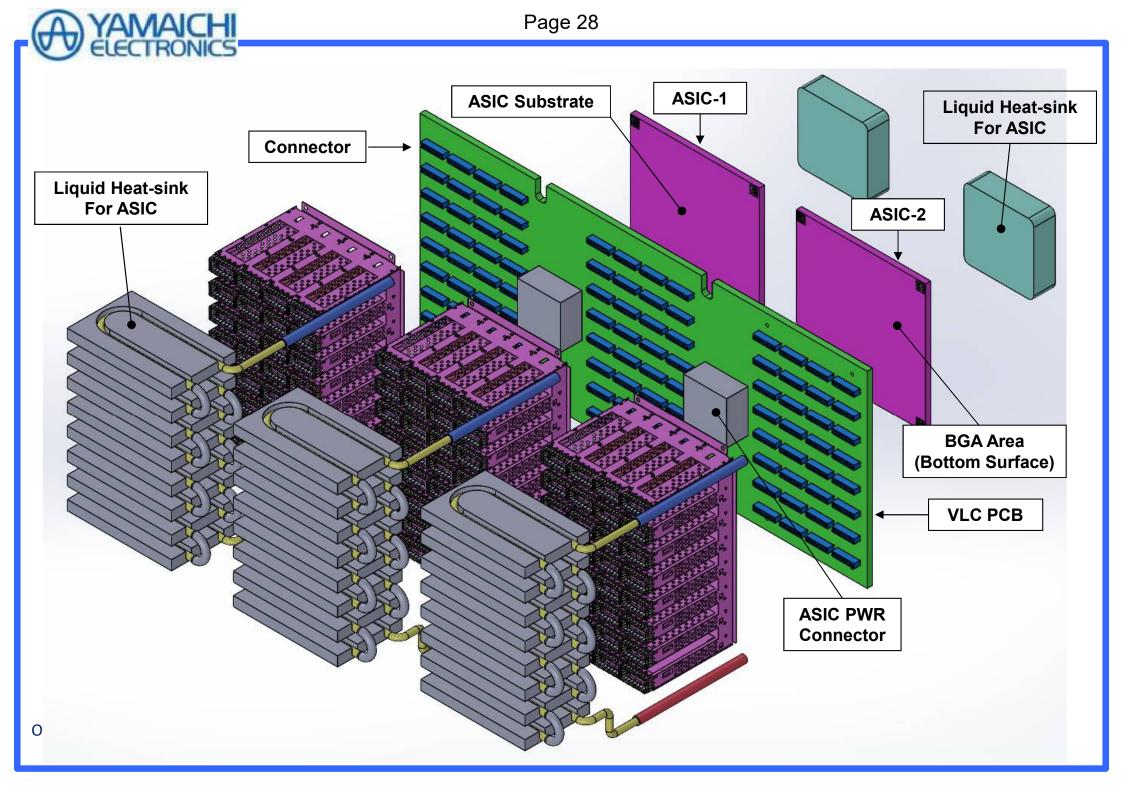


PLAN-3



Appropriate compression pressure needed for electrical contact.

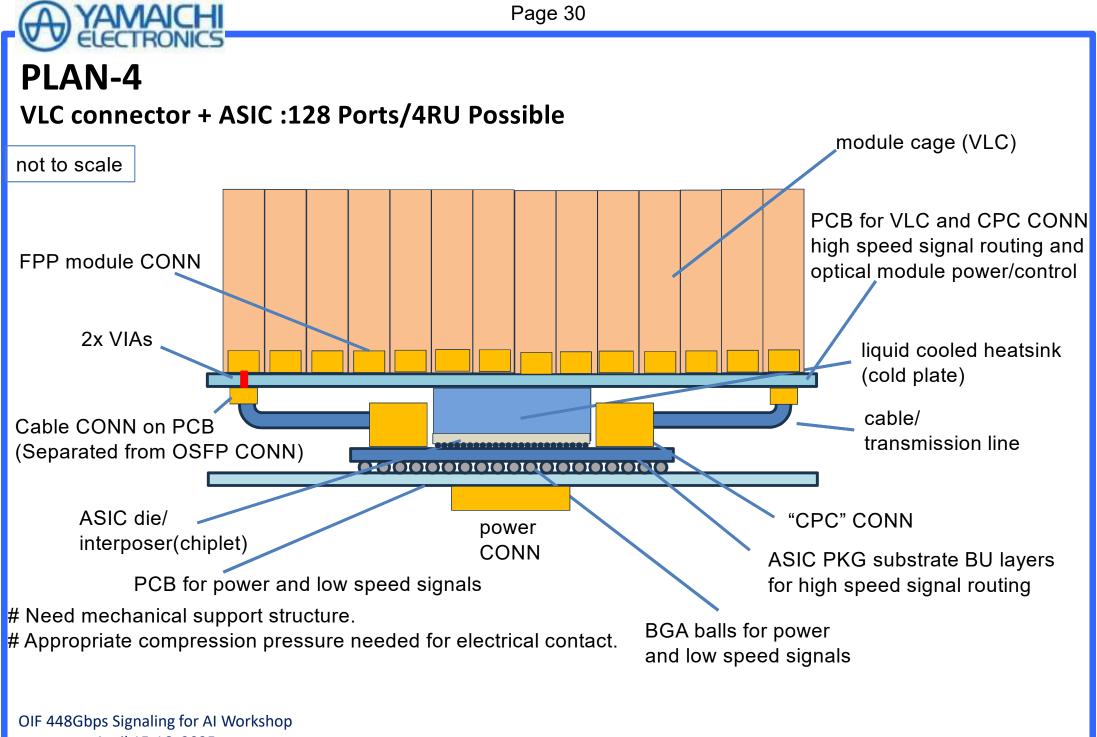




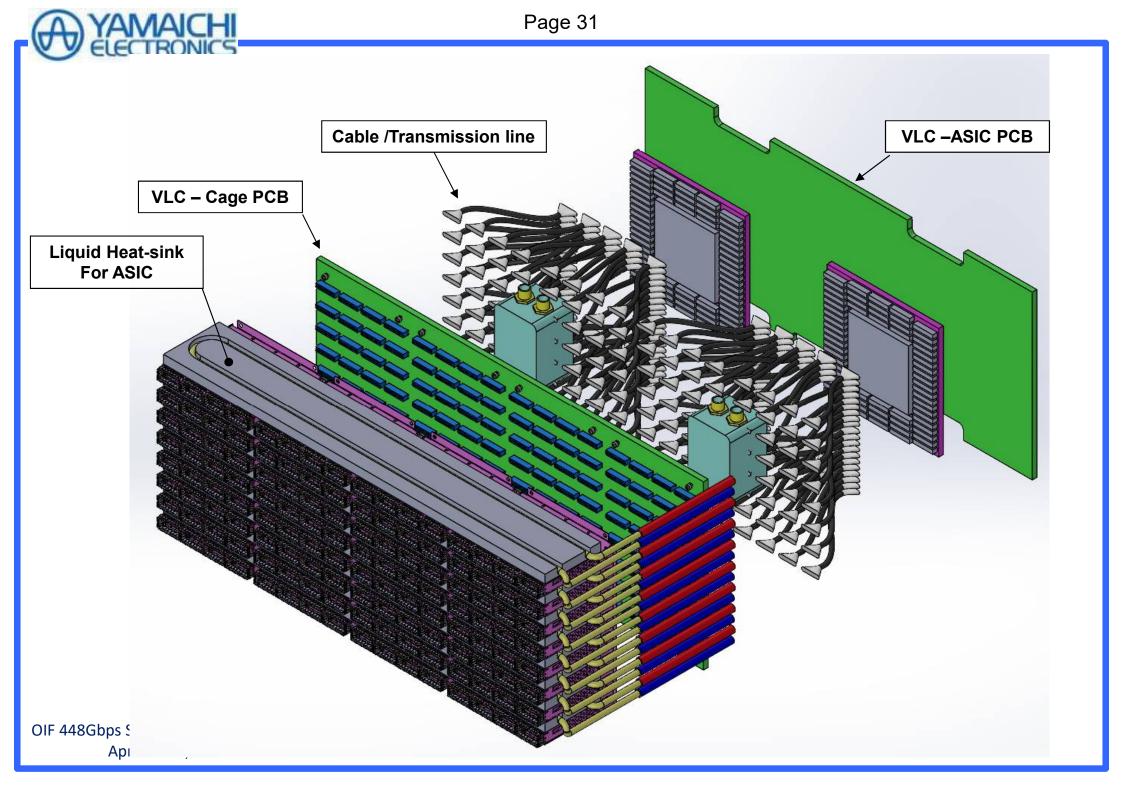


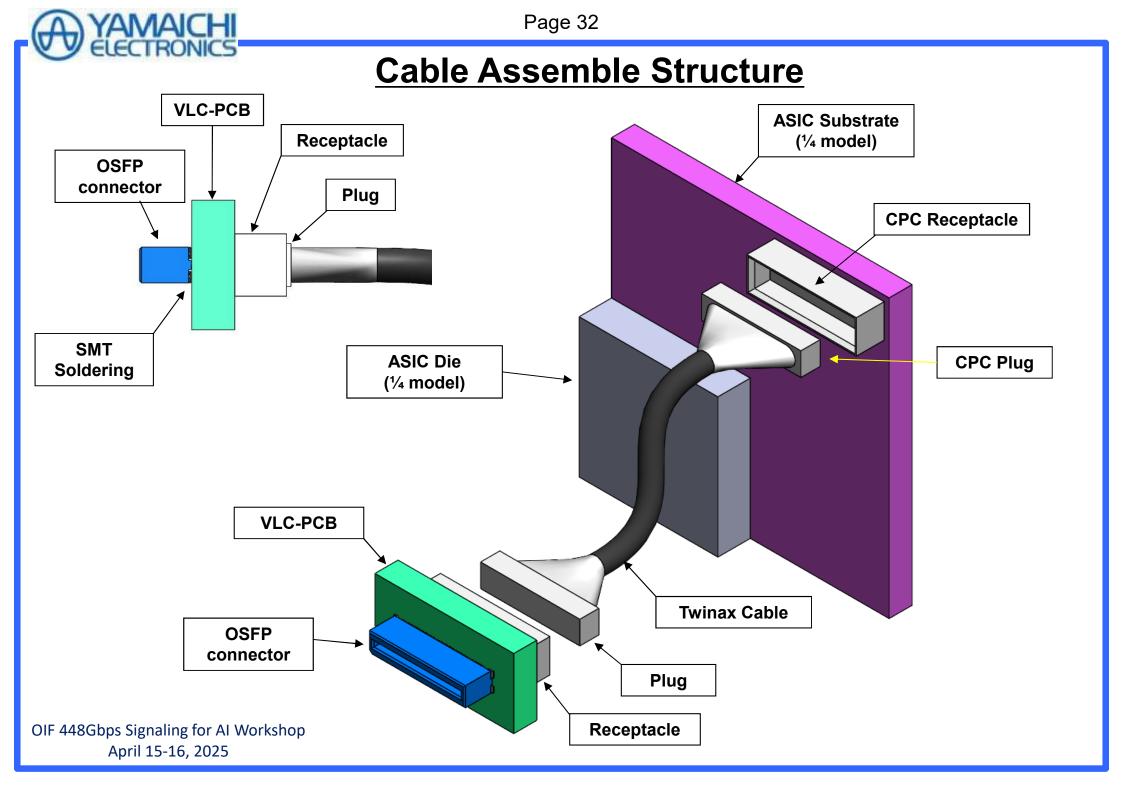
PLAN-4

Cable Assemble of 3 Points Connection



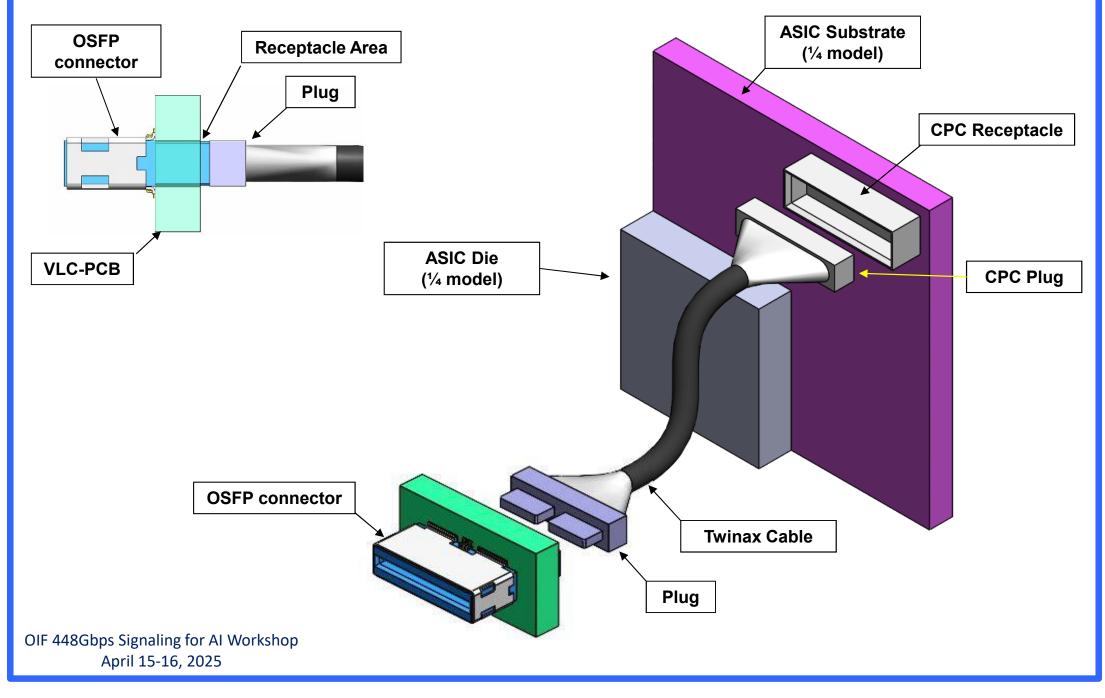
April 15-16, 2025





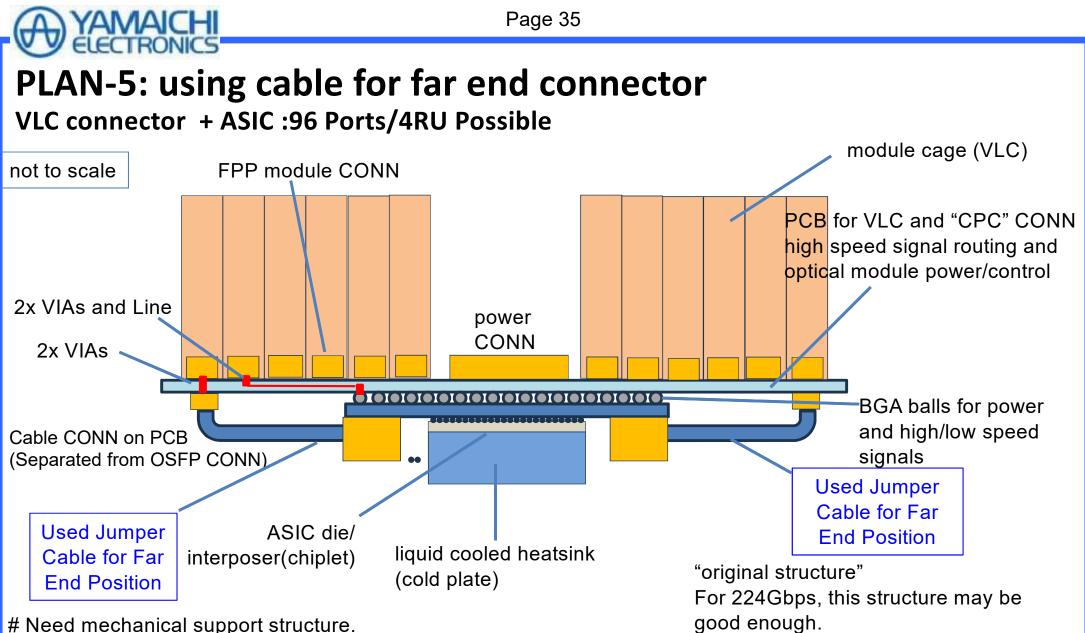


Cable Assemble Structure





PLAN-5



Need mechanical support structure.

Appropriate compression pressure needed for electrical contact.





SI Performance of 448G Connectors By Simulation

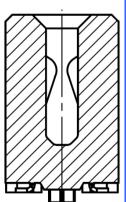
OIF 448Gbps Signaling for AI Workshop April 15-16, 2025

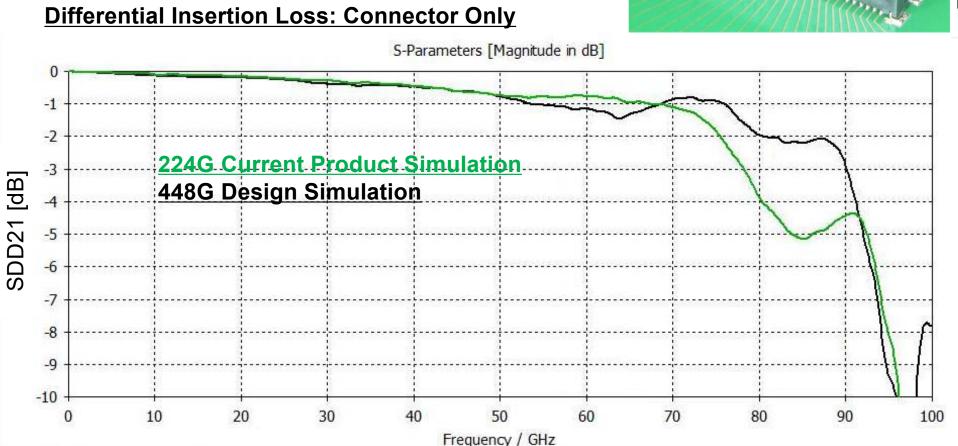
VLC-OSFP Connector for 448G

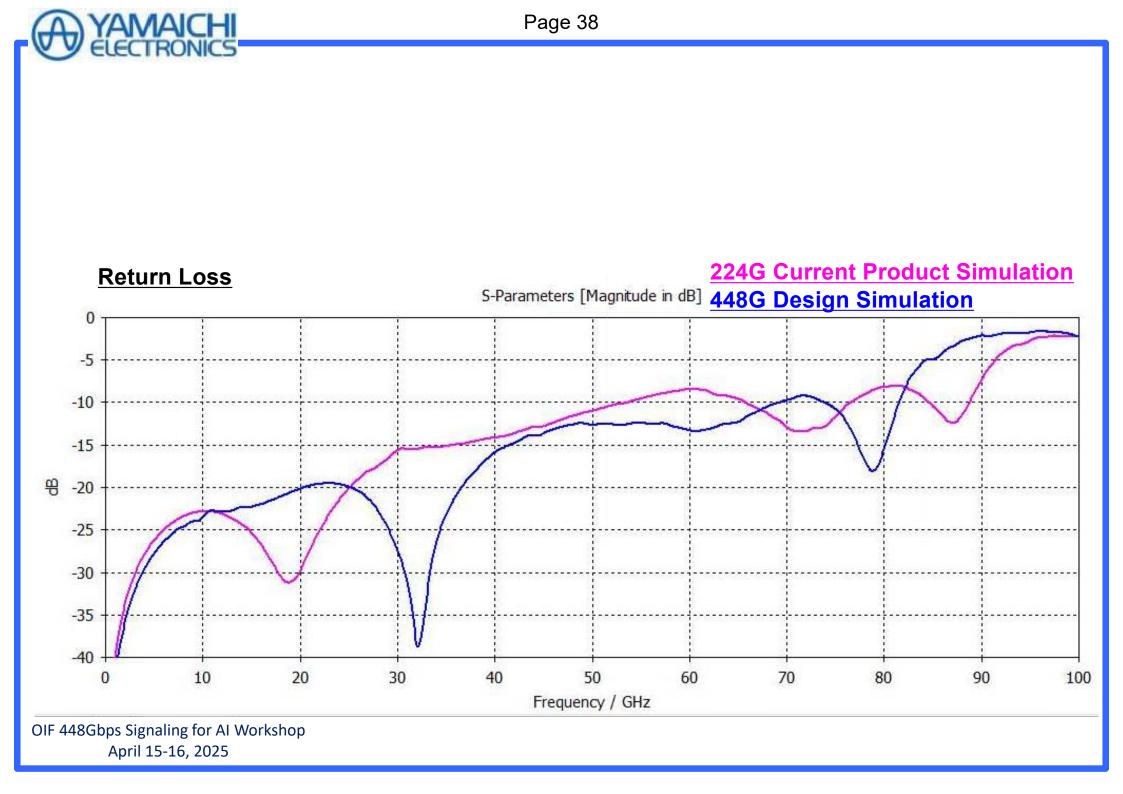
- Vertical Mounted OSFP Connector Simulation
- Connector have same pin mapping of OSFP.
- Connector Impedance is 92.5 ohm now.

Current OSFP-OSFP Connector



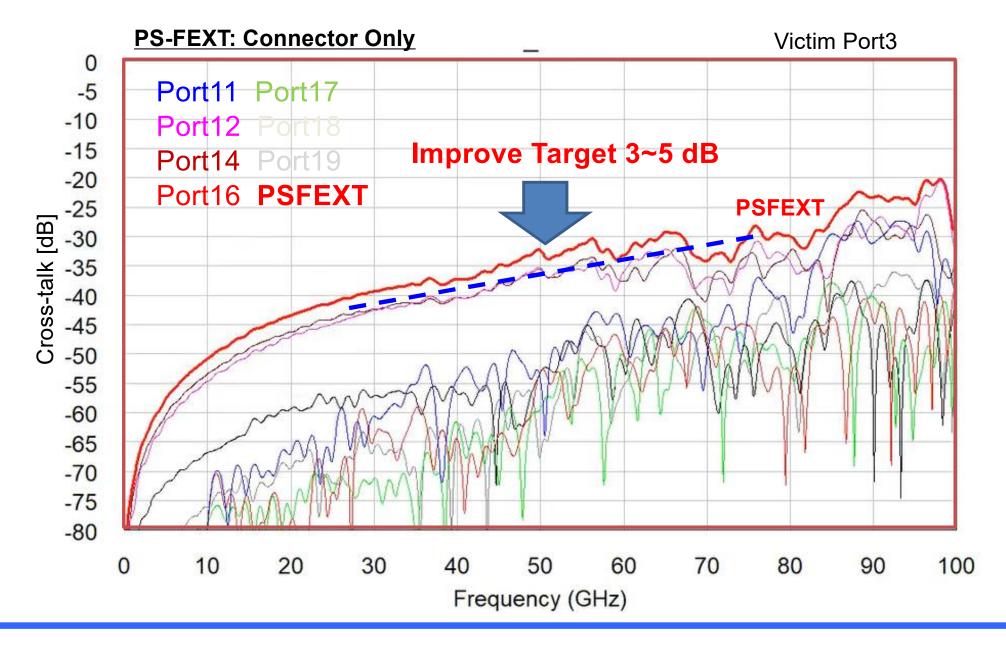


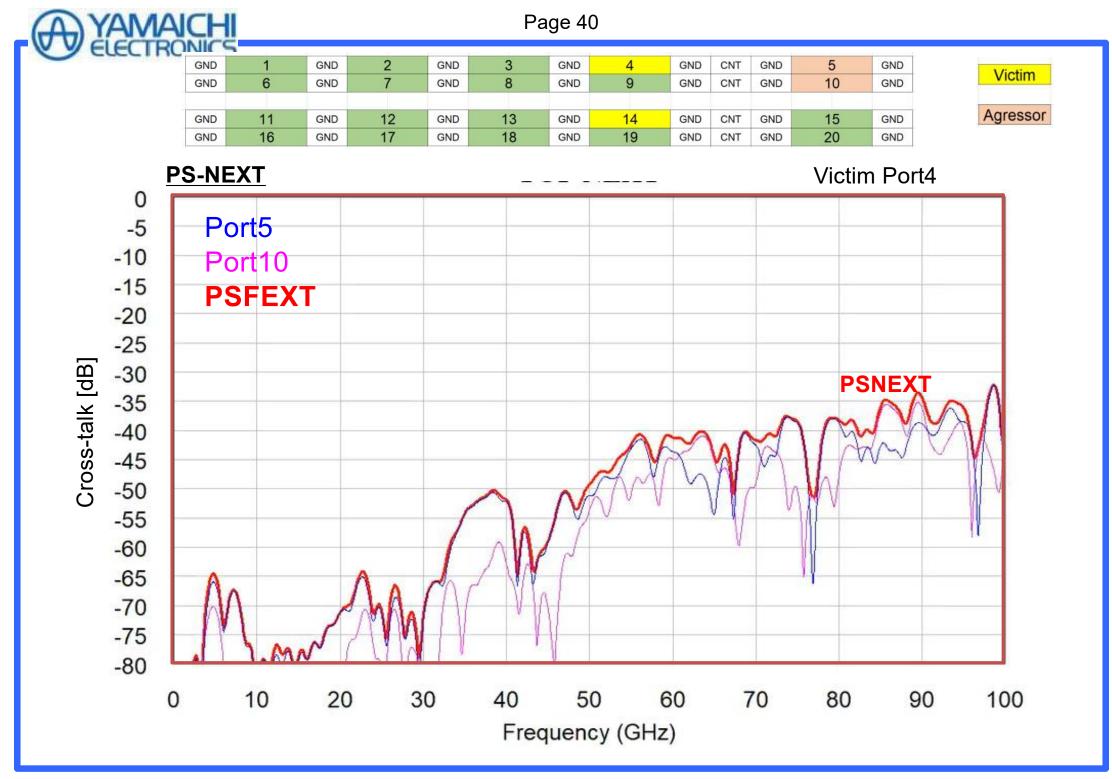






GND	1	GND	2	CNID	2	CNID	٨	CNID	CNT	CNID	5	GND	
GND	1.	GND	۷ ک	GND	3	GND	4	GND	CNT	GND	3	GND	
GND	6	GND	7	GND	8	GND	9	GND	CNT	GND	10	GND	Victim
GND	11	GND	12	GND	13	GND	14	GND	CNT	GND	15	GND	Aggroood
GND	16	GND	17	GND	18	GND	19	GND	CNT	GND	20	GND	Aggresso



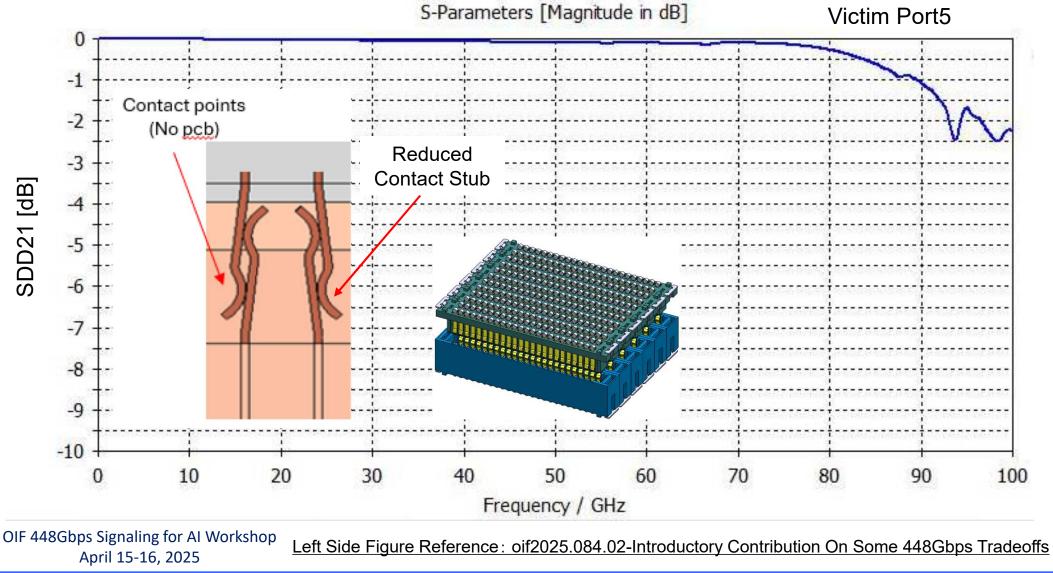




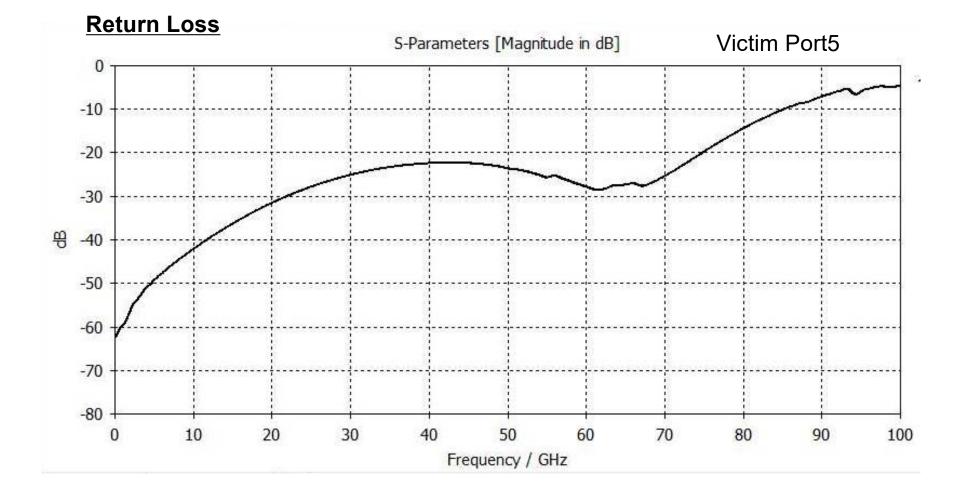
2D Connector for 448G

- Tuning of Yamaichi Original 2D Connector Simulation
- Connector Impedance is 92.5 ohm now.

Differential Insertion Loss: Connector Only



A YAMAICHI ELECTRONICS



OIF 448Gbps Signaling for AI Workshop April 15-16, 2025

A YAMAICHI ELECTRONICS

Page 43

