



Measurement Results for a 448 Gbps Physical Channel

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April 15, 2025

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Agenda

- **Motivation:**

- Demonstrate the 448 Gbps performance of measured interconnect hardware

- **Illustrate:**

- The upper bounds of interconnect performance with precision hardware

- **Insights:**

- From the anatomy of measurements spanning 110 GHz

- **PAM4/6/8 Tradeoffs**

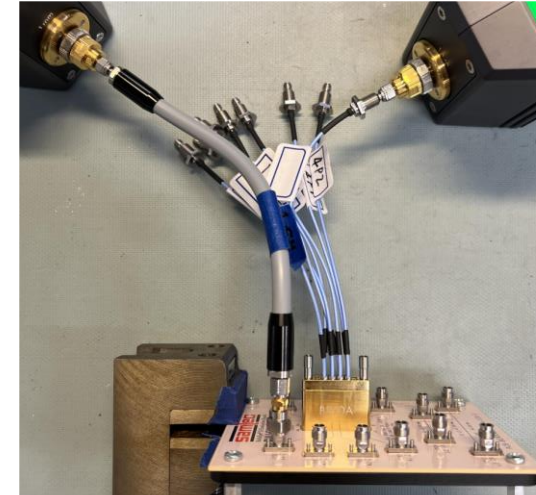
- Focused on channel consideration from COM Results

- **Discussion:**

- Relationships to future practical interconnect design

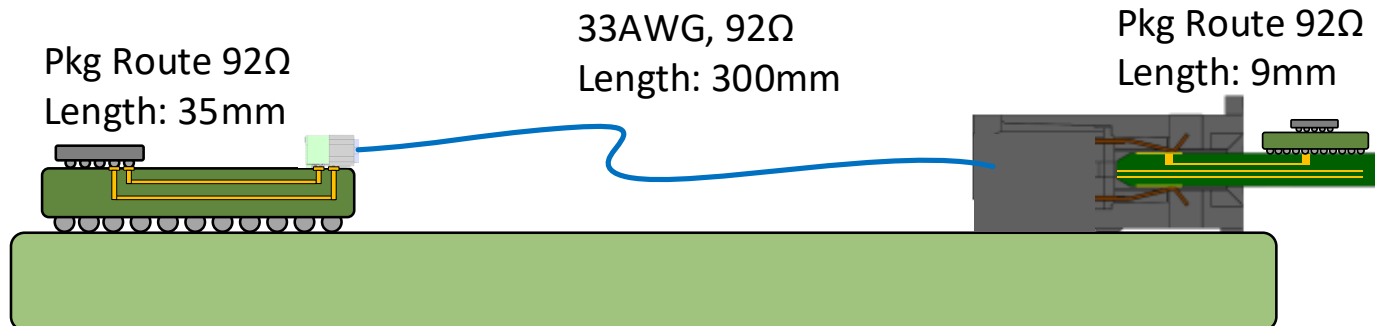
Cabled Host Empirical Upper Bound

- Generalize cabled host interconnect as 35mm of planar routing to cable to front panel connector with 100% implementation freedom.
- The result is very similar to today's precision RF test fixtures with 1.00mm cabling.
- Leverage existing empirical characterization to 110GHz.
- Non-scalable RF fixture design rules

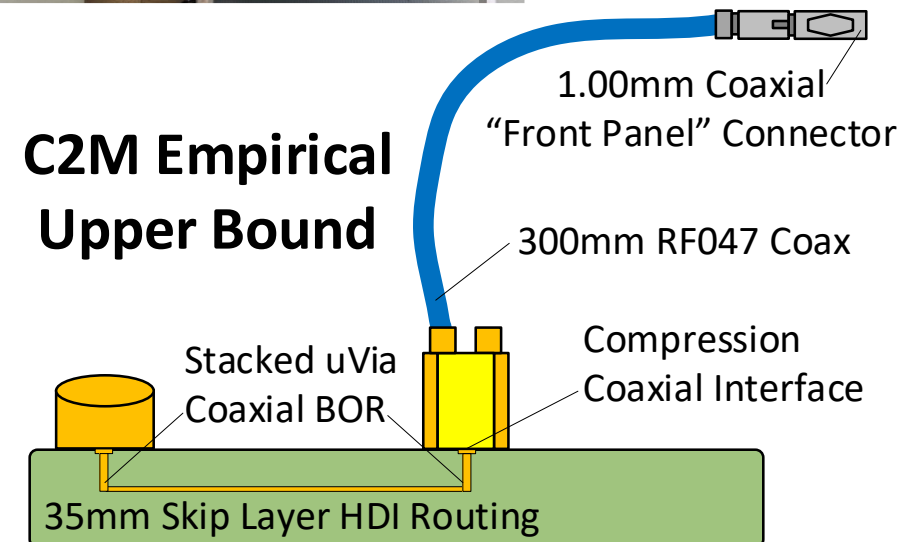


BE90 EVB
Measurement
Setup

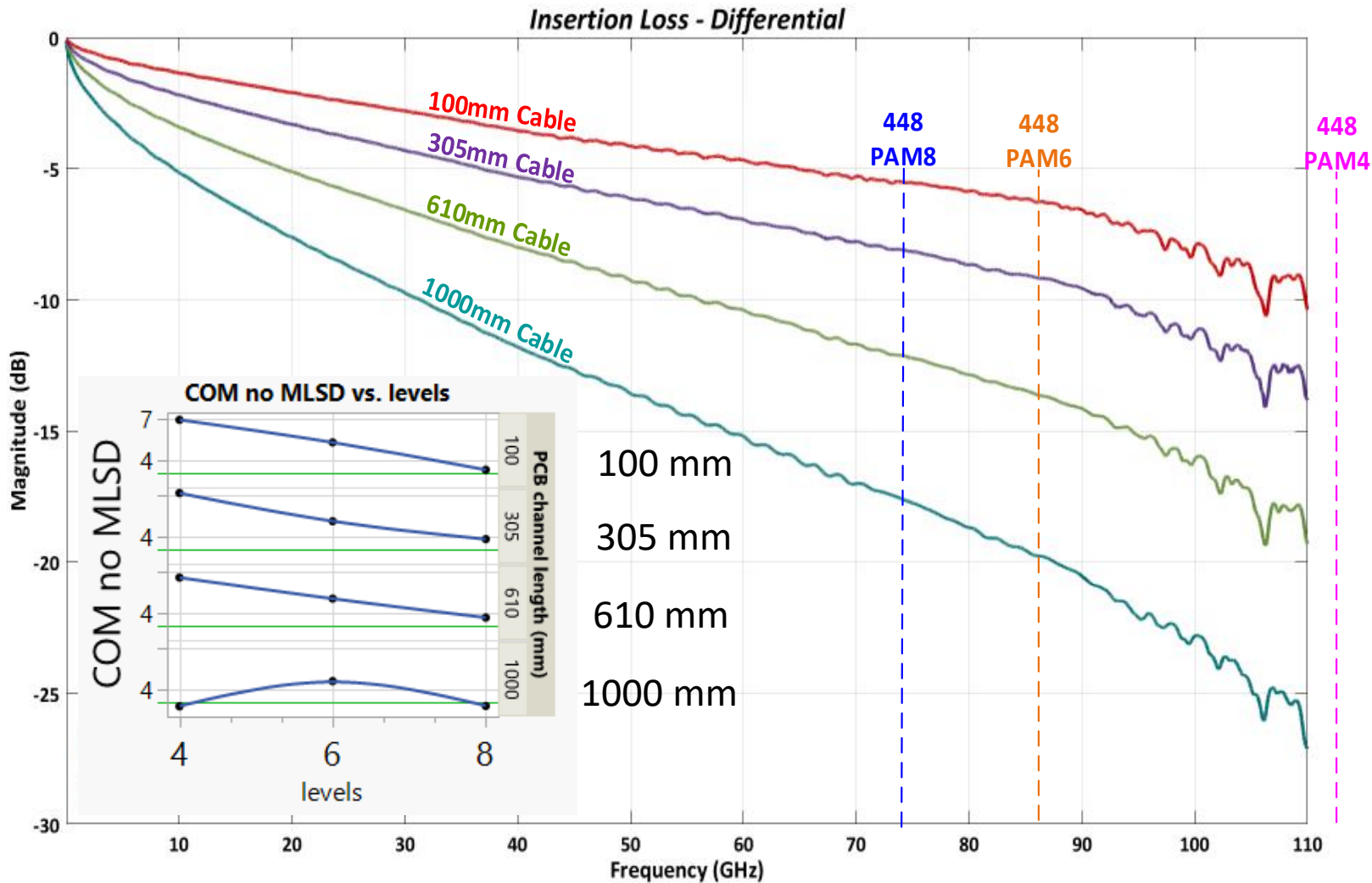
Chip to Module (C2M)



C2M Empirical Upper Bound



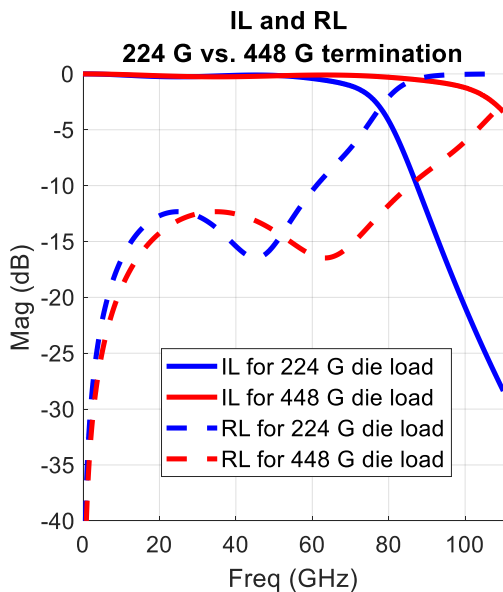
BE90 EVB Measured Performance



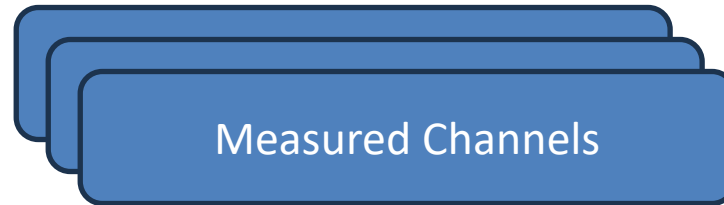
- 4.5dB to 14dB 224Gbps Channels
- No resonant notch filter response to 110GHz
- -1dB ILD BW ~ 95GHz
- -15dB RL BW ~ 95GHz
- P/N Skew < 0.5ps
- **P/N Coupling <80dB to 90GHz**
- 1.65dB/25mm PCB Strip lines @56GHz
- 1.00mm coax termination to RF047 Coax Cable to BE90C ferrule.

Set up for Computing 448Gbps COM

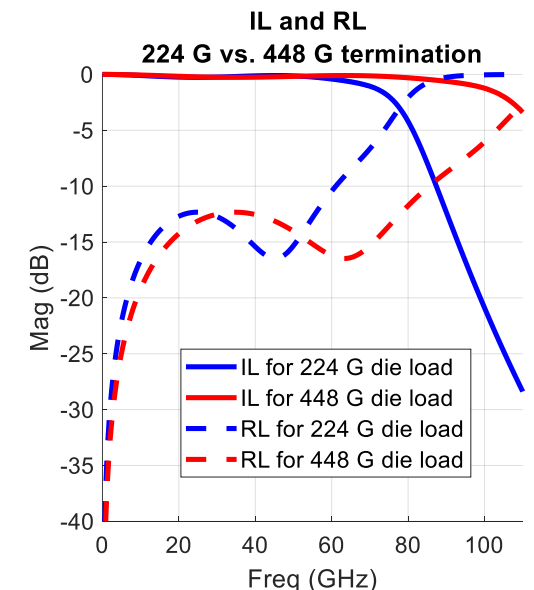
- **COM with improved die load terminations**
 - Blue is 224 Gbps reference model
 - Red is 448 Gbps estimated model



0 mm ,
10mm,
30 mm
package



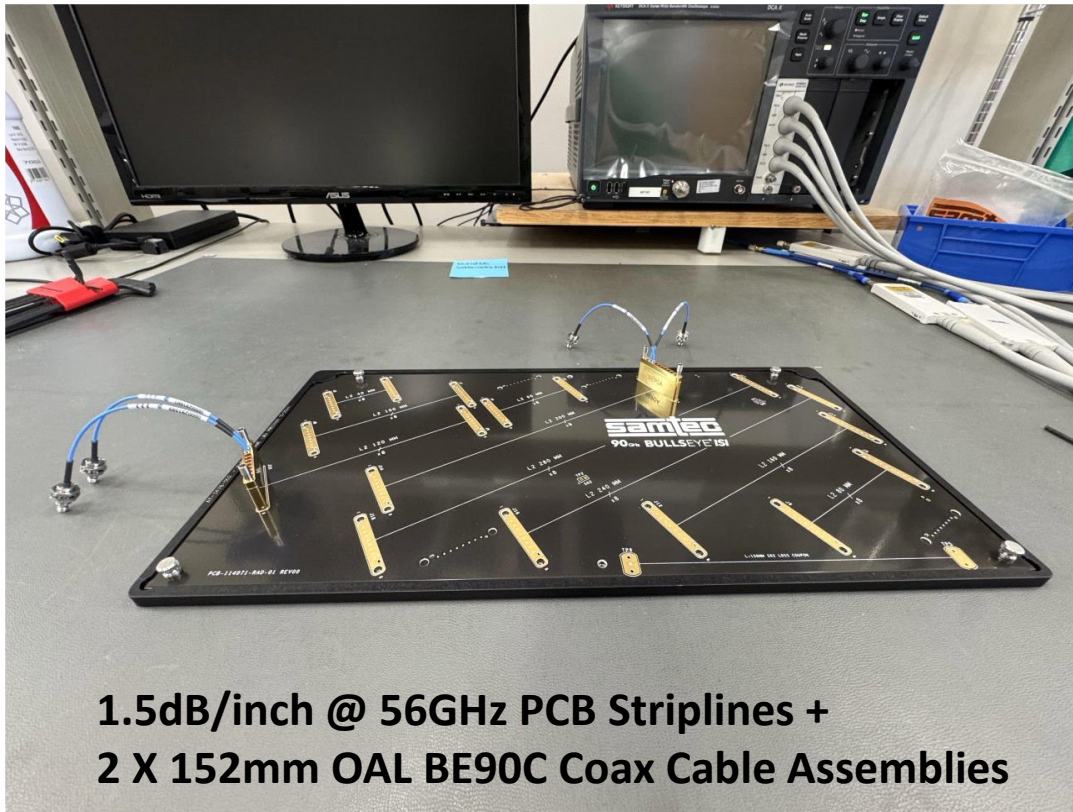
0 mm ,
10mm,
30 mm
package



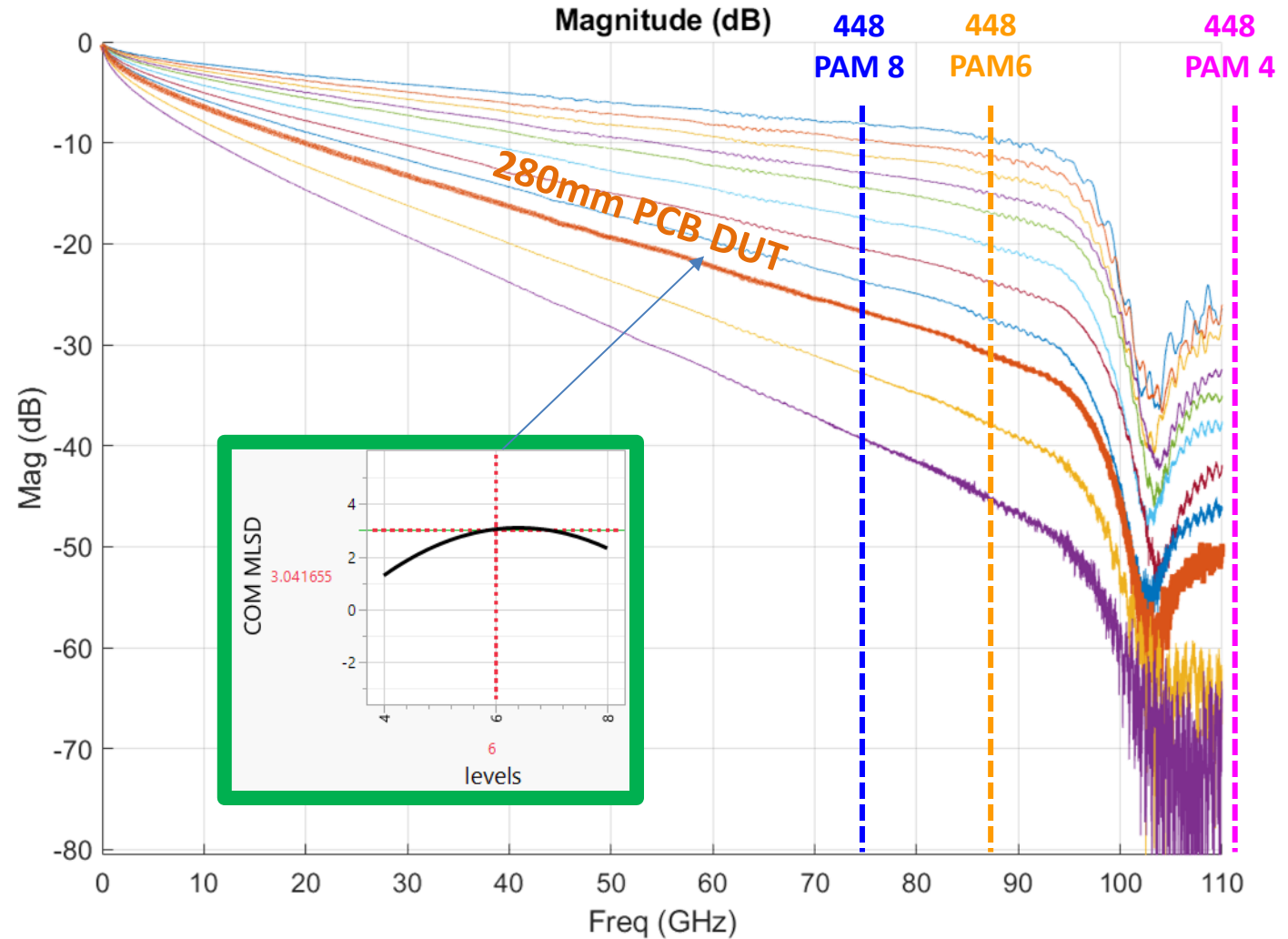
Some 448 Gbps COM Set-up Parameters

- **Quantization (ENOB)**
 - 5 and 6.5 bits
- **Noise eta_0**
 - 1e-9, 3e-9, & 5e-9 V²/GHz
- **Modulation**
 - PAM 4,6,8
- **224 Gbps and 448 Gbps die terminations**
 - Reduced loss (~ 40% lower loss) estimated for 448 Gbps termination
 - 0 mm, 10 mm, and 30 mm 224 Gbps packages but co-package connection
 - 0 mm emulates test equipment
- **Using 224 Gbps reference package t-line model, single element**
- **RxFFE**
 - 7 Pre/ 18 post, 2 groups of 4 floating taps to 100 UI
- **DER_0 = 2e-5**
- **R_LM = 0.95**
- **1+α MLSD**

BE90 ISI Loss Channel Emulator Responses



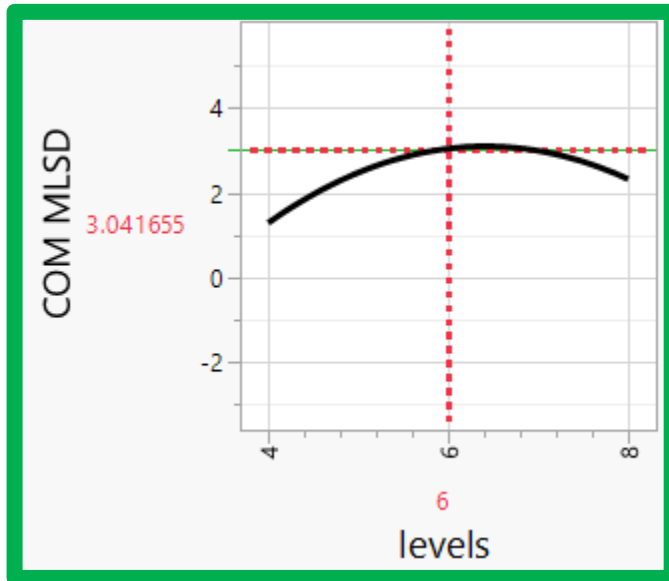
1.5dB/inch @ 56GHz PCB Striplines +
2 X 152mm OAL BE90C Coax Cable Assemblies



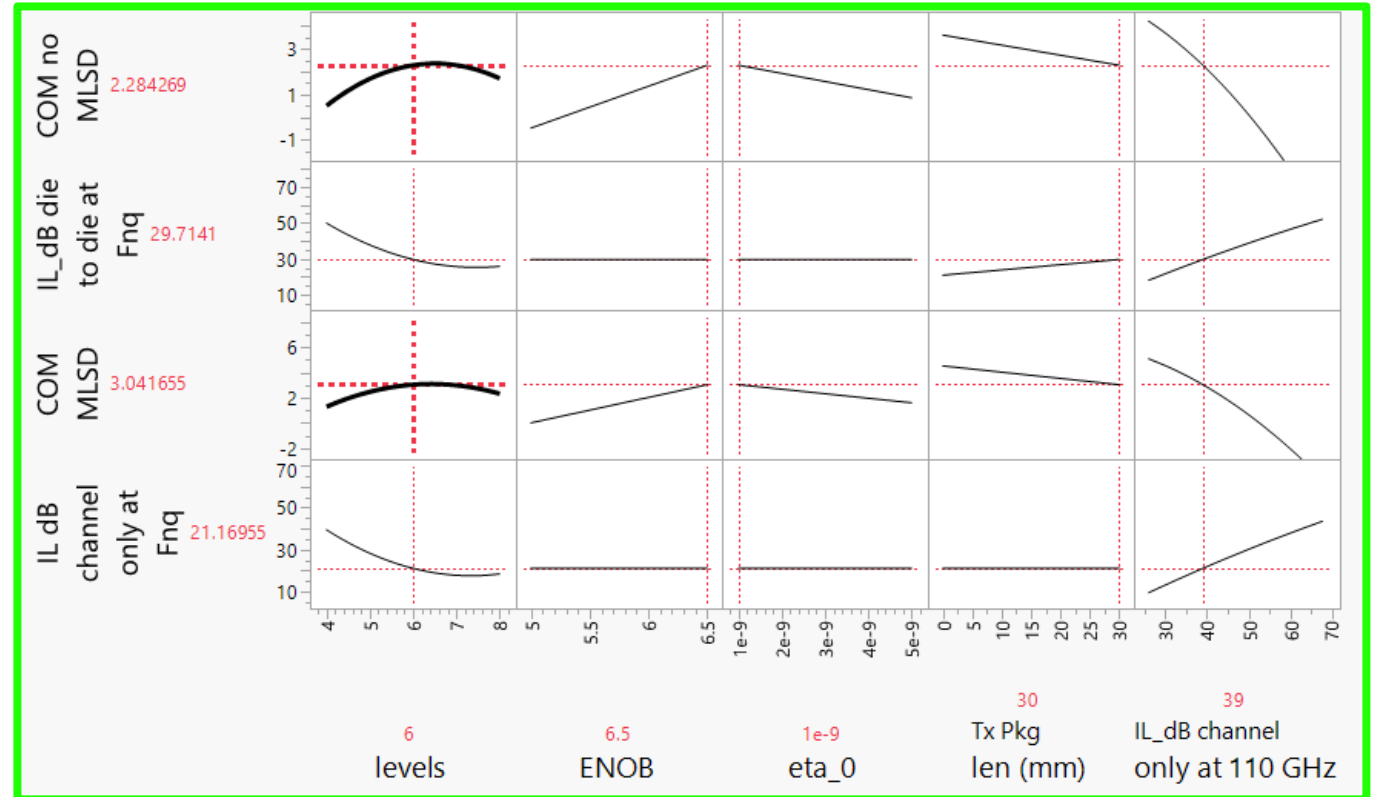
COM appears to favor PAM 6

PAM 6 seem to be an optimum when

- $\eta_0=1e-9$
- package length = 30 mm
- channel loss at 87 GHz = 30 dB
- ENOB = 6.5 bits



COM (w/wo MLSD) and IL (die to die/channel only)

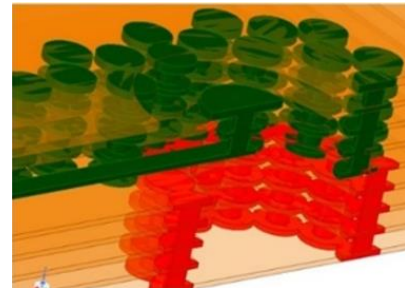
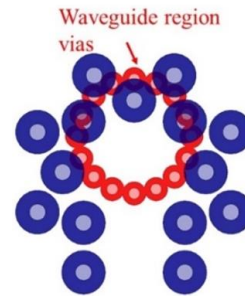


The performance has high linear relation to noise (η_0), package loss (length), and quantization (ENOB)

Scaling is a Challenge

Layer	Type	Thickness (um)	Construction	Dk	Df	Stripline Wiring Cross Section				
L01		38	18um + Plating	HVLP2		215				215
D01	Preg	76	1X1078 (67%)	2.84	0.0015	100				100
L02		25	12um + Plating	HVLP2		215				215
D02	Preg	76	1X1078 (67%)	2.84	0.0015	100				100
L03		25	12um + Plating	HVLP2		215	272	218	272	215
D03	Preg	76	1X1078 (67%)	2.84	0.0015	100				100
L04		25	12um + Plating	HVLP2		215				215
D04	Preg	76	1X1078 (67%)	2.84	0.0015	100				100
L05		25	18um + Plating	HVLP2		215				215
D05	Core	76	1X1078 (64%)	2.84	0.0015	100				100
L06		25	18um + Plating	HVLP2		215				215
D06	Preg	76	1X1078 (67%)	2.84	0.0015	100				100
L07		25	12um + Plating	HVLP2		215				215
D07	Preg	76	1X1078 (67%)	2.84	0.0015	100				100
L08		25	12um + Plating	HVLP2		215				215
D08	Preg	76	1X1078 (67%)	2.84	0.0015	100				100
L09		25	12um + Plating	HVLP2		215				215
D09	Preg	76	1X1078 (67%)	2.84	0.0015	100				100
L10		38	18um + Plating	HVLP2		215				215

BE90 EVB Via BOR



- Precision RF test fixtures do not require scalable design rules as do digital applications.
- Qty = 146 unique laser drills per 110GHz SE BOR down to 250um pitch.
- One 218um wide trace in skip layer routing layer in 5 HDI buildup layers netting 1.65dB/inch at 56GHz.
- 6mm Diff Pair Pitch

- Leveraging HDI technology for z-axis interconnect bandwidth is not independent from achievable stripline loss/inch.
 - Low surface roughness copper foils are challenging in buildup due to decreased peel strength. Inner layer in buildup are outer layers of the sub-assembly.

Summary

- Today's precision RF test fixtures give access to empirical channel s-parameter data sets of relevant bandwidth, loss, and physical reach for 448G COM parameter analysis.
- Understanding their implementations and performance limitations gives insight into our future scalable 448Gbps system design space.
 - Maximizing both planar package Z-axis interconnect BW and stripline loss performance beyond these implementation 'local maximums' will be extremely challenging while also dimensionally shrinking to enable digital systems scaling.

