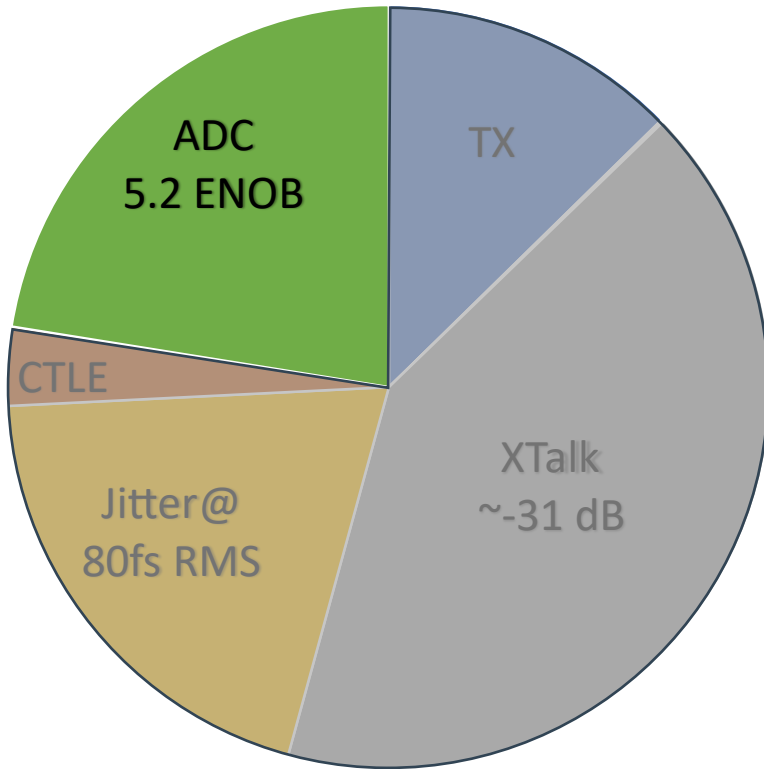# 448G Signaling for AI

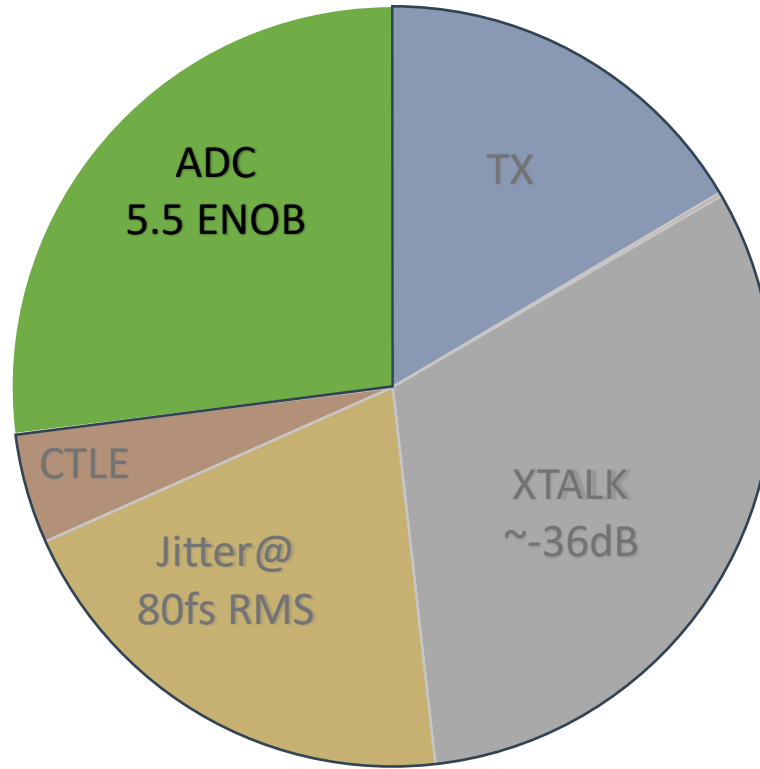Curtis Ling and Sridhar Ramesh
April 2025

Outline

- ADC efficiency trades versus SNDR and Nyquist frequency for PAMx

- FEC options

- Advanced equalization and detection schemes

- Copackaged optics and copper (CPx)

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Electrical Link Budget: 448G PAM4/6/8 Noise

PAM4, 212 GBaud

- TX
- ADC 5.2 ENOB
- CTLE
- Jitter@ 80fs RMS
- XTalk ~-31 dB

PAM6, 164 GBaud

- TX
- ADC 5.5 ENOB
- CTLE
- Jitter@ 80fs RMS
- XTALK ~-36dB

PAM8, 142 GBaud

- TX
- ADC 6.1 ENOB
- CTLE
- Jitter@ 80fs RMS
- XTALK ~-38dB
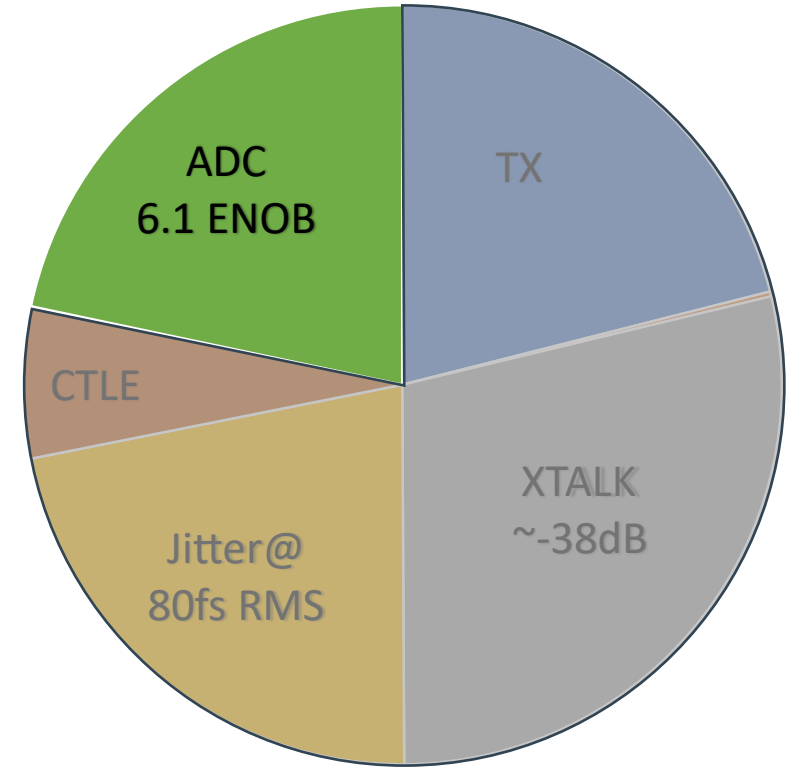
- ENOB alone is not a useful metric, while the pJ/b tradeoff space is complex

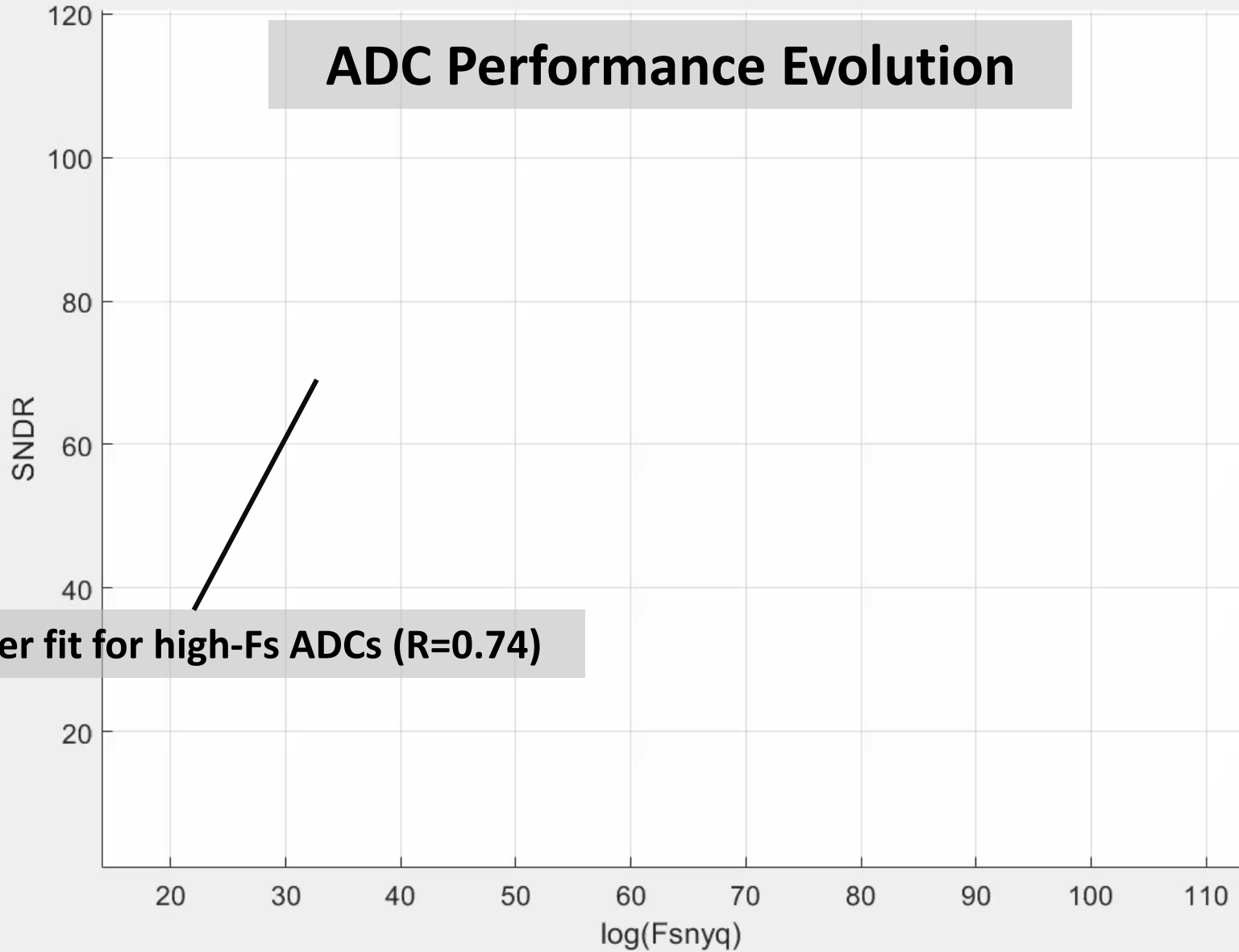ENVISIONING ▪ EMPOWERING ▪ EXCELLING

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Converter Tradeoff Data – Murmann ADC Survey[1]
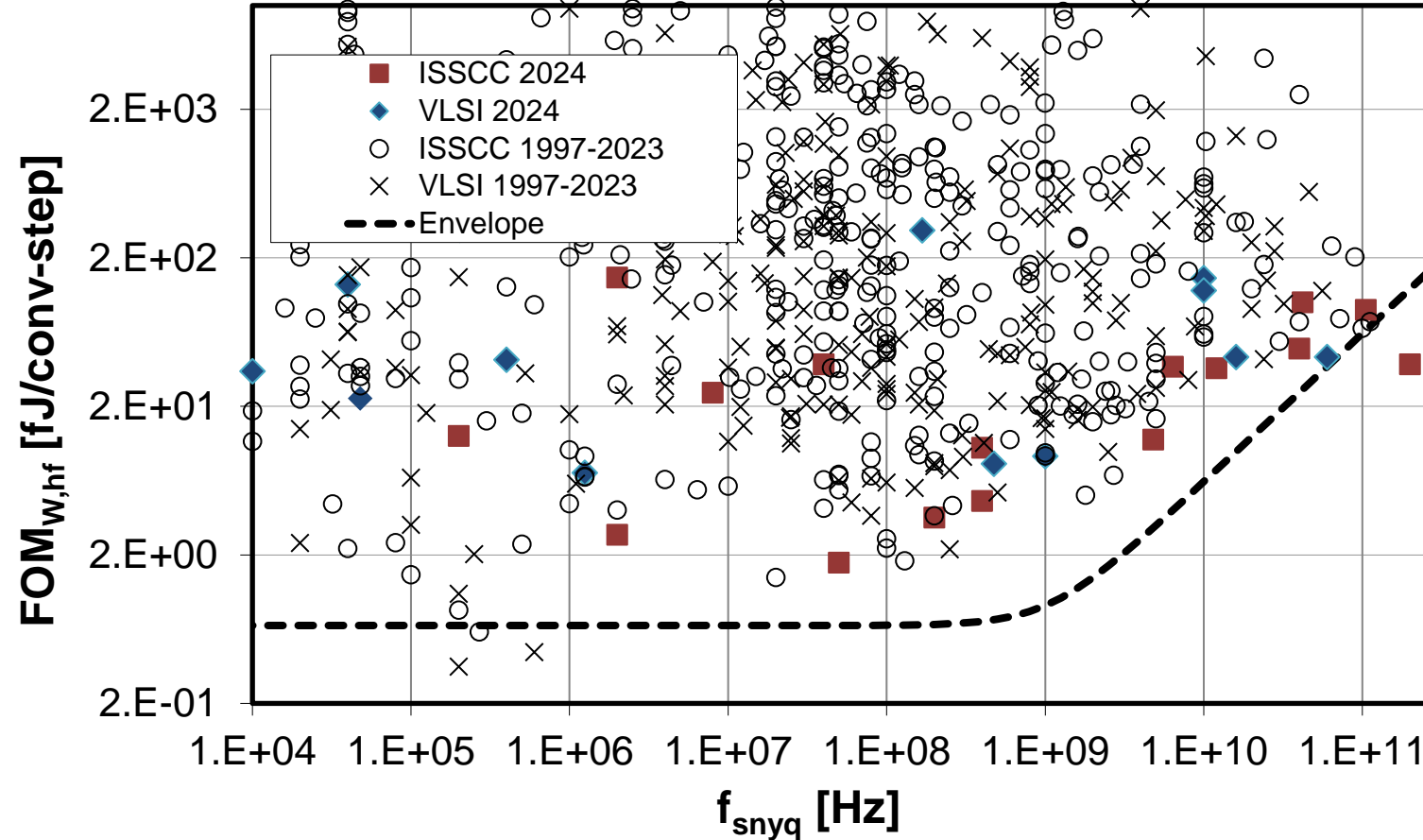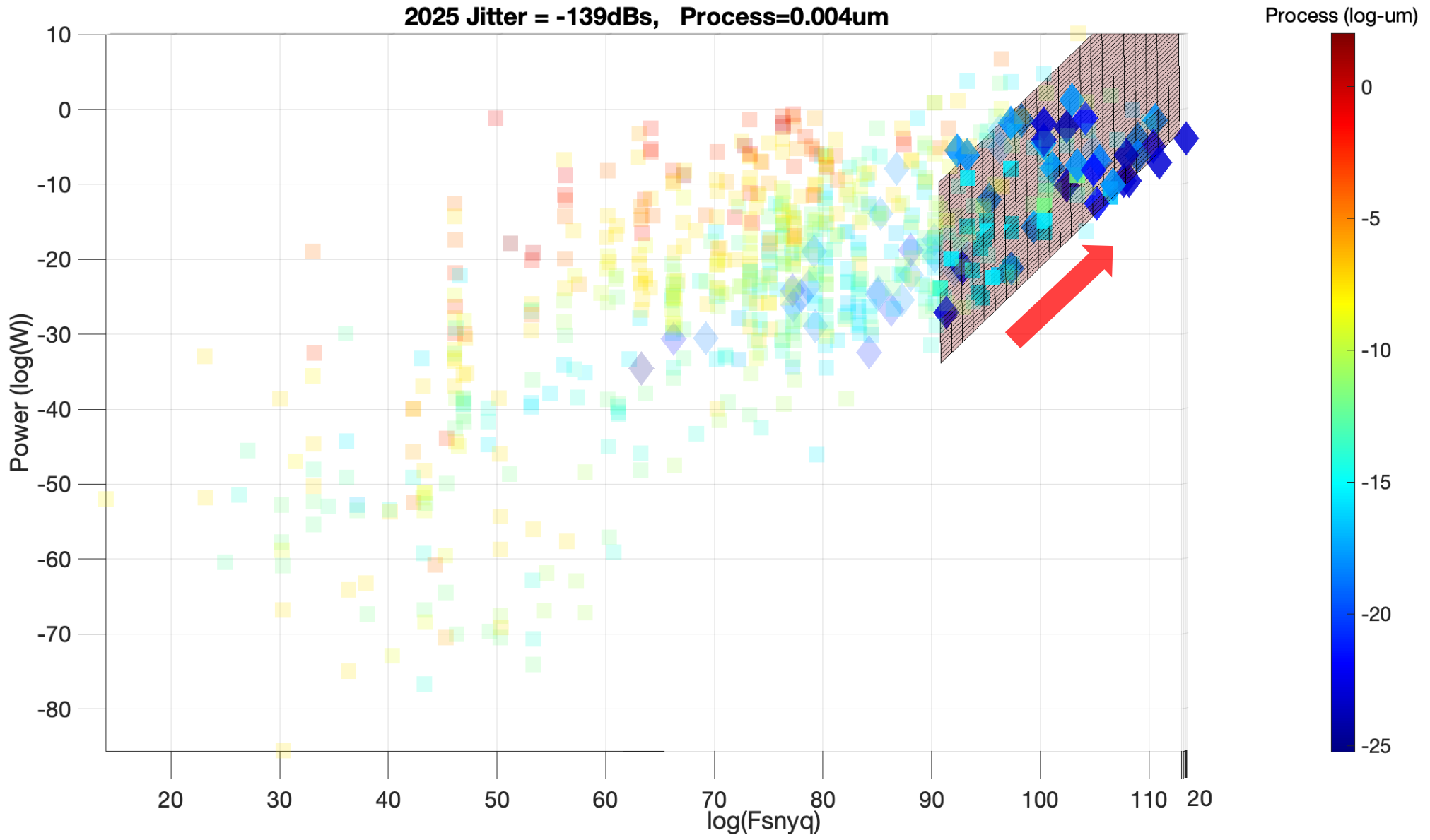

- Survey catalogues all ADCs published in ISSCC and VLSI since 1997

- We can use this data to predict (CMOS) ADC performance trades

[1] https://github.com/bmurmann/ADC-survey

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ADC Performance Evolution

First-order fit for high-Fs ADCs (R=0.74)

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ADC power vs Fs (constant SNDR): 1.4dBW/dBHz (0.1dB σ)

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2025 Jitter = -139dBs,   Process=0.004um
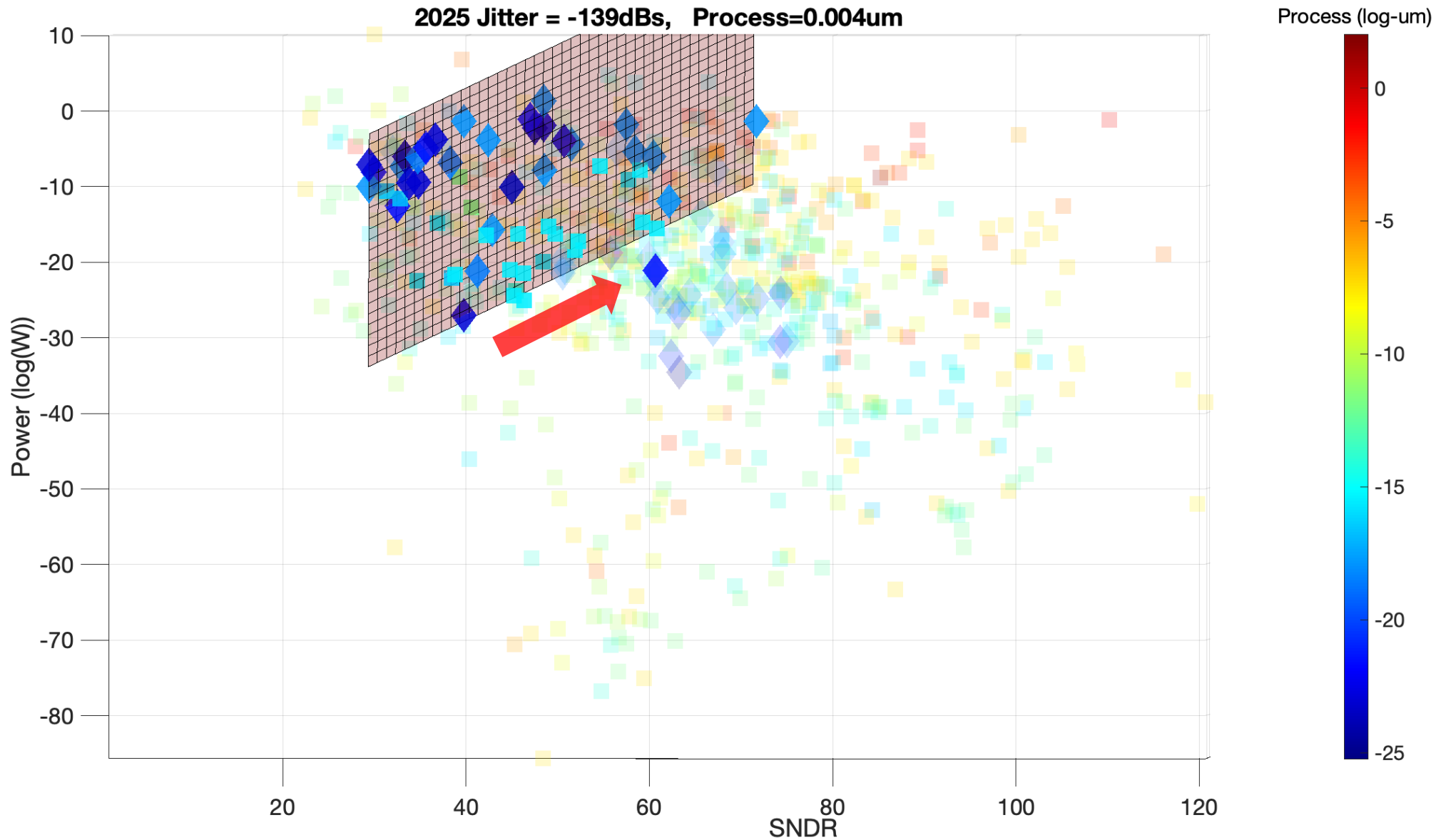
ADC power vs SNDR (constant Fs): 0.6dBW/dB (0.07dB σ)

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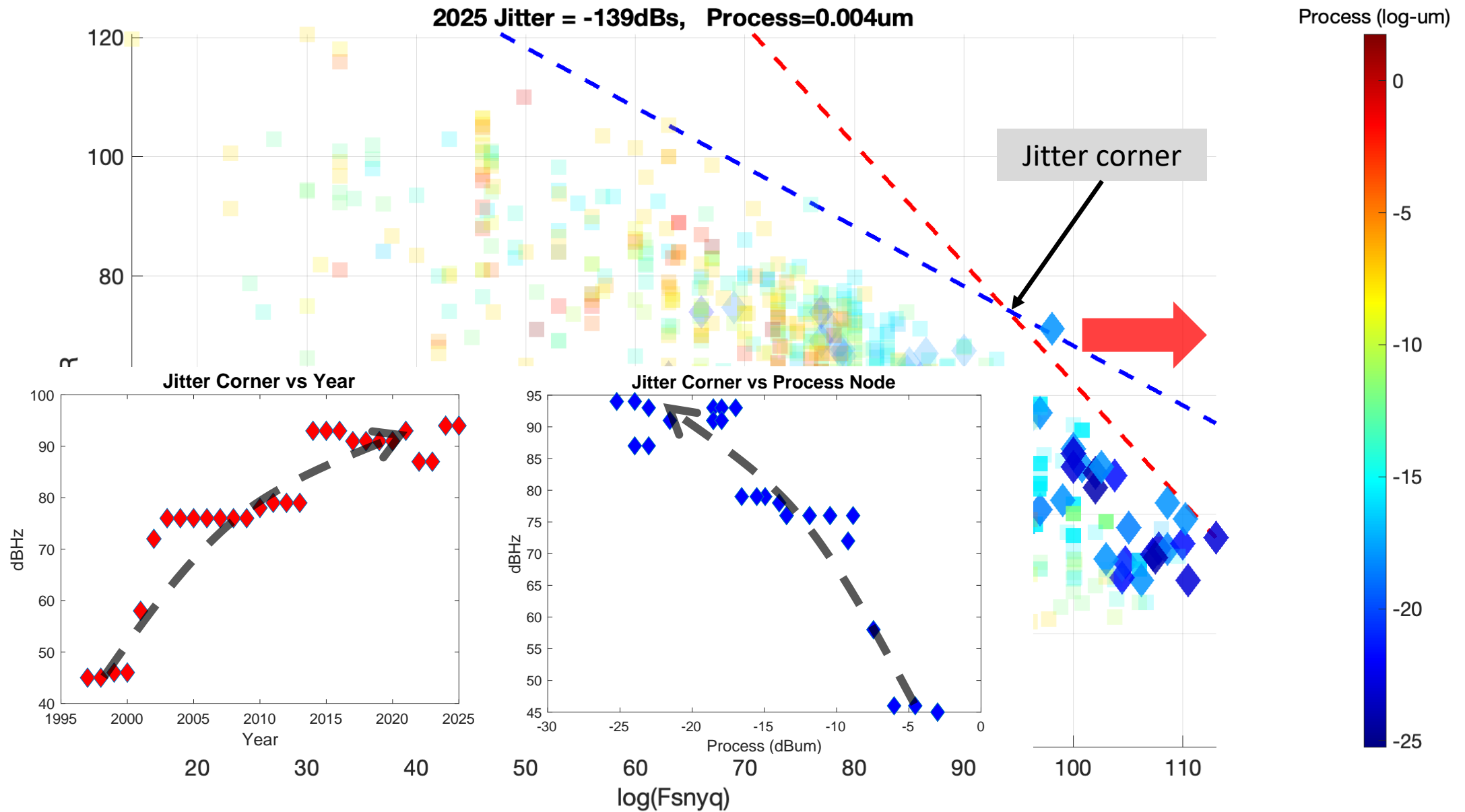
Jitter corner improvement ~ 1dB/yr, 2dBHz/dBum

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ADC Performance Trade: PAM4 vs PAM6 vs PAM8

- **Power vs frequency and SNDR tradeoff can be projected for 400G/lane**

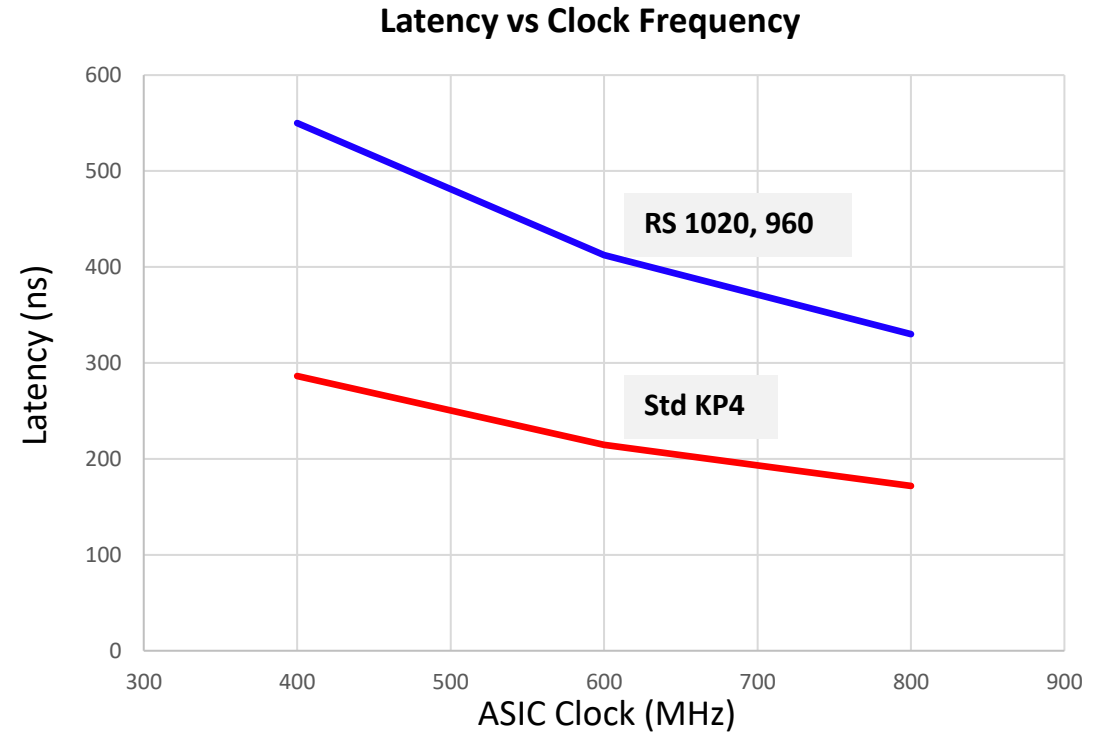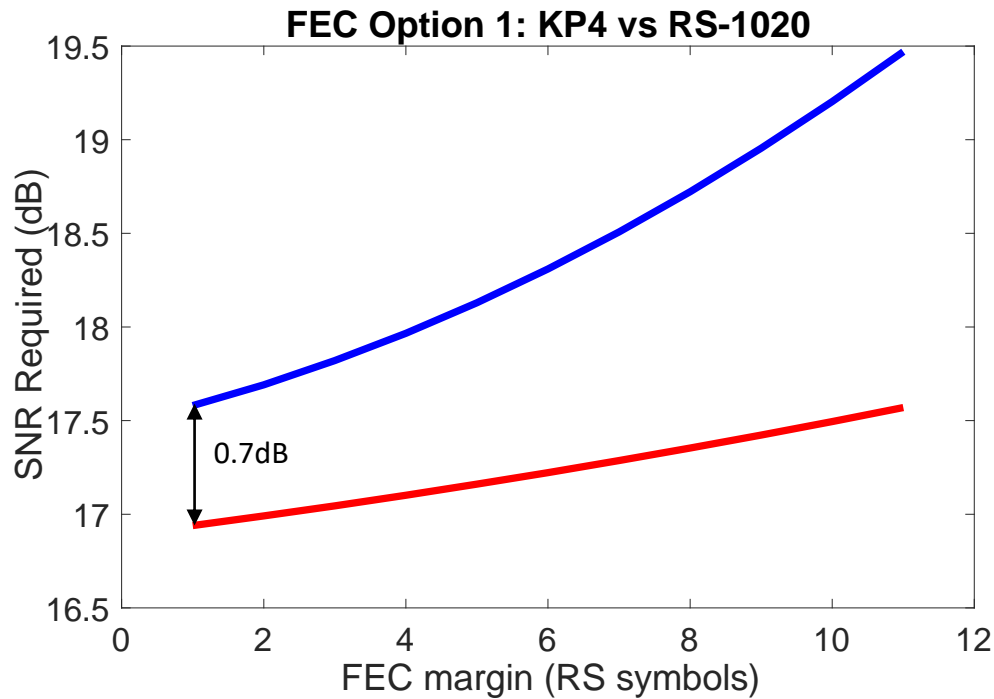|	Mean	+3σ	-3σ
Power vs Fs (dB/dB)	1.4	1.7	1.1
Power vs SNDR (dB/dB)	0.59	0.79	0.38

- **ADC efficiency Summary**

|	**PAM4**	**PAM4+3s**	**PAM4-3s**	**PAM6**	**PAM6 +3s**	**PAM6-3s**	**PAM8**	**PAM8+3s**	**PAM8-3s**
pJ/bit	**0.63**	0.54	**0.74**	**0.48**	**0.42**	**0.55**	0.56	**0.55**	0.56

  › Accounts for differences in Fs, target SNDR, and information per sample with a code rate of 0.94

  › Requires modestly improved efficiencies from 100G, but 4x faster

  › The Goldilocks choice is PAM6 from an ADC efficiency perspective, with PAM8 surprisingly close

- **The analysis is based on Channel "C" model – therefore optimistic for PAM4**

- **This represents a data-driven best-guess, not reality**

  › Actual ADC designs are likely to improve upon these numbers

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FEC improvements – Option 1) RS 1020, 960

FEC Option 1: KP4 vs RS-1020


Latency vs Clock Frequency

- **Simple upgrade to existing KP4 entailing O(n) increase in complexity**
  - › Analysis holds code rate, baud, and Nyquist frequency constant
  - › Offers ~0.7dB gain over KP4 at 1e-15 post-FEC BER, improving with FEC margin
- **~2x latency of KP4, partly offset by higher baud, parallelism and ASIC clock**

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FEC improvements – Option 2) Concatenated Code
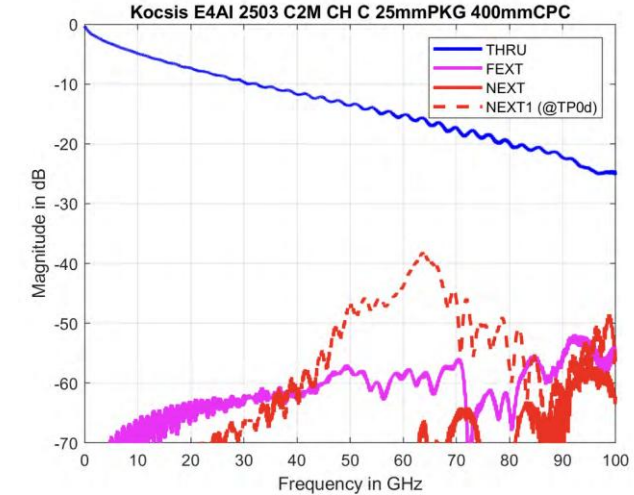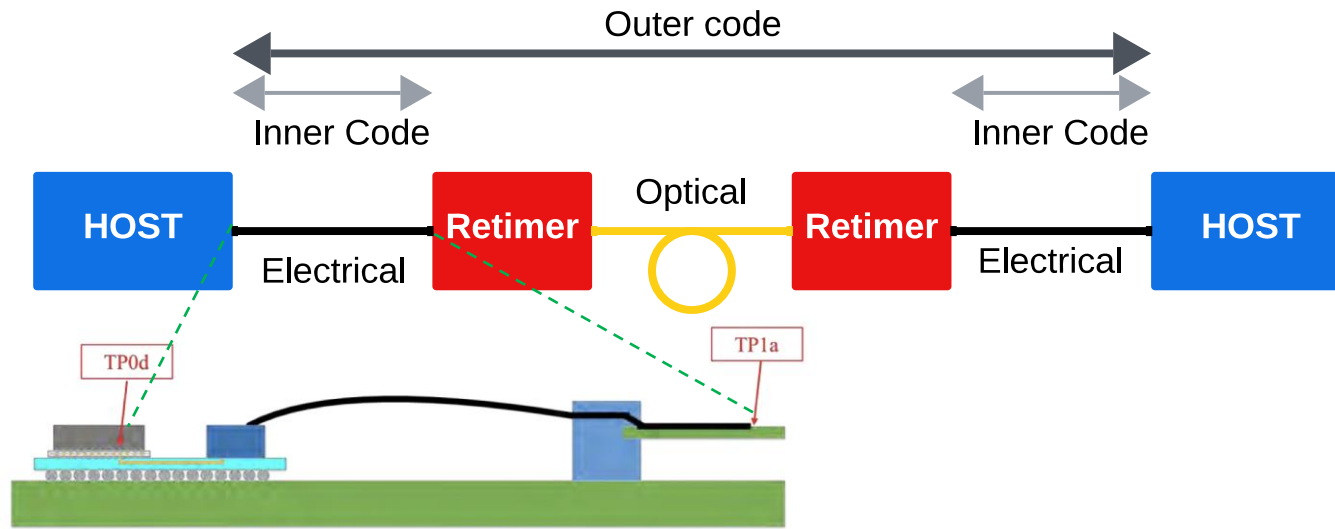
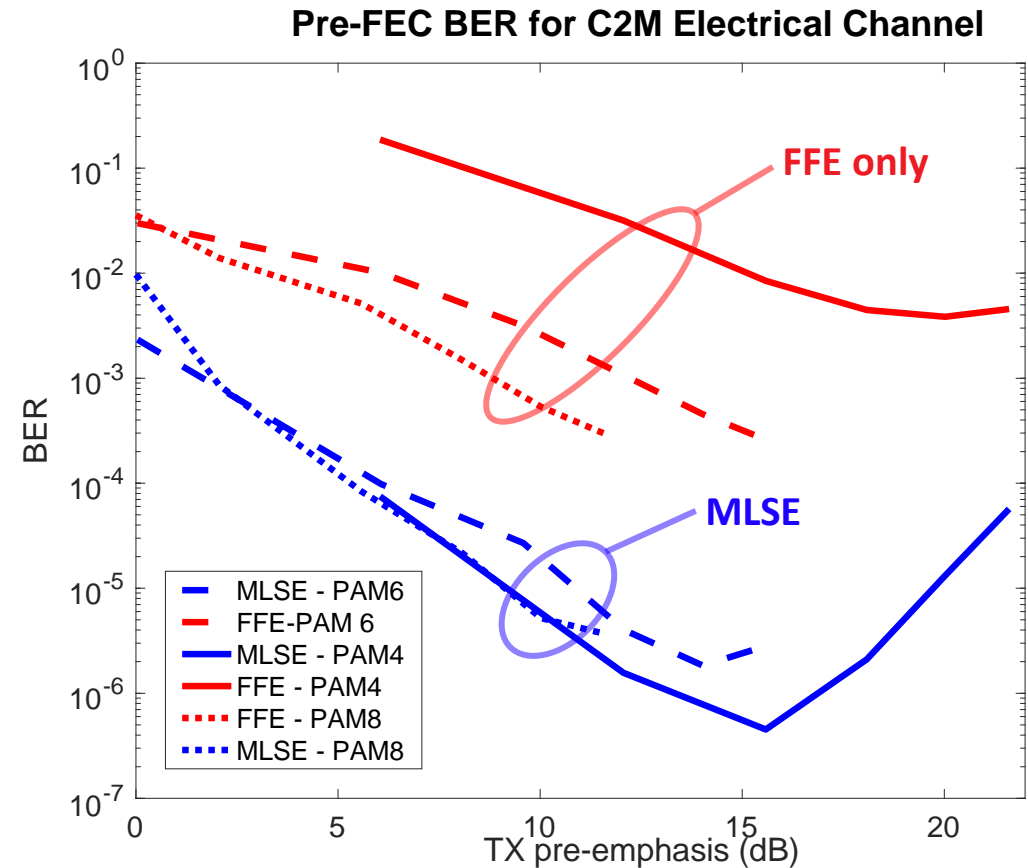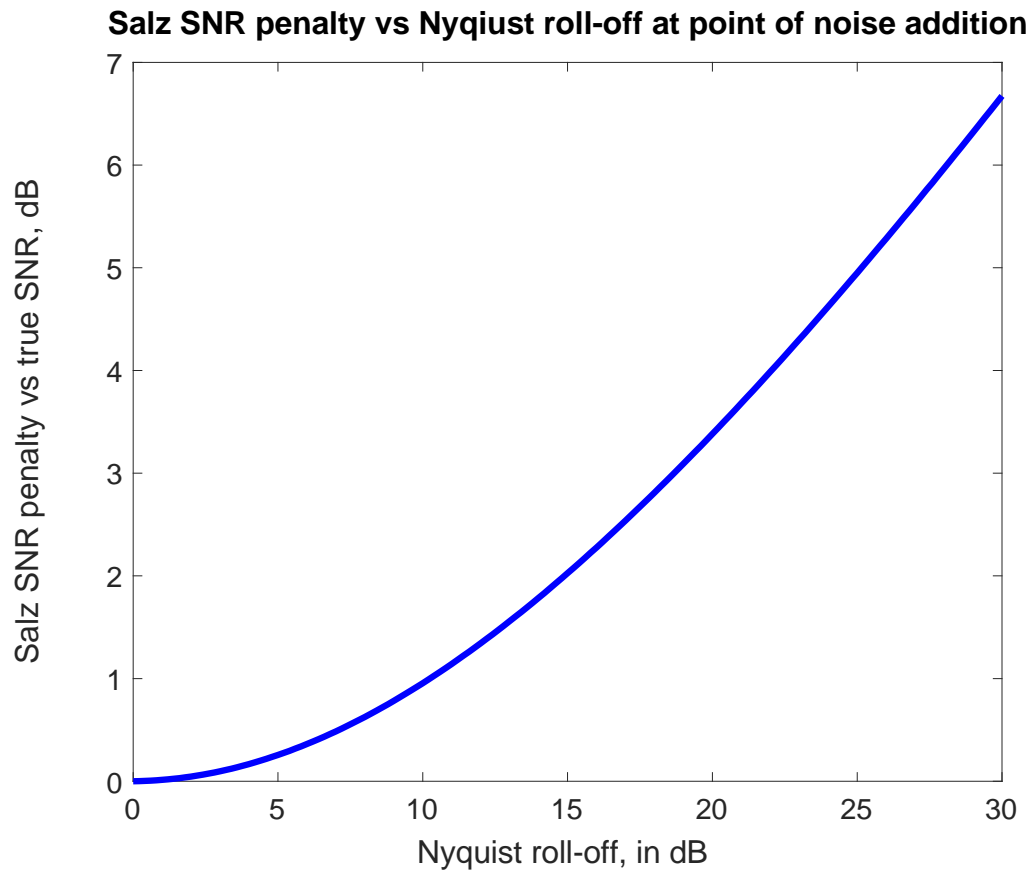**FEC Options: KP4 vs RS-1020,960 vs BCH**
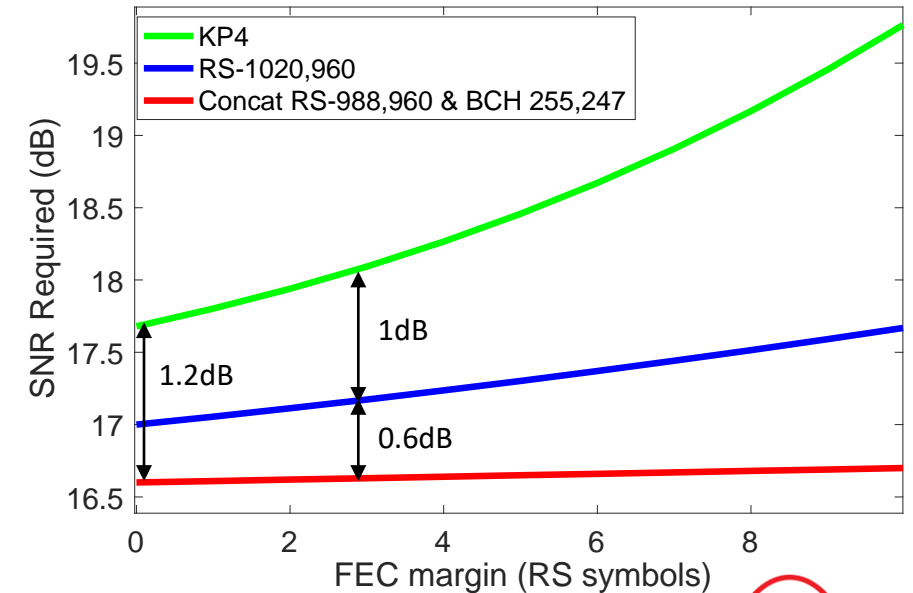
- **Higher level of protection on electrical links**
  - › Soft information enables higher code performance

- **> 1dB coding gain vs KP4 @1e-4 pre-FEC BER**

- **With very little additional SNR, retains full error correction capacity of the link**

[2] https://www.ieee802.org/3/ad_hoc/E4AI/public/25_0327/kocsis_e4ai_01_250327.pdf

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Advanced Equalization and Detection

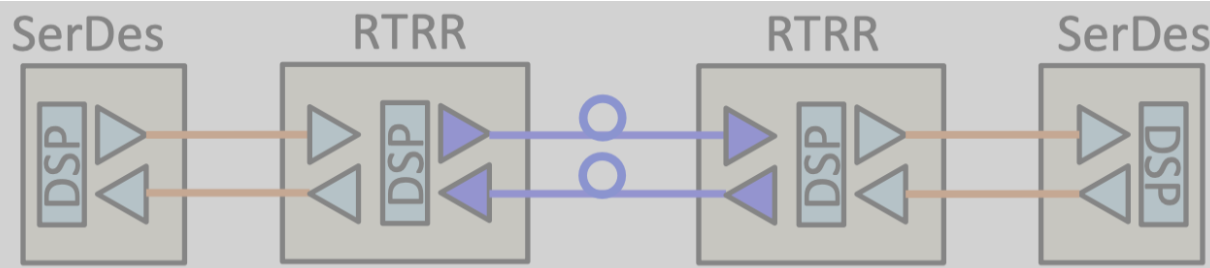Salz SNR penalty vs Nyqiust roll-off at point of noise addition

Pre-FEC BER for C2M Electrical Channel

- ■ >20 dB Nyquist loss in channel incurs heavy Salz SNR penalty
- ■ This can be mitigated via ~25dB CTLE peaking and 10-15 dB TX equalization
- ■ MLSE delivers 2-3 decades BER improvement over FFE only

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Evolution toward CPx (x=**o**ptical, **c**opper)

Retimed [3]
- Signal integrity challenge
- High power
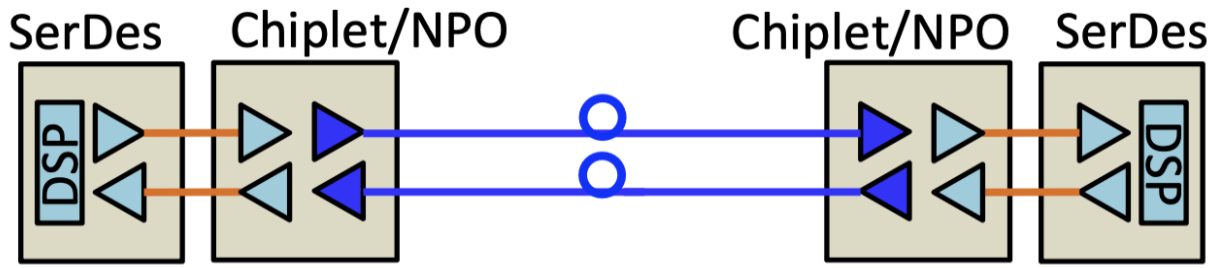
Non-Retimed
"Analog CPx" Current approach
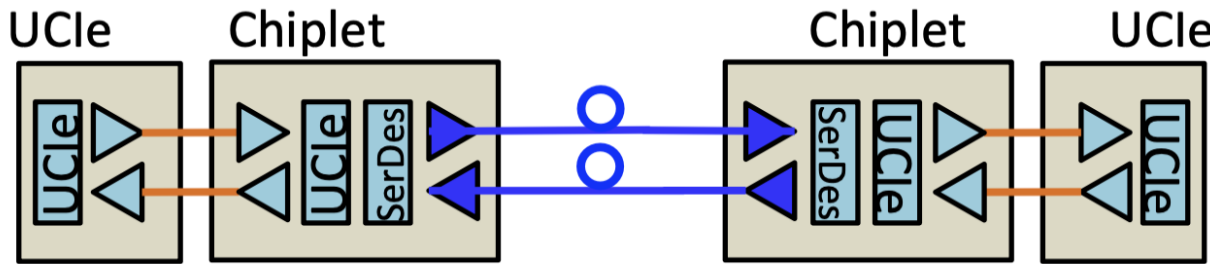
Slow Wide I/F
"Digital CPx" The way forward?

[3] Figures from "Considerations for next generation AI compute interconnect", Hutchins, Jeff, presentation given at the Technology Exploration Forum (TEF), in Santa Clara, CA on October 22-23, 2024, https://ethernetalliance.org/ethernet-in-the-age-of-ai-agenda/

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Non-Retimed Analog CPx
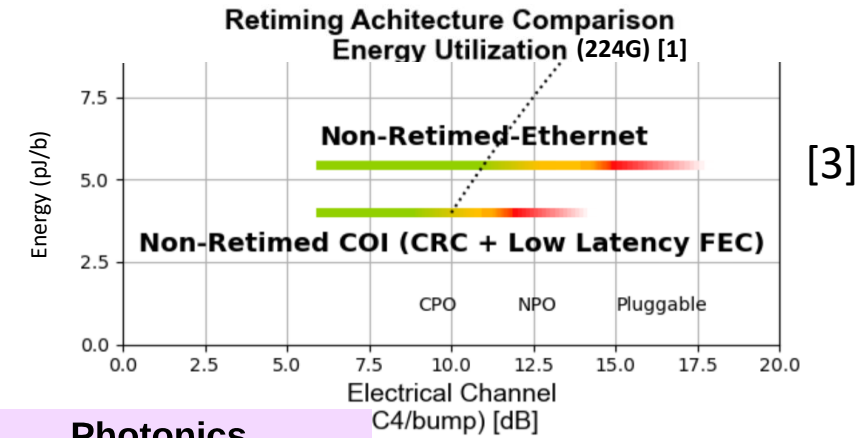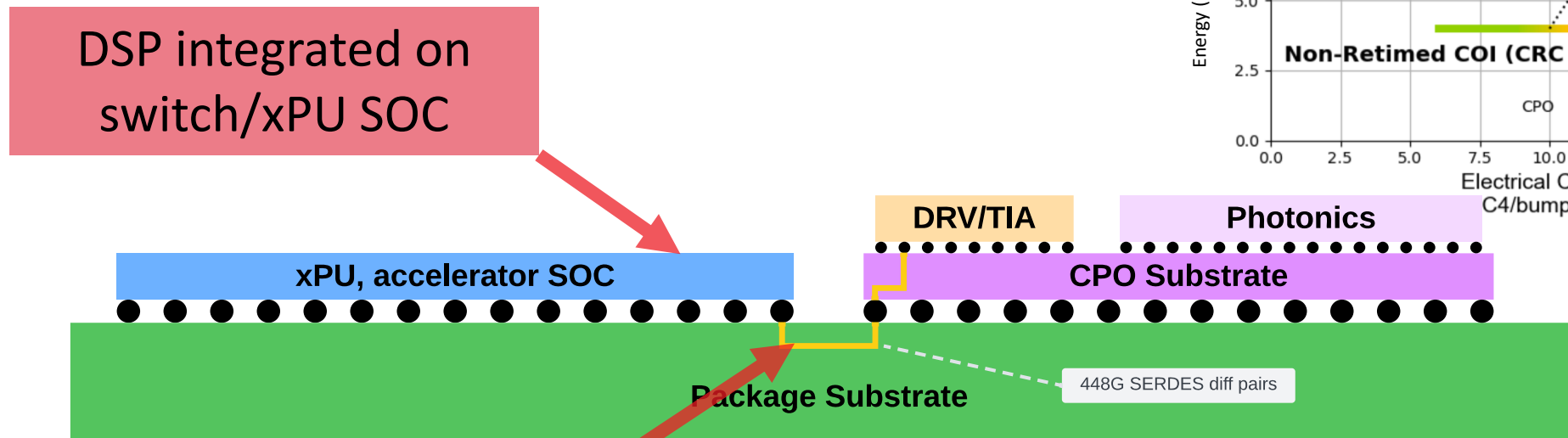
DSP integrated on switch/xPU SOC

Retiming Achitecture Comparison
Energy Utilization (224G) [1]

[3]

Non-Retimed-Ethernet

Non-Retimed COI (CRC + Low Latency FEC)

CPO   NPO   Pluggable

Energy (pJ/b) — Electrical Channel C4/bump) [dB]

DRV/TIA | Photonics

xPU, accelerator SOC | CPO Substrate

Package Substrate

448G SERDES diff pairs

- Even at 224G, ~>7.5dB channel loss[1] imposes energy penalty of ~1pJ/b
  › This interface does not scale easily to future CPx generations
- DSP/SERDES beachfront costs ~4mm per Rx/Tx 8-lane port
- Interoperability: each ASIC-CPx combo needs reoptimization & requalification
- No standard interface; vendors are not easily interchangeable

[3] Graph adapted from "Considerations for next generation AI compute interconnect", Hutchins, Jeff, presentation given at the Technology Exploration Forum (TEF), in Santa Clara, CA on October 22-23, 2024, https://ethernetalliance.org/ethernet-in-the-age-of-ai-agenda/
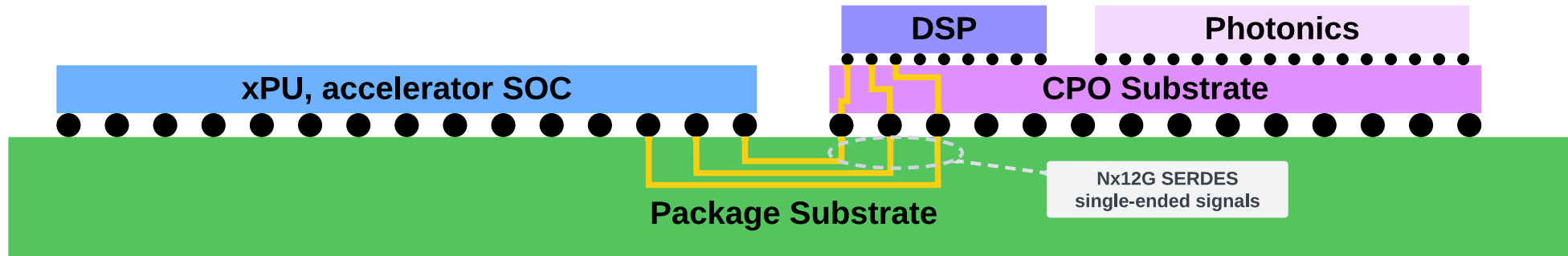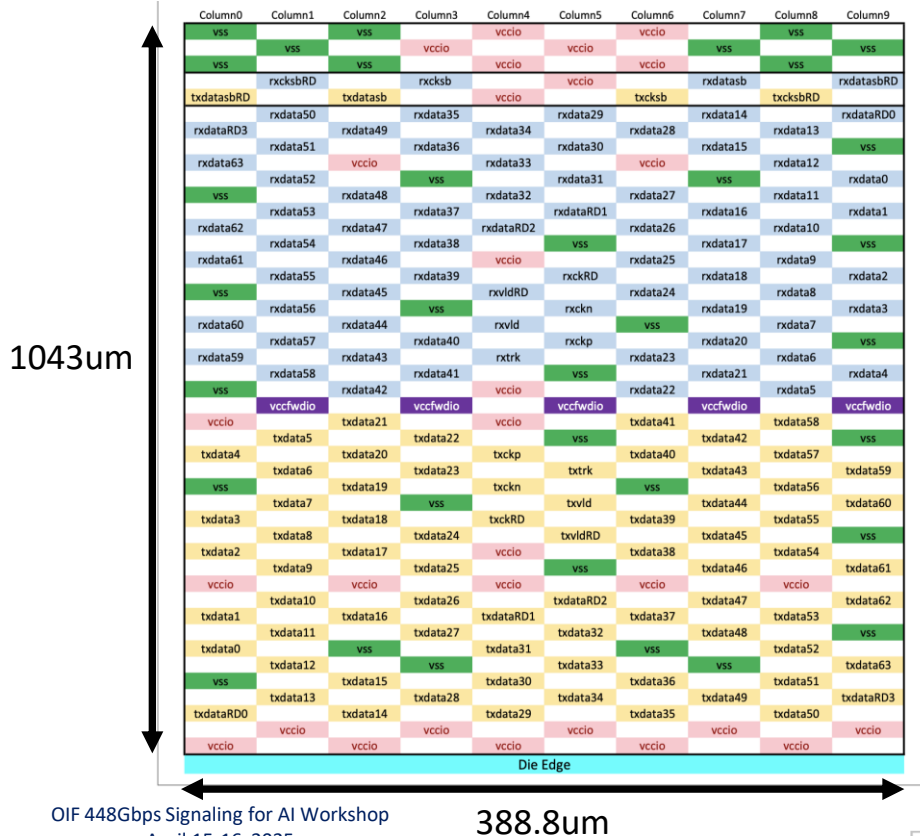
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Slow-wide UCIe Digital CPx

64 Tx/Rx UCIe Module, 12GT/s (768Gbps bidirectional) [4]

1043um

388.8um

- **High beachfront density**
  - › 3.94T/mm at 12G/lane on 2mm reach
  - › More than twice the 448G SERDES density
- **High energy efficiency**
  - › 0.25pJ/b with advanced packaging
- **Spreads SERDES heat over ~5x larger area**
- **Lane tracking and repair for reliability & yield**

[4] UCIe Specification Revision 2.0, Version 1.0 August 6, 2024

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Slow-wide Digital vs Fast-narrow Analog CPx

	Digital CPx (2mm reach)	Analog CPx
Energy (pJ/b)	0.25	~1 (driver, TIA, DAC/ADC delta)
Beachfront density (Tb/mm)	3.95 (at 12GTps)	1.8 [6]
Beachfront required for 32 ports x 8x448G bidirectional	59mm	128mm
LPO Link Budget Impact	None	>7.5dB loss
ASIC die area per port	~1.8mm^2 including bumps	~4mm^2 excluding bumps [6]
Latency impact	~<2ns	<1ns
SERDES power density [7]	20%	100%
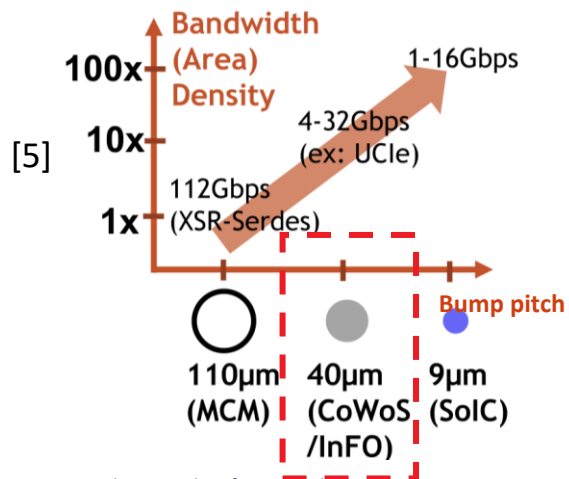
[5] Figure from "High-Bandwidth Chiplet Interconnects for Advanced Packaging Technologies in AI/ML Applications: Challenges and Solutions," Lin, Mu-Shan et al., DOI: 10.1109/OJSSCS.2024.3506694
[6] Assumes die area is comparable to 224G transceiver implementations in 3nm
[7] This is calculated as SERDES power divided by the additional footprint available to dissipate heat, due to fan-out

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More Reasons for Slow-Wide Digital CPx

- **Removes linear host-CPx channel → scalable for many generations**
  - › No board redesign, link optimization or box requal required with each CPx vendor
- **Host compatibility with any CPx device**
- **Reuse of one CPx product class across many host types (e.g. xPU)**
  - › Important for CPx economies of scale
- **Host ASICs can evolve at a rate/process node which is independent of CPx**
  - › Accelerates the innovation and deployment of new host ASICs
- **Supply chain resilience: *allows CPx vendors to be interchangeable***

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Closing statement

- PAM6 is a sensible choice from an ADC efficiency and SI standpoint
- Concatenated codes are well worth a look for resilience and performance
- Advanced equalization and detection keep front panel pluggables in play
- Slow-wide CPx interface offers big efficiency, density, ecosystem benefits

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Thank You

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