Implementation Agreement for Coherent CMIS

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TITLE: Implementation Agreement for Coherent Module Management Interface Spec

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ABSTRACT: Implementation Agreement created by the Optical Internetworking Forum for the MIS of Coherent Modules. The first module to use this MIS is based on the 400ZR spec and the first release of this document will be focused on 400ZR. The project start was approved at the Q2 Technical Meeting, April 2013 (Albuquerque, USA).

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4 Document Revision History

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Document	Date	Revisions/Comments
OIF-C-CMIS-01.0	Jan 14th 2020	Initial document release
OIF-C-CMIS-01.1	June 10th 2020	Minor update to update link to 400ZR IA and IC-TROSA

Table 1: IA Document Revision History

5 Introduction

5.1 Scope

This Implementation Agreement extends the Common Management Interface Specification [CMIS] to allow management of digital coherent optics (DCO) modules. This Implementation Agreement will be referred to as Coherent CMIS or C-CMIS and is used in conjunction with [CMIS].

Coherent CMIS defines additional management registers, messages (CDB), and monitors (VDM), together with new functionality, mechanisms, or behaviors, as needed. The relevant address spaces or name spaces have been reserved "for coherent" in [CMIS].

The initial release of C-CMIS covers 400ZR modules [400ZR IA] only, which support a single data path with eight-lane host interface for a 400GBASE-R PCS signal and a single-lane 400G coherent media interface (with a new signal format called 400ZR). However, the C-CMIS scope is expected to be extended to other types of DCO modules in the future.

NOTE – C-CMIS deliberately defines also some host side registers which are expected to be used in DCO modules only (Section 0

Host Interface registers).

5.2 Memory Page Structure

The following figure shows the organization of the memory pages described in this document. The baseline specification pages used to manage a module are defined in [CMIS].

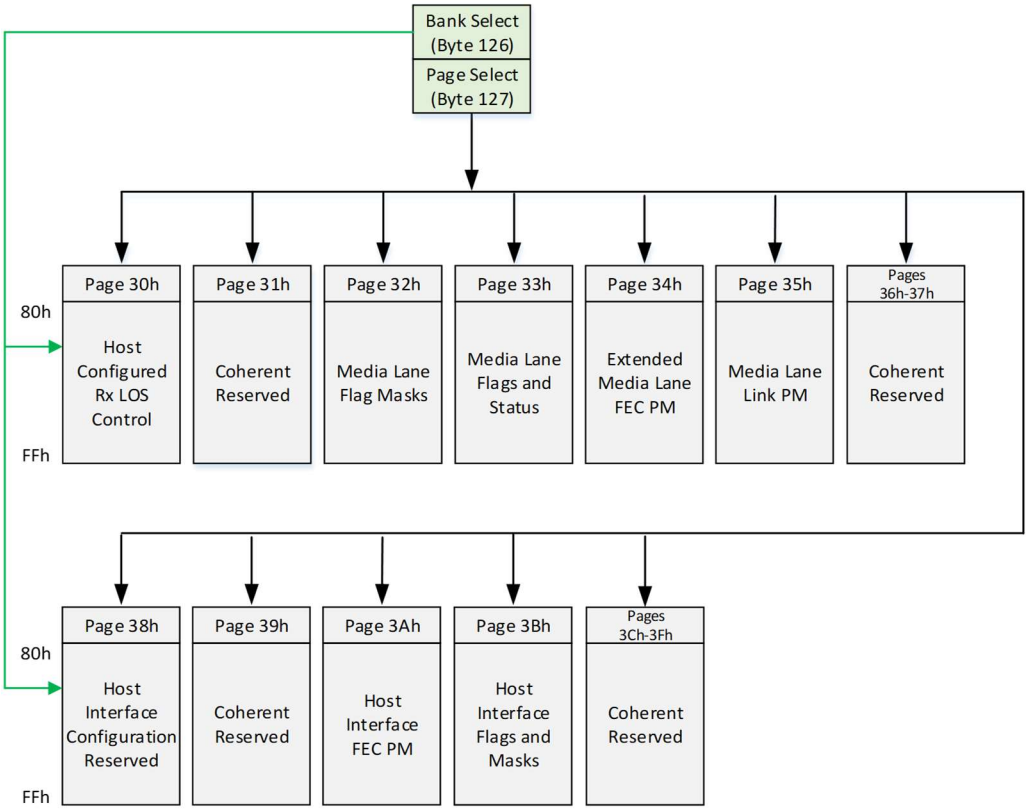

Figure 1: Diagram of Coherent Pages Extending CMIS Memory Map

5.3 Terminology Mapping (C-CMIS versus CMIS and 400ZR)

CMIS describes the function of a module with the concept of data paths carrying applications. In this model, a 400ZR module implements a single data path with eight host lanes and one media lane. This 400ZR data path can carry one of two possible applications. These 400ZR applications are referred to a “DWDM, noise limited” and “Single-Channel, loss limited”, respectively.

The CMIS register model is based on individual electrical host lanes and media lanes, with data path related attributes replicated on all lanes. However, in the context of Coherent CMIS, it is more appropriate to move away from the physical lane view and instead refer to the transported useful 400GBASE R multi-lane signal as a whole. At the same time the replication of data path related attributes across the physical lanes of the data path are avoided in the C-CMIS registers.

The 400ZR line side interface is considered to use a single media lane (wavelength), so Coherent CMIS will continue to refer to the network side related registers as media lane registers.

The 400ZR host side interface of a 400ZR application is 400GAUI-8, an eight-lane electrical interface which is an example of a multi-lane interface. All registers pertaining to processing the entire client signal carried over this multi lane interfaces are referred to as host interface registers (there is no duplication of these registers for individual lanes).

To prepare for future modules possibly providing more than one data path, strictly we need to distinguish a module's host interface and media interface from the host interface and media interface of an individual data path.

To simplify the language and because of its data path centric view, C-CMIS uses the term host interface and media interface always in relation to a data path. If (rarely) the module view is needed, we use the prefixed terms module host interface and module media interface.

5.4 Register Nomenclature:

5.4.1 Register Names

The register naming convention is camelback. The names are unique within the table.

5.4.2 Register Data Notation

When referring to register data types, the following data notation is used:

Data Notation	Data Type
U8	Unsigned 8 bit register
U16	Unsigned 16 bit register
S16	Signed 16 bit register
U32	Unsigned 32 bit register
S32	Signed 32 bit register
U64	Unsigned 64 bit register
S64	Signed 64 bit register
F16	16 bit floating point register
F32	32 bit floating point register

5.4.3 Register Address Notation

When referring to certain registers, bits, or fields using the following address notation is used:

<reference> := [<bank-range>: [<page-range>:]] <byte-range> [.<bit-or-field>]
<bank-range> := [<bank>-]<bank>
<page-range> := [<page>-]<page>
<bit-or-field> := <bit>[-<bit>]
<bit> := “single digit decimal” (0 … 7)
<byte> := “decimal” (0 … 255)
<page> := “hexadecimal” (00h … FFh)

<bank> := “decimal” (0 … 255)

Table 2 - Register Notation Description

Example notation	Description of displayed register	Description of Register
1h:30h:128-129	Any valid bank, page 30h bytes 128-129	Lane 2 Rx Channel Power Monitor
85	Lower memory 0, Byte 85	Module Type advertising code
04h:128.2-1	Page 04h, Byte 128, Bits 2 and 1	12.5 and 6.25 GHz grid supported
1:30h:146.1	Bank 1 page 30h, Byte 146, bit 1	Lane 2 Rx Power Monitor Type

Table 3 - Register notation Example

6 Implementation Notes

6.1 400ZR implementation notes

This section specifies how certain CMIS features shall be used by 400ZR modules.

6.1.1 400ZR CMIS Module Application Advertisement

CMIS requires pluggable modules to identify supported application in the Application Advertising tables 00h:85-117 and 01h:176.

A 400ZR module advertises its default application code in 00h:85-89 and 01h:176 as illustrated in Table 2.

A dual mode 400ZR module will have to advertise both applications.

Table 4 CMIS Application Advertisement for 400ZR

Byte	Bits	ApSel Code	Name	Value	Description
85	7-0	N/A	Module Type Encoding	02h	Optical Interface: SMF
86	7-0	0001b	Host Electrical Interface Code	11h	400GAUI-8 C2M
87	7-0		Module Media Interface Code	TBD	see note 1 below
88	7-4		Host Lane Count	1000b	8 host electrical lanes
	3-0		Media Lane Count	0001b	1 media lane
89	7-0		Host Lane Assignment Options	01h	Permissible first host lane number for Application: lane 1
01h:176	7-0		Media Lane Assignment Options	01h	Permissible first media lane number for Application: lane 1

Note 1: Module Media Interface Codes are generally defined in SFF-8024. Two codes are foreseen for the 400ZR application (TBD for amplified and unamplified, where TBD will be replaced by the actual codes once the ID is available).

6.1.2 400ZR Loopback Implementation

Generic register-based management of 400ZR loopbacks shall be possible via the existing CMIS registers. Note that CMIS allows to manage only four loopbacks while a 400ZR module actually provides a set of six loopbacks.

Table 5: Loopback Mapping to CMIS describes the six 400ZR loopbacks and their possible mapping to the four CMIS controls, including the default mapping. Vendors can choose a non-default set of 4 loopbacks and they must clearly document what they have selected. If a vendor chooses to implement the Modem Rx loopback, they can use it as the Media Side Input or as the Host Side Output loopback. If a vendor chooses to implement the Modem Tx loopback, they can use it as the Host Side Input or as the Media Side Output loopback.

Table 5: Loopback Mapping to CMIS

400 ZR Loopback Name	CMIS Loopback	Default	Description
Media Side Rx Loopback	Media Side Input	Y	Loopback in DSP. After polarity split and symbol de-interleave -> Grey mapper, symbol Interleave. Network loop timed.
Modem Rx Loopback	Media Side Input or Host Side Output	N	Loopback after GMP De-mapping -> GMP mapping. Data retransmitted relative to local clock.
Host Side Rx Loopback	Host Side Output	Y	Loopback after distribution/interleaving block on host ingress path, and before lane reorder and interleave
Host Side Tx Loopback	Host Side Input	Y	Loopback after Alignment lock and lane Deskew -> PMA sublayer. Host loop timed.
Modem Tx Loopback	Host Side Input or Media Side Output	N	Loopback after GMP mapping -> GMP Demapping. Data re-transmitted relative to local clock
Media Side Tx Loopback	Media Side Output	Y	Loopback after TX DSP processing blocks and before RX DSP processing blocks

7 Coherent Extensions to CMIS

This chapter defines the extensions to CMIS referred to as C-CMIS.

7.1 PM Interval

The PM interval is defined by the host. The host uses the latch handshaking mechanism that is defined in [CMIS]. The basic update period for VDM monitors is defined as one second.

7.2 Flag Conformance

Table 7: Identifiers for Coherent Monitors describes the flag conformance for all lane-specific flags, per Data Path State. In Data Path States where a flag is indicated as 'Not Allowed', the module shall not set the associated flag bit while the data path is in that state. The flag conformance shown in Table 6 Coherent Lane Specific Flag Conformance is applicable to High Alarm, Low Alarm, High Warning and Low Warning for each listed VDM Coherent Identifier and other coherent flags.

DataPath Deactivated	DataPath Initialized	DataPathInit	DataPathDeinit	DataPath Activated	DataPath TxTurnOn	DataPath TxTurnOff
Not Allowed	Allowed	Not Allowed	Not Allowed	Allowed	Allowed	Allowed

Table 6 Coherent Lane Specific Flag Conformance

7.3 Versatile Diagnostics Monitor (VDM) Extensions

The VDM functionality and some basic VDM monitors are defined in CMIS. Each VDM monitor has an associated numerical identifier, and the identifiers for C-CMIS defined monitors are defined in Table 7: Identifiers for Coherent Monitors (taking values from a range reserved for C-CMIS).

Note: If there is agreement on the flag conformance shown in Table 7: Identifiers for Coherent Monitors, the table could be replaced with a statement on which States the conformance is Allowed or Not Allowed since the VDM Coherent Identifiers share the same flag conformance.

- the module shall update the register values of VDM real-time (current value) monitors every second.

- the module shall update the register values of VDM statistics (min, max, average) monitors every second, unless the host has requested to latch statistics registers via the CMIS Latch Request bit 2Fh:144.7 (see [CMIS] for a description of the latching mechanism and its usage).

7.3.1 Data path Monitors

Unless specified differently, the VDM monitors for a DCO are all associated with a data path. Thererfore, the Lane or Data Path Identifier (bits 3-0 of the MSB of VDM Configuration Registers in pages 20h-23h) of those VDM monitors shall indicate the first lane of the relevant data path.

Table 7: Identifiers for Coherent Monitors

Identifier	Description	Data Type	LSB Scaling	Unit
128	Modulator Bias X/I	U16	100/65,535	%
129	Modulator Bias X/Q	U16	100/65,535	%
130	Modulator Bias Y/I	U16	100/65,535	%
131	Modulator Bias Y/Q	U16	100/65,535	%
132	Modulator Bias X_Phase	U16	100/65,535	%
133	Modulator Bias Y_Phase	U16	100/65,535	%
134	CD – high granularity, short link	S16	1	Ps/nm
135	CD – low granularity, long link	S16	20	Ps/nm
136	DGD	U16	0.01	Ps
137	SOPMD	U16	0.01	Ps^2
138	PDL	U16	0.1	dB
139	OSNR	U16	0.1	dB
140	eSNR	U16	0.1	dB
141	CFO	S16	1	MHz
142	EVM_modem	U16	100/65,535	%
143	Tx Power	S16	0.01	dBm
144	Rx Total Power	S16	0.01	dBm
145	Rx Signal Power	S16	0.01	dBm
146	SOP ROC	U16	1	krad/s
147	MER	U16	0.1	dB

Note: If there are multiple TECs in a lane then the module may aggregate information from these TECs.

7.4 Media Interface registers

Media interface registers are in banked pages with each bank referring to the media interface of a single media lane (wavelength). The bank index of a data path is the smallest index of the media lanes belonging to the data path.

Table 8: Media Interface registers

Page Number	Page Description	Notes

30h	Media Lane Configurable Thresholds	
31h	Media Lane Provisioning	
32h	Media Lane Flag Masks	
33h	Media Lane Flags and Status	
34h	Media Lane FEC Performance Monitoring	
35h	Media Lane Link Performance Monitoring	
36-37h	Reserved	

7.4.1 Media Lane Configurable Thresholds (page30h)

Page 30h is a banked page with each bank referring to the media interface of a single media lane (wavelength). The bank index of a data path is the smallest index of the media lanes belonging to the data path.

7.4.2 Power related thresholds

Page 30h allows the host to configure optical receive power related thresholds, alarms or warnings flags, and masks. By default, the module uses thresholds advertised in page 02h, however, hosts can program their own thresholds in page 30h. These configured thresholds must be in the range advertised by the module on page 41h.

Hysteresis around the thresholds is left as an implementation detail.

7.4.3 Link degradation feature

Page 30h allows to configure link degradation detection and reporting for two types of link degradations [400ZR IA]: FEC Detected Degrade (FDD) and FEC Excessive Degrade (FED).

Link degradation detection requires monitoring the pre-FEC BER over a performance monitoring interval, as described in detail in [400ZR IA].

When FDD reporting is enabled in 30h:168.0, the module compares the average BER computed over the PM interval against two thresholds: When the average BER exceeds the activate FDD BER threshold, FDD is asserted and the alarm bit 33h:132.0 (FECdetectdegraded) is set. When the average BER drops below the clear FDD BER threshold, FDD is deasserted and the alarm bit clears.

When FED is enabled in 30h:168.1, the module performs analogous operations using the FED thresholds and reports FED via alarm bit 33h:132.1 (FECexcessdegraded).

Table 9: Media Lane Configurable Thresholds (Page 30h)

Byte	Bits	Name	Description	Type
Power Alarm Thresholds				
128-129	15-0	totalPwrHiAlarmThresh	Configured threshold for Rx Total Power high alarm. S16 in increments of 0.01 dBm.	RW Opt.
130-131	15-0	totalPwrLoAlarmThresh	Configured threshold for Rx Total Power low alarm. S16 in increments of 0.01 dBm.	RW Opt.
132-133	15-0	totalPwrHiWarnThresh	Configured threshold for Rx Total Power high warning. S16 in increments of 0.01 dBm.	RW Opt.
134-135	15-0	totalPwrLoWarnThresh	Configured threshold for Rx Total Power low warning. S16 in increments of 0.01 dBm.	RW Opt.
136-137	15-0	sigPwrHiAlarmThresh	Configured threshold for Rx Signal Power high alarm. S16 in increments of 0.01 dBm.	RW Opt.
138-139	15-0	sigPwrLoAlarmThresh	Configured threshold for Rx Signal Power low alarm. S16 in increments of 0.01 dBm.	RW Opt.
140-141	15-0	sigPwrHiWarnThresh	Configured threshold for Rx Signal Power high warning. S16 in increments of 0.01 dBm.	RW Opt.
142-143	15-0	sigPwrLoWarnThresh	Configured threshold for Rx Signal Power low warning. S16 in increments of 0.01 dBm	RW Opt.
144	7-2	Reserved	Reserved	RO
	1	totalPwrUseCfgThresh	This bit selects between default and host configured thresholds for Rx total power monitor from the VDM identifier table. 0 = default 1= host configured	RW Opt.
	0	sigPwrUseCfgThresh	This bit selects between default and host configured thresholds for Rx signal power monitor from the VDM identifier table. 0 = default 1= host configured	RW Opt.
145 - 159	All	Reserved	Reserved	RO
Degrade Thresholds				
160-161	15-0	fddRaiseThresh	media Rx BER threshold for FEC Detected Degrade (FDD) to be set active. F16 BER floating point format	RW Opt.
162 - 163	15-0	fddClearThresh	media Rx BER threshold for FEC Detected Degrade (FDD) to clear. F16 BER floating point format	RW Opt.
164 - 165	15-0	fedRaiseThresh	media Rx BER threshold for FEC Excessive Degrade (FED) to be set active. F16 BER floating point format	RW Opt.

166 - 167	15-0	fedClearThresh	media Rx BER threshold for FEC Excessive Degrade (FED) to clear. F16 BER floating point format	RW Opt.
Degrade Feature Advertisement				
168	7-2	Reserved		RO
	1	fedEnable	enable for media Rx FEC Excessive Degrade (FED) monitoring feature.	RW Opt.
	0	fddEnable	enable for media Rx FEC Detected Degrade (FDD) monitoring feature	RW Opt.
169-255	All	Reserved		RO

7.4.4 Media Lane Provisioning (Page 31h)

Page 31h contains parameters for coherent provisioning. It is a banked page with each bank corresponding to a unique media lane.

Table 10: Media Lane Provisioning (Page 31h)

Byte	Bits	Name	Description	Type
128	7-2	Reserved	Reserved for future	RO
	1	lfInsertionOnLdEnable	Enable for insertion of LF on the detection of LD. Default is disabled.	RW Opt.
	0	txFilterEnable	Enable for Tx Transmit shape control	RW Opt.
129	7-0	txFilterType	The type of Tx shaping to be used. 1 = Root-Raised-Cosine 2 = Raised-Cosine 3 = Gaussian	RW Opt.
130	7-0	txFilterRollOff	Scaled roll off factor (0.0 to 1.0). U8 in increments of 1/255	RW Opt.
131-255	All	Reserved	Reserved	RO

7.4.5 Media Lane Flag Masks (Page 32h)

Page 32h contains the masks for the media lane alarms. It is a banked page with each bank corresponding to a unique media lane.

Table 11: Media Lane Flag Masks (Page 32h)

Byte	Bits	Name	Description	Type
128	7-6	Reserved	Reserved for future Tx Lane Status Masks	RO
	5	mTxLoa	Mask for (vendor defined) Tx Loss of Alignment alarm	RW Opt.

	4	mTxOoa	Mask for (vendor defined) Tx Out of Alignment alarm	RW Opt.
	3	mTxLolCmu	Mask for (vendor defined) Tx CMU Loss of Lock alarm	RW Opt.
	2	mTxLolRefClk	Mask for (vendor defined) Tx Reference Clock Loss of Lock alarm	RW Opt.
	1	mTxLolDeSkew	Mask for (vendor defined) Tx Deskew Loss of Lock alarm	RW Opt.
	0	mTxFIFO	Mask for (vendor defined) Tx FIFO Error	RW Opt.
129	7-0	Reserved	Reserved for future Tx Lane Status Masks	RO
130	7-6	Reserved	Reserved for future Rx Lane Status Masks	RO
	5	mRxLolDemod	Mask for (vendor defined) Rx Demodulator Loss of Lock	RW Opt.
	4	mRxLolCd	Mask for (vendor defined) Rx Chromatic Dispersion Compensation Loss of Lock	RW Opt.
	3	mRxLoa	Mask for (vendor defined) Rx Loss of Alignment alarm	RW Opt.
	2	mRxOoa	Mask for (vendor defined) Rx Out of Alignment alarm	RW Opt.
	1	mRxLolDeskew	Mask for (vendor defined) Rx Deskew Loss of Lock alarm	RW Opt.
	0	mRxLolFifo	Mask for (vendor defined) Rx FIFO Error	RW Opt.
131	7-0	Reserved	Reserved for future Rx Lane Status Masks	RO
132	7-2	Reserved	Reserved	RO
	1	mRxFedPm	Mask for FEC Excessive Degrade (FED) over PM Interval alarm	RW Opt.
	0	mRxFddPm	Mask for FEC Detected Degrade (FDD) over PM Interval alarm	RW Opt.
133	7-3	Reserved	Reserved	RO
	2	mRD	Mask for Remote Degrade alarm	RW Opt.
	1	mLD	Mask for Local Degrade alarm	RW Opt.
	0	mRPF	Mask for Remote Phy Fault alarm	RW Opt.
134-255	All	Reserved	Reserved	RO

7.4.6 Media Lane Flags and Status (Page 33h)

Page 33h contains the latches for the media lane alarms. It is a banked page with each bank corresponding to a unique media lane.

Table 12: Media Lane Flags and Status (Page 33h)

Byte	Bits	Name	Description	Type
128	7-6	Reserved	Reserved for future Tx Lane Status Latches	RO
	5	lTxLoa	Latched (vendor defined) Tx Loss of Alignment alarm	COR opt
	4	lTxOoa	Latched (vendor defined) Tx Out of Alignment alarm	COR opt
	3	lTxLolCmu	Latched (vendor defined) Tx CMU Loss of Lock alarm	COR opt
	2	lTxLolRefClk	Latched (vendor defined) Tx Reference Clock Loss of Lock alarm	COR opt
	1	lTxLolDeSkew	Latched (vendor defined) Tx Deskew Loss of Lock alarm	COR opt
	0	lTxFIFO	Latched (vendor defined) Tx FIFO Error	COR opt
129	7-0	Reserved	Reserved for future Tx Lane Status Latches	RO
130	7-6	Reserved	Reserved for future Rx Lane Status Latches	RO
	5	lRxLolDemod	Latched (vendor defined) Rx Demodulator Loss of Lock	COR opt
	4	lRxLolCd	Latched (vendor defined) Rx Chromatic Dispersion Compensation Loss of Lock	COR opt
	3	lRxLoa	Latched (vendor defined) Rx Loss of Alignment alarm	COR opt
	2	lRxOoa	Latched (vendor defined) Rx Out of Alignment alarm	COR opt
	1	lRxLolDeskew	Latched (vendor defined) Rx Deskew Loss of Lock alarm	COR opt
	0	lRxLolFifo	Latched (vendor defined) Rx FIFO Error	COR opt
131	7-0	Reserved	Reserved for future Rx Lane Status Latches	RO
132	7-2	Reserved	Reserved	RO
	1	lRxFedPm	Latched FEC Excessive Degrade (FED) over PM Interval alarm	COR opt
	0	lRxFddPm	Latched FEC Detected Degrade (FDD) over PM Interval alarm	COR opt
133	7-3	Reserved	Reserved	RO
	2	lRD	Latched Remote Degrade alarm	COR opt
	1	lLD	Latched Local Degrade alarm	COR opt
	0	lRPF	Latched Remote Phy Fault alarm	COR opt

134-255	All	Reserved	Reserved	RO

7.4.7 Media Lane FEC Performance Monitoring (page 34h)

Page 34h contains read-only media FEC performance monitoring counters. The module collects the information in these registers during the prior PM interval. Page 34h is a banked page with each bank referring to a single media lane. For example, if the module supports 2 media lanes, then bank 1 will be used for lane 2.

Table 13: Media Lane FEC Performance Monitoring (Page 34h)

Byte	Bits	Name	Description	Type
128-135	63-0	rxBitsPm	Number of bits received during prior PM interval. U64 with MSB in byte 128.	RO opt
136-143	63-0	rxBitsSubIntPm	Number of bits received during any sub-interval of prior PM interval. U64 with MSB in byte 136.	RO opt
144-151	63-0	rxCorrBitsPm	Number of corrected bits during prior PM interval. U64 with MSB in byte 144.	RO opt
152-159	63-0	rxMinCorrBitsSubIntPm	Minimum number of corrected bits over any sub-interval during prior PM interval. U64 with MSB in byte 152.	RO opt
160-167	63-0	rxMaxCorrBitsSubIntPm	Maximum number of corrected bits over any sub-interval during prior PM interval. U64 with MSB in byte 160.	RO opt
168-171	31-0	rxFramesPm	Number of frames received during prior PM interval. U32 with MSB in byte 168.	RO opt
172-175	31-0	rxFramesSubIntPm	Number of frames received over any sub-interval during prior PM interval. U32 with MSB in byte 172.	RO opt
176-179	31-0	rxFramesUncorrErrPm	Number of frames received with uncorrectable errors during prior PM interval. U32 with MSB in byte 176.	RO opt
180-183	31-0	rxMinFramesUncorrErrSubintPm	Minimum number of frames received with uncorrectable errors over any sub-interval during prior PM interval. U32 with MSB in byte 180.	RO opt
184-187	31-0	rxMaxFramesUncorrErrSubintPm	Maximum number of frames received with uncorrectable errors over any sub-interval during prior PM interval. U32 with MSB in byte 184.	RO opt
188-255	All	Reserved		RO

7.4.8 Media Lane Link Performance Monitoring (page 35h)

Page 35h contains optional media lane read-only statistics reporting on the link performance. The module collects the information in these registers during the prior PM interval. Page 35h is a banked page with each bank referring to a single media lane. For example, if the module supports 2 media lanes, then bank 1 will be used for lane 2. All media interface link performance monitors supported in page 35h shall also support a corresponding real-time VDM monitor (in page 20h-2Fh).

Table 14: Media Lane Link Performance Monitoring (Page 35h)

Byte	Bits	Name	Description	Type
128-131	31-0	rxAvgCdPm	Average value of DSP compensated chromatic dispersion over PM interval. S32 in increments of 1ps/nm.	RO Opt.
132-135	31-0	rxMinCdPm	Minimum value of DSP compensated chromatic dispersion over PM interval. S32 in increments of 1ps/nm.	RO Opt.
136-139	31-0	rxMaxCdPm	Maximum value of DSP compensated chromatic dispersion over PM interval. S32 in increments of 1ps/nm.	RO Opt.
140-141	15-0	rxAvgDgdPm	Average value of differential group delay over PM interval. U16 in increments of 0.01ps.	RO Opt.
142-143	15-0	rxMinDgdPm	Minimum value of differential group delay over PM interval. U16 in increments of 0.01ps.	RO Opt.
144-145	15-0	rxMaxDgdPm	Maximum value of differential group delay over PM interval. U16 in increments of 0.01ps.	RO Opt.
146-147	15-0	rxAvgSopmdPm	Average value of SOPMD over PM interval. U16 in increments of 0.01ps^2.	RO Opt.
148-149	15-0	rxMinSopmdPm	Minimum value of SOPMD over PM interval. U16 in increments of 0.01ps^2.	RO Opt.
150-151	15-0	rxMaxSopmdPm	Maximum value of SOPMD over PM interval. U16 in increments of 0.01ps^2.	RO Opt.
152-153	15-0	rxAvgPdlPm	Average value of polarization dependent loss over PM interval. U16 in increments of 0.1dB.	RO Opt.
154-155	15-0	rxMinPdlPm	Minimum value of polarization dependent loss over PM interval. U16 in increments of 0.1dB.	RO Opt.
156-157	15-0	rxMaxPdlPm	Maximum value of polarization dependent loss over PM interval. U16 in increments of 0.1dB.	RO Opt.
158-159	15-0	rxAvgOsnrPm	Average value of OSNR estimate over PM interval. U16 in increments of 0.1dB.	RO Opt.
160-161	15-0	rxMinOsnrPm	Minimum value of OSNR estimate over PM interval. U16 in increments of 0.1dB.	RO Opt.

162-163	15-0	rxMaxOsnrPm	Maximum value of OSNR estimate over PM interval. U16 in increments of 0.1dB.	RO Opt.
164-165	15-0	rxAvgEsnrPm	Average value of eSNR over PM Interval. U16 in increments of 0.1 dB.	RO Opt.
166-167	15-0	rxMinEsnrPm	Minimum value of eSNR over PM Interval. U16 in increments of 0.1 dB.	RO Opt.
168-169	15-0	rxMaxEsnrPm	Maximum value of eSNR over PM Interval. U16 in increments of 0.1 dB.	RO Opt.
170-171	15-0	rxAvgCfoPm	Average value of carrier frequency offset over PM interval. S16 in increments of 1MHz.	RO Opt.
172-173	15-0	rxMinCfoPm	Minimum value of carrier frequency offset over PM interval. S16 in increments of 1MHz.	RO Opt.
174-175	15-0	rxMaxCfoPm	Maximum value of carrier frequency offset over PM interval. S16 in increments of 1MHz.	RO Opt.
176-177	15-0	rxAvgEvmModemPm	Average value of error vector magnitude of the modem over PM interval. U16 in increments of 100/65535%	RO Opt.
178-179	15-0	rxMinEvmModemPm	Minimum value of error vector magnitude over PM interval. U16 in increments of 100/65535%	RO Opt.
180-181	15-0	rxMaxEvmModemPm	Maximum value of error vector magnitude over PM interval. U16 in increments of 100/65535%	RO Opt.
182-183	15-0	txAvgPowerPm	Average value of Tx output optical power over PM interval. S16 in increments of 0.01 dBm.	RO Opt.
184-185	15-0	txMinPowerPm	Minimum value of Tx output optical power over PM interval. S16 in increments of 0.01 dBm.	RO Opt.
186-187	15-0	txMaxPowerPm	Maximum value of Tx output optical power over PM interval. S16 in increments of 0.01 dBm.	RO Opt.
188-189	15-0	rxAvgPowerPm	Average value of Rx input optical power over PM interval. S16 in increments of 0.01 dBm.	RO Opt.
190-191	15-0	rxMinPowerPm	Minimum value of Rx input optical power over PM interval. S16 in increments of 0.01 dBm.	RO Opt.
192-193	15-0	rxMaxPowerPm	Maximum value of Rx input optical power over PM interval. S16 in increments of 0.01 dBm.	RO Opt.
194-195	15-0	rxAvgSigPowerPm	Average value of Rx input optical Signal power over PM interval. S16 in increments of 0.01 dBm.	RO Opt.
196-197	15-0	rxMinSigPowerPm	Minimum value of Rx input optical Signal power over PM interval. S16 in increments of 0.01 dBm.	RO Opt.
198-199	15-0	rxMaxSigPowerPm	Maximum value of Rx input optical Signal power over PM interval. S16 in increments of 0.01 dBm.	RO Opt.
200-201	15-0	rxAvgSopcrPm	Average value of state of polarization change rate over PM interval. U16 in increments of 1 krads/s.	RO Opt.

202-203	15-0	rxMinSopcrPm	Minimum value of state of polarization change rate over PM interval. U16 in increments of 1 krads/s.	RO Opt.
204-205	15-0	rxMaxSopcrPm	Maximum value of state of polarization change rate over PM interval. U16 in increments of 1 krads/s.	RO Opt.
206-207	15-0	rxAvgMerPm	Average value of Modulation Error Ratio over PM interval. U16 in increments of 0.1 dB	RO Opt.
208-209	15-0	rxMinMerPm	Minimum value of Modulation Error Ratio over PM interval. U16 in increments of 0.1 dB	RO Opt.
210-211	15-0	rxMaxMerPm	Maximum value of Modulation Error Ratio over PM interval. U16 in increments of 0.1 dB	RO Opt.
212-255	7-0	Reserved		RO

7.5 Host Interface registers

The host interfaces of different data paths are described in pages with different bank index. The bank index for a data path is the smallest lane index of all host lanes of the data path.

Table 15: Host Interface registers

Page Number	Page Description	Notes
38h	Data Path Host Interface Configuration	
39h	Reserved Datatpath Interface Future Use	
3Ah	Data Path Host Interface Performance Monitoring	
3Bh	Data Path Host Interface Flags and Masks	
3C-3Fh	Reserved	

7.5.1 Data Path Host Interface Configuration (Page 38h)

The host uses page 38h to configure data path host interface specific features.

One configurable feature is the host link degrade monitoring. This optional capability requires monitoring the pre-FEC BER in the Ethernet RS(544,514) decoder block over a performance monitoring interval. Section 8.10 in the 400ZR Implementation Agreement [400ZR IA] describes the details of the host Link Degrade Indication (LDI) functions. The 400ZR IA also defines monitoring for the FEC Detected Degrade (FDD) and FEC Excessive Degrade (FED)

functions, which that the host can configure per data path interface on page 38h and associated banked pages.

The enable bits for the FDD and FED are located in 38h:136.1-0. When the host enables FDD, the module compares the FDD activate and clear BER thresholds to the average BER computed over the PM interval. If the average BER exceeds the activate FDD BER threshold FDD is set and the over PM Interval Latch is asserted (38h:132.0). If the average BER drops below the clear FDD BER threshold, the state of FDD clears. The module performs analogous operations when the host enables FED, except that that asserted alarm bit for FED is located in 38h:132.1.

Hysteresis will be left as an implementation detail.

Table 16: Data Path Host Interface Configuration (Page 38h)

Byte	Bits	Name	Description	Type
128-129	15-0	fddActBerThresh	BER threshold for FEC Detected Degrade (FDD) to become active on the data path host interface. Data format: F16.	RW Opt.
130-131	15-0	fddClrBerThresh	BER threshold for FEC Detected Degrade (FDD) to clear on the data path host interface. Data format: F16.	RW Opt.
132-133	15-0	fedActBerThresh	BER threshold for FEC Excessive Degrade (FED) to become active on the data path host interface. Data format: F16.	RW Opt.
134-135	15-0	fedClrBerThresh	BER threshold for FEC Excessive Degrade (FED) to clear on the data path host interface. Data format: F16.	RW Opt.
136	7-3	Reserved	Reserved	RO
	2	lfInsertionOnLdEnable	Enable for insertion of LF on the detection of LD. Default is disabled.	RW Opt.
	1	fedMonEnable	Enable for FEC Excessive Degrade (FED) monitoring feature.	RW Opt.
	0	fddMonEnable	Enable for FEC Detected Degrade (FDD) monitoring feature	RW Opt.
137-255	All	Reserved	Reserved	RO

7.5.2 Data Path Host Interface Performance Monitoring (Page 3Ah)

Page 3Ah contains optional host read-only statistics reporting of errors on the data path host interface. The module collects the information in these registers during the prior PM interval. The bank index for a data path is the smallest lane index of all host lanes of the data path.

Table 17: Data Path Host Interface Performance Monitoring (Page 3Ah)

Byte	Bits	Name	Description	Type
128-135	63-0	rxBitsPm	Number of bits received from the host side during prior PM interval. U64.	RO
136-143	63-0	rxBitsSubIntPm	Number of corrected bits received from the host side during prior PM interval. U64.	RO
144-151	63-0	rxCorrBitsPm	Number of bits received from the host side during a sub-interval. U64.	RO
152-159	63-0	rxMinCorrBitsSubIntPm	Minimum number of corrected bits from the host side over any sub-interval during prior PM interval. U64.	RO
160-167	63-0	rxMaxCorrBitsSubIntPm	Maximum number of corrected bits from the host side over any sub-interval during prior PM interval. U64.	RO
168-171	31-0	rxFramesPm	Number of frames received from the host side during prior PM interval. U32.	RO
172-175	31-0	rxFramesSubIntPm	Number of frames received from the host side during a sub-interval. U32.	RO
176-179	31-0	rxFramesUncorrErrPm	Number of frames received from the host side with uncorrectable errors during prior PM interval. U32.	RO
180-183	31-0	rxMinFramesUncorrErrSubintPm	Minimum number of frames received from the host side with uncorrectable errors over any sub-interval during prior PM interval. U32.	RO
184-187	31-0	rxMaxFramesUncorrErrSubintPm	Maximum number of frames received from the host side with uncorrectable errors over any sub-interval during prior PM interval. U32.	RO
188-255	All	Reserved		RO

7.5.3 Data Path host Interface Flags and Masks (page 3Bh)

Page 3Bh contains the masks and latches for the host data path alarms. It is a banked page with each bank corresponding to a unique data path.

Table 18: Data Path host Interface Flags and Masks (page 3Bh)

Byte	Bits	Name	Description	Type

128	7-2	Reserved	Reserved	RO
	1	mRxFedPm	Mask for FEC Excessive Degrade (FED) over PM Interval alarm	RW
	0	mRxFddPm	Mask for FEC Detected Degrade (FDD) over PM Interval alarm	RW
129	7-2	Reserved	Reserved	RO
	1	mRD	Mask for Remote Degrade alarm	RW
	0	mLD	Mask for Local Degrade alarm	RW
130-191	All	Reserved	Reserved	RO
192	7-2	Reserved	Reserved	RO
	1	lRxFedPm	Latched FEC Excessive Degrade (FED) over PM Interval alarm	COR
	0	lRxFddPm	Latched FEC Detected Degrade (FDD) over PM Interval alarm	COR
193	7-2	Reserved	Reserved	RO
	1	lRD	Latched Remote Degrade alarm	COR
	0	lLD	Latched Local Degrade alarm	COR
194-255	7-0	Reserved	Reserved	RO

7.6 Coherent Module Capabilities Advertisement

Table 19: Coherent Module Capabilities Advertisement

Page Number	Page Description	Notes
40h	Reserved for Applications Advertisement	
41h	Rx Signal Power Advertisement and Ranges for Configurable Thresholds	
42h	Performance Monitoring Advertisement	
43h	Media Lane Provisioning Advertisement	
44h – 4Fh	Reserved	

7.6.1 Rx Signal Power Advertisement and Ranges for Configurable Thresholds (Page 41h)

Hysteresis will be left as an implementation detail.

Table 20: Rx Signal Power Advertisement and Ranges for Configurable Thresholds (Page 41h)

Byte	Bits	Name	Description	Type
128	7-2	Reserved	Reserved	RO
	1	rxSigPowerImp	0b: Not implemented 1b: Implemented	RO
	0	rxPowerImp	0b: Not implemented 1b: Implemented	RO Opt.
129-131	All	Reserved	Reserved	RO
132-133	15-0	rxTotalPwrHiAlmThreshMax	Maximum allowed value for Rx Total Power Configured High Alarm Threshold. S16 in increments of 0.01 dBm.	RO Opt.
134-135	15-0	rxTotalPwrHiAlmThreshMin	Minimum allowed value for Rx Total Power Configured High Alarm Threshold. S16 in increments of 0.01 dBm.	RO Opt.
136-137	15-0	rxTotalPwrLoAlmThreshMax	Maximum allowed value for Rx Total Power Configured Low Alarm Threshold. S16 in increments of 0.01 dBm.	RO Opt.
138-139	15-0	rxTotalPwrLoAlmThreshMin	Minimum allowed value for Rx Total Power Configured Low Alarm Threshold. S16 in increments of 0.01 dBm.	RO Opt.
140-141	15-0	rxTotalPwrHiWarnThreshMax	Maximum allowed value for Rx Total Power Configured High Warning Threshold. S16 in increments of 0.01 dBm.	RO Opt.
142-143	15-0	rxTotalPwrHiWarnThreshMin	Minimum allowed value for Rx Total Power Configured High Warning Threshold. S16 in increments of 0.01 dBm.	RO Opt.
144-145	15-0	rxTotalPwrLoWarnThreshMax	Maximum allowed value for Rx Total Power Configured Low Warning Threshold. S16 in increments of 0.01 dBm.	RO Opt.
146-147	15-0	rxTotalPwrLoWarnThreshMin	Minimum allowed value for Rx Total Power Configured Low Warning Threshold. S16 in increments of 0.01 dBm.	RO Opt.
148-149	15-0	rxSigPwrHiAlmThreshMax	Maximum allowed value for Rx Signal Power Configured High Alarm Threshold. S16 in increments of 0.01 dBm.	RO Opt.
150-151	15-0	rxSigPwrHiAlmThreshMin	Minimum allowed value for Rx Signal Power Configured High Alarm Threshold. S16 in increments of 0.01 dBm.	RO Opt.

152-153	15-0	rxSigPwrLoAlmThreshMax	Maximum allowed value for Rx Signal Power Configured Low Alarm Threshold. S16 in increments of 0.01 dBm.	RO Opt.
154-155	15-0	rxSigPwrLoAlmThreshMin	Minimum allowed value for Rx Signal Power Configured Low Alarm Threshold. S16 in increments of 0.01 dBm.	RO Opt.
156-157	15-0	rxSigPwrHiWarnThreshMax	Maximum allowed value for Rx Signal Power Configured High Warning Threshold. S16 in increments of 0.01 dBm.	RO Opt.
158-159	15-0	rxSigPwrHiWarnThreshMin	Minimum allowed value for Rx Signal Power Configured High Warning Threshold. S16 in increments of 0.01 dBm.	RO Opt.
160-161	15-0	rxSigPwrLoWarnThreshMax	Maximum allowed value for Rx Signal Power Configured Low Warning Threshold. S16 in increments of 0.01 dBm.	RO Opt.
162-163	15-0	rxSigPwrLoWarnThreshMin	Minimum allowed value for Rx Signal Power Configured Low Warning Threshold. S16 in increments of 0.01 dBm.	RO Opt.
164-255	All	Reserved		RO

7.6.2 Performance Monitoring Advertisement (Page 42h)

Page 42h advertises which media lane performance monitors and performance statistics are implemented.
The implementation advertisements on this page are global, i.e. if a feature is advertised as implemented (bit value 1b), this feature is implemented for all media lanes (banks).

Table 21: Performance Monitoring Advertisement (Page 42h)

Byte	Bit	Name	Description	Type
128	7-5	Reserved		RO Rqd.
	4	rxBitsPmImpl	0b = Not implemented, 1b = Implemented	
	3	rxBitsSubIntPmImpl	0b = Not implemented, 1b = Implemented	
	2	rxCorrBitsPmImpl	0b = Not implemented, 1b = Implemented	
	1	rxMinCorrBitsSubIntPmImpl	0b = Not implemented, 1b = Implemented	
	0	rxMaxCorrBitsSubIntPmImpl	0b = Not implemented, 1b = Implemented	
129	7-5	Reserved		RO Rqd.
	4	rxFramesPmImpl	0b = Not implemented, 1b = Implemented	
	3	rxFramesSubIntPmImpl	0b = Not implemented, 1b = Implemented	

	2	rxFramesUncorrErrPmImpl	0b = Not implemented, 1b = Implemented	
	1	rxMinFramesUncorrErrSubintPmImpl	0b = Not implemented, 1b = Implemented	
	0	rxMaxFramesUncorrErrSubintPmImpl	0b = Not implemented, 1b = Implemented	
130	7	rxCdImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	6	rxAvgCdPmImpl	0b = Not implemented, 1b = Implemented	
	5	rxMinCdPmImpl	0b = Not implemented, 1b = Implemented	
	4	rxMaxCdPmImpl	0b = Not implemented, 1b = Implemented	
	3	rxDgdImpl	0b = Not implemented, 1b = Implemented	
	2	rxAvgDgdPmImpl	0b = Not implemented, 1b = Implemented	
	1	rxMinDgdPmImpl	0b = Not implemented, 1b = Implemented	
	0	rxMaxDgdPmIpl	0b = Not implemented, 1b = Implemented	
131	7	rxSopmdPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	6	rxAvgSopmdPmImpl	0b = Not implemented, 1b = Implemented	
	5	rxMinSopmdPmImpl	0b = Not implemented, 1b = Implemented	
	4	rxMaxSopmdPmImpl	0b = Not implemented, 1b = Implemented	
	3	rxPdlImpl	0b = Not implemented, 1b = Implemented	
	2	rxAvgPdlPmImpl	0b = Not implemented, 1b = Implemented	
	1	rxMinPdlPmImpl	0b = Not implemented, 1b = Implemented	
	0	rxMaxPdlPmImpl	0b = Not implemented, 1b = Implemented	
132	7	rxOsnrImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	6	rxAvgOsnrPmImpl	0b = Not implemented, 1b = Implemented	
	5	rxMinOsnrPmImpl	0b = Not implemented, 1b = Implemented	

	4	rxMaxOsnrPmImpl	0b = Not implemented, 1b = Implemented	
	3	rxEsnrImpl	0b = Not implemented, 1b = Implemented	
	2	rxAvgEsnrPmImpl	0b = Not implemented, 1b = Implemented	
	1	rxMinEsnrPmImpl	0b = Not implemented, 1b = Implemented	
	0	rxMaxEsnrPmImpl	0b = Not implemented, 1b = Implemented	
133	7	rxCfoImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	6	rxAvgCfoPmImpl	0b = Not implemented, 1b = Implemented	
	5	rxMinCfoPmImpl	0b = Not implemented, 1b = Implemented	
	4	rxMaxCfoPmImpl	0b = Not implemented, 1b = Implemented	
	3	rxEvmModemImpl	0b = Not implemented, 1b = Implemented	
	2	rxAvgEvmModemPmImpl	0b = Not implemented, 1b = Implemented	
	1	rxMinEvmModemPmImpl	0b = Not implemented, 1b = Implemented	
	0	rxMaxEvmModemPmImpl	0b = Not implemented, 1b = Implemented	
134	7	rxSopcrImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	6	rxAvgSopcrPmImpl	0b = Not implemented, 1b = Implemented	
	5	rxMinSopcrPmImpl	0b = Not implemented, 1b = Implemented	
	4	rxMaxSopcrPmImpl	0b = Not implemented, 1b = Implemented	
	3	txPowerImpl	0b = Not implemented, 1b = Implemented	
	2	txAvgPowerPmImpl	0b = Not implemented, 1b = Implemented	
	1	txMinPowerPmImpl	0b = Not implemented, 1b = Implemented	
	0	txMaxPowerPmImpl	0b = Not implemented, 1b = Implemented	
135	7	rxPowerImpl	0b = Not implemented, 1b = Implemented	RO Rqd.

	6	rxAvgPowerPmImpl	0b = Not implemented, 1b = Implemented	
	5	rxMinPowerPmImpl	0b = Not implemented, 1b = Implemented	
	4	rxMaxPowerPmImpl	0b = Not implemented, 1b = Implemented	
	3	rxSigPowerImpl	0b = Not implemented, 1b = Implemented	
	2	rxAvgSigPowerPmImpl	0b = Not implemented, 1b = Implemented	
	1	rxMinSigPowerPmImpl	0b = Not implemented, 1b = Implemented	
	0	rxMaxSigPowerPmImpl	0b = Not implemented, 1b = Implemented	
136	7-2	Reserved	Reserved	RO
	1	rxMediaFedPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	0	rxMediaFddPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
137	7-2	Reserved	Reserved	RO
	1	txHostFedPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	0	txHostFddPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
138 - 255	7-0	Reserved	Reserved	RO

7.6.3 Media Lane Provisioning Advertisement (Page 43h)

Page 43h advertises which media lane provisioning parameters are implemented.
The implementation advertisements on this page are global, i.e. if a feature is advertised as implemented (bit value 1b), this feature is implemented for all media lanes (banks).

Table 22: Media Lane Provisioning Advertisement (Page 43h)

Byte	Bit	Name	Description	Type
128	7-1	Reserved	Reserved	RO
	0	txFilterImpl	0b = Not implemented, 1b = Implemented	
129 - 255	7-0	Reserved	Reserved	RO

8 Reference Documents

8.1 Normative References

[CMIS] Common Management Interface Specification Rev 4.0 - http://www.qsfp-dd.com/wp-content/uploads/2019/05/QSFP-DD-CMIS-rev4p0.pdf

[400ZR IA] Implementation Agreement 400ZR : https://www.oiforum.com/wp-content/uploads/OIF-400ZR-01.0_reduced2.pdf

8.2 Informational References

[ICTROSA IA] Implementation Agreement for Integrated Coherent Transmit-Receive Optical Sub Assembly- https://www.oiforum.com/wp-content/uploads/OIF-IC-TROSA-01.0.pdf
[CFP MIS] CFP MSA Management Interface Specification http://www.cfp-msa.org/Documents/CFP_MSA_MIS_V2p6r06a.pdf

9 Appendix A: Glossary

The Glossary presents definitions for acronyms used in this IA.

Term	Definition	Term	Definition
BER	Bit Error Rate	**LSB**	Least Significant Bit
CD	Chromatic Dispersion	**MER**	Modulation Error Ratio
CDB	Common Data Block	**MHz**	MegaHertz
CFO	Carrier Frequency Offset	**MSB**	Most Significant Bit
CMIS	Common Management Interface Specification	**nm**	nanometer
CMU	Clock Monitor Unit	**NVR**	Non-Volatile Memory
COR	Clear on Read	**OSNR**	Optical Signal to Noise Ratio
dB	Decibels	**OOA**	Out of Alignment
dBm	Decibels reference to 1mW	**PDL**	Polarization Dependent Loss
DGD	Differential Group Delay	**PM**	Performance Monitoring
eSNR	Electrical Signal to Noise Ratio	**PMA**	Physical Medium
EVM_modem	Error Vector Magnitude of the entire modem	**PMD**	Polarization Mode Dispersion
FDD	FEC Detected Degrade	**Ps**	Picoseconds
FEC	Forward Error Correction	**Rx**	Receiver
FED	FEC Excessive Degrade	**RO**	Read Only
FER	Frame Error Rate	**ROC**	Rate of Change
FIFO	First In First Out	**RW**	Read Write
GHz	GigaHertz	**SOP**	State of Polarization
GMP	Generic Mapping Procedure	**SOPMD**	Second Order Polarization Mode Dispersion
IA	Implementation Agreement	**SOP ROC**	State Of Polarization Rate Of Change
Krad/s	Thousand rads per second	**Tx**	Transmitter

LOA	Loss of Alignment	**VDM**	Versatile Diagnostics Monitor
LOL	Loss of Lock	**VR**	Volatile Memory
LOS	Loss of Signal		

Table 23: Glossary

10 Appendix B: Open Issues / Current Work Items

- Add additional loopbacks through CDB to support all 6 loopbacks as defined in the 400ZR IA
- Add constellation pull through CDB

11 Appendix C: List of Companies Belonging to OIF when Document is Approved

Acacia Communications	Finisar Corporation	Marvell Semiconductor, Inc.	Rockley Photonics
ADVA Optical Networking	Foxconn Interconnect Technology, Ltd.	Maxim Integrated Inc.	Rosenberger Hochfrequenztechnik GmbH & Co. KG
Alibaba	Fujikura	MaxLinear Inc.	Samsung Electronics Co. Ltd.
Alphawave IP Inc.	Fujitsu	MediaTek	Samtec Inc.
Amphenol Corp.	Furukawa Electric Japan	Mellanox Technologies	Semtech Canada Corporation
AnalogX Inc.	Global Foundries	Microsemi Inc.	SiFotonics Technologies Co., Ltd.
Applied Optoelectronics, Inc.	Google	Microsoft Corporation	Socionext Inc.
Arista Networks	Hewlett Packard Enterprise (HPE)	Mitsubishi Electric Corporation	Spirent Communications
BizLink Technology Inc.	IBM Corporation	Molex	Sumitomo Electric Industries, Ltd.
Broadcom Inc.	Idea Sistemas Electronicos S.A.	Multilane SAL Offshore	Sumitomo Osaka Cement
Cadence Design Systems	Infinera	NEC Corporation	Synopsys, Inc.
China Telecom Global Limited	InnoLight Technology Limited	NeoPhotonics	TE Connectivity
CICT	Innovium	Nokia	Tektronix
Ciena Corporation	Inphi	NTT Corporation	Telefonica SA
Cisco Systems	Integrated Device Technology	O-Net Communications (HK) Limited	TELUS Communications, Inc.
Corning	Intel	Open Silicon Inc.	UNH InterOperability Laboratory (UNH-IOL)
Credo Semiconductor (HK) LTD	IPG Photonics Corporation	Optomind Inc.	Verizon
Dell, Inc.	Juniper Networks	Orange	Viavi Solutions Deutschland GmbH

EFFECT Photonics B.V.	Kandou Bus	PETRA	Xelic
Elenion Technologies, LLC	KDDI Research, Inc.	Precise-ITC, Inc.	Xilinx
Epson Electronics America, Inc.	Keysight Technologies, Inc.	Rambus Inc.	Yamaichi Electronics Ltd.
eSilicon Corporation	Lumentum	Ranovus	ZTE Corporation
Facebook	MACOM Technology Solutions	Rianta Solutions, Inc.	