Implementation Agreement for Coherent CMIS

IA OIF-C-CMIS-01.3

October 12, 2023

Implementation Agreement created and approved
OIF
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TITLE: Implementation Agreement for Coherent Module Management Interface Spec

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ABSTRACT: Implementation Agreement created by the Optical Internetworking Forum for the MIS of Coherent Modules. The first module to use this MIS is based on the 400ZR spec and the first release of this document will be focused on 400ZR. The project start was approved at the Q2 Technical Meeting, April 2013 (Albuquerque, USA).

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4 Document Revision History

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DATE: **October 12, 2023**

Table 1: IA Document Revision History

Document	Date	Revisions/Comments
OIF-C-CMIS-01.0	Jan 14th 2020	Initial document release
OIF-C-CMIS-01.1	June 10th 2020	Minor update to update link to 400ZR IA and IC-TROSA
OIF-C-CMIS-01.2	March 21st 2022	This version was voted on as V2.0 but the nature of the changes did not warrant a major up version. Updates from maintenance comments, additions of new VDMs, additions of new flags, addition of page 43h for provisioning advertising, addition of page 44h for flag advertising
OIF-C-CMIS-01.3	October 12th 2023	Maintenance update to address issues reported since last update.

Rev 1.2
Revision 1.2 made the following updates.

- General – add custom registers to all pages at the end of the page
- Section 5.2 – remove the memory map diagram and replace it with a table that provides page details and describes banking for each page.
- Section 5.3 – add text to clarify that alarm direction is normalized to the module.
- Section 7.1 – clarify that the freeze mechanism is described in the VDM section of CMIS
- Section 7.3.1
    - Updated type 137 from SOPMD to SOPMD – high granularity
    - Added type 148 Clock recovery loop
    - Added type 149 SOPMD – low granularity
    - Removed note about multiple TECs, not applicable to C-CMIS

  - Added note1 to describe clock recovery loop
  - Added note2 to describe chromatic dispersion
- Section 7.4.2 – clarified the relationship between power threshold in page 02h (CMIS) vs page 30h (C-CMIS)
- Section 7.4 – added RxLOF and RxLOM masks flags to 32h:130 and 33:130
- Section 7.4.7 – adding text to clarify that it is CMIS fine interval
- Section 7.4.8
  - Updated SOPMD to HGSOPMD
  - Added Clock recovery loop registers
  - Added LGSOPMD registers
- Section 7.5 - updated flag direction of all host alarms. Rx = media to host and Tx = host to media
- Section 7.5.1 – correct page for host FED alarm bit
- Section 7.5.3 – added FlexE and PCS layer flags and masks
- Section 7.6.2
  - Updated SOPMD to HGSOPMD
  - Added Clock recovery loop registers
  - Added LGSOPMD registers
- Section 7.6.3 – added lfInsertionOnLdEnableImpl
- Section 7.6.4 – added page 44h for alarm implemented
- Section 9 – updated Glossary

Rev 1.3

Revision 1.3 made the following updates.

- Add note in implementation notes section about HG and LG advertising mistake.
- Add MER implemented advertising in 42h:139
- Add missing Flexe RPF flag and mask in page 3Bh and advertisement in 44h:134
- Add C-CMIS revision number in 40h:128
- Add SNR margin, Q factor and Q margin PMs to VDM types, page 35h and page 42h
- Clarify bank to leading host lane relationship in section 5.3
- Add RS-FEC corrected frames counter to page 3Ah
- Changed name of VDM EVM_modem to EVM and updated the note
- Added Q-value to Glossary
- Updated links to reference documents.
- Clarified FDD/FED flag timing.
- Added RxLOSType in page 41h

5 Introduction

5.1 Scope

This Implementation Agreement extends the Common Management Interface Specification [CMIS] to allow management of digital coherent optics (DCO) modules. This Implementation Agreement will be referred to as Coherent CMIS or C-CMIS and is used in conjunction with [CMIS].

Coherent CMIS defines additional management registers, messages (CDB), and monitors (VDM), together with new functionality, mechanisms, or behaviors, as needed. The relevant address spaces or name spaces have been reserved "for coherent" in [CMIS].

The initial release of C-CMIS covers 400ZR modules [400ZR IA] only, which support a single data path with eight-lane host interface for a 400GBASE-R PCS signal and a single-lane 400G coherent media interface (with a new signal format called 400ZR). However, the C-CMIS scope is expected to be extended to other types of DCO modules in the future.

NOTE – C-CMIS deliberately defines some host side registers which are expected to be used in DCO modules only (Section 0

Host Interface registers).

5.2 Memory Page Structure

The following table lists the pages described in this document. The baseline specification pages used to manage a module are defined in [CMIS].

Table 2: Memory Page Structure

Page Number	Page Description	Notes
30h	Media Lane Configurable Thresholds	Media Lane Banking
31h	Media Lane Provisioning	Media Lane Banking
32h	Media Lane Flag Masks	Media Lane Banking
33h	Media Lane Flags and Status	Media Lane Banking
34h	Media Lane FEC Performance Monitoring	Media Lane Banking
35h	Media Lane Link Performance Monitoring	Media Lane Banking
36-37h	Reserved	
38h	Data Path Host Interface Configuration	Host Lane Banking

39h	Reserved Data Path Interface Future Use	
3Ah	Data Path Host Interface Performance Monitoring	Host Lane Banking
3Bh	Data Path Host Interface Flags and Masks	Host Lane Banking
3C-3Fh	Reserved	
40h	Reserved for Applications Advertisement	
41h	Rx Signal Power Advertisement and Ranges for Configurable Thresholds	
42h	Performance Monitoring Advertisement	
43h	Media Lane Provisioning Advertisement	
44h	Alarm Advertisement	
45h – 4Fh	Reserved	

Note 1: Media Lane Banking means 1 bank per media lane.
Note 2: Host Lane Banking means banked per data path, Bank Index is the host lane id of the lowest host lane in the data path.
Note 3: C-CMIS defines VDM types that are used in pages 20h-2Fh. The register definitions for these pages and description of VDM usage is captured in CMIS.

5.3 Terminology Mapping (C-CMIS versus CMIS and 400ZR)

CMIS describes the function of a module with the concept of data paths carrying applications. In this model, a 400ZR module implements a single data path with eight host lanes and one media lane. This 400ZR data path can carry one of two possible applications. These 400ZR applications are referred to a “DWDM, noise limited” and “Single-Channel, loss limited”, respectively.

The CMIS register model is based on individual electrical host lanes and media lanes, with data path related attributes replicated on all lanes. However, in the context of Coherent CMIS, it is more appropriate to move away from the physical lane view and instead refer to the transported useful 400GBASE-R multi-lane signal as a whole. At the same time the replication of data path related attributes across the physical lanes of the data path are avoided in the C-CMIS registers.

The 400ZR line side interface is considered to use a single media lane (wavelength), so Coherent CMIS will continue to refer to the network side related registers as media lane registers.

The 400ZR host side interface of a 400ZR application is 400GAUI-8 or 4x100GAUI-2, an eight-lane electrical interface which is an example of a multi-lane interface. All registers pertaining to processing the entire client signal carried over this multi lane interfaces are referred to as host interface registers (there is no duplication of these registers for individual lanes). The relationship between host lane and bank is shown below.

Bank 0 = Leading Host Lane 1

Bank 1 = Leading Host Lane 2

Bank 2 = Leading Host Lane 3

Bank 3 = Leading Host Lane 4

Bank 4 = Leading Host Lane 5

Bank 5 = Leading Host Lane 6

Bank 6 = Leading Host Lane 7

Bank 7 = Leading Host Lane 8

For a 4x100GE 400ZR module, the leading host lanes are 1,3,5,7 and the corresponding banks are 0,2,4,6

To prepare for future modules possibly providing more than one data path, strictly we need to distinguish a module's host interface and media interface from the host interface and media interface of an individual data path.

To simplify the language and because of its data path centric view, C-CMIS uses the term host interface and media interface always in relation to a data path. If (rarely) the module view is needed, we use the prefixed terms module host interface and module media interface. The direction of alarms and PMs is normalized to the module view. All Tx alarms/PMs are in the host to media direction and all Rx alarms/PMs are in media to host direction.

5.4 Register Nomenclature:

5.4.1 Register Names

The register naming convention is camelback. The names are unique within the table.

5.4.2 Register Data Notation

When referring to register data types, the following data notation is used:

Table 3: Register Data Notation

Data Notation	Data Type
U8	Unsigned 8 bit register
U16	Unsigned 16 bit register
S16	Signed 16 bit register

U32	Unsigned 32 bit register
S32	Signed 32 bit register
U64	Unsigned 64 bit register
S64	Signed 64 bit register
F16	16 bit floating point register
F32	32 bit floating point register

5.4.3 Register Address Notation

When referring to certain registers, bits, or fields using the following address notation is used:

<reference> := [<bank-range>: [<page-range>:]] <byte-range> [.<bit-or-field>]
<bank-range> := [<bank>-]<bank>
<page-range> := [<page>-]<page>
<bit-or-field> := <bit>[-<bit>]
<bit> := "single digit decimal" (0 … 7)
<byte> := "decimal" (0 … 255)
<page> := "hexadecimal" (00h … FFh)
<bank> := "decimal" (0 … 255)

Table 4 - Register notation Example

Example notation	Description of displayed register	Description of Register
2h:3Ah:128-135	Bank 2h, page 3Ah bytes 128-135	txBitsPm for lane 3
85	Lower memory 0, Byte 85	Module Type advertising code
04h:128.2-1	Page 04h, Byte 128, Bits 2 and 1	12.5 and 6.25 GHz grid supported

6 Implementation Notes

6.1 400ZR implementation notes

This section specifies how certain CMIS features shall be used by 400ZR modules.

6.1.1 400ZR CMIS Module Application Advertisement

CMIS requires pluggable modules to identify supported application in the Application Advertising tables 00h:85-117 and 01h:176.

A 400ZR module advertises its default application code in 00h:85-89 and 01h:176 as illustrated in Table 5.

A dual mode 400ZR module will have to advertise both applications.

Table 5 CMIS Application Advertisement for 400ZR

Byte	Bits	ApSel Code	Name	Value	Description
85	7-0	N/A	Module Type Encoding	02h	Optical Interface: SMF
86	7-0	0001b	Host Electrical Interface Code	11h	400GAUI-8 C2M
87	7-0		Module Media Interface Code	see Note 1 below	
88	7-4		Host Lane Count	1000b	8 host electrical lanes
	3-0		Media Lane Count	0001b	1 media lane
89	7-0		Host Lane Assignment Options	01h	Permissible first host lane number for Application: lane 1
01h:176	7-0		Media Lane Assignment Options	01h	Permissible first media lane number for Application: lane 1

Note 1: Module Media Interface Codes are generally defined in SFF-8024. Two codes are defined for the 400ZR application: 3Eh (400ZR, DWDM amplified) and 3Fh (400ZR, single wavelength unamplified).

6.1.2 400ZR Loopback Implementation

Generic register-based management of 400ZR loopbacks shall be possible via the existing CMIS registers. Note that CMIS allows to manage only four loopbacks while a 400ZR module actually provides a set of six loopbacks.

Table 6: Loopback Mapping to CMIS describes the six 400ZR loopbacks and their possible mapping to the four CMIS controls, including the default mapping. Vendors can choose a non-default set of 4 loopbacks and they must clearly document what they have selected. If a vendor chooses to implement the Modem Rx loopback, they can use it as the Media Side Input or as the Host Side Output loopback. If a vendor chooses to implement the Modem Tx loopback, they can use it as the Host Side Input or as the Media Side Output loopback.

Table 6: Loopback Mapping to CMIS

400 ZR Loopback Name	CMIS Loopback	Default	Description
Media Side Rx Loopback	Media Side Input	Y	Loopback in DSP. After polarity split and symbol de-interleave -> Grey mapper, symbol Interleave. Network loop timed.
Modem Rx Loopback	Media Side Input or Host Side Output	N	Loopback after GMP De-mapping -> GMP mapping. Data retransmitted relative to local clock.
Host Side Rx Loopback	Host Side Output	Y	Loopback after distribution/interleaving block on host ingress path, and before lane reorder and interleave
Host Side Tx Loopback	Host Side Input	Y	Loopback after Alignment lock and lane Deskew -> PMA sublayer. Host loop timed.
Modem Tx Loopback	Host Side Input or Media Side Output	N	Loopback after GMP mapping -> GMP Demapping. Data re-transmitted relative to local clock
Media Side Tx Loopback	Media Side Output	Y	Loopback after TX DSP processing blocks and before RX DSP processing blocks

6.1.3 Note on SOPMD implementation

Note: between C-CMIS 1.1 and 1.2, SOPMD was split into a HG (High Granularity) and an LG (Low Granularity) reading. The original SOPMD became HG SOPMD and LG SOPMD was added. The advertising in 42h:131 was for the original SOPMD and should have become the HG SOPMD advertising bit but it was erroneously listed as LG SOPMD advertising and HG SOPMD added at 42h:138. We do not plan to reverse this order at this point and will keep the advertising from C-CMIS 1.2.

6.1.4 Note on Q factor

The reported Q factor should follow the definition presented in ITU-T Series G, supplement 41 (02/2018), section 7.1.1.

7 Coherent Extensions to CMIS

This chapter defines the extensions to CMIS referred to as C-CMIS.

7.1 PM Interval

The PM interval is defined by the host. The host uses the PM freeze mechanism that is defined in the VDM section of [CMIS] in page 2Fh:144-145. The basic update period for VDM monitors is defined as one second. Unfrozen VDM monitors should be updated at least once per second.

7.2 Flag Conformance

Table 7 Coherent Lane Specific Flag Conformance describes the flag conformance for all lane-specific flags, per data path state. In data path states where a flag is indicated as 'Not Allowed', the module shall not set the associated flag bit while the data path is in that state. The flag conformance shown in Table 7 Coherent Lane Specific Flag Conformance is applicable to High Alarm, Low Alarm, High Warning and Low Warning for each listed VDM Coherent Identifier and other coherent flags.

Table 7 Coherent Lane Specific Flag Conformance

DataPath Deactivated	DataPath Initialized	DataPathInit	DataPathDeinit	DataPath Activated	DataPath TxTurnOn	DataPath TxTurnOff
Not Allowed	Allowed	Not Allowed	Not Allowed	Allowed	Allowed	Allowed

7.3 Versatile Diagnostics Monitor (VDM) Extensions

The VDM functionality and some basic VDM monitors are defined in CMIS. Each VDM monitor has an associated numerical identifier, and the identifiers for C-CMIS defined monitors are defined in Table 8: Identifiers for Coherent Monitors (taking values from a range reserved for C-CMIS). All VDM parameters are optional.

Note: If there is agreement on the flag conformance shown in Table 8: Identifiers for Coherent Monitors, the table could be replaced with a statement on which States the conformance is Allowed or Not Allowed since the VDM Coherent Identifiers share the same flag conformance.

- the module shall update the register values of VDM real-time (current value) monitors every second.

- the module shall update the register values of VDM statistics (min, max, average) monitors every second, unless the host has requested to freeze statistics registers via the CMIS FreezeRequest bit 2Fh:144.7 (see [CMIS] for a description of the freeze mechanism and its usage).

7.3.1 Data Path Monitors

Unless specified differently, the VDM monitors for a DCO are all associated with a data path. Therefore, the lane or data path identifier (bits 3-0 of the MSB of VDM Configuration Registers in pages 20h-23h) of those VDM monitors shall indicate the first lane of the relevant data path.

Table 8: Identifiers for Coherent Monitors

Identifier	Description	Data Type	LSB Scaling	Unit
128	Modulator Bias X/I	U16	100/65,535	%
129	Modulator Bias X/Q	U16	100/65,535	%
130	Modulator Bias Y/I	U16	100/65,535	%
131	Modulator Bias Y/Q	U16	100/65,535	%
132	Modulator Bias X_Phase	U16	100/65,535	%
133	Modulator Bias Y_Phase	U16	100/65,535	%
134	CD – high granularity, short link: Note2	S16	1	Ps/nm
135	CD – low granularity, long link: Note2	S16	20	Ps/nm
136	DGD	U16	0.01	Ps
137	SOPMD – high granularity	U16	0.01	Ps^2
138	PDL	U16	0.1	dB
139	OSNR	U16	0.1	dB
140	eSNR	U16	0.1	dB
141	CFO	S16	1	MHz
142	EVM Note 3:	U16	100/65,535	%
143	Tx Power	S16	0.01	dBm
144	Rx Total Power	S16	0.01	dBm
145	Rx Signal Power	S16	0.01	dBm
146	SOP ROC	U16	1	krad/s
147	MER	U16	0.1	dB
148	Clock recovery loop: Note1	S16	100/32,767	%
149	SOPMD – low granularity	U16	1	Ps^2
150	SNR_margin	S16	0.1	dB
151	Q-factor	U16	0.1	dB
152	Q-margin	S16	0.1	dB

Note1: The clock recovery control loop monitor range will be -100 to 100% with nominal at 0%. Defect thresholds are set by the vendor to indicate that operation is outside of the normal range and traffic impact may be imminent. It is understood that the monitor value is a vendor-specific best-effort metric without guaranteed semantics, except for being monotonic. Values reported by different modules are not comparable.

Note2: CD is a measured value of the Chromatic dispersion of the media side fiber as estimated from DSP compensation. For C-Band applications, as the fiber length increases, this estimated value is expected to increase.

Note 3: EVM_modem has been renamed to EVM and will provide the recommended EVM measurement for the applicable IA.

7.4 Media Interface registers

Media interface registers are in banked pages with each bank referring to the media interface of a single media lane (wavelength). The bank index of a data path is the smallest index of the media lanes belonging to the data path.

Table 9: Media Interface registers

Page Number	Page Description	Notes
30h	Media Lane Configurable Thresholds	
31h	Media Lane Provisioning	
32h	Media Lane Flag Masks	
33h	Media Lane Flags and Status	
34h	Media Lane FEC Performance Monitoring	
35h	Media Lane Link Performance Monitoring	
36-37h	Reserved	

7.4.1 Media Lane Configurable Thresholds (page30h)

Page 30h is a banked page with each bank referring to the media interface of a single media lane (wavelength). The bank index of a data path is the smallest index of the media lanes belonging to the data path.

7.4.2 Power related thresholds

Page 30h allows the host to configure optical receive power related thresholds, alarms or warnings flags, and masks. By default, the module uses thresholds advertised in page 02h, however, hosts can program their own thresholds in page 30h. The Page 30h thresholds should be used for VDM power flags and do not overwrite the Page 02h thresholds which have results displayed in Page 11h. These configured thresholds must be in the range advertised by the module on page 41h.

Hysteresis around the thresholds is left as an implementation detail.

7.4.3 Link degradation feature

Page 30h allows to configure link degradation detection and reporting for two types of link degradations [400ZR IA]: FEC Detected Degrade (FDD) and FEC Excessive Degrade (FED).

Link degradation detection requires monitoring the pre-FEC BER over a performance monitoring interval, as described in detail in [400ZR IA].

When FDD reporting is enabled in 30h:168.0, the module compares the average BER computed over the PM interval against two thresholds: When the average BER exceeds the activate FDD BER threshold, FDD is asserted and the alarm bit 33h:132.0 (lRxFddPm) is set. When the average BER drops below the clear FDD BER threshold, FDD is deasserted and the alarm bit clears. The alarm bit should be updated at least once per second.

When FED is enabled in 30h:168.1, the module performs analogous operations using the FED thresholds and reports FED via alarm bit 33h:132.1 (lRxFedPm).

Table 10: Media Lane Configurable Thresholds (Page 30h)

Byte	Bits	Name	Description	Type
Power Alarm Thresholds				
128-129	15-0	totalPwrHiAlarmThresh	Configured threshold for Rx Total Power high alarm. S16 in increments of 0.01 dBm.	RW Opt.
130-131	15-0	totalPwrLoAlarmThresh	Configured threshold for Rx Total Power low alarm. S16 in increments of 0.01 dBm.	RW Opt.
132-133	15-0	totalPwrHiWarnThresh	Configured threshold for Rx Total Power high warning. S16 in increments of 0.01 dBm.	RW Opt.
134-135	15-0	totalPwrLoWarnThresh	Configured threshold for Rx Total Power low warning. S16 in increments of 0.01 dBm.	RW Opt.
136-137	15-0	sigPwrHiAlarmThresh	Configured threshold for Rx Signal Power high alarm. S16 in increments of 0.01 dBm.	RW Opt.
138-139	15-0	sigPwrLoAlarmThresh	Configured threshold for Rx Signal Power low alarm. S16 in increments of 0.01 dBm.	RW Opt.
140-141	15-0	sigPwrHiWarnThresh	Configured threshold for Rx Signal Power high warning. S16 in increments of 0.01 dBm.	RW Opt.
142-143	15-0	sigPwrLoWarnThresh	Configured threshold for Rx Signal Power low warning. S16 in increments of 0.01 dBm	RW Opt.
144	7-2	Reserved	Reserved	RO

	1	totalPwrUseCfgThresh	This bit selects between default and host configured thresholds for Rx total power monitor from the VDM identifier table. 0 = default 1= host configured	RW Opt.
	0	sigPwrUseCfgThresh	This bit selects between default and host configured thresholds for Rx signal power monitor from the VDM identifier table. 0 = default 1= host configured	RW Opt.
145 - 159	All	Reserved	Reserved	RO
Degrade Thresholds				
160-161	15-0	fddRaiseThresh	media Rx BER threshold for FEC Detected Degrade (FDD) to be set active. F16 BER floating point format	RW Opt.
162 - 163	15-0	fddClearThresh	media Rx BER threshold for FEC Detected Degrade (FDD) to clear. F16 BER floating point format	RW Opt.
164 - 165	15-0	fedRaiseThresh	media Rx BER threshold for FEC Excessive Degrade (FED) to be set active. F16 BER floating point format	RW Opt.
166 - 167	15-0	fedClearThresh	media Rx BER threshold for FEC Excessive Degrade (FED) to clear. F16 BER floating point format	RW Opt.
Degrade Feature Advertisement				
168	7-2	Reserved		RO
	1	fedEnable	enable for media Rx FEC Excessive Degrade (FED) monitoring feature.	RW Opt.
	0	fddEnable	enable for media Rx FEC Detected Degrade (FDD) monitoring feature	RW Opt.
169-247	All	Reserved		RO
248-255	All	Custom		

7.4.4 Media Lane Provisioning (Page 31h)

Page 31h contains parameters for coherent provisioning. It is a banked page with each bank corresponding to a unique media lane.

Table 11: Media Lane Provisioning (Page 31h)

Byte	Bits	Name	Description	Type
128	7-2	Reserved	Reserved for future	RO
	1	lfInsertionOnLdEnable	Enable for insertion of LF on the detection of LD. Default is disabled.	RW Opt.
	0	txFilterEnable	Enable for Tx Transmit shape control	RW Opt.

129	7-0	txFilterType	The type of Tx shaping to be used. 1 = Root-Raised-Cosine 2 = Raised-Cosine 3 = Gaussian	RW Opt.
130	7-0	txFilterRollOff	Scaled roll off factor (0.0 to 1.0). U8 in increments of 1/255	RW Opt.
131-247	All	Reserved	Reserved	RO
248-255	All	Custom		

7.4.5 Media Lane Flag Masks (Page 32h)

Page 32h contains the masks for the media lane alarms. It is a banked page with each bank corresponding to a unique media lane.

Table 12: Media Lane Flag Masks (Page 32h)

Byte	Bits	Name	Description	Type
128	7-6	Reserved	Reserved for future Tx Lane Status Masks	RO
	5	mTxLoa	Mask for (vendor defined) Tx Loss of Alignment alarm	RW Opt.
	4	mTxOoa	Mask for (vendor defined) Tx Out of Alignment alarm	RW Opt.
	3	mTxLolCmu	Mask for (vendor defined) Tx CMU Loss of Lock alarm	RW Opt.
	2	mTxLolRefClk	Mask for (vendor defined) Tx Reference Clock Loss of Lock alarm	RW Opt.
	1	mTxLolDeSkew	Mask for (vendor defined) Tx Deskew Loss of Lock alarm	RW Opt.
	0	mTxFIFO	Mask for (vendor defined) Tx FIFO Error	RW Opt.
129	7-0	Reserved	Reserved for future Tx Lane Status Masks	RO
130	7	mRxLof	Mask for (vendor defined) Rx Loss of Frame: Note 1	RW Opt
	6	mRxLom	Mask for (vendor defined) Rx Loss of Multi Frame: Note 1	RW Opt
	5	mRxLolDemod	Mask for (vendor defined) Rx Demodulator Loss of Lock	RW Opt.
	4	mRxLolCd	Mask for (vendor defined) Rx Chromatic Dispersion Compensation Loss of Lock	RW Opt.
	3	mRxLoa	Mask for (vendor defined) Rx Loss of Alignment alarm	RW Opt.
	2	mRxOoa	Mask for (vendor defined) Rx Out of Alignment alarm	RW Opt.

	1	mRxLolDeskew	Mask for (vendor defined) Rx Deskew Loss of Lock alarm	RW Opt.
	0	mRxLolFifo	Mask for (vendor defined) Rx FIFO Error	RW Opt.
131	7-0	Reserved	Reserved for future Rx Lane Status Masks	RO
132	7-2	Reserved	Reserved	RO
	1	mRxFedPm	Mask for FEC Excessive Degrade (FED) over PM Interval alarm	RW Opt.
	0	mRxFddPm	Mask for FEC Detected Degrade (FDD) over PM Interval alarm	RW Opt.
133	7-3	Reserved	Reserved	RO
	2	mRD	Mask for Remote Degrade alarm	RW Opt.
	1	mLD	Mask for Local Degrade alarm	RW Opt.
	0	mRPF	Mask for Remote Phy Fault alarm	RW Opt.
134-247	All	Reserved	Reserved	RO
248-255	All	Custom		

Note 1: The description of 400ZR frames and multi-frames can be found in the 400ZR IA document.

7.4.6 Media Lane Flags and Status (Page 33h)

Page 33h contains the latches for the media lane alarms. It is a banked page with each bank corresponding to a unique media lane.

Table 13: Media Lane Flags and Status (Page 33h)

Byte	Bits	Name	Description	Type
128	7-6	Reserved	Reserved for future Tx Lane Status Latches	RO
	5	lTxLoa	Latched (vendor defined) Tx Loss of Alignment alarm	COR opt
	4	lTxOoa	Latched (vendor defined) Tx Out of Alignment alarm	COR opt
	3	lTxLolCmu	Latched (vendor defined) Tx CMU Loss of Lock alarm	COR opt
	2	lTxLolRefClk	Latched (vendor defined) Tx Reference Clock Loss of Lock alarm	COR opt
	1	lTxLolDeSkew	Latched (vendor defined) Tx Deskew Loss of Lock alarm	COR opt

	0	lTxFIFO	Latched (vendor defined) Tx FIFO Error	COR opt
129	7-0	Reserved	Reserved for future Rx Lane Status Latches	RO
130	7	lRxLof	Latched (vendor defined) Rx Loss of Frame	COR opt
	6	lRxLom	Latched (vendor defined) Rx Loss of Multi Frame	COR opt
	5	lRxLolDemod	Latched (vendor defined) Rx Demodulator Loss of Lock	COR opt
	4	lRxLolCd	Latched (vendor defined) Rx Chromatic Dispersion Compensation Loss of Lock	COR opt
	3	lRxLoa	Latched (vendor defined) Rx Loss of Alignment alarm	COR opt
	2	lRxOoa	Latched (vendor defined) Rx Out of Alignment alarm	COR opt
	1	lRxLolDeskew	Latched (vendor defined) Rx Deskew Loss of Lock alarm	COR opt
	0	lRxLolFifo	Latched (vendor defined) Rx FIFO Error	COR opt
131	7-0	Reserved	Reserved for future Rx Lane Status Latches	RO
132	7-2	Reserved	Reserved	RO
	1	lRxFedPm	Latched FEC Excessive Degrade (FED) over PM Interval alarm	COR opt
	0	lRxFddPm	Latched FEC Detected Degrade (FDD) over PM Interval alarm	COR opt
133	7-3	Reserved	Reserved	RO
	2	lRD	Latched Remote Degrade alarm	COR opt
	1	lLD	Latched Local Degrade alarm	COR opt
	0	lRPF	Latched Remote Phy Fault alarm	COR opt
134-247	All	Reserved	Reserved	RO
248-255	All	Custom		

7.4.7 Media Lane FEC Performance Monitoring (page 34h)

Page 34h contains read-only media FEC performance monitoring counters. The module collects the information in these registers during the prior PM interval. Page 34h is a banked page with each bank referring to a single media lane. For example, if the module supports 2 media lanes, then bank 1 will be used for lane 2.

Table 14: Media Lane FEC Performance Monitoring (Page 34h)

Byte	Bits	Name	Description	Type
128-135	63-0	rxBitsPm	Number of bits received during prior PM interval. U64 with MSB in byte 128.	RO opt
136-143	63-0	rxBitsSubIntPm	Number of bits received during any sub-interval (CMIS fine interval) of prior PM interval. U64 with MSB in byte 136.	RO opt
144-151	63-0	rxCorrBitsPm	Number of corrected bits during prior PM interval. U64 with MSB in byte 144.	RO opt
152-159	63-0	rxMinCorrBitsSubIntPm	Minimum number of corrected bits received during any sub-interval (CMIS fine interval) of prior PM interval. U64 with MSB in byte 152.	RO opt
160-167	63-0	rxMaxCorrBitsSubIntPm	Maximum number of corrected bits received during any sub-interval (CMIS fine interval) of prior PM interval. U64 with MSB in byte 160.	RO opt
168-171	31-0	rxFramesPm	Number of frames received during prior PM interval. U32 with MSB in byte 168.	RO opt
172-175	31-0	rxFramesSubIntPm	Number of frames received during any sub-interval (CMIS fine interval) of prior PM interval. U32 with MSB in byte 172.	RO opt
176-179	31-0	rxFramesUncorrErrPm	Number of frames received with uncorrectable errors during prior PM interval. U32 with MSB in byte 176.	RO opt
180-183	31-0	rxMinFramesUncorrErrSubintPm	Minimum number of frames with uncorrectable errors received during any sub-interval (CMIS fine interval) of prior PM interval. U32 with MSB in byte 180.	RO opt
184-187	31-0	rxMaxFramesUncorrErrSubintPm	Maximum number of frames with uncorrectable errors received during any sub-interval (CMIS fine interval) of prior PM interval. U32 with MSB in byte 184.	RO opt
188-247	All	Reserved		RO
248-255	All	Custom		

7.4.8 Media Lane Link Performance Monitoring (page 35h)

Page 35h contains optional media lane read-only statistics reporting on the link performance. The module collects the information in these registers during the prior PM interval. Page 35h is a banked page with each bank referring to a single media lane. For example, if the module supports 2 media lanes, then bank 1 will be used for lane 2. All media interface link

performance monitors supported in page 35h shall also support a corresponding real-time VDM monitor (in page 20h-2Fh).

Table 15: Media Lane Link Performance Monitoring (Page 35h)

Byte	Bits	Name	Description	Type
128-131	31-0	rxAvgCdPm	Average value of DSP compensated chromatic dispersion over PM interval. S32 in increments of 1ps/nm.	RO Opt.
132-135	31-0	rxMinCdPm	Minimum value of DSP compensated chromatic dispersion over PM interval. S32 in increments of 1ps/nm.	RO Opt.
136-139	31-0	rxMaxCdPm	Maximum value of DSP compensated chromatic dispersion over PM interval. S32 in increments of 1ps/nm.	RO Opt.
140-141	15-0	rxAvgDgdPm	Average value of differential group delay over PM interval. U16 in increments of 0.01ps.	RO Opt.
142-143	15-0	rxMinDgdPm	Minimum value of differential group delay over PM interval. U16 in increments of 0.01ps.	RO Opt.
144-145	15-0	rxMaxDgdPm	Maximum value of differential group delay over PM interval. U16 in increments of 0.01ps.	RO Opt.
146-147	15-0	rxAvgHGSopmdPm	Average value of high granularity SOPMD over PM interval. U16 in increments of 0.01ps^2.	RO Opt.
148-149	15-0	rxMinHGSopmdPm	Minimum value of high granularity SOPMD over PM interval. U16 in increments of 0.01ps^2.	RO Opt.
150-151	15-0	rxMaxHGSopmdPm	Maximum value of high granularity SOPMD over PM interval. U16 in increments of 0.01ps^2.	RO Opt.
152-153	15-0	rxAvgPdlPm	Average value of polarization dependent loss over PM interval. U16 in increments of 0.1dB.	RO Opt.
154-155	15-0	rxMinPdlPm	Minimum value of polarization dependent loss over PM interval. U16 in increments of 0.1dB.	RO Opt.
156-157	15-0	rxMaxPdlPm	Maximum value of polarization dependent loss over PM interval. U16 in increments of 0.1dB.	RO Opt.
158-159	15-0	rxAvgOsnrPm	Average value of OSNR estimate over PM interval. U16 in increments of 0.1dB.	RO Opt.
160-161	15-0	rxMinOsnrPm	Minimum value of OSNR estimate over PM interval. U16 in increments of 0.1dB.	RO Opt.
162-163	15-0	rxMaxOsnrPm	Maximum value of OSNR estimate over PM interval. U16 in increments of 0.1dB.	RO Opt.
164-165	15-0	rxAvgEsnrPm	Average value of eSNR over PM Interval. U16 in increments of 0.1 dB.	RO Opt.
166-167	15-0	rxMinEsnrPm	Minimum value of eSNR over PM Interval. U16 in increments of 0.1 dB.	RO Opt.
168-169	15-0	rxMaxEsnrPm	Maximum value of eSNR over PM Interval. U16 in increments of 0.1 dB.	RO Opt.

170-171	15-0	rxAvgCfoPm	Average value of carrier frequency offset over PM interval. S16 in increments of 1MHz.	RO Opt.
172-173	15-0	rxMinCfoPm	Minimum value of carrier frequency offset over PM interval. S16 in increments of 1MHz.	RO Opt.
174-175	15-0	rxMaxCfoPm	Maximum value of carrier frequency offset over PM interval. S16 in increments of 1MHz.	RO Opt.
176-177	15-0	rxAvgEvmModemPm	Average value of error vector magnitude of the modem over PM interval. U16 in increments of 100/65535%	RO Opt.
178-179	15-0	rxMinEvmModemPm	Minimum value of error vector magnitude over PM interval. U16 in increments of 100/65535%	RO Opt.
180-181	15-0	rxMaxEvmModemPm	Maximum value of error vector magnitude over PM interval. U16 in increments of 100/65535%	RO Opt.
182-183	15-0	txAvgPowerPm	Average value of Tx output optical power over PM interval. S16 in increments of 0.01 dBm.	RO Opt.
184-185	15-0	txMinPowerPm	Minimum value of Tx output optical power over PM interval. S16 in increments of 0.01 dBm.	RO Opt.
186-187	15-0	txMaxPowerPm	Maximum value of Tx output optical power over PM interval. S16 in increments of 0.01 dBm.	RO Opt.
188-189	15-0	rxAvgPowerPm	Average value of Rx input optical power over PM interval. S16 in increments of 0.01 dBm.	RO Opt.
190-191	15-0	rxMinPowerPm	Minimum value of Rx input optical power over PM interval. S16 in increments of 0.01 dBm.	RO Opt.
192-193	15-0	rxMaxPowerPm	Maximum value of Rx input optical power over PM interval. S16 in increments of 0.01 dBm.	RO Opt.
194-195	15-0	rxAvgSigPowerPm	Average value of Rx input optical Signal power over PM interval. S16 in increments of 0.01 dBm.	RO Opt.
196-197	15-0	rxMinSigPowerPm	Minimum value of Rx input optical Signal power over PM interval. S16 in increments of 0.01 dBm.	RO Opt.
198-199	15-0	rxMaxSigPowerPm	Maximum value of Rx input optical Signal power over PM interval. S16 in increments of 0.01 dBm.	RO Opt.
200-201	15-0	rxAvgSopcrPm	Average value of state of polarization change rate over PM interval. U16 in increments of 1 krads/s.	RO Opt.
202-203	15-0	rxMinSopcrPm	Minimum value of state of polarization change rate over PM interval. U16 in increments of 1 krads/s.	RO Opt.
204-205	15-0	rxMaxSopcrPm	Maximum value of state of polarization change rate over PM interval. U16 in increments of 1 krads/s.	RO Opt.
206-207	15-0	rxAvgMerPm	Average value of Modulation Error Ratio over PM interval. U16 in increments of 0.1 dB	RO Opt.

208-209	15-0	rxMinMerPm	Minimum value of Modulation Error Ratio over PM interval. U16 in increments of 0.1 dB	RO Opt.
210-211	15-0	rxMaxMerPm	Maximum value of Modulation Error Ratio over PM interval. U16 in increments of 0.1 dB	RO Opt.
212-213	15-0	rxAvgClockRecPm	Average value of clock recovery loop monitor over PM interval. S16 in increments of 100/32767%	RO Opt.
214-215	15-0	rxMinClockRecPm	Minimum value of clock recovery loop monitor over PM interval. S16 in increments of 100/32767%	RO Opt.
216-217	15-0	rxMaxClockRecPm	Maximum value of clock recovery loop monitor over PM interval. S16 in increments of 100/32767%	RO Opt.
218-219	15-0	rxAvgLGSopmdPm	Average value of low granularity SOPMD over PM interval. U16 in increments of 1ps^2.	RO Opt.
220-221	15-0	rxMinLGSopmdPm	Minimum value of low granularity SOPMD over PM interval. U16 in increments of 1ps^2.	RO Opt.
222-223	15-0	rxMaxLGSopmdPm	Maximum value of low granularity SOPMD over PM interval. U16 in increments of 1ps^2.	RO Opt.
224-225	15-0	rxAvgSNRMarginPm	Average value of SNR Margin over PM interval. S16 in increments of 0.1 dB.	RO Opt.
226-227	15-0	rxMinSNRMarginPm	Minimum value of SNR Margin over PM interval. S16 in increments of 0.1 dB.	RO Opt.
228-229	15-0	rxMaxSNRMarginPm	Maximum value of SNR Margin over PM interval. S16 in increments of 0.1 dB.	RO Opt.
230-231	15-0	rxAvgQFactorPm	Average value of Q factor over PM interval. U16 in increments of 0.1 dB.	RO Opt.
232-233	15-0	rxMinQFactorPm	Minimum value of Q factor value over PM interval. U16 in increments of 0.1 dB.	RO Opt.
234-235	15-0	rxMaxPmQFactor	Maximum value of Q factor value over PM interval. U16 in increments of 0.1 dB.	RO Opt.
236-237	15-0	rxAvgQMarginPm	Average value of Q Margin over PM interval. S16 in increments of 0.1 dB.	RO Opt.
238-239	15-0	rxMinQMarginPm	Minimum value of Q Margin over PM interval. S16 in increments of 0.1 dB.	RO Opt.
240-241	15-0	rxMaxQMarginPm	Maximum value of Q Margin over PM interval. S16 in increments of 0.1 dB.	RO Opt.
242-247	7-0	Reserved		RO
248-255	All	Custom		

7.5 Host Interface registers

The host interfaces of different data paths are described in pages with different bank index. The bank index for a data path is the smallest lane index of all host lanes of the data path, bank 0 = lane1. For an application that supports 4x100GE (GAUI2) for host interfaces, the banks would be 0, 2, 4, and 6.

Table 16: Host Interface registers

Page Number	Page Description	Notes
38h	Data Path Host Interface Configuration	
39h	Reserved Data Path Interface Future Use	
3Ah	Data Path Host Interface Performance Monitoring	
3Bh	Data Path Host Interface Flags and Masks	
3C-3Fh	Reserved	

7.5.1 Data Path Host Interface Configuration (Page 38h)

The host uses page 38h to configure data path host interface specific features.

One configurable feature is the host link degrade monitoring. This optional capability requires monitoring the pre-FEC BER in the Ethernet RS(544,514) decoder block over a performance monitoring interval. Section 8.8.4 in the 400ZR Implementation Agreement [400ZR IA] describes the details of the host Link Degrade Indication (LDI) functions. The 400ZR IA also defines monitoring for the FEC Detected Degrade (FDD) and FEC Excessive Degrade (FED) functions, which that the host can configure per data path interface on page 38h and associated banked pages.

The enable bits for the FDD and FED are located in 38h:136.1-0. When the host enables FDD, the module compares the FDD activate and clear BER thresholds to the average BER computed over the PM interval. If the average BER exceeds the activate FDD BER threshold FDD is set and the over PM Interval Latch is asserted (3Bh:192.0). If the average BER drops below the clear FDD BER threshold, the state of FDD clears. The alarm bit should be updated at least once per second. The module performs analogous operations when the host enables FED, except that that asserted alarm bit for FED is located in 3Bh:192.1 .

Hysteresis will be left as an implementation detail.

Table 17: Data Path Host Interface Configuration (Page 38h)

Byte	Bits	Name	Description	Type
128-129	15-0	fddActBerThresh	BER threshold for FEC Detected Degrade (FDD) to become active on the data path host interface. Data format: F16.	RW Opt.
130-131	15-0	fddClrBerThresh	BER threshold for FEC Detected Degrade (FDD) to clear on the data path host interface. Data format: F16.	RW Opt.
132-133	15-0	fedActBerThresh	BER threshold for FEC Excessive Degrade (FED) to become active on the data path host interface. Data format: F16.	RW Opt.
134-135	15-0	fedClrBerThresh	BER threshold for FEC Excessive Degrade (FED) to clear on the data path host interface. Data format: F16.	RW Opt.
136	7-3	Reserved	Reserved	RO
	2	lfInsertionOnLdEnable	Enable for insertion of LF on the detection of LD. Default is disabled.	RW Opt.
	1	fedMonEnable	Enable for FEC Excessive Degrade (FED) monitoring feature.	RW Opt.
	0	fddMonEnable	Enable for FEC Detected Degrade (FDD) monitoring feature	RW Opt.
137-247	All	Reserved	Reserved	RO
248-255	All	Custom		

7.5.2 Data Path Host Interface Performance Monitoring (Page 3Ah)

Page 3Ah contains optional host read-only statistics reporting of errors on the data path host interface. The module collects the information in these registers during the prior PM interval. The bank index for a data path is the smallest lane index of all host lanes of the data path.

Table 18: Data Path Host Interface Performance Monitoring (Page 3Ah)

Byte	Bits	Name	Description	Type
128-135	63-0	txBitsPm	Number of bits received from the host side during prior PM interval. U64.	RO
136-143	63-0	txBitsSubIntPm	Number of bits received from the host side during any sub-interval (CMIS fine interval) of prior PM interval. U64.	RO
144-151	63-0	txCorrBitsPm	Number of corrected bits received from the host side during prior PM interval. U64.	RO

152-159	63-0	txMinCorrBitsSubIntPm	Minimum number of corrected bits received from the host side during any sub-interval (CMIS fine interval) of prior PM interval. U64.	RO
160-167	63-0	txMaxCorrBitsSubIntPm	Maximum number of corrected bits received from the host side during any sub-interval (CMIS fine interval) of prior PM interval. U64.	RO
168-171	31-0	txFramesPm	Number of frames received from the host side during prior PM interval. U32.	RO
172-175	31-0	txFramesSubIntPm	Number of frames received from the host side during any sub-interval (CMIS fine interval) of prior PM interval. U32.	RO
176-179	31-0	txFramesUncorrErrPm	Number of frames received from the host side with uncorrectable errors during prior PM interval. U32.	RO
180-183	31-0	txMinFramesUncorrErrSubintPm	Minimum number of frames received from the host side with uncorrectable errors during any sub-interval (CMIS fine interval) of prior PM interval. U32.	RO
184-187	31-0	txMaxFramesUncorrErrSubintPm	Maximum number of frames received from the host side with uncorrectable errors during any sub-interval (CMIS fine interval) of prior PM interval. U32.	RO
188-191	31-0	txCorrectedFramesPm	Number of frames received from the host side with corrected errors during prior PM interval. U32.	RO
192-195	31-0	txCorrectedFramesSubintPm	Number of frames received from the host side with corrected errors during any sub-interval (CMIS fine interval) of prior PM interval. U32.	RO
196-247	All	Reserved		RO
248-255	All	Custom		

7.5.3 Data Path host Interface Flags and Masks (page 3Bh)

Page 3Bh contains the masks and latches for the host data path alarms. It is a banked page with each bank corresponding to a unique data path.

Table 19: Data Path Host Interface Flags and Masks (page 3Bh)

Byte	Bits	Name	Description	Type
128	7-2	Reserved	Reserved	RO
	1	mtxFedPm	Mask for FEC Excessive Degrade (FED) over PM Interval alarm	RW
	0	mtxFddPm	Mask for FEC Detected Degrade (FDD) over PM Interval alarm	RW Opt.
129	7-2	Reserved	Reserved	RO
	1	mtxRD	Mask for Remote Degrade alarm	RW Opt.
	0	mtxLD	Mask for Local Degrade alarm	RW Opt.
130	7	mrxFlexeRPF	Mask for flexe Remote PHY Fault alarm	RW Opt.
	6	mrxFlexegidMM	Mask for flexe GID Mismatch alarm	RW Opt.
	5	mrxFlexeInstanceMapMM	Mask for flexe Instance Map Mismatch alarm	RW Opt.
	4	mrxFlexeCalendarMM	Mask for flexe Calendar Mismatch alarm	RW Opt.
	3	mrxFlexeiidMM	Mask for flexe Instance Id Mismatch alarm	RW Opt.
	2	mrxFlexeLOF	Mask for flexe Loss of Frame alarm	RW Opt.
	1	mrxFlexeLOM	Mask for flexe Loss of Multi-Frame alarm	RW Opt.
	0	mrxFlexeLOPB	Mask for flexe Loss of Pad Block alarm	RW Opt.
131	7-3	Reserved	Reserved	RO
	2	mtxLOA	Mask for transmit Loss of Alignment	RW Opt.
	1	mtxRF	Mask for transmit Remote Fault	RW Opt.
	0	mtxLF	Mask for transmit Local Fault	RW Opt.
132	7-3	Reserved	Reserved	RO
	2	mrxLOA	Mask for receive Loss of Alignment	RW Opt.
	1	mrxRF	Mask for receive Remote Fault	RW Opt.
	0	mrxLF	Mask for receive Local Fault	RW Opt.
133-174	All	Reserved	Reserved	RO

175-191	All	Custom		
192	7-2	Reserved	Reserved	RO
	1	ltxFedPm	Latched FEC Excessive Degrade (FED) over PM Interval alarm	COR opt
	0	ltxFddPm	Latched FEC Detected Degrade (FDD) over PM Interval alarm	COR opt
193	7-2	Reserved	Reserved	RO
	1	ltxRD	Latched Remote Degrade alarm	COR opt
	0	ltxLD	Latched Local Degrade alarm	COR opt
194	7	lrxFlexeRPF	Latched flexe Remote PHY Fault alarm	COR opt
	6	lrxFlexegidMM	Latched flexe GID Mismatch alarm	COR opt
	5	lrxFlexeInstanceMapMM	Latched flexe Instance Map Mismatch alarm	COR opt
	4	lrxFlexeCalendarMM	Latched flexe Calendar Mismatch alarm	COR opt
	3	lrxFlexeiidMM	Latched flexe Instance Id Mismatch alarm	COR opt
	2	lrxFlexeLOF	Latched flexe Loss of Frame alarm	COR opt
	1	lrxFlexeLOM	Latched flexe Loss of Multi-Frame alarm	COR opt
	0	lrxFlexeLOPB	Latched flexe Loss of Pad Block alarm	COR opt
195	7-3	Reserved	Reserved	RO
	2	ltxLOA	Latched transmit Loss of Alignment	COR opt
	1	ltxRF	Latched transmit Remote Fault alarm	COR opt
	0	ltxLF	Latched transmit Local Fault alarm	COR opt
196	7-3	Reserved	Reserved	RO
	2	lrxLOA	Latched receive Loss of Alignment alarm	COR opt
	1	lrxRF	Latched receive Remote Fault alarm	COR opt
	0	lrxLF	Latched receive Local Fault alarm	COR opt
197-247	7-0	Reserved	Reserved	RO

248-255	All	Custom		

7.6 Coherent Module Capabilities Advertisement

Table 20: Coherent Module Capabilities Advertisement

Page Number	Page Description	Notes
40h	Reserved for Applications Advertisement	
41h	Rx Signal Power Advertisement and Ranges for Configurable Thresholds	
42h	Performance Monitoring Advertisement	
43h	Media Lane Provisioning Advertisement	
44h	Alarm Advertisement	
45h – 4Fh	Reserved	

7.6.1 Applications Advertisement (Page 40h)

Page 40h advertises application and module information.

Table 21: Media Lane Provisioning Advertisement (Page 40h)

Byte	Bit	Name	Description	Type
128	7-0	C-CmisRevision	C-CMIS revision number (decimal): The upper nibble (bits 7-4) is the integer part (major number) The lower nibble (bits 3-0) is the decimal part (minor number) Example: 01h indicates version 0.1, 21h indicates version 2.1.	RO
129 - 247	7-0	Reserved	Reserved	RO
248-255	All	Custom		

7.6.2 Rx Signal Power Advertisement and Ranges for Configurable Thresholds (Page 41h)

Hysteresis will be left as an implementation detail.

Table 22: Rx Signal Power Advertisement and Ranges for Configurable Thresholds (Page 41h)

Byte	Bits	Name	Description	Type
128	7-2	Reserved	Reserved	RO
	1	rxSigPowerImpl	0b: Not implemented 1b: Implemented	RO Opt.
	0	rxPowerImpl	0b: Not implemented 1b: Implemented	RO Opt.
129	7-3	Reserved	Reserved	RO
	2-0	RxLosType	000b: Reserved for backward compatibility. 001b: Rx LOS Responds to Rx Total Power 010b: Rx LOS Responds to Rx Signal Power 011b: Rx LOS Responds to Rx DSP frame Loss of Lock 100b: Total Power detection and DSP frame Loss of Lock hybrid Rx LOS Assert: “Total Power < LOS Asset threshold” AND “DSP LOL=True” Rx LOS De-assert: “Total Power > LOS De-asset threshold” OR “DSP LOL=False” 101b: Signal Power detection and DSP frame Loss of Lock hybrid Rx LOS Assert: “Signal Power < LOS Asset threshold” AND “DSP LOL=True” Rx LOS De-assert: “Signal Power > LOS De-asset threshold” OR “DSP LOL=False” 110b~111b: Reserved	RO Opt.
130-131	All	Reserved	Reserved	RO
132-133	15-0	rxTotalPwrHiAlmThreshMax	Maximum allowed value for Rx Total Power Configured High Alarm Threshold. S16 in increments of 0.01 dBm.	RO Opt.
134-135	15-0	rxTotalPwrHiAlmThreshMin	Minimum allowed value for Rx Total Power Configured High Alarm Threshold. S16 in increments of 0.01 dBm.	RO Opt.
136-137	15-0	rxTotalPwrLoAlmThreshMax	Maximum allowed value for Rx Total Power Configured Low Alarm Threshold. S16 in increments of 0.01 dBm.	RO Opt.
138-139	15-0	rxTotalPwrLoAlmThreshMin	Minimum allowed value for Rx Total Power Configured Low Alarm Threshold. S16 in increments of 0.01 dBm.	RO Opt.
140-141	15-0	rxTotalPwrHiWarnThreshMax	Maximum allowed value for Rx Total Power Configured High Warning Threshold. S16 in increments of 0.01 dBm.	RO Opt.

142-143	15-0	rxTotalPwrHiWarnThreshMin	Minimum allowed value for Rx Total Power Configured High Warning Threshold. S16 in increments of 0.01 dBm.	RO Opt.
144-145	15-0	rxTotalPwrLoWarnThreshMax	Maximum allowed value for Rx Total Power Configured Low Warning Threshold. S16 in increments of 0.01 dBm.	RO Opt.
146-147	15-0	rxTotalPwrLoWarnThreshMin	Minimum allowed value for Rx Total Power Configured Low Warning Threshold. S16 in increments of 0.01 dBm.	RO Opt.
148-149	15-0	rxSigPwrHiAlmThreshMax	Maximum allowed value for Rx Signal Power Configured High Alarm Threshold. S16 in increments of 0.01 dBm.	RO Opt.
150-151	15-0	rxSigPwrHiAlmThreshMin	Minimum allowed value for Rx Signal Power Configured High Alarm Threshold. S16 in increments of 0.01 dBm.	RO Opt.
152-153	15-0	rxSigPwrLoAlmThreshMax	Maximum allowed value for Rx Signal Power Configured Low Alarm Threshold. S16 in increments of 0.01 dBm.	RO Opt.
154-155	15-0	rxSigPwrLoAlmThreshMin	Minimum allowed value for Rx Signal Power Configured Low Alarm Threshold. S16 in increments of 0.01 dBm.	RO Opt.
156-157	15-0	rxSigPwrHiWarnThreshMax	Maximum allowed value for Rx Signal Power Configured High Warning Threshold. S16 in increments of 0.01 dBm.	RO Opt.
158-159	15-0	rxSigPwrHiWarnThreshMin	Minimum allowed value for Rx Signal Power Configured High Warning Threshold. S16 in increments of 0.01 dBm.	RO Opt.
160-161	15-0	rxSigPwrLoWarnThreshMax	Maximum allowed value for Rx Signal Power Configured Low Warning Threshold. S16 in increments of 0.01 dBm.	RO Opt.
162-163	15-0	rxSigPwrLoWarnThreshMin	Minimum allowed value for Rx Signal Power Configured Low Warning Threshold. S16 in increments of 0.01 dBm.	RO Opt.
164-247	All	Reserved		RO
248-255	All	Custom		

7.6.3 Performance Monitoring Advertisement (Page 42h)

Page 42h advertises which media lane performance monitors and performance statistics are implemented.
The implementation advertisements on this page are global, i.e. if a feature is advertised as implemented (bit value 1b), this feature is implemented for all media lanes (banks).

Table 23: Performance Monitoring Advertisement (Page 42h)

Byte	Bit	Name	Description	Type
128	7-5	Reserved		RO Rqd.
	4	rxBitsPmImpl	0b = Not implemented, 1b = Implemented	
	3	rxBitsSubIntPmImpl	0b = Not implemented, 1b = Implemented	
	2	rxCorrBitsPmImpl	0b = Not implemented, 1b = Implemented	
	1	rxMinCorrBitsSubIntPmImpl	0b = Not implemented, 1b = Implemented	
	0	rxMaxCorrBitsSubIntPmImpl	0b = Not implemented, 1b = Implemented	
129	7-5	Reserved		RO Rqd.
	4	rxFramesPmImpl	0b = Not implemented, 1b = Implemented	
	3	rxFramesSubIntPmImpl	0b = Not implemented, 1b = Implemented	
	2	rxFramesUncorrErrPmImpl	0b = Not implemented, 1b = Implemented	
	1	rxMinFramesUncorrErrSubintPmImpl	0b = Not implemented, 1b = Implemented	
	0	rxMaxFramesUncorrErrSubintPmImpl	0b = Not implemented, 1b = Implemented	
130	7	rxCdImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	6	rxAvgCdPmImpl	0b = Not implemented, 1b = Implemented	
	5	rxMinCdPmImpl	0b = Not implemented, 1b = Implemented	
	4	rxMaxCdPmImpl	0b = Not implemented, 1b = Implemented	
	3	rxDgdImpl	0b = Not implemented, 1b = Implemented	
	2	rxAvgDgdPmImpl	0b = Not implemented, 1b = Implemented	
	1	rxMinDgdPmImpl	0b = Not implemented, 1b = Implemented	
	0	rxMaxDgdPmIpl	0b = Not implemented, 1b = Implemented	
131	7	rxLGSopmdPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	6	rxAvgLGSopmdPmImpl	0b = Not implemented, 1b = Implemented	

	5	rxMinLGSopmdPmImpl	0b = Not implemented, 1b = Implemented	
	4	rxMaxLGSopmdPmImpl	0b = Not implemented, 1b = Implemented	
	3	rxPdlImpl	0b = Not implemented, 1b = Implemented	
	2	rxAvgPdlPmImpl	0b = Not implemented, 1b = Implemented	
	1	rxMinPdlPmImpl	0b = Not implemented, 1b = Implemented	
	0	rxMaxPdlPmImpl	0b = Not implemented, 1b = Implemented	
132	7	rxOsnrImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	6	rxAvgOsnrPmImpl	0b = Not implemented, 1b = Implemented	
	5	rxMinOsnrPmImpl	0b = Not implemented, 1b = Implemented	
	4	rxMaxOsnrPmImpl	0b = Not implemented, 1b = Implemented	
	3	rxEsnrImpl	0b = Not implemented, 1b = Implemented	
	2	rxAvgEsnrPmImpl	0b = Not implemented, 1b = Implemented	
	1	rxMinEsnrPmImpl	0b = Not implemented, 1b = Implemented	
	0	rxMaxEsnrPmImpl	0b = Not implemented, 1b = Implemented	
133	7	rxCfoImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	6	rxAvgCfoPmImpl	0b = Not implemented, 1b = Implemented	
	5	rxMinCfoPmImpl	0b = Not implemented, 1b = Implemented	
	4	rxMaxCfoPmImpl	0b = Not implemented, 1b = Implemented	
	3	rxEvmModemImpl	0b = Not implemented, 1b = Implemented	
	2	rxAvgEvmModemPmImpl	0b = Not implemented, 1b = Implemented	
	1	rxMinEvmModemPmImpl	0b = Not implemented, 1b = Implemented	
	0	rxMaxEvmModemPmImpl	0b = Not implemented, 1b = Implemented	

134	7	rxSopcrImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	6	rxAvgSopcrPmImpl	0b = Not implemented, 1b = Implemented	
	5	rxMinSopcrPmImpl	0b = Not implemented, 1b = Implemented	
	4	rxMaxSopcrPmImpl	0b = Not implemented, 1b = Implemented	
	3	txPowerImpl	0b = Not implemented, 1b = Implemented	
	2	txAvgPowerPmImpl	0b = Not implemented, 1b = Implemented	
	1	txMinPowerPmImpl	0b = Not implemented, 1b = Implemented	
	0	txMaxPowerPmImpl	0b = Not implemented, 1b = Implemented	
135	7	rxPowerImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	6	rxAvgPowerPmImpl	0b = Not implemented, 1b = Implemented	
	5	rxMinPowerPmImpl	0b = Not implemented, 1b = Implemented	
	4	rxMaxPowerPmImpl	0b = Not implemented, 1b = Implemented	
	3	rxSigPowerImpl	0b = Not implemented, 1b = Implemented	
	2	rxAvgSigPowerPmImpl	0b = Not implemented, 1b = Implemented	
	1	rxMinSigPowerPmImpl	0b = Not implemented, 1b = Implemented	
	0	rxMaxSigPowerPmImpl	0b = Not implemented, 1b = Implemented	
136	7-2	Reserved	Reserved	RO
	1	rxMediaFedPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	0	rxMediaFddPmImpl	0b = Not implemented, 1b = Implemented	
137	7-2	Reserved	Reserved	RO
	1	txHostFedPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	0	txHostFddPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
138	7	rxClockRecPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.

	6	rxAvgClockRecPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	5	rxMinClockRecPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	4	rxMaxClockRecPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	3	rxHGSopmdPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	2	rxAvgHGSopmdPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	1	rxMinHGSopmdPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	0	rxMaxHGSopmdPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
139	7	rxSNRMarginPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	6	rxAvgSNRMarginPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	5	rxMinSNRMarginPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	4	rxMaxSNRMarginPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	3	rxMERPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	2	rxAvgMERPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	1	rxMinMERPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	0	rxMaxMERPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
140	7	rxQFactorPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	6	rxAvgQFactorPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	5	rxMinQFactorPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	4	rxMaxQFactorPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	3	rxQMarginPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	2	rxAvgQMarginPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	1	rxMinQMarginPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.

	0	rxMaxQMarginPmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
141 - 247	7-0	Reserved	Reserved	RO
248-255	All	Custom		

7.6.4 Media Lane Provisioning Advertisement (Page 43h)

Page 43h advertises which media lane provisioning parameters are implemented.
The implementation advertisements on this page are global, i.e. if a feature is advertised as implemented (bit value 1b), this feature is implemented for all media lanes (banks).

Table 24: Media Lane Provisioning Advertisement (Page 43h)

Byte	Bit	Name	Description	Type
128	7-2	Reserved	Reserved	RO
	1	lfInsertionOnLdEnableImpl	0b = Not implemented, 1b = Implemented	
	0	txFilterImpl	0b = Not implemented, 1b = Implemented	
129 - 247	7-0	Reserved	Reserved	RO
248-255	All	Custom		

7.6.5 Alarm Advertisement (Page 44h)

Page 44h advertises which media and host lane alarms are implemented.
The implementation advertisements on this page are global, i.e. if a feature is advertised as implemented (bit value 1b), this feature is implemented for all lanes (banks).

Table 25: Alarm Advertisement (Page 44h)

Byte	Bit	Name	Description	Type
128	7-6	Reserved		RO Rqd.
	5	MediaTxLoaImpl	0b = Not implemented, 1b = Implemented	
	4	MediaTxOoaImpl	0b = Not implemented, 1b = Implemented	
	3	MediaTxLolCmuImpl	0b = Not implemented, 1b = Implemented	
	2	MediaTxLolRefClkImpl	0b = Not implemented, 1b = Implemented	
	1	MediaTxLolDeSkewImpl	0b = Not implemented, 1b = Implemented	

	0	MediaTxFIFOImpl	0b = Not implemented, 1b = Implemented	
129	7	MediaRxLofImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	6	MediaRxLomImpl	0b = Not implemented, 1b = Implemented	
	5	MediaRxLolDemodImpl	0b = Not implemented, 1b = Implemented	
	4	MediaRxLolCdImpl	0b = Not implemented, 1b = Implemented	
	3	MediaRxLoaImpl	0b = Not implemented, 1b = Implemented	
	2	MediaRxOoaImpl	0b = Not implemented, 1b = Implemented	
	1	MediaRxLolDeskewImpl	0b = Not implemented, 1b = Implemented	
	0	MediaRxLolFifoImpl	0b = Not implemented, 1b = Implemented	
130	7-2	Reserved	Reserved	RO
	1	MediaRxFedAlmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	0	MediaRxFddAlmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
131	7-3	Reserved	Reserved	RO
	2	MediaRDImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	1	MediaLDImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	0	MediaRPFImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
132	7-2	Reserved	Reserved	RO
	1	HostTxFedAlmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	0	HostTxFddAlmImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
133	7-2	Reserved	Reserved	RO
	1	HostTxRDImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	0	HostTxLDImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
134	7	HostRxFlexeRPFImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	6	HostRxFlexegidMMImpl	0b = Not implemented, 1b = Implemented	RO Rqd.

	5	HostRxFlexeInstanceMapMMImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	4	HostRxFlexeCalendarMMImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	3	HostRxFlexeiidMMImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	2	HostRxFlexeLOFImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	1	HostRxFlexeLOMImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	0	HostRxFlexeLOPBImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
135	7-3	Reserved	Reserved	RO
	2	HostTxLOAImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	1	HostTxRFImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	0	HostTxLFImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
136	7-3	Reserved	Reserved	RO
	2	HostRxLOAImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	1	HostRxRFImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
	0	HostRxLFImpl	0b = Not implemented, 1b = Implemented	RO Rqd.
137 - 247	7-0	Reserved	Reserved	RO
248-255	All	Custom		

8 Reference Documents

8.1 Normative References

[CMIS] Common Management Interface Specification Rev 5.2 - https://www.oiforum.com/wp-content/uploads/OIF-CMIS-05.2.pdf

[400ZR IA] Implementation Agreement 400ZR : https://www.oiforum.com/wp-content/uploads/OIF-400ZR-02.0.pdf

8.2 Informational References

[ICTROSA IA] Implementation Agreement for Integrated Coherent Transmit-Receive Optical Sub Assembly- https://www.oiforum.com/wp-content/uploads/OIF-IC-TROSA-01.0.pdf

[CFP MIS] CFP MSA Management Interface Specification http://www.cfp-msa.org/Documents/CFP_MSA_MIS_V2p6r06a.pdf

9 Appendix A: Glossary

The Glossary presents definitions for acronyms and terms used in this IA.

Table 26: Glossary

Term	Definition	Term	Definition
BER	Bit Error Rate	**LOS**	Loss of Signal
CD	Chromatic Dispersion	**LSB**	Least Significant Bit
CDB	Common Data Block	**MER**	Modulation Error Ratio
CFO	Carrier Frequency Offset	**MHz**	MegaHertz
CMIS	Common Management Interface Specification	**MSB**	Most Significant Bit
CMU	Clock Monitor Unit	**nm**	nanometer
COR	Clear on Read	**NVR**	Non-Volatile Memory
dB	Decibels	**OSNR**	Optical Signal to Noise Ratio
dBm	Decibels reference to 1mW	**OOA**	Out of Alignment
DGD	Differential Group Delay	**PDL**	Polarization Dependent Loss
eSNR	Electrical Signal to Noise Ratio	**PM**	Performance Monitoring
EVM_modem	Error Vector Magnitude of the entire modem	**PMA**	Physical Medium
FDD	FEC Detected Degrade	**PMD**	Polarization Mode Dispersion
FEC	Forward Error Correction	**Q-Value**	Decibel (dB) value representing BER
FED	FEC Excessive Degrade	**Ps**	Picoseconds
FER	Frame Error Rate	**Rx**	Receiver
FIFO	First In First Out	**RF**	Remote Fault
GHz	GigaHertz	**RO**	Read Only
GMP	Generic Mapping Procedure	**ROC**	Rate of Change
IA	Implementation Agreement	**RW**	Read Write
Krad/s	Thousand rads per second	**SOP**	State of Polarization
LF	Local Fault	**SOPMD**	Second Order Polarization Mode Dispersion
LOA	Loss of Alignment	**SOP ROC**	State Of Polarization Rate Of Change
LOF	Loss of Frame	**Tx**	Transmitter
LOL	Loss of Lock	**VDM**	Versatile Diagnostics Monitor
LOM	Loss of Multiframe	**VR**	Volatile Memory

10 Appendix B: Open Issues / Current Work Items

- Add additional loopbacks through CDB to support all 6 loopbacks as defined in the 400ZR IA
- Add constellation pull through CDB

11 Appendix C: List of Companies Belonging to OIF when Document is Approved

Accton Technology Corporation	EFFECT Photonics B.V.	Lessengers Inc.	Rosenberger Hochfrequenztechnik
ADTRAN	Eoptolink Technology	Linktel Technologies Co., Ltd.	Ruijie Networks Co., Ltd.
Advanced Fiber Resources (AFR)	Epson Electronics America, Inc.	LIPAC	Samsung Electronics Co. Ltd.
Advanced Micro Devices, Inc.	Ericsson	Lumentum	Samtec Inc.
AIO Core Co., Ltd	EXFO	Luxshare-ICT	SCINTIL Photonics
Alibaba	Fathom Radiant	MACOM Technology Solutions	Semtech Canada Corporation
Aloe Semiconductor, Inc.	Foxconn Interconnect Technology Ltd	Marvell Semiconductor, Inc.	Senko Advanced Components
Alphawave Semi	Fujikura	MaxLinear Inc.	SeriaLink Systems Ltd.
Amphenol Corp.	Fujitsu	MediaTek	Sicoya GmbH
Applied Optoelectronics, Inc.	Furukawa Electric Co., Ltd.	Meta Platforms	SiFotonics Technologies Inc.
Arista Networks	Global Foundries	Microchip Technology Incorporated	Silith Technology
Astera Labs	Google	Microsoft Corporation	Socionext Inc.
Ayar Labs	H3C	Mitsubishi Electric Corporation	Source Photonics, Inc.
BitifEye Digital Test Solutions GmbH	Hakusan Inc	Molex	Spirent Communications
BizLink Technology, Inc.	Hewlett Packard Enterprise (HPE)	Multilane Inc.	Sumitomo Electric Industries, Ltd.
Broadcom Inc.	Hirose Electric Co. Ltd.	NEC Corporation	Sumitomo Osaka Cement
Cadence Design Systems	Hisense Broadband Multimedia Technologies Co., LTD	Nokia	Synopsys, Inc.
Casela Technologies USA	Huawei Technologies Co., Ltd.	NTT Corporation	TE Connectivity
Celestica	Infinera	Nubis Communications, Inc.	Tektronix
China Information Communication Technologies Group	InfiniLink	NVIDIA Corporation	Telefonica S.A.
China Telecom	InnoLight Technology Limited	O-Net Communications	TELUS Communications, Inc.
Ciena Corporation	Integrated Device Technology	Optomind Inc.	Teramount
Cisco Systems	Intel	Orange	US Conec
Coherent	Jabil Canada Corporation	PETRA	Viavi Solutions Deutschland GmbH
Cornelis Networks, Inc.	Juniper Networks	Precision Optical Transceivers, Inc.	Wilder Technologies, LLC
Corning	Kandou Bus	Quantifi Photonics USA Inc.	Wistron Corporation

Credo Semiconductor (HK) LTD	KDDI Research, Inc.	Quintessent Inc.	Yamaichi Electronics Ltd.
Dell, Inc.	Keysight Technologies, Inc.	Rambus Inc.	ZTE Corporation
Dexerials Corporation	Kuaishou Technology	Ranovus	
DustPhotonics	KYOCERA Corporation	Retym	