IA Title: Common Electrical I/O (CEI) - Electrical and Jitter Interoperability agreements for 6G+ bps, 11G+ bps, 25G+ bps, 56G+ bps and 112G+ bps I/O

IA # OIF-CEI-05.3

July 17, 2025

Implementation Agreement created and approved

by the Optical Internetworking Forum

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Implementation Agreement: OIF-CEI-05.3

Working Group: Physical and Link Layer

Title: Common Electrical I/O (CEI) - Electrical and Jitter Interoperability agreements for 6G+ bps, 11G+ bps, 25G+ bps, 56G+ bps and 112G+ bps I/O

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ABSTRACT:

This document is the CEI implementation agreement, which specifies the transmitter, receiver and interconnect channel associated with 6G+ bps, 11G+ bps, 25G+ bps, 56G+ bps and 112G+ bps interfaces for application in high speed backplanes, chip to chip interconnect and optical modules. Also included is the Jitter definition and measurement methodologies associated with CEI interfaces.

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0 Document Structure and Contents

0.1 Revision History

The OIF document 2003.104 was the working document used for the development of the CEI-6G-SR, CEI-6G-LR, CEI-11G-SR interfaces and the jitter methodology. The history of this document is detailed in the table below:

Revision	Date	Description
OIF 2003.104.00	28th March 2003,	Draft 1.0. Compiled from baseline documents oif2002.605.03 (clause 0, 1), OIF2002.536.06 (clause 2), oif2002.520.02 (clauses 4, 5), OIF2002.506.02 (clause 6)
OIF 2003.104.01	3rd May 2003	Draft 2.0. Contains changes as result from comments received from Draft 1.0. Section added in Clause 6 relating to transparent application, derived from XFP specification. Parameters added re DC coupling option, derived from OIF2003.129
OIF 2003.104.02	24th May 2003	Draft 3.0. Updated to include approved changes from the OIF Plenary meeting in Scottsdale, 6-8 May 2003
OIF 2003.104.03	2nd October 2003	Draft 4.0. Updated to include changes as results of comment resolution from CEI Straw ballot (ballot#41), approved at the Ottawa meeting July 2003
OIF 2003.104.04	17th November 2003	Draft 4.1. As draft 4.0 but including changes approved at the Berlin interim/ plenary meetings 13 - 16 October 2003. These changes are summarized in OIF2003.326.03.
OIF2003.104.05	10th February 2004	Draft 5.0. Updated to include changes as results of comment resolution from the second CEI Straw ballot (ballot#49), approved at the San Diego meeting January 2004
OIF2003.104.06	5th May 2004	Draft 6.0. Updated to include changes as result of comment resolution from 3rd Straw ballot (ballot no 52), as approved at the Orlando Interim meeting March 15th 2004.
OIF2003.104.07	14th July 2004	Draft 7.0. As Draft 6.0, but updated to include changes approved at the Budapest Plenary meeting. Clause 2 reconstructed and SXI-5 and TFI-5 interfaces described as new clauses 4 and 5. Previous clauses 4,5,6 are renumbered as clauses 6,7,8
OIF2003.104.08	26th August 2004	Clause 8 modified to include changes agreed at the Hawaii Plenary meeting, to address discrepancies between CEI and XFP specifications.
OIF2003.104.09	20th October 2004	Draft 9.0. Updated to include changes as result of comment resolution from 4th Straw ballot (ballot no 55),
OIF2003.104.10	8th November 2004	Draft 10.0. As draft 9.0 with specific reference to version no of State Eye scripts in section 2.C.5 removed.

This revision was published as OIF-CEI-01.00 in December 2004.

The OIF document 2003.253 was the working document used for the development of the CEI-11G-MR and CEI-11G-LR interfaces. The history of this document is detailed in the table below:

Revision	Date	Description
OIF 2003.253.00	20th July 2003,	Draft 1.0. Compiled from baseline document oif2002.127.0 with changes and modifications from Scottsdale motions
OIF 2003.253.01	5th October 2003	Draft 1.1. adding changes and modifications from the July 2003 meeting in Ottawa. - New entries for table 1-1 moved to OIF2003.104. - Removed figure 1-1, table 1-2 and sections 1.8 and 3.2.10. - Moved appendix 3B to OIF2003.104 - Changed 7.2.8, 8 Taps down to 4 Taps - Changed 7.1 to required BER of 1e-15
OIF 2003.253.02	9th November 2003	Draft 2.0. adding changes and modifications from the October 2003 meeting in Berlin.
OIF2003.253.03	2nd February 2004	Draft 2.1 resolving comments from Straw ballot #50, motions and resolutions as agreed in the San Diego 2004 meeting. Corrections include: - DC coupling introduced with VTT = 1.2V - Channel compliance, section 7.2.7 - with introduction of reference transmitter and -receiver. - Changes in transmit amplitude to 1200mVppd max Comment resolution spread sheet, OIF2004.054.03 Clause 7 Editors report, OIF2004.053.01 PLL Meeting motions: OIF2004.076.00
OIF2003.253.04	3rd May 2004	Draft 2.2 resolving comments from straw ballot 53 and orlando interim meeting, March 15th. Corrections include - DC coupling editorials - Tap weight clarification - T_Y1 = 400 mVpp, T_Y2 = 600mVpp - driver and receiver absolute min and max voltages - Return loss alignment to 6G-LR
OIF2003.252.05	6 September 2004	Draft 2.3 including motions from Budapest and Hawaii meetings: - Changed clause no from 7 to 9 - Changed values in Table 9-1 and 9-8d - Changed reference receiver B definitions - Added appendix B, the StatEye.org template.
OIF2003.253.06	6 December 2004	Draft 3.0 including the motions from the Alexandria meeting, October 26-28 - Added CEI-11G-MR - Further specification of Reference Receiver B - StatEye templates for -LR Ref Receiver A and B and for -MR
OIF2003.253.06	25 January 2005	Draft 3.1 includes corrections to table 9.11 following discussions and motion from the Dallas meeting, 18-20 January 2005. Source documents uploaded as OIF2005.090.00

This revision was published as OIF-CEI-02.00 in February 2005.

The OIF document 2011.004 was the working document used for the development of maintenance updates to OIF-CEI-02.00. The comment resolution for this update is contained in 2011.121. These updates were published as part of OIF-CEI-03.00 in August 2011.

The OIF document 2008.029 was the working document used for the development of the CEI-28G-SR interface defined in clause 10. The history of this document is detailed in the table below:

Revision	Date	Description
OIF 2008.029.03	28th July 2008,	Document taken over from Beth Donnay
OIF 2008.029.04	23rd April 2009	Inserted text for all tbd locations according to work session results of Q2/09 meeting in Boston
OIF 2008.029.05	23rd April 2009	Finalized text proposal after continued discussion in Q2/09 meeting in Boston. Text proposal sent to Straw Ballot in Boston
OIF 2008.029.06	23rd July 2009	oif2009.129.02: Comment resolution according CEI-28-SR/25-LR Editors Report Finalized text proposal after continued discussion in Q3/09 meeting in Vancouver. Text proposal sent to Straw Ballot in Vancouver
OIF 2008.029.07	15th October 2009	oif2009.280.03: Comment Resolution Worksheet for CEI-28-SR Finalized text proposal after continued discussion in Q4/09 meeting in Lannion. Text proposal sent to Straw Ballot in Lannion and sent as liaison to IEEE 802.3ba for comments
OIF 2008.029.08	21st May 2010	oif2009.408.01: Comment Resolution Worksheet for CEI-28-SR Finalized text proposal after continued discussion in Q2/10 meeting in Hong Kong. Text proposal sent to Straw Ballot in electronic motion after Hong Kong meeting.
OIF 2008.029.09	25th August 2010	oif2010.239.01: Comment Resolution Worksheet for CEI-28-SR Finalized text proposal after continued discussion in Q3/10 meeting in Baltimore. Text proposal sent to Straw Ballot in electronic motion after Baltimore meeting.
OIF 2008.029.10	16th November 2010	oif2010.337.02: Comment Resolution Worksheet for CEI-25/28 Finalized text proposal after continued discussion in Q4/10 meeting in Nuremberg. Text proposal sent to Straw Ballot in electronic motion after Nuremberg meeting
OIF 2008.029.11	14th February 2011	oif2010.452.01: Comment Resolution Worksheet for CEI-25/28 Finalized text proposal after continued discussion in Q1/11 meeting in Dallas. Text proposal sent to Straw Ballot in electronic motion after Dallas meeting
OIF 2008.029.12	7th April 2011	oif2011.129.04: Comment Resolution Worksheet for CEI-25/28 Finalized text proposal after continued discussion in Q2/11 meeting in Glasgow. Text proposal sent to Straw Ballot during Glasgow meeting with option for Principal.
OIF 2008.029.13	3rd June 2011	oif2011.198.01: Comment Resolution Worksheet for CEI-25/28 Resolution of LSI, Qlogic Straw Ballot comments. Text proposal sent to another Straw Ballot in electronic motion. oif2011.271.01: Comment Resolution Worksheet for CEI-25/28 Document sent to principal member ballot at Philadelphia meeting

The OIF document 2008.161 was the working document used for the development of the CEI-25G-LR interface defined in clause 11. The history of this document is detailed in the table below:

Revision	Date	Description
OIF 2008.161.03	28th July 2008,	Document taken over from Beth Donnay
OIF 2008.161.04	23rd April 2009	Inserted text for all tbd locations according to work session results of Q2/09 meeting in Boston
OIF 2008.161.05	23rd April 2009	Finalized text proposal after continued discussion in Q2/09 meeting in Boston. Text proposal sent to Straw Ballot in Boston
OIF 2008.161.06	23rd July 2009	oif2009.129.02: Comment resolution according CEI-28-SR/25-LR Editors Report Finalized text proposal after continued discussion in Q3/09 meeting in Vancouver. Text proposal sent to Straw Ballot in Vancouver
OIF 2008.161.07	15th October 2009	oif2009.281.02: Comment Resolution Worksheet for CEI-25-LR Finalized text proposal after continued discussion in Q4/09 meeting in Lannion. Text proposal sent to Straw Ballot in Lannion and sent as liaison to IEEE 802.3ba for comments
OIF 2008.161.08	21st May 2010	oif2009.409.01: Comment Resolution Worksheet for CEI-25-LR Finalized text proposal after continued discussion in Q2/10 meeting in Hong Kong. Text proposal sent to Straw Ballot in electronic motion after Hong Kong meeting.
OIF 2008.161.09	25th August 2010	oif2010.240.01: Comment Resolution Worksheet for CEI-25-LR Finalized text proposal after continued discussion in Q3/10 meeting in Baltimore. Text proposal sent to Straw Ballot in electronic motion after Baltimore meeting.
OIF 2008.161.10	16th November 2010	oif2010.337.02: Comment Resolution Worksheet for CEI-25/28 Finalized text proposal after continued discussion in Q4/10 meeting in Nuremberg. Text proposal sent to Straw Ballot in electronic motion after Nuremberg meeting
OIF 2008.161.11	14th February 2011	oif2010.452.01: Comment Resolution Worksheet for CEI-25/28 Finalized text proposal after continued discussion in Q1/11 meeting in Dallas. Text proposal sent to Straw Ballot in electronic motion after Dallas meeting
OIF 2008.161.12	7th April 2011	oif2011.129.04: Comment Resolution Worksheet for CEI-25/28 Finalized text proposal after continued discussion in Q2/11 meeting in Glasgow. Text proposal sent to Straw Ballot during Glasgow meeting with option for Principal.
OIF 2008.161.13	3rd June 2011	oif2011.198.01: Comment Resolution Worksheet for CEI-25/28 Resolution of LSI, Qlogic Straw Ballot comments. Text proposal sent to another Straw Ballot in electronic motion. oif2011.271.01: Comment Resolution Worksheet for CEI-25/28 Document sent to principal member ballot at Philadelphia meeting

The OIF document 2010.189 was the working document used for the development of the Test Methodologies for CEI-28G-SR and CEI-25G-LR defined in clause 12. The history of this document is detailed in the table below:

Revision	Date	Description
OIF 2010.189.00	12th May 2010	Separate Clause extracted for common 'TX Jitter and Channel Compliance Methodologies for CEI-28G-SR and CEI-25G-LR' in Q2/10 meeting in Hong Kong.
OIF 2010.189.01	12th May 2010	Modifications during Hong Kong meeting
OIF 2010.189.02	21st May 2010	Editorial changes of PLL chair, see change bars Text proposal sent to Straw Ballot in electronic motion after Hong Kong meeting.
OIF 2010.189.03	25th August 2010	oif2010.241.01: Comment Resolution Worksheet for Clause 12 Finalized text proposal after continued discussion in Q3/10 meeting in Baltimore. Text proposal sent to Straw Ballot in electronic motion after Baltimore meeting.
OIF 2010.189.04	16th November 2010	oif2010.337.02: Comment Resolution Worksheet for CEI-25/28 Finalized text proposal after continued discussion in Q4/10 meeting in Nuremberg. Text proposal sent to Straw Ballot in electronic motion after Nuremberg meeting
OIF 2010.189.05	14th February 2011	oif2010.452.01: Comment Resolution Worksheet for CEI-25/28 Finalized text proposal after continued discussion in Q1/11 meeting in Dallas. Text proposal sent to Straw Ballot in electronic motion after Dallas meeting
OIF 2010.189.06	7th April 2011	oif2011.129.04: Comment Resolution Worksheet for CEI-25/28 Finalized text proposal after continued discussion in Q2/11 meeting in Glasgow. Text proposal sent to Straw Ballot during Glasgow meeting with option for Principal.
OIF 2010.189.07	3rd June 2011	oif2011.198.01: Comment Resolution Worksheet for CEI-25/28 Resolution of LSI, Qlogic Straw Ballot comments. Text proposal sent to another Straw Ballot in electronic motion. oif2011.271.01: Comment Resolution Worksheet for CEI-25/28 Document sent to principal member ballot at Philadelphia meeting

The combined revision including changes of above documents was published as OIF-CEI-03.00 in September 2011.

The OIF document oif2013.329 was the working document used for the development of maintenance updates to OIF-CEI-03.00. The comment resolution for this update is contained in oif2014.051. These updates were published as part of OIF-CEI-05.3 in October 2013.

The OIF document 2010.404 was the working document used for the development of the CEI-28G-VSR interface defined in clause 13. The history of this document is detailed in the table below:

Revision	Date	Description
OIF 2010.404.00	26th October 2010,	Baseline text proposal
OIF 2010.404.01	28th October 2010,	Updated baseline text proposal
OIF 2010.404.02	26th May 2011	Updated baseline text proposal
OIF 2010.404.03	14th July 2011	Updated baseline text proposal
OIF 2010.404.04	27th July 2011	oif2011.180.00: VSR change document
OIF 2010.404.05	2nd December 2011	oif2011.411.02: VSR editor report
OIF 2010.404.06	12th March 2012	oif2012.055.01: VSR editor report -05
OIF 2010.404.07	14th May 2012	oif2012.164.02: VSR rev6-0 editor recommendations
OIF 2010.404.08	18th October 2012	oif2012.253.02: CEI-28G-VSR draft 7 comment summary
OIF 2010.404.09	6th February 2013	oif2013.036.02: VSR editor report Jan 2013
OIF 2010.404.10	21st May 2013	oif2013.150.01: CEI-28G-VSR 9-0 comment summary with editor recommendations
OIF 2010.404.11	25th July 2013	oif2013.255.02: CEI-28G-VSR rev10-0 editor report
OIF 2010.404.12	17th September 2013	oif2013.317.00: Working document for CEI VSR draft 11-1
OIF 2010.404.13	18th September 2013	Wrong file uploaded
OIF 2010.404.14	18th September 2013	oif2013.380.01: CEI-28G-VSR 14-0 comments
OIF 2010.404.15	30th October 2013	oif2014.068.00: CEI-VSR rev 0-15 comments

The OIF document 2013.066 was the working document used for the development of the CEI-28G-MR interface defined in clause 14. The history of this document is detailed in the table below:

Revision	Date	Description
OIF 2013.066.00	17th January 2013	oif2013.037.01: MR editor report Jan 2013
OIF 2013.066.01	21st May 2013	oif2013.162.02: MR 1-0 comment resolution spreadsheet
OIF 2013.066.02	25th July 2013	oif2013.254.03: CEI-28G-MR rev2-0 editors report
OIF 2013.066.03	17th September 2013	Final version

The combined revision including changes of above documents was published as OIF-CEI-03.01 in February 2014.

The OIF document oif2017.059 was the working document used for the development of maintenance updates to OIF-CEI-03.01 according worklist in oif2015.001.02. The comment resolution for this update is contained in oif2017.321. These updates were published as part of OIF-CEI-04.0 in December 2017.

The OIF document 2014.230 was the working document used for the development of the CEI-56G-VSR-PAM4 interface defined in clause 16. The history of this document is detailed in the table below:

Revision	Date	Description
OIF 2014.230.00	07/21/2014	Baseline Text Proposal
OIF 2014.230.01	10/22/2014	oif2014.372.00 CEI-56G-VSR-PAM4 Editor's report
OIF 2014.230.02	02/06/2015	oif2014.443.02 CEI-56G-VSR-PAM4 comments resolution spreadsheet
OIF 2014.230.03	05/08/2015	oif2015.144.02 CEI-56G-VSR-PAM4 comment and resolution spreadsheet
OIF 2014.230.04	09/09/2015	
OIF 2014.230.05	11/06/2015	oif2015.492.01CEI-56G-VSR/XSR-PAM4 comment and resolution spreadsheets
OIF 2014.230.06	02/22/2016	oif2016.004.04 CEI-56G-VSR/XSR-PAM4 comment and resolution spreadsheets
OIF 2014.230.07	06/10/2016	oif2016.128.05 Prague CEI-56G-VSR/XSR-PAM4 comment and resolution spreadsheets
OIF 2014.230.08	09/13/2016	oif2016.252.04 Quebec City CEI-56G-VSR-PAM4 comment and resolution spreadsheet
OIF 2014.230.09	11/18/2016	oif2016.402.03 Auckland CEI-56G-VSR-PAM4 comment and resolution spreadsheet
OIF 2014.230.10	02/17/2017	oif2017.027.01 San Jose CEI-56G-VSR-PAM4 comment and resolution spreadsheet
OIF 2014.230.11	06/06/2017	oif2017.148.02 Ljub. CEI-56G-VSR-PAM4 comment and resolution spreadsheet
OIF 2014.230.12	09/25/2017	oif2017.333.02 Halifax CEI-56G-VSR-PAM4 comment and resolution spreadsheet
OIF 2014.230.13	11/01/2017	Final version: oif2017.492.01 Shanghai CEI-56G-VSR-PAM4 comment and resolution spreadsheet

The OIF document 2014.245 was the working document used for the development of the CEI-56G-MR-PAM4 interface defined in clause 17. The history of this document is detailed in the table below:

Revision	Date	Description
OIF 2014.245.00	07/21/2014	Baseline Text Proposal
OIF 2014.245.01	10/22/2014	oif2014.247.00 Method and Highlights for Creating a CEI-56G-MR Baseline Proposal
OIF 2014.245.02	03/08/2015	oif2014.444.03 CEI-56G-MR comment and resolution spreadsheet
OIF 2014.245.03	05/13/2015	oif2015.198.02 Editor's initial responses to the comments received against CEI-56G-MR spec (OIF2014.245.02) ballot
OIF 2014.245.04	09/11/2015	oif2015.358.02 CEI-56G-MR-PAM4 comment resolution spreadsheet - OIF Q3/2015 Meeting
OIF 2014.245.05	12/13/2015	oif2015.504.02 Editor's initial responses to comments and resolutions against the CEI-56G-MR-PAM4 (i.e., oif2014.245.04.pdf) spec draft
OIF 2014.245.06	04/03/2016	oif2016.060.02 Editor's initial responses to comments and resolutions against the CEI-56G-MR-PAM4 (i.e., oif2014.245.05.pdf) spec draft
OIF 2014.245.07	06/28/2016	oif2016.194.03 Editor's initial responses to comments and resolutions
OIF 2014.245.08	09/27/2016	oif2016.331.02 Editor's Responses for Comment Resolution for CEI-56G-MR-PAM4 (oif2014.245.07)

Revision	Date	Description
OIF 2014.245.09	12/12/2016	oif2016.446.02 Editor's initial responses to CEI-56G-MR-PAM4 comments and resolutions
OIF 2014.245.10	04/09/2017	oif2017.082.02 Editor's responses to CEI-56G-MR-PAM4 comments and resolutions (Q1/2017)
OIF 2014.245.11	06/27/2017	oif2017.233.03 Editor's responses to CEI-56G-MR-PAM4 comments and resolutions (Q2/2017)
OIF 2014.245.12	08/25/2017	oif2017.419.02 Editor's responses to CEI-56G-MR-PAM4 comments and resolutions (Q3/2017)
OIF 2014.245.13	11/01/2017	Final version: oif2017.563.02 Worksheet with editor's comment&resolution pre-Q4/17 meeting for CEI-56G-MR-PAM4 (oif2014.245.12)

The OIF document 2014.267 was the working document used for the development of the CEI-56G-USR-NRZ interface defined in clause 18. The history of this document is detailed in the table below:

Revision	Date	Description
OIF 2014.267.00	07/25/2014	Baseline Text Proposal
OIF 2014.267.01	10/14/2014	oif2014.304.00 CEI 56G USR Editorial Comments on oif2014.267.00
OIF 2014.267.02	10/21/2014	oif2014.369.00 Editors report for 56G-USR
OIF 2014.267.03	01/22/2015	oif2015.002.03 CEI-56G-USR-NRZ comment and resolution spreadsheet
OIF 2014.267.04	04/22/2015	oif2015.103.02 CEI-56G-USR Version3 comment and resolution spreadsheet
OIF 2014.267.05	07/29/2015 D	oif2015.254.01 CEI-56G-USR Version4 comment and resolution spreadsheet
OIF 2014.267.06	11/05/2015	oif2015.472.02 CEI-56G-USR-NRZ Comment Resolution
OIF 2014.267.07	01/27/2016	oif2016.038.03 CEI-56G-USR-NRZ Comment Resolution
OIF 2014.267.08	05/10/2016	oif2016.121.02 CEI-56G-USR-NRZ Comment Resolution 07
OIF 2014.267.09	08/10/2016	oif2016.267.02 Comment resolution for CEI-56G-USR-NRZ 08
OIF 2014.267.10	10/31/2016	oif2016.363.03 Comment resolution for CEI-56G-USR-NRZ 09
OIF 2014.267.11	01/17/2017	Final Version: oif2016.485.01 Comment resolution for CEI-56G-USR-NRZ 10

The OIF document 2014.268 was the working document used for the development of the CEI-56G-XSR-NRZ interface defined in clause 19. The history of this document is detailed in the table below:

Revision	Date	Description
OIF 2014.268.00	07/25/2014	Baseline Text Proposal
OIF 2014.268.01	10/14/2014	oif2014.305.00 CEI 56G XSR Editorial Comments on oif2014.268.00
OIF 2014.268.02	10/21/2014	oif2014.370.00 Editors report for CEI-56G-XSR-NRZ
OIF 2014.268.03	01/22/2015	oif2015.003.04 CEI-56G-XSR-NRZ comment and resolution spreadsheet
OIF 2014.268.04	04/22/2015	oif2015.102.02 CEI-56G-XSR-NRZ Version3 comment and resolution spreadsheet
OIF 2014.268.05	07/29/2015	oif2015.255.01 CEI-56G-XSR-NRZ Version4 comment and resolution spreadsheet
OIF 2014.268.06	11/05/2015	oif2015.476.02 CEI-56G-XSR-NRZ Comment Resolution
OIF 2014.268.07	01/27/2016	oif2016.043.04 CEI-56G-XSR-NRZ Comment Resolution
OIF 2014.268.08	05/10/2016	oif2016.123.02 CEI-56G-XSR-NRZ Comment Resolution 07

Revision	Date	Description
OIF 2014.268.09	08/10/2016	oif2016.269.01 Comment resolution for CEI-56G-XSR-NRZ 08
OIF 2014.268.10	10/31/2016	oif2016.364.02 Comment resolution for CEI-56G-XSR-NRZ 09
OIF 2014.268.11	01/17/2017	Final Version: oif2016.486.01 Comment resolution for CEI-56G-XSR-NRZ 10

The OIF document 2014.380 was the working document used for the development of the CEI-56G-LR-PAM4 interface defined in clause 21. The history of this document is detailed in the table below:

Revision	Date	Description
OIF 2014.380.00	10/18/2014	Baseline Text Proposal
OIF 2014.380.01	04/18/2015	oif2014.381.03 Method and Highlights for Creating a PAM-4 Baseline Proposal for CEI-56G-LR
OIF 2014.380.02	04/03/2016	oif2015.505.01 Editor's initial responses to comments and resolutions against the CEI-56G-LR-PAM4 (i.e., oif2014.380.01.pdf) spec draft
OIF 2014.380.03	06/28/2016	oif2016.205.02 Editor's initial responses to CEI-56G-LR-PAM4 comments and resolutions
OIF 2014.380.04	09/28/2016	oif2016.334.03 Editor's Responses for Comment Resolution for CEI-56G-LR-PAM4 (oif2014.380.03)
OIF 2014.380.05	12/12/2016	oif2016.447.02 Editor's initial responses to CEI-56G-LR-PAM4 comments and resolutions (Q4/16)
OIF 2014.380.06	04/09/2017	oif2017.083.02 Editor's responses to CEI-56G-LR-PAM4 comments and resolutions (Q1/2017)
OIF 2014.380.07	06/27/2017	oif2017.234.02 Editor's responses to CEI-56G-LR-PAM4 comments and resolutions (Q2/2017)
OIF 2014.380.08	08/25/2017	oif2017.420.02 Editor's responses to CEI-56G-LR-PAM4 comments and resolutions (Q3/2017)
OIF 2014.380.09	11/01/2017	Final version: oif2017.564.02 Worksheet with editor's comment&resolution pre Q4/17 meeting for CEI-56G-LR-PAM4 (oif2014.380.08)

The OIF document 2014.364 was the working document used for the development of the CEI-56G-LR-ENRZ interface defined in clause 22. The history of this document is detailed in the table below:

Revision	Date	Description
OIF 2014.364.00	10/13/2014	Baseline Text Proposal
OIF 2014.364.01	01/14/2015	oif2015.046.00 CEI-56G-LR ENRZ Proposal Updates
OIF 2014.364.02	04/12/2015	oif2015.046.00 CEI-56G-LR ENRZ Proposal Updates
OIF 2014.364.03	07/30/2015	oif2015.341.00 CEI-56G-LR-ENRZ Proposed Updates to Baseline Text
OIF 2014.364.04	01/28/2016	oif2015.440.01 CEI-56G-LR-ENRZ Comment Resolution 4Q2015
OIF 2014.364.05	05/12/2016	Final version: oif2016.155.00 CEI-56G-LR-ENRZ Comment Resolution Spreadsheet 2Q2016

The OIF document oif2018.360 was the working document used for the development of maintenance updates to OIF-CEI-04.00 according worklists in oif2018.007.03 and oif2020.015.06. These updates were published as part of OIF-CEI-05.0 in February 2022.

The OIF document 2014.286.18 was the working document used for the development of the CEI-56G-XSR-PAM4 interface defined in clause 20. The history of this document is detailed in the table below:

Revision	Date	Description
OIF 2014.286.00	07/30/2014	Baseline Text Proposal
OIF 2014.286.01	07/30/2014	Baseline Text Proposal Update
OIF 2014.286.02	07/31/2014	Baseline Text Proposal Update
OIF 2014.286.3	07/31/2014	Baseline Text Proposal Update
OIF 2014.286.04	10/22/2014	oif2014.340.00 updates to CEI-56G-XSR-PAM4 baseline
OIF 2014.286.05	02/06/2015	oif2015.021.02 CEI-56G-XSR-PAM4 comments resolution spreadsheet
OIF 2014.286.06	06/01/2015	oif2015.143.01 CEI-56G-XSR-PAM4 comment and resolution spreadsheet
OIF 2014.286.07	09/09/2015	oif2015.387.01 Working copy of CEI-56G-XSR-PAM4 (post-Ottawa meeting)
OIF 2014.286.08	11/19/2015	oif2015.492.01 CEI-56G-XSR-PAM4 comment and resolution spreadsheet
OIF 2014.286.09	03/07/2016	oif2016.004.04 CEI-56G-XSR-PAM4 comment and resolution spreadsheet
OIF 2014.286.10	06/15/2016	oif2016.128.05 CEI-56G-XSR-PAM4 comment and resolution spreadsheet
OIF 2014.286.11	09/15/2016	oif2016.252.04 CEI-56G-XSR-PAM4 comment and resolution spreadsheet
OIF 2014.286.12	11/21/2016	oif2016.403.04 CEI-56G-XSR-PAM4 comment and resolution spreadsheet
OIF 2014.286.13	02/17/2017	oif2017.028.01 CEI-56G-XSR-PAM4 comment and resolution spreadsheet
OIF 2014.286.14	06/06/2017	oif2017.149.02 CEI-56G-XSR-PAM4 comment and resolution spreadsheet
OIF 2014.286.15	08/25/2017	oif2017.334.02 CEI-56G-XSR-PAM4 comment and resolution spreadsheet
OIF 2014.286.16	11/01/2017	oif2017.493.01 CEI-56G-XSR-PAM4 comment and resolution spreadsheet
OIF 2014.286.17	02/23/2018	oif2017.611.04 CEI-56G-XSR-PAM4 comment and resolution spreadsheet
OIF 2014.286.18	04/25/2018	Final version: oif2018.179.01 Nuremberg CEI-56G-XSR-PAM4 comment and resolution spreadsheet

The OIF document 2017.171.08 was the working document used for the development of the CEI-112G-MCM-CNRZ interface defined in clause 23. The history of this document is detailed in the table below:

Revision	Date	Description
OIF 2017.171.00	04/27/2017	Baseline Text Proposal
OIF 2017.171.01	05/09/2017	Baseline Text Proposal Update
OIF 2017.171.02	07/15/2017	Baseline Text Proposal Update
OIF 2017.171.03	11/01/2017	Baseline Text Proposal Update
OIF 2017.171.04	04/25/2018	oif2018.036.01 CEI-112G-MCM-CNRZ Comment Resolution 1Q2018
OIF 2017.171.05	10/15/2018	oif2018.285.00 CEI-112G-MCM-CNRZ Comment Resolution 3Q2018

Revision	Date	Description
OIF 2017.171.06	10/31/2018	oif2018.368.00 CEI-112G-MCM-CNRZ Proposed Updates to Baseline Text v4
OIF 2017.171.07	02/21/2019	oif2019.020.00 CEI-112G-MCM-CNRZ Comment Resolution 1Q2019
OIF 2017.171.08	07/31/2019	Final version: oif2019.209.00 CEI-112G-MCM-CNRZ Comment Resolution 3Q2019

The OIF document 2019.340.08 was the working document used for the development of the CEI-112G-MR-PAM4 interface defined in clause 26. The history of this document is detailed in the table below:

Revision	Date	Description
OIF 2019.340.00	10/21/2019	Baseline Text Proposal
OIF 2019.340.01	10/23/2019	Baseline Text Proposal Update
OIF 2019.340.02	06/21/2020	oif2020.185.02 Q2/20 Comment Resolution Worksheet CEI-112G-MR-PAM4
OIF 2019.340.03	09/17/2020	oif2020.302.02 Q3/20 Comment Resolution Worksheet CEI-112G-MR-PAM4
OIF 2019.340.04	01/06/2021	oif2020.445.02 Q4/20 Comment Resolution Worksheet CEI-112G-MR-PAM4
OIF 2019.340.05	02/25/2021	oif2021.095.02 Q1/21 Comment Resolution Worksheet CEI-112G-MR-PAM4
OIF 2019.340.06	05/14/2021	oif2021.279.02 Q2/21 Comment Resolution Worksheet CEI-112G-MR-PAM4
OIF 2019.340.07	08/06/2021	oif2021.463.02 Q3/21 Comment Resolution Worksheet CEI-112G-MR-PAM4
OIF 2019.340.08	11/05/2021	Final version: oif2021.635.02 Q4/21 Comment Resolution Worksheet CEI-112G-MR-PAM4

The OIF document 2018.212.15 was the working document used for the development of the CEI-112G-LR-PAM4 interface defined in clause 27. The history of this document is detailed in the table below:

Revision	Date	Description
OIF 2018.212.00	04/25/2018	Baseline Text Proposal
OIF 2018.212.01	04/30/2018	Baseline Text Proposal Update
OIF 2018.212.02	08/02/2018	Baseline Text Proposal Update
OIF 2018.212.03	10/31/2018	Baseline Text Proposal Update
OIF 2018.212.04	03/25/2019	oif2019.074.02 Q1/19 Comment Resolution Worksheet CEI-112G-LR-PAM4
OIF 2018.212.05	07/01/2019	oif2019.185.02 Q2/19 Comment Resolution Worksheet CEI-112G-LR-PAM4
OIF 2018.212.06	09/13/2019	oif2019.268.02 Q3/19 Comment Resolution Worksheet CEI-112G-LR-PAM4
OIF 2018.212.07	12/10/2019	oif2019.393.02 Q4/19 Comment Resolution Worksheet CEI-112G-LR-PAM4
OIF 2018.212.08	03/24/2020	oif2020.084.01 Q1/20 Comment Resolution Worksheet CEI-112G-LR-PAM4
OIF 2018.212.09	06/21/2020	oif2020.184.02 Q2/20 Comment Resolution Worksheet CEI-112G-LR-PAM4
OIF 2018.212.10	09/17/2020	oif2020.299.02 Q3/20 Comment Resolution Worksheet CEI-112G-LR-PAM4
OIF 2018.212.11	01/06/2021	oif2020.444.02 Q4/20 Comment Resolution Worksheet CEI-112G-LR-PAM4
OIF 2018.212.12	02/25/2021	oif2021.096.02 Q1/21 Comment Resolution Worksheet CEI-112G-LR-PAM4
OIF 2018.212.13	05/14/2021	oif2021.278.02 Q2/21 Comment Resolution Worksheet CEI-112G-LR-PAM4
OIF 2018.212.14	08/06/2021	oif2021.462.02 Q3/21 Comment Resolution Worksheet CEI-112G-LR-PAM4
OIF 2018.212.15	11/05/2021	Final version: oif2021.634.02 Q4/21 Comment Resolution Worksheet CEI-112G-LR-PAM4

The OIF document 2019.065.12 was the working document used for the development of the CEI-112G-XSR-PAM4 interface defined in clause 24. The history of this document is detailed in the table below:

Revision	Date	Description
OIF 2019.065.00	02/19/2019	Baseline Text Proposal
OIF 2019.065.01	05/11/2019	Baseline Text Proposal Update
OIF 2019.065.02	05/15/2019	Baseline Text Proposal Update
OIF 2019.065.03	12/16/2019	oif2019.389.02 Comment Resolution Worksheet CEI-112G-XSR-PAM4
OIF 2019.065.04	03/24/2020	oif2020.078.01 Comment Resolution Worksheet CEI-112G-XSR-PAM4
OIF 2019.065.05	06/21/2020	oif2020.182.03 Comment Resolution Worksheet CEI-112G-XSR-PAM4
OIF 2019.065.06	09/17/2020	oif2020.282.03 Comment Resolution Worksheet CEI-112G-XSR-PAM4
OIF 2019.065.07	01/06/2021	oif2020.440.03 Comment Resolution Worksheet CEI-112G-XSR-PAM4
OIF 2019.065.08	03/28/2021	oif2021.094.02 Comment Resolution Worksheet CEI-112G-XSR-PAM4
OIF 2019.065.09	06/07/2021	oif2021.280.03 Comment Resolution Worksheet CEI-112G-XSR-PAM4
OIF 2019.065.10	08/31/2021	oif2021.464.02 Comment Resolution Worksheet CEI-112G-XSR-PAM4
OIF 2019.065.11	11/05/2021	oif2021.636.02 Comment Resolution Worksheet CEI-112G-XSR-PAM4
OIF 2019.065.12	02/10/2022	Final version: oif2022.064.02 Comment Resolution Worksheet CEI-112G-XSR-PAM4

The OIF document 2017.346.23 was the working document used for the development of the CEI-112G-VSR-PAM4 interface defined in clause 25. The history of this document is detailed in the table below:

Revision	Date	Description
OIF 2017.346.00	08/01/2017	Baseline Text Proposal
OIF 2017.346.01	08/03/2017	Baseline Text Proposal Update
OIF 2017.346.02	08/03/2017	Baseline Text Proposal Update
OIF 2017.346.03	11/01/2017	Baseline Text Proposal Update
OIF 2017.346.04	03/16/2018	oif2018.060.02 Comment Resolution Worksheet CEI-112G-VSR-PAM4
OIF 2017.346.05	06/18/2018	oif2018.193.02 Comment Resolution Worksheet CEI-112G-VSR-PAM4
OIF 2017.346.06	10/11/2018	oif2018.319.05 Comment Resolution Worksheet CEI-112G-VSR-PAM4
OIF 2017.346.07	12/21/2018	oif2019.048.02 Comment Resolution Worksheet CEI-112G-VSR-PAM4
OIF 2017.346.08	04/15/2019	oif2019.177.01 Comment Resolution Worksheet CEI-112G-VSR-PAM4
OIF 2017.346.09	06/26/2019	oif2019.276.02 Comment Resolution Worksheet CEI-112G-VSR-PAM4
OIF 2017.346.10	09/16/2019	oif2019.384.01 Comment Resolution Worksheet CEI-112G-VSR-PAM4
OIF 2017.346.11	12/18/2019	oif2020.081.01 Comment Resolution Worksheet CEI-112G-VSR-PAM4
OIF 2017.346.12	03/25/2020	oif2020.181.02 Comment Resolution Worksheet CEI-112G-VSR-PAM4
OIF 2017.346.13	06/27/2020	oif2020.291.03 Comment Resolution Worksheet CEI-112G-VSR-PAM4
OIF 2017.346.14	09/21/2020	oif2020.438.01 Comment Resolution Worksheet CEI-112G-VSR-PAM4
OIF 2017.346.15	01/05/2021	oif2021.101.02 Comment Resolution Worksheet CEI-112G-VSR-PAM4
OIF 2017.346.16	04/01/2021	oif2021.277.02 Comment Resolution Worksheet CEI-112G-VSR-PAM4
OIF 2017.346.17	06/11/2021	oif2021.454.01 Comment Resolution Worksheet CEI-112G-VSR-PAM4
OIF 2017.346.18	08/13/2021	oif2021.567.03 Comment Resolution Worksheet CEI-112G-VSR-PAM4

Revision	Date	Description
OIF 2017.346.19	12/03/2021	oif2022.058.03 Comment Resolution Worksheet CEI-112G-VSR-PAM4
OIF 2017.346.20	03/24/2022	oif2022.171.02 Comment Resolution Worksheet CEI-112G-VSR-PAM4
OIF 2017.346.21	05/31/2022	oif2022.345.02 Comment Resolution Worksheet CEI-112G-VSR-PAM4
OIF 2017.346.22	08/03/2022	oif2022.429.02 Comment Resolution Worksheet CEI-112G-VSR-PAM4
OIF 2017.346.23	11/01/2022	Final version CEI-112G-VSR-PAM4

The OIF document 2021.603 was the working document used for the development of the CEI-112G-XSR+-PAM4 interface defined in clause 28. The history of this document is detailed in the table below:

Revision	Date	Description
OIF 2021.603.00	10/31/2021	Baseline Text Proposal
OIF 2021.603.01	11/02/2021	Modifications of baseline text proposal
OIF 2021.603.02	01/11/2022	Modifications of baseline text proposal
OIF 2021.603.03	01/31/2022	Modifications of baseline text proposal
OIF 2021.603.04	05/02/2022	Modifications of baseline text proposal
OIF 2021.603.05	07/26/2022	Modifications of baseline text proposal
OIF 2021.603.06	09/29/2022	oif2022.581.03 Straw ballot comments for CEI-112G-XSR+-PAM4 (2021.603.06)
OIF 2021.603.07	01/18/2023	oif2023.110.03 Straw ballot comments for CEI-112G-XSR+-PAM4 (2021.603.07)
OIF 2021.603.08	05/25/2023	oif2023.110.03 Straw ballot comments for CEI-112G-XSR+-PAM4 (2021.603.07)
OIF 2021.603.09	08/22/2023	Final version: oif2023.289.02 Straw ballot comments for CEI-112G-XSR+-PAM4 (2021.603.08)

The OIF document 2021.405 was the working document used for the development of the CEI-112G-Linear-PAM4 interface defined in clause 29. The history of this document is detailed in the table below:

Revision	Date	Description
OIF 2021.405.00	08/02/2021	Baseline Text Proposal
OIF 2021.405.01	11/02/2021	Baseline Text Proposal Update
OIF 2021.405.02	05/06/2021	Baseline Text Proposal Update
OIF 2021.405.03	11/01/2022	Baseline Text Proposal Update
OIF 2021.405.04	11/01/2022	Baseline Text Proposal Update
OIF 2021.405.05	06/27/2023	oif2023.018.03 Comment Resolution Worksheet CEI-112G-LINEAR-PAM4
OIF 2021.405.06	09/07/2023	oif2023.393.01 Comment Resolution Worksheet CEI-112G-LINEAR-PAM4
OIF 2021.405.07	11/20/2023	oif2023.544.01 Comment Resolution Worksheet CEI-112G-LINEAR-PAM4
OIF 2021.405.08	02/21/2024	oif2024.003.04 Comment Resolution Worksheet CEI-112G-LINEAR-PAM4
OIF 2021.405.09	06/05/2024	oif2024.234.03 Comment Resolution Worksheet CEI-112G-LINEAR-PAM4
OIF 2021.405.10	09/11/2024	oif2024.438.00 Comment Resolution Worksheet CEI-112G-LINEAR-PAM4
OIF 2021.405.11	12/02/2024	oif2024.571.02 Comment Resolution Worksheet CEI-112G-LINEAR-PAM4

Revision	Date	Description
OIF 2021.405.12	02/27/2025	oif2025.088.01 Comment Resolution Worksheet CEI-112G-LINEAR-PAM4
OIF 2021.405.13	05/22/2025	oif2025.191.02 Comment Resolution Worksheet CEI-112G-LINEAR-PAM4
OIF 2021.405.14	06/20/2025	Final version: oif2025.285.00 Comment Resolution Worksheet CEI-112G-LINEAR-PAM4

0.2 Document Structure

The CEI document is created as a clause based document to allow for a successive completion of the document as clauses are added. This reflects the split project schedule where there are different schedules for completion different application specifications.

The first release of the document included all clauses common for the applications covered by the CEI project. These clauses were completed to cover the requirements of the included applications. Further common specifications may be included as new application clauses are added, resulting in an update of the common clauses. The process of creating the CEI document can be explained as follows:

1. Prepare and complete all clauses necessary for the first release of the document, make it the master for future documents and submit it for its approval process (balloting cycles).
2. Follow on documents include new clauses for new functions and corrections and additions to all affected clauses of the Master document. Unchanged clauses from prior documents are not included, only deltas are listed (additions and deletions).
3. Once the Master document and following documents are approved it is an editorial task to merge the documents.
4. All requirements and specifications in the application specific clauses shall be referenced to the common clauses when appropriate.
5. Annexes and Appendices providing explanatory and informative text for a specific application shall be included in the corresponding clause and covered by the clause revision history. Information included in Annexes is normative with respect to the particular clause. Information included in Appendices is informative only with respect to the particular clause.

0.3 List of companies belonging to the OIF when the document is approved

1Finity	Accelight Technologies, Inc.
Accton Technology Corporation	Adtran Networks SE
Advanced Fiber Resources (AFR)	Advanced Micro Devices, Inc.
AIO Core	Alibaba
Alphawave Semi	Amphenol Corp.
Anritsu	Applied Optoelectronics, Inc.
Arista Networks	Astera Labs
Ayar Labs	BizLink Technology, Inc.
Broadcom Inc.	Cadence Design Systems
Casela Technologies USA	Celero Communications Inc.
Celestica	China Information Comm. Tech. Group
China Telecom	Ciena Corporation
CIG Photonics Japan Limited	Cisco Systems
Coherent	Cornelis Networks
Corning	Credo Semiconductor
Dai Nippon Printing	Dell
Dexerials Corporation	DustPhotonics
EFFECT Photonics	Eoptolink Technology
Epson Electronics America	Ericsson
EXFO	Femtum Inc.
Formerica Optoelectronics	Foxconn Interconnect Technology
Fujikura	Furukawa Electric
GlobalFoundries	Google
H3C Technologies	Hakusan Inc
Hewlett Packard Enterprise (HPE)	HGGenuine Optics Tech Company
Huawei Technologies	InfiniLink US
Intel	Juniper Networks
Kandou Bus	KDDI Research
Keysight Technologies	Kuaishou Technology
KYOCERA Corporation	Lessengers Inc.
Ligent, Inc.	Lightelligence
Lightmatter	Linktel Technologies
Lumentum	Lumilens
Lumiphase AG	LUXIC Technology
Luxshare Technologies	MACOM Technology Solutions
Marvell Semiconductor, Inc.	MaxLinear Inc.
MediaTek	Meta Platforms
Microchip Storage	Microsoft Corporation

Mitsubishi Electric	Molex
Multilane Inc.	NEC Corporation
Nokia	NTT Corporation
Nubis Communications	NVIDIA
O-Net Technologies	Omattrix Ltd Co
Optomind Inc.	Orange
PETRA	Point2 Technology
Precision Optical Technologies	Quantifi Photonics
Quintessent Inc.	Ranovus
Renesas Electronics	Retym
Rosenberger Hochfrequenztechnik	Ruijie Networks
Samtec Inc.	SCINTIL Photonics
Semtech Canada Corporation	Senko Advanced Components
SeriaLink Systems	Socionext
Source Photonics	Sumitomo Electric Industries, Ltd.
Sumitomo Osaka Cement	Suzhou TFC Optical Communication Co (TFC)
Synopsys, Inc.	TE Connectivity
Tektronix	Telefonica S.A.
TELUS Communications, Inc.	TeraHop
Texas Instruments	US Conec
Viavi Solutions	Wilder Technologies
Wistron Corporation	Xphor Ltd.
Yamaichi Electronics Ltd.	ZTE Corporation

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1 Common electrical I/O project - Introduction, definitions and formats.

1.1 Introduction

The development of a Next Generation Common Electrical I/O Project was proposed in the OIF 2002.571.01 and approved in the Orlando Plenary meeting November 14, 2002. The purpose of the project is outlined in the problem statement:

A faster electrical interface is required to provide higher density and/or lower cost interfaces for payloads of 10Gbps and higher, including SERDES to Framer Interface (SFI), System Packet Interface (SPI), TDM-Fabric to framer Interface (TFI).

1.2 Overview

This Common Electrical IO Implementation Agreement includes:

- Electrical and jitter methodologies for new high speed interfaces and including the following older OIF interfaces: SxI-5, SFI-4.2, SFI-5.1, SPI-5.1 and TFI-5.
- A CEI-6G-SR specification for:
  Data lane(s) that support bit rates from 4.976 to 6.375Gsym/s over PCB.
  Physical reach from 0 to 200mm and up to 1 connector.
- A CEI-6G-LR specification for
  Data lane(s) that support bit rates from 4.976 to 6.375Gsym/s over PCB.
  Physical reach from 0 to 1m and up to 2 connectors.
- A CEI-11G-SR specification for:
  Data lane(s) that support bit rates from 9.95 to 11.2Gsym/s over PCB.
- A CEI-11G-LR specification for:
  Data lane(s) that support bit rates from 9.95 to 11.2Gsym/s over PCB.
  Physical reach from 0 to 1m with up to two connectors
- A CEI-11G-MR specification for:
  Data lane(s) that support bit rates from 9.95 to 11.2Gsym/s over PCB.
  Physical reach from 0 to 600mm with up to two connectors
- A CEI-28G-SR specification for:
  Data lane(s) that support bit rates from 19.90 to 28.05Gsym/s over PCB.
  Physical reach from 0 to 300mm with up to one connector
- A CEI-25G-LR specification for:
  Data lane(s) that support bit rates from 19.90 to 25.80Gsym/s over PCB.
  Physical reach from 0 to 686mm with up to two connectors

- A CEI-28G-VSR specification for:
  Data lane(s) that support bit rates from 19.60 to 28.10Gsym/s over PCB.
  Physical reach from a minimum of ***100 mm*** of host PCB trace plus one connector and a minimum of **50 mm** of module PCB trace
- A CEI-28G-MR specification for:
  Data lane(s) that support bit rates from 19.90 to 28.10Gsym/s over PCB.
  Physical reach from 0 to 500 mm with up to one connector
- A CEI-56G-VSR-PAM4 specification for:
  Data lane(s) that support bit rates from 18.0 to 29.0 Gsym/s over PCB.
  Physical reach from a minimum of **125 mm** of host PCB trace plus one connector and a minimum of **25 mm** of module PCB trace
- A CEI-56G-MR-PAM4 specification for:
  Data lane(s) that support bit rates from 18.0 to 29.0 Gsym/s over PCB.
  Physical reach from 0 to 500 mm with up to one connector
- A CEI-56G-USR-NRZ specification for:
  Data lane(s) that support bit rates from 19.6 to 58.0 Gsym/s inside a package.
  Physical reach from 0 to 10 mm on package substrate
- A CEI-56G-XSR-NRZ specification for:
  Data lane(s) that support bit rates from 39.8 to 58.0 Gsym/s over PCB.
  Physical reach from 0 to 50 mm of PCB trace
- A CEI-56G-XSR-PAM4 specification for:
  Data lane(s) that support bit rates from 18.0 to 29.0 Gsym/s over PCB.
  Physical reach from 0 to 50 mm of PCB trace
- A CEI-56G-LR-PAM4 specification for:
  Data lane(s) that support bit rates from 18.0 to 29.0 Gsym/s over PCB.
  Physical reach from 0 to 1000 mm of PCB and up to 2 connectors
- A CEI-56G-LR-ENRZ specification for:
  Data lane(s) that support bit rates from 99.5 Gbit/s and 112.4 Gbit/s across four wires over PCB.Corresponding baud rates are within the range of 33.16 Gsym/s and 37.50 Gsym/s.
  Physical reach from 0 to 1000 mm of PCB and up to 2 connectors
- A CEI-112G-MCM-CNRZ specification for:
  Data lane(s) that support data rates within the range of 99.5 Gbit/s and 112.4 Gbit/s across six wires. Corresponding baud rates are within the range of 47.5 Gsym/s to 69.6 Gsym/s.
  Physical reach from 0 to 25 mm of package substrate

- A CEI-112G-XSR-PAM4 specification for:
  Data lane(s) that support bit rates from 36.0 to 58.0 Gsym/s inside a package.
  Physical reach from 0 to 50 mm of package substrate
- A CEI-112G-VSR-PAM4 specification for:
  Data lane(s) that support bit rates from 36.0 to 58.0 Gsym/s over PCB.
  Physical reach from a minimum of 200 mm of host PCB trace plus one connector and a minimum of 20 mm of module PCB trace
- A CEI-112G-MR-PAM4 specification for:
  Data lane(s) that support bit rates from 36.0 to 58.0 Gsym/s over PCB.
  Physical reach from 0 to 500 mm with up to one connector
- A CEI-112G-LR-PAM4 specification for:
  Data lane(s) that support bit rates from 36.0 to 58.0 Gsym/s over PCB.
  Physical reach from 0 to 1000 mm of PCB and up to 2 connectors
- A CEI-112G-XSR+-PAM4 specification for:
  Data lane(s) that support bit rates from 36.0 to 58.0 Gsym/s for die-to-die (D2D) and die-to-optical-engine (D2OE) interconnect with bump-to-bump insertion loss up to 13 dB at the Nyquist frequency. Target platforms include multiple-chip module (MCM), co-packaged optics (CPO), and near-package optics (NPO) assemblies.

The Implementation Agreement defines applicable data characteristics (e.g. DC balance, transition density, maximum run length), channel models and compliance points/parameters supporting the physical reach and conditions. The Implementation Agreement specifically excludes any pinout, management interface, power-supply specification, connector or higher-level activity such as addressing or error control. It does not endorse or specify any particular data protocol.

1.3 Objectives and Requirements

The objectives and requirements for the CEI are given by the project definition as follows:

The data path shall:

- allow single and multi-lane applications
- support AC coupling
- support Hot Plug
- achieve Bit Error Ratio of lower than 10^{-15} per lane but the test requirement will be to verify 10^{-12} per lane.

The CEI Electrical Implementation Agreement and the CEI Protocol Implementation Agreement are peer documents. Adherence to one does not force adherence to the other. For example, a 10G SONET framer may connect directly to an optical module using CEI electricals with SONET scrambled data. In this case, CEI Protocol would be absent. It is also possible to use CEI Protocol without CEI Electricals. An example would be to encapsulate TFI-5 frames with CEI Protocol to provide forward error correction capability.

1.4 References

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1.5 Abbreviations

Table 1-1. Abbreviations

Abbreviation	Meaning
BER	Bit Error Ratio
BERT	Bit Error Ratio Test or Tester
BUJ	Bounded Uncorrelated Jitter
CBGJ	Correlated Bounded Gaussian Jitter
CBHPJ	Correlated Bounded High Probability Jitter
CEI	Common Electrical I/O
CDF	Cumulative Distribution Function
CDR	Clock Data Recovery
CID	Consecutive Identical Digits
CML	Current Mode Logic
Cn	Cursor number
DCD	Duty Cycle Distortion
dB	Decibel
DDJ	Data Dependent Jitter
DFE	Decision Feedback Equalizer
DJ	Deterministic Jitter
DUT	Device Under Test
EMI	Electro-Magnetic Interference
erf	error function
erfinv	inverse error function
ESD	Electro-Static Discharge
FEXT	Far End Cross Talk
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
Gbps	Giga bits per second
GJ	Gaussian Jitter
Gsym/s	Giga symbols per second
HF	High Frequency
HPF	High Pass Filter
HPJ	High Probability Jitter
IA	Implementation Agreement
ISI	Inter-Symbol Interference

Table 1-1. Abbreviations

Abbreviation	Meaning
LMS	Least Mean Square
LPF	Low Pass Filter
LVDS [20]	Low Voltage Differential Signal
LR	Long Reach
mA	milli-Amp
mV	milli-Volt
NEXT	Near End Cross Talk
NRZ	Non Return to Zero
PCB	Printed Circuit Board
PDF	Probability Distribution Function
PECL	Positive Emitter Coupled Logic
PJ	Periodic Jitter
pp	Peak to Peak
ppd	Peak to Peak Differential (as in 300mVppd)
PLL	Phase Locked Loop
ps	pico second
PRBS	Pseudo Random Bit Stream
Q	Inverse error function
RJ	Random Jitter
RV	Random Variable
RX	Receiver
S11 and S22	reflection coefficient
S21	transmission coefficient
SCC11 and SCC22	Common mode reflection coefficients
SCD11 and SCD22	Differential to common mode conversion coefficient
SDD11 and SDD22	Differential reflection coefficients
SDC11 and SDC22	Common mode to differential conversion coefficient
SFI	SERDES - Framer Interface
SJ	Sinusoidal Jitter
SPI	System Packet Interface
SR	Short Reach
sym/s	symbols/second
TJ	Total Jitter
TDM	Time Division Multiplexed data
TFI	TDM Fabric to Framer Interface

Table 1-1. Abbreviations

Abbreviation	Meaning
TX	Transmitter
UBHPJ	Uncorrelated Bounded High Probability Jitter
UI	Unit Interval = 1/(baud rate)
UUGJ	Uncorrelated Unbounded Gaussian Jitter
XAUI	10 Gigabit Attachment Unit Interface

1.6 Definitions

Table 1-2. General Definitions (with exception of Jitter and Wander) (Sheet 1 of 2)

Parameter	Description
Bit Error Ratio	A parameter that reflects the quality of the serial transmission and detection scheme. The Bit Error Ratio is calculated by counting the number of erroneous bits output by a receiver and dividing by the total number of transmitted bits over a specified transmission period.
Baud rate	Number of symbols per second, where a symbol can consist of more than one bit.
Channel	In this specification Channel shall mean electrical differential channel. The channel is combination of electrical interconnects that together form the signal path from reference points T to R - see Figure 1-6. The channel will typically consist of PCB traces, via holes, component attachment pads and connectors. A characteristic of a signal channel is the complex characteristic impedance Z.
Common Mode Voltage	Average of the Vhigh and Vlow voltage levels - see Figure 1-1
Confidence level	The use of this definition shall be understood as being with reference to a Gaussian Distribution
Differential Termination Resistance mismatch	The difference in the DC termination resistance with respect to ground of any two signals forming a differential pair. Usually due to large process spread the absolute termination resistance is specified relatively loose, e.g. 20% where the relative difference of resistors of the same device will be much less, e.g 5%. This parameter is used to specify the relative difference tighter than the overall resistance for the purpose of minimizing differential signal mode conversion
Gaussian	A statistical distribution (also termed “normal”) characterized by populations that are not bound in value and have well defined “tails”. The term “random” in this document always refers to a Gaussian distribution.
Golden PLL	Refers to a defined clock extraction unit which phase tracks the inherent clock present in a data signal. The phase tracking bandwidth is usually defined in terms of a corner frequency and if not defined with a corner frequency of baud/1667, a roll off of 20dB/dec and <0.1dB peaking

Table 1-2. General Definitions (with exception of Jitter and Wander) (Sheet 2 of 2)

Parameter	Description
Stress Channel	An otherwise compliant channel that has been selected or altered to test receiver or transmitter compliance (see also *Stressed Signal (or) Stressed Eye*.)
Intersymbol Interference	Data dependent deterministic jitter caused by the time differences required for the signal to arrive at the receiver threshold when starting from different places in bit sequences (symbols). For example when using media that attenuates the peak amplitude of the bit sequence consisting of alternating 0, 1, 0, 1... more than peak amplitude of the bit sequence consisting of 0, 0, 0, 0, 1, 1, 1, 1... the time required to reach the receiver threshold with the 0, 1, 0, 1... is less than required from the 0, 0, 0, 0, 1, 1, 1, 1... The run length of 4 produces a higher amplitude which takes more time to overcome when changing bit values and therefore produces a time difference compared to the run length of 1 bit sequence. When different run lengths are mixed in the same transmission the different bit sequences (symbols) therefore interfere with each other. Intersymbol Interference is expected whenever any bit sequence has frequency components that are propagated at different rates by the transmission media.
Lane	A single CEI Channel
Link	A functional connection between the Tx and Rx ports of 2 components, that can be multiple or parallel CEI Lanes defined as 1:N. The definition a Link does not imply duplex operation.
non-transparent applications	Defines an application where the high frequency transmit jitter of a device is defined independently to the high frequency jitter present at any data input of the same device
Skew	The constant portion of the difference in the arrival time between the data of any two in-band signals.
Stressed Signal (or) Stressed Eye	In order to test the tolerance of a receiver a stressed signal or eye is defined which when applied to the receiver must be received with the defined Bit Error Rate. The stressed signal or eye is defined in terms of its horizontal closure or jitter and amplitude normally in conjunction with an eye-mask.
Transparent applications	Defines an application where the high frequency transmit jitter of a device is dependent on the high frequency jitter present at one or more of the data inputs of the same device
Symbol	Unit of information conveyed by a single state transition in the medium
Symbol spaced	Describes a time difference equal to the nominal period of the data signal
Unit Interval	One nominal bit period for a given signaling speed. It is equivalent to the shortest nominal time between signal transitions. UI is the reciprocal of Symbol.

Table 1-3. Jitter and Wander Definitions (Sheet 1 of 3)

Parameter		Description
Jitter		Jitter is deviation from the ideal timing of an event at the mean amplitude of the signal population. Low frequency deviations are tracked by the clock recovery circuit, and do not directly affect the timing allocations within a bit interval. Jitter that is not tracked by the clock recovery circuit directly affects the timing allocations in a bit interval. Jitter is phase variations in a signal (clock or data) after filtering the phase with a single pole high pass filter with the -3 dB point at the jitter corner frequency.
	Total Jitter	Convolution of all jitter components.
	Jitter Generation	Jitter generation is the process whereby jitter appears at the output port in the absence of applied input jitter at the input port.
	Jitter Transfer	The ratio of the jitter output and jitter input for a component, device, or system often expressed in dB. A negative dB jitter transfer indicates the element removed jitter. A positive dB jitter transfer indicates the element added jitter. A zero dB jitter transfer indicates the element had no effect on jitter. The ratio should be applied separately to deterministic components and Gaussian (random) jitter components.
Previous Terminology		To enable enhancements in jitter methodology, more descriptive terminology has been adopted. To enable the reader to understand the mapping of previous descriptions the following terms are included for clarity.
	Data Dependent Jitter	Now referred to as Correlated Bounded High Probability Jitter
	Deterministic Jitter	Now referred to as High Probability Jitter
	Random Jitter	Now referred to as Gaussian Jitter
	Duty Cycle Distortion	The term Duty Cycle Distortion was formerly used for both Duty Cycle Distortion and Even-Odd Jitter.
Gaussian Jitter		An overall term that defines a jitter distribution that at the BER of interest e.g. 1e-15 still shows a Gaussian distribution. Unless otherwise specified Gaussian Jitter is the RMS sum of CBGJ and UUGJ.
	Jitter, Unbounded Gaussian	Jitter distribution that shows a true Gaussian distribution where the observed peak to peak value has an expected value that grows as a function of the measurement time. This form of jitter is assumed to arise from phase noise random processes typically found in VCO structures or clock sources. It is usually quantified as either the Root Mean Square (RMS) or Sigma of the Gaussian distribution, or as the expected peak value for a given measurement population. (Formally defined as T_RJ)
	Correlated Bounded Gaussian Jitter	Jitter distribution where the value of the jitter shows a correlation to the signal level being transmitted. The distribution is quantified, using a Gaussian approximation, as the gradient of the bathtub linearization at the Bit Error Rate of interest. R_RJ = R_GJ

Table 1-3. Jitter and Wander Definitions (Sheet 2 of 3)

Parameter		Description
High probability Jitter		Jitter distribution that at the BER of interest is approximated by a dual Dirac. Unless otherwise specified High Probability Jitter is the convolution of UBHPJ, CBHPJ, PJ, SJ, DCD. The distribution is quantified, using a dual Dirac approximation, as the offset of the bathtub linearization at the Bit Error Rate of interest.
	Uncorrelated Bounded High Probability Jitter.	Jitter distribution where the value of the jitter show no correlation to any signal level being transmitted. Formally defined as T_DJ.
	Correlated Bounded High Probability Jitter	Jitter distribution where the value of the jitter shows a strong correlation to the signal level being transmitted. This jitter may considered as being equalisable due to its correlation to the signal level.
	Periodic Jitter	A sub form of HPJ that defines a jitter which has a single fundamental harmonic plus possible multiple even and odd harmonics.
	Sinusoidal Jitter	A sub form of HPJ that defines a jitter which has a single frequency harmonic.
	Even-Odd Jitter	Even-Odd Jitter is measured on two repetitions of a repeating pattern with an odd number of bits such as PRBS9. The deviation of the time of each transition from an ideal clock at the signaling rate is measured. Even-Odd Jitter is defined as the magnitude of the difference between the average deviation of all even-numbered transitions and the average deviation of all odd-numbered transitions but only actual transitions are measured and averaged. Even-Odd Jitter is part of the UBHPJ distribution and is measured at the time-averaged signal level.
	Duty Cycle Distortion	The absolute value of the difference in the average width of a ’1’ symbol or a ’0’ symbol and the ideal periodic time in a clock-like repeating 0,1,0,1 sequence. Duty Cycle Distortion is part of the CBHPJ distribution and is measured at the time-averaged signal level.
Wander		The peak to peak variation in the phase of a signal (clock or data) after filtering the phase with a single pole low pass filter with the -3db point at the wander corner frequency. Wander does not include skew.
	Correlated wander	Components of wander that are common across all applicable in band signals.
	Relative wander	Components of wander that are uncorrelated between any two in band signals (See Figure 1-2)
	Total wander	The convolution of the correlated and uncorrelated wander. (See Figure 1-3)
	Uncorrelated wander	Components of wander that are not correlated across all applicable in band signals.

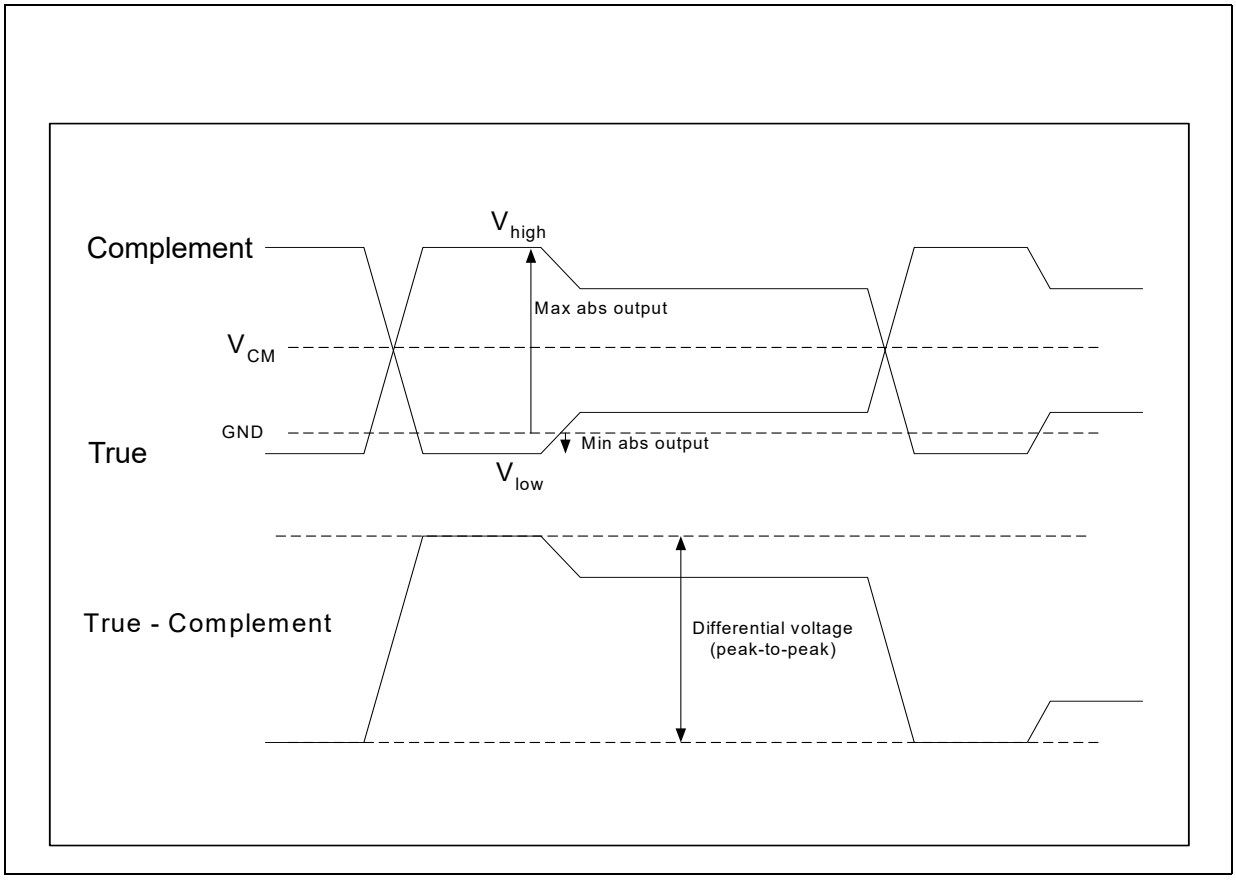
Table 1-3. Jitter and Wander Definitions (Sheet 3 of 3)

Parameter		Description
Unit		
	Peak-to-Peak Jitter	For any type of jitter, Peak to Peak Jitter is the full range of the jitter distribution that contributes within the specified BER.
	Jitter RMS	The root mean square value or standard deviation of jitter. See clause 2 for more information.
	Sigma	Refers to the standard deviation of a random variable modelled as a Gaussian Distribution. When used in reference to jitter, it refers to the standard deviation of the Gaussian Jitter component(s). When used in reference to confidence levels of a result refers to the probability that the result is correct given a Gaussian Mode, e.g. a measured result with 3 sigma confidence level would imply that 99.9% of the measurements are correct.

1.6.1 Definition of Amplitude and Swing

See Figure 1-1 for an illustration of absolute driver output voltage limits and definition of differential peak-to-peak amplitude.

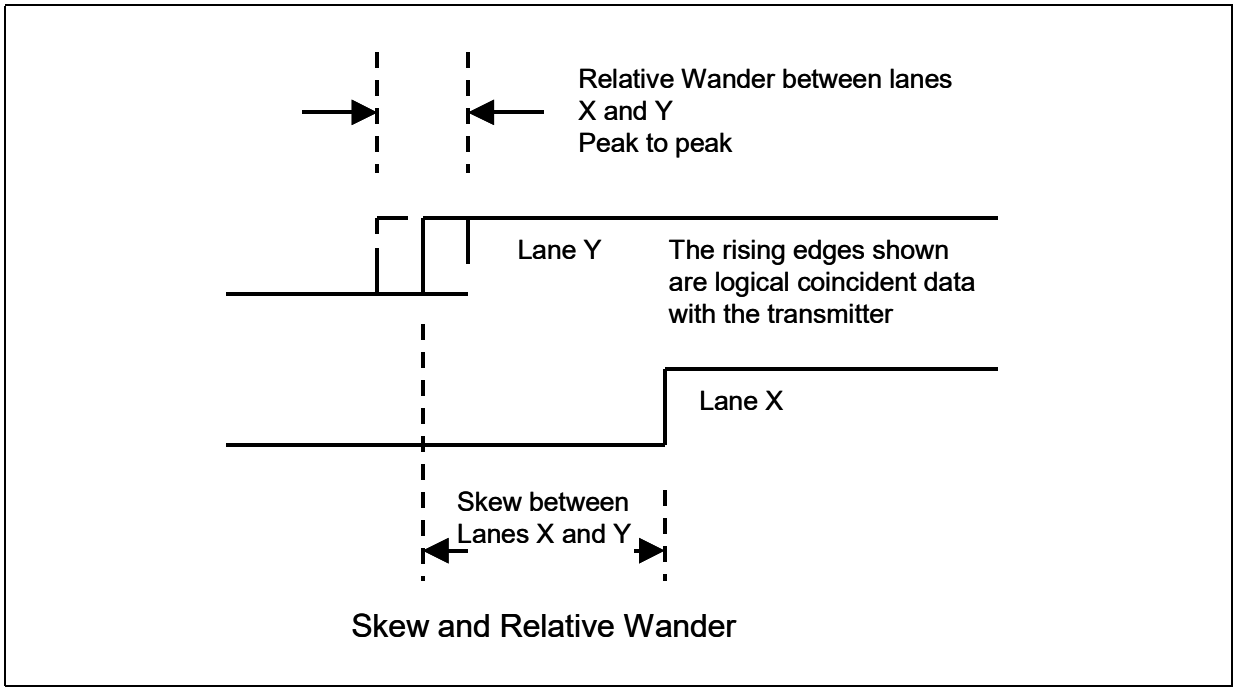
Figure 1-1. Definition of Driver Amplitude and Swing



1.6.2 Definition of Skew and Relative wander

See Figure 1-2 for an illustration of skew and relative wander.

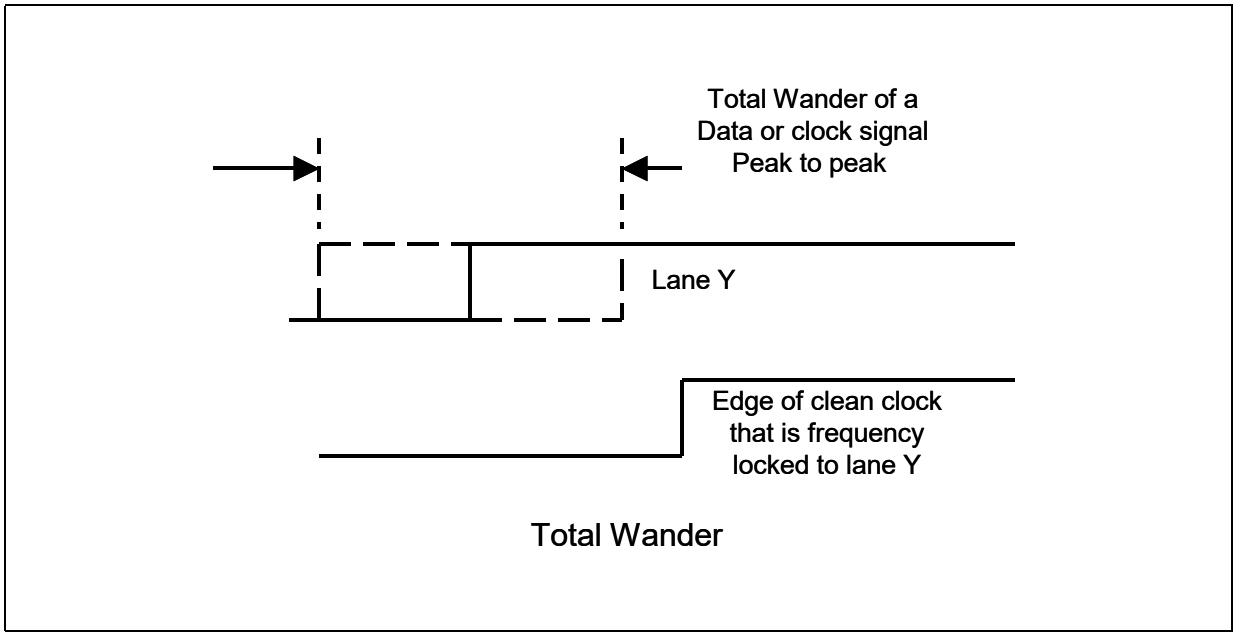
Figure 1-2. Skew and Relative Wander between in band Signals



1.6.3 Definition of Total wander

See Figure 1-3 for an illustration of total wander in a signal

Figure 1-3. Total Wander of a Signal



1.7 Table Entries and Specifications

The CEI IA shall use a common tabular definition of the parameters specified. The following section outlines examples of tables required for the definitions and the corresponding entries. All clauses must use this structure. Additional clause specific parameters are allowed.

1.7.1 Transmitter Electrical Output Specification

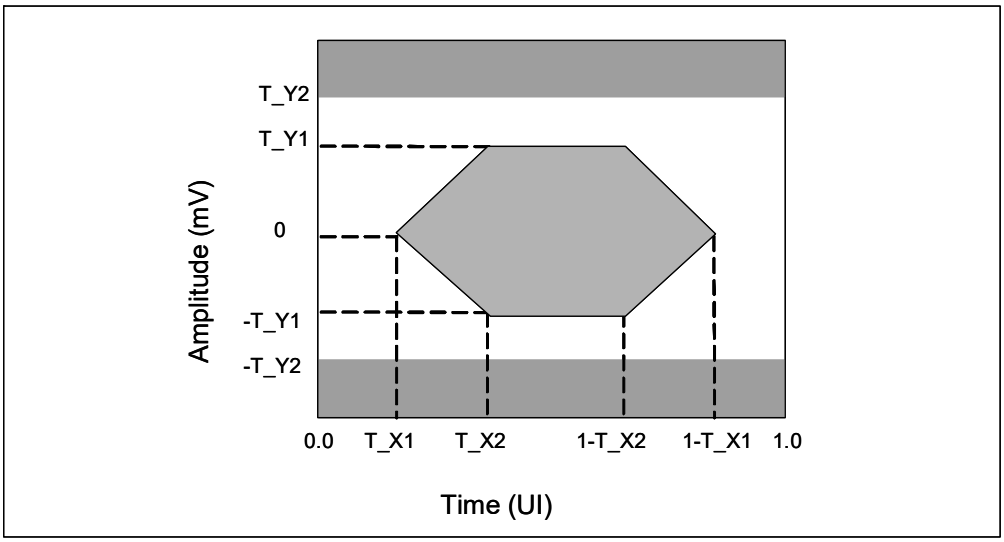
Table 1-4. Transmitter Electrical Output Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	T_Baud					Gsym/s
Output Differential Voltage	T_Vdiff					mVppd
DC Common mode Voltage	T_Vcm					mV
Output AC Common Mode Voltage	T_VcmAC					mVrms
Differential Resistance	T_Rd					Ω
Differential Termination Resistance Mismatch	T_Rdm					%
Output Rise and Fall Time (20% to 80%)	T_tr, T_tf					ps
Differential Output Return Loss	T_SDD22					dB
Common Mode Output Return Loss	T_SCC22					dB
NOTES:						

Table 1-5. Transmitter Output Jitter Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Uncorrelated Bounded High probability Jitter	T_UBHPJ					UIpp
Uncorrelated Unbounded Gaussian Jitter	T_UUGJ					UIpp
Duty cycle distortion	T_DCD					UIpp
Total Jitter	T_TJ					UIpp
Eye Mask	T_X1					UI
Eye Mask	T_X2					UI
Eye Mask	T_Y1					mV
Eye Mask	T_Y2					mV
NOTES: 1. Uncorrelated Unbounded Gaussian Jitter must be defined with respect to specified BER of 1e-15, Q=7.94						

Figure 1-4. Transmit Eye Mask



1.7.2 Receiver Electrical Input Specification

Table 1-6. Receiver Electrical Input Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	R_Baud					Gsym/s
Input Differential Voltage	R_Vdiff					mVppd
DC Common mode voltage	R_Vrcm					mV
AC Common mode Voltage	R_VcmAC					mV
Differential Input Resistance	R_Rdin					Ω
Input Resistance Mismatch	R_Rm					%
Differential Input Return Loss	R_SDD11					dB
Common Mode Input Return Loss	R_SCC11					dB
Differential to Common Mode Input Conversion2	R_SCD11					dB
NOTES:						

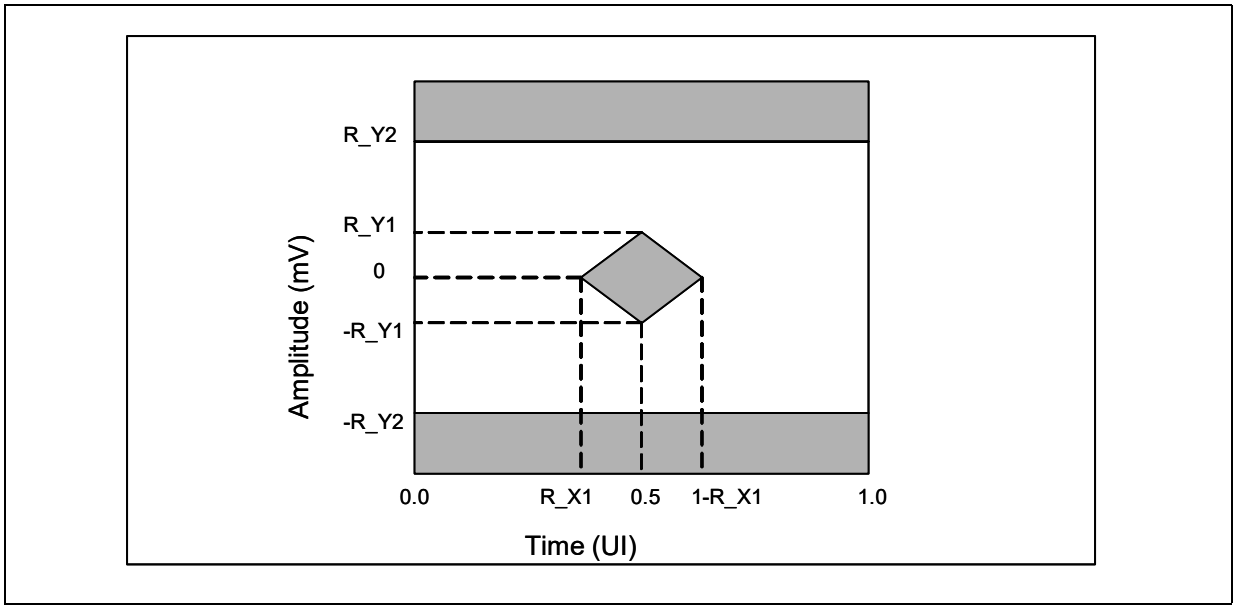
1.7.3 Receiver input Jitter Specification

Table 1-7. Receiver Input Jitter Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Uncorrelated Bounded High probability Jitter	R_UBHPJ					UIpp
Correlated Bounded High probability Jitter	R_CBHPJ					UIpp
Gaussian Jitter	R_GJ					UIpp
Sinusoidal Jitter	R_SJ					UIpp
Total Jitter	R_TJ					UIpp
Eye Mask	R_X1					UI
Eye Mask	R_Y1					mV
Eye Mask	R_Y2					mV

NOTES:
1. Gaussian Jitter must be defined with respect to specified BER of 1e-15, Q=7.94

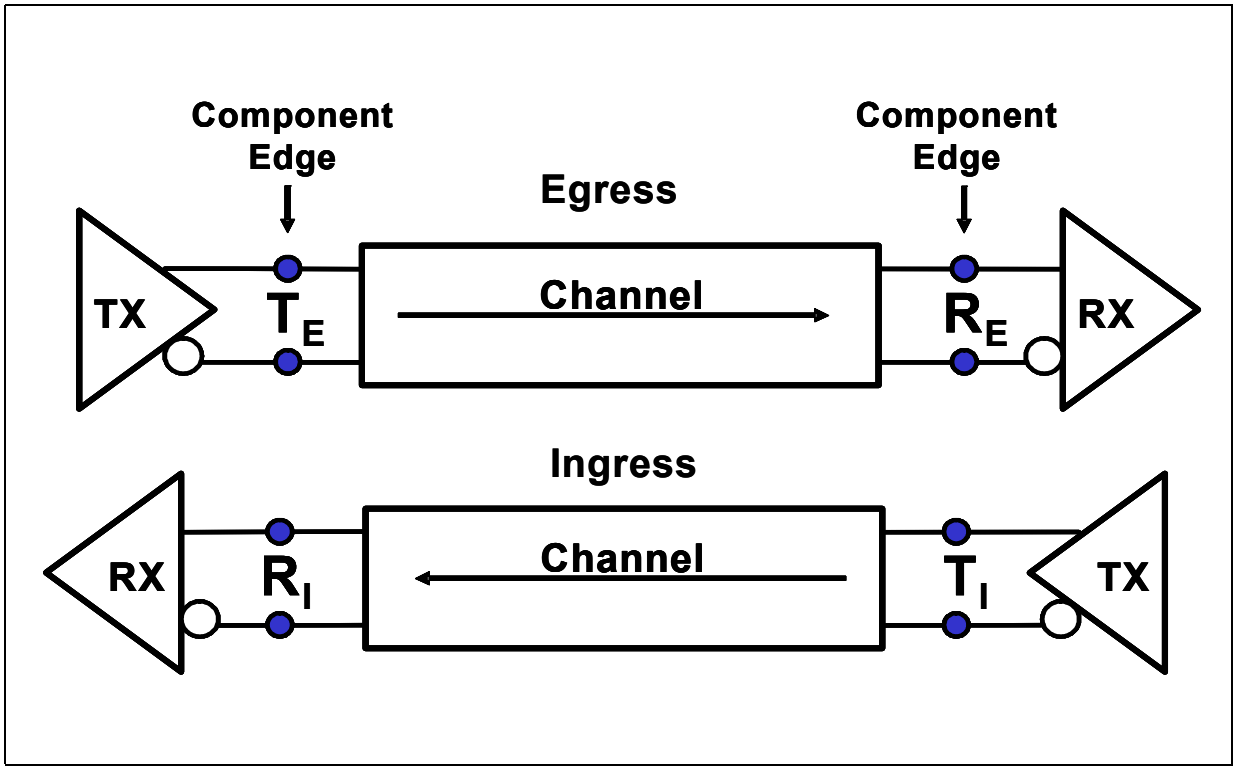
Figure 1-5. Receiver Input Mask



1.8 Reference Model

The CEI common reference model is defined in Figure 1-6. In cases where transmission direction matters the Ingress and Egress suffix is used, e.g. R_I for Receiver in the Ingress direction. In all other cases the R and T are used without a suffix. Note that the RX and TX blocks include all off-chip components associated with the respective function. Note also that a CEI Link does not imply a duplex connection, so the reference model shown in Figure 1-6 represents 2 CEI links.

Figure 1-6. Reference Model



1.A Appendix - Signal Definitions

Signals defined in this appendix are not referred to in this document, but relate to subsequent applications of CEI Links, e.g. SFI, SPI, TFI. Possible applications for CEI Links are described, but do not try to limit applications.

Whilst it is shown that CEI links can originate from a Serdes component, this is by no means essential. It is likely that CEI Links will be generated and received by TX and RX ports of an ASIC or FPGA component. In this case it will be necessary to have multiplexing and demultiplexing functions within the ASIC or FPGA. When a Serdes component is referred to, it can mean the Serializer/Deserializer is integrated within an ASIC or FPGA component, as well as being a separate component. In some applications, it will be necessary to also transmit control or status signals in parallel with the CEI Link. Some applications will also require clocks to be transmitted with the data.

The signal paths or CEI Lanes are unidirectional point-to-point connections. Each CEI Lane is made up of a balanced differential pair. A CEI Link can be comprised of a unidirectional single lane or parallel lanes in either the transmit or receive direction. A CEI Link does not imply duplex operation. See Figure 1-7 below for more information, which shows 2 CEI Links, in the receive and transmit directions.

Figure 1-7. Signal Diagram

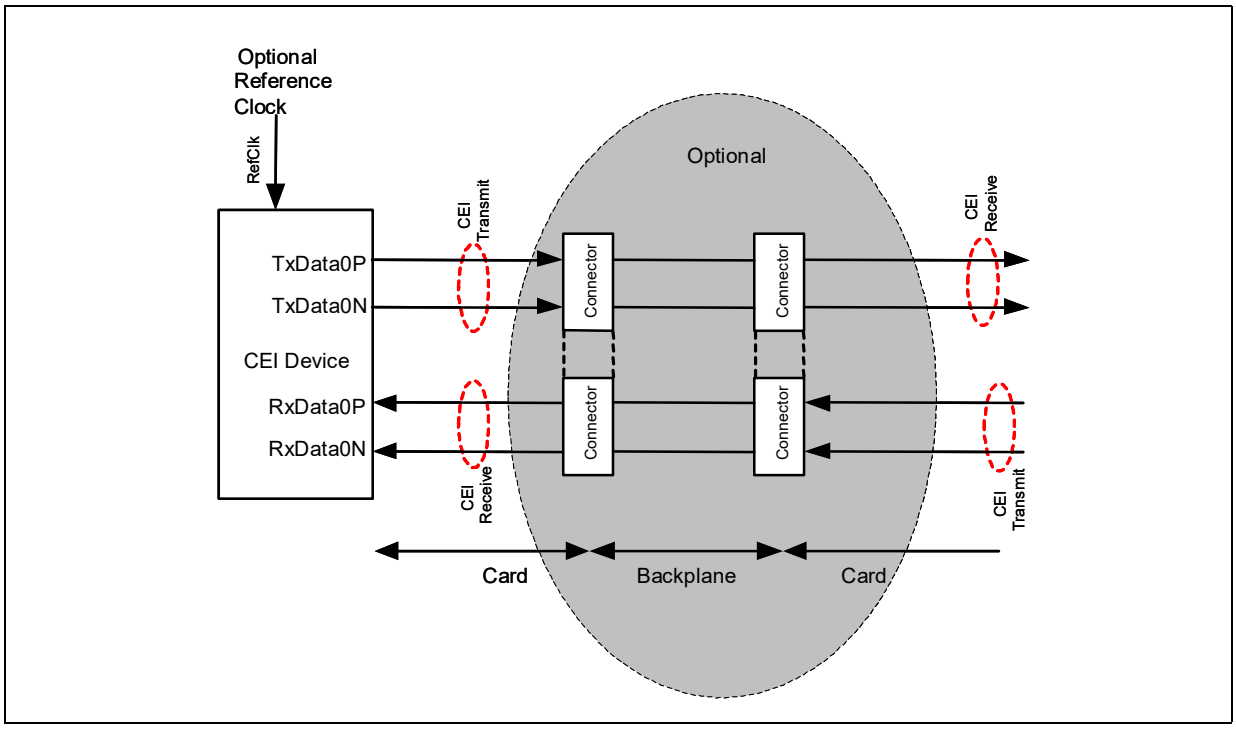


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Table 1-8. Receive Signal Summary

Signal Name	Direction	Function
RXDATA[n..0]P/N	Input to SERDES Component	The Receive Data (RXDATA[n]) signals are the inputs to the SERDES component.

Table 1-9. Transmit Signal Summary

Signal Name	Direction	Function
TXDATA[n..0]P/N	Output of SERDES Component	The Transmit Data (TXDATA[n]) signals are the outputs of the SERDES component.

An example specification for the reference clock for a typical application is proposed in Table 1-10 below.

Table 1-10. Example specification of reference clock

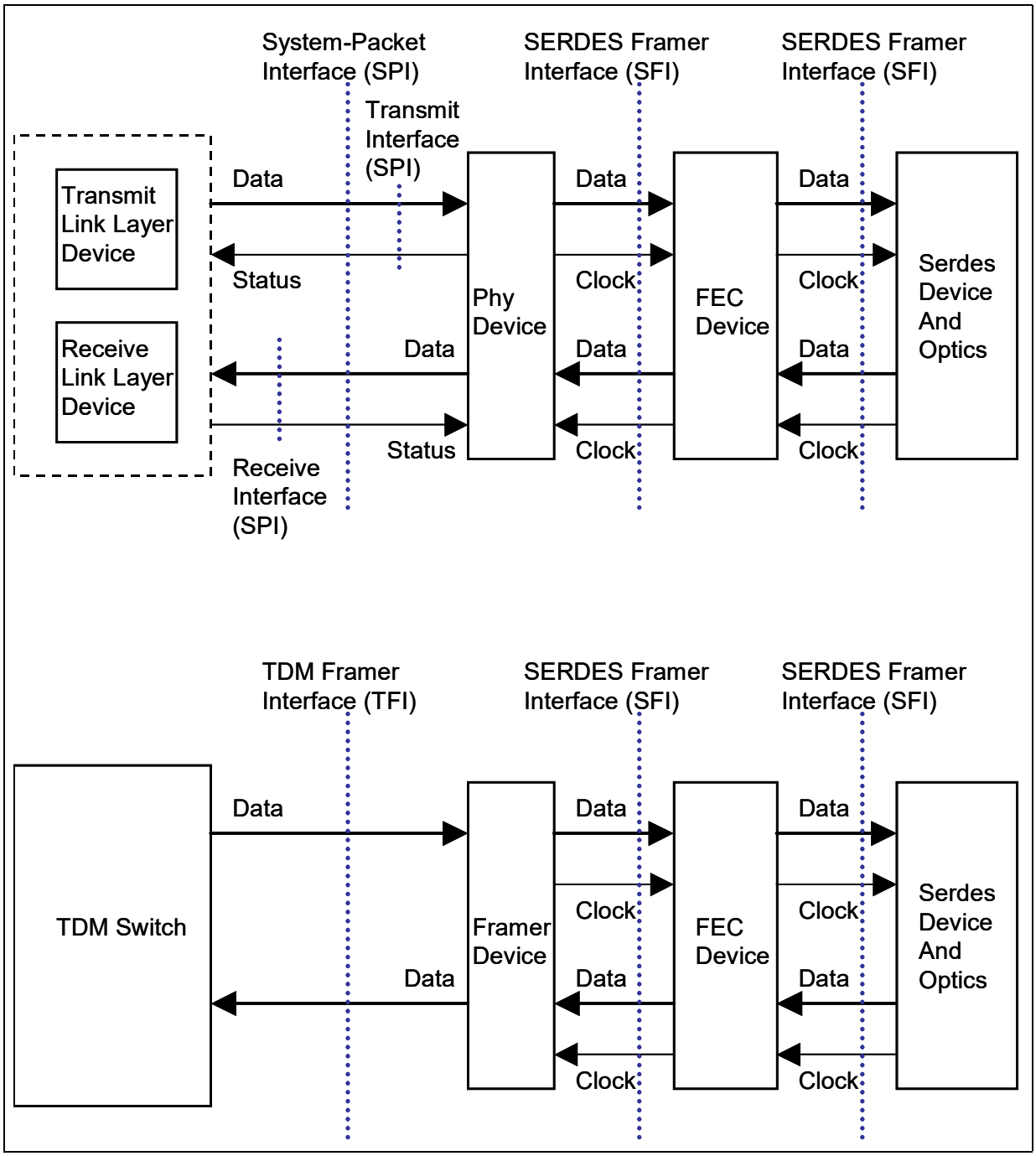
Characteristic	Description
Input Buffer	Internal Terminated LVDS
Frequency	Divide by 16 (e.g. 622MHz @9.95Gsym/s)
Rise/fall time (20/80%)	200ps
Duty cycle variation	<10%
Receiver Reference Clock frequency tolerance against data	+/-100ppm
Phase noise	-125dBc at 1MHz

It is expected that the reference clock input supports DC coupling, with AC coupling being optional (LVDS input having center tap or self biasing).

One reference clock input can support multiple Rx and Tx channels.

1.B Appendix - Examples of CEI links in Typical systems

Figure 1-8. Some typical systems



2 Jitter and Interoperability Methodology

This clause describes the requirements for interoperability testing of electrical interfaces as defined within this implementation agreement. The clause is organized into several methods of which the later Clauses will reference as the method for jitter or interoperability testing.

2.1 Method A

This sub-clause defines the interoperability methodology specifically for interfaces where neither transmit emphasis or receiver equalization are required for the receiver eye to be open to within the BER of interest.

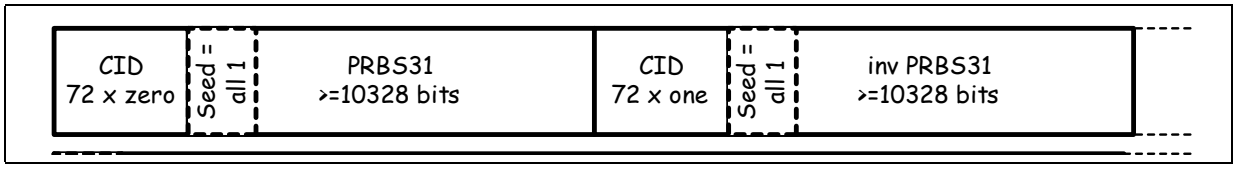
2.1.1 Defined Test Patterns[1]

The following patterns shall be used for the testing of jitter tolerance and output jitter compliance.

2.1.1.1 CID Jitter Tolerance Pattern

- The pattern is inverting to exercise possible weaknesses in rise and fall time symmetry
- 72 bits are defined for the Consecutive Identical Digits (CID) which aligns to [22.] recommendation
- The length of the PRBS31 is defined as greater than or equal to 10328
- The pattern is based on transition density comparisons between various PRBS patterns and a 3 sigma worst case analysis of a scrambled OC-768 frame.

Figure 2-1. CID Jitter Tolerance Pattern



2.1.1.2 Jitter Tolerance and General Test Patterns

- The pattern is a free running PRBS31 polynomial

2.1.2 Channel Compliance

The following steps shall be made to identify which channels are to be considered compliant.

1. All descriptions to PRBS31 imply the standard polynomial as described in [21.]

1. The forward channel and significant crosstalk channels shall be measured using a Network analyzer for the maximum baud rate that the channel is to operate at shall be used (see Appendix 2.E.6 for a suggested method)
2. An effective transmit filter as defined by the reference transmitter shall be used
3. An amplitude as defined by the reference transmitter shall be used
4. A transmitter jitter distribution (see Annex 2.C.4) as defined by the reference transmitter shall be used
5. A transmitter return loss as defined by the reference transmitter shall be used
6. A sampling point as defined by the reference receiver shall be used
7. A receiver return loss as defined by the reference receiver shall be used
8. The opening of the eye shall be calculated using Statistical Eye Analysis methods, as per Annex 2.C.5, and confirmed to be within the requirements at the required BER of the Implementation Agreement, usually,

   — Amplitude at the zero time offset sampling point

   — Time jitter measured at the zero amplitude sampling point

2.1.3 Transmitter Compliance

The following steps shall be made to identify which transmitters are to be considered compliant.

1. The high frequency transmit jitter shall be within that specified (see Appendix 2.E.1 for suggested methods)
2. The specified transmit eye mask shall not be violated (see Appendix 2.E.7 for a suggested method), after adjusting the horizontal time positions for the measured time with a confidence level of 3 sigma (see Appendix 2.F.3 for a suggested method of calculating Q given a measurement population)
3. The total wander shall be within that specified (see Appendix 2.E.2 for a suggested measurement method)
4. The relative wander shall be within that specified (see Appendix 2.E.3 for a suggested measurement method)

2.1.4 Receiver Compliance

The following step shall be made to identify which receivers are to be considered compliant.

1. The DUT shall be measured to have a BER[1] better than specified for a stressed signal (see Appendix 2.E.4.1 for a suggested method) with a confidence level of three sigma (see Appendix 2.F.2 for a suggested method), given:

1. if the defined measurement BER is different to system required BER, adjustments to applied stressed eye TJ are necessary

— The defined sinusoidal jitter mask for relative and total wander as per Annex 2.A.1 and Annex 2.A.2, with a high frequency total/relative wander of 0.1UI and a maximum total/relative wander as defined in the Implementation Agreement. Note that in some Implementation Agreements one needs to reduce the amount of High Probability Jitter by 0.1UI to account for this sinusoidal jitter.

2.2 Method B

This sub-clause defines the interoperability methodology specifically for interfaces where transmit emphasis may be used however receiver equalization is not required for the receiver eye to be open to within the BER of interest.

2.2.1 Defined Test Patterns[1]

The following pattern shall be used for the testing of jitter tolerance and output jitter compliance.

- A free running PRBS31 polynomial

2.2.2 Channel Compliance

The following steps shall be made to identify which channels are to be considered compliant.

1. The forward channel and significant crosstalk channels shall be measured using a Network analyzer for the maximum baud rate that the channel is to operate at shall be used (see Appendix 2.E.6 for a suggested method)
2. An n-tap emphasized transmitter as per Annex 2.B.3, where “n” is defined by the reference transmitter shall be used
3. An effective transmit filter as defined by the reference transmitter shall be used
4. An amplitude as defined by the reference transmitter shall be used
5. A transmitter jitter distribution (see Annex 2.C.4) as defined by the reference transmitter shall be used
6. A transmitter return loss as defined by the reference transmitter shall be used
7. A sampling point as defined by the reference receiver shall be used
8. A receiver return loss as defined by the reference receiver shall be used
9. The opening of the eye shall be calculated using Statistical Eye Analysis methods, as per Annex 2.C.5, and confirmed to be within the requirements at the required BER of the Implementation Agreement, usually:
   — Amplitude at the zero time offset sampling point
   — Time jitter measured at the zero amplitude sampling point

1. All descriptions to PRBS31 imply the standard polynomial as described in [21.]

2.2.3 Transmitter Compliance

The following step shall be made to identify which transmitters are to be considered compliant.

1. It shall be verified that the measured eye is equal or better than the calculated eye for the given measurement probability Q (see Appendix 2.F.3 for a suggested method of calculating Q given a measurement population), given:
   - A stress channel that is otherwise compliant as per 2.2.2, that requires at least half the maximum transmit emphasis as specified in the relevant clause or IA, with no receiver filtering or equalisation to produce an open eye.
   - Using this channel the transmitter shall be then optimally adjusted and the resulting eye measured (see Appendix 2.E.7 for a suggested method).
   - Using this channel the statistical eye shall then be calculated, as per Annex 2.C.5, using the maximum defined transmit jitter and the actual transmitter's amplitude and emphasis.

If the transmit jitter or transmit eye mask is additionally defined then the following steps shall also be made to identify which transmitters are to be considered compliant:

1. The high frequency transmit jitter shall be within that specified (see Appendix 2.E.1 for suggested methods)
2. The specified transmit eye mask shall not be not violated (see Appendix 2.E.7 for a suggested method), after adjusting the horizontal time positions for the measured time with a confidence level of 3 sigma (see Appendix 2.F.3 for a suggested method)

2.2.4 Receiver Compliance

The following step shall be made to identify which receivers are to be considered compliant.

1. The DUT shall be measured to have a BER[1] better than specified for a stressed signal (see Appendix 2.E.4.2 for a suggested method) with a confidence level of three sigma (see Appendix 2.F.2 for a suggested method), given:
   - The defined sinusoidal jitter mask for total and relative wander as per Annex 2.A.1 and Annex 2.A.2, with a high frequency total/relative wander and a maximum total/relative wander as defined in the Implementation Agreement
   - The specified amount of High Probability Jitter and Gaussian jitter.

1. if the defined measurement BER is different to system required BER, adjustments to applied stressed eye TJ are necessary

2.3 Method C

This sub-clause defines the interoperability methodology specifically for interfaces where transmit emphasis may be used and the receiver eye requires Linear Continuous Time equalization (from channel interoperability point of view) to be open to within the BER of interest.

2.3.1 Defined Test Patterns[1]

The following pattern shall be used for the testing of jitter tolerance and output jitter compliance.

- A free running PRBS31 polynomial

2.3.2 Channel Compliance

The following steps shall be made to identify which channels are to be considered compliant.

1. The forward channel and significant crosstalk channels shall be measured using a Network analyzer for the maximum baud rate that the channel is to operate at shall be used (see Appendix 2.E.6 for a suggested method)
2. An n-tap emphasized transmitter as per Annex 2.B.3, where “n” is defined by the reference transmitter shall be used
3. An effective transmit filter as defined by the reference transmitter shall be used
4. An amplitude as defined by the reference transmitter shall be used
5. A transmitter jitter distribution (see Annex 2.C.4) as defined by the reference transmitter shall be used
6. A transmitter return loss as defined by the reference transmitter shall be used
7. An ideal receiver filter of the form in Annex 2.B.7, using the restrictions as defined by the reference receiver shall be used
8. A sampling point as defined by the reference receiver shall be used
9. A receiver return loss as defined by the reference receiver shall be used
10. The opening of the eye shall be calculated using Statistical Eye Analysis methods, as per Annex 2.C.5, and confirmed to be within the requirements at the required BER of the Implementation Agreement, usually:

    — Amplitude at the zero time offset sampling point

    — Time jitter measured at the zero amplitude sampling point

1. All descriptions to PRBS31 imply the standard polynomial as described in [21.]

2.3.3 Transmitter Compliance

The following step shall be made to identify which transmitters are to be considered compliant.

1. It shall be verified that the measured eye is equal or better than the calculated eye for the given measurement probability Q (see Appendix 2.F.3 for a suggested method of calculating Q given a measurement population), given:
   - A stress channel that is otherwise compliant as per 2.3.2, that requires at least half the maximum transmit emphasis as specified in the relevant clause or IA, with no receiver filtering or equalisation to produce an open eye.
   - Using this channel the transmitter shall be then optimally adjusted and the resulting eye measured (see Appendix 2.E.7 for a suggested method).
   - Using this channel the statistical eye shall then be calculated, as per Annex 2.C.5, using the maximum defined transmit jitter and the actual transmitter's amplitude and emphasis.

If the transmit jitter or transmit eye mask is additionally defined then the following steps shall also be made to identify which transmitters are to be considered compliant:

1. The high frequency transmit jitter shall be within that specified (see Appendix 2.E.1 for suggested methods)
2. The specified transmit eye mask shall not be violated (see Appendix 2.E.7 for a suggested method), after adjusting the horizontal time positions for the measured time with a confidence level of 3 sigma (see Appendix 2.F.3 for a suggested method)

2.3.4 Receiver Compliance

The following step shall be made to identify which receivers are to be considered compliant.

1. The DUT shall be measured to have a BER[1] better than specified for a stressed signal (see Appendix 2.E.4.3 for a suggested method) with a confidence level of three sigma (see Appendix 2.F.2 for a suggested method), given:
   - The defined sinusoidal jitter mask for total and relative wander as per Annex 2.A.1 and Annex 2.A.2, with a high frequency total/relative wander and a maximum total/relative wander as defined in the Implementation Agreement
   - The specified amount of High Probability Jitter and Gaussian jitter.
   - A stress channel or filter as identified by the methods of 2.3.2. If the optional transmit filter of Appendix 2.E.4.3 is not included then no transmit emphasis shall be enabled in the reference transmitter. If the transmitter filter of Appendix 2.E.4.3 is present then the standard reference transmitter (as used in channel compliance) shall be used. The transmit filter characteristics (e.g. emphasis

1. if the defined measurement BER is different to system required BER, adjustments to applied stressed eye TJ are necessary

settings) shall be set in accordance with the optimised values resulting when the methods of 2.3.2 are applied.

— An additive crosstalk signal of amplitude such that the resulting statistical eye, given the channel, jitter and crosstalk, is as close as feasible in amplitude when compared to the defined minimum amplitude for channel compliance.

2.4 Method D

This sub-clause defines the interoperability methodology specifically for interfaces where transmit emphasis may be used and the receiver eye requires DFE equalization (from channel interoperability point of view) to be open to within the BER of interest.

2.4.1 Defined Test Patterns[1]

The following pattern shall be used for the testing of jitter tolerance and output jitter compliance.

- A free running PRBS31 polynomial

2.4.2 Channel Compliance

The following steps shall be made to identify which channels are to be considered compliant.

1. The forward channel and significant crosstalk channels shall be measured using a Network analyzer for the maximum baud rate that the channel is to operate at shall be used (see Appendix 2.E.6 for a suggested method)
2. An n-tap emphasized transmitter as per Annex 2.B.3, where “n” is defined by the reference transmitter shall be used
3. An effective transmit filter as defined by the reference transmitter shall be used
4. An amplitude as defined by the reference transmitter shall be used
5. A transmitter jitter distribution (see Annex 2.C.4) as defined by the reference transmitter shall be used
6. A transmitter return loss as defined by the reference transmitter shall be used
7. An ideal receiver filter of the form in Annex 2.B.6, using the restrictions as defined by the reference receiver shall be used
8. Any parameters that have degrees of freedom e.g. filter coefficients or sampling point, shall be optimised against the amplitude, at the zero phase offset, as generated by the Statistical Eye Output. e.g. by sweeping all degrees of freedom and selecting the parameters giving the maximum amplitude. A receiver return loss, as defined by the reference receiver, shall be used

1. All descriptions to PRBS31 imply the standard polynomial as described in [21.]

9. The opening of the eye shall be calculated using Statistical Eye Analysis methods, as per Annex 2.C.5, and confirmed to be within the requirements at the required BER of the Implementation Agreement, usually:

   — Amplitude at the zero time offset sampling point

   — Time jitter measured at the zero amplitude sampling point

2.4.3 Transmitter Compliance

The following step shall be made to identify which transmitters are to be considered compliant.

1. It shall be verified that the measured eye is equal or better than the calculated eye for the given measurement probability Q (see Appendix 2.F.3 for a suggested method of calculating Q given a measurement population), given:

   — A stress channel that is otherwise compliant as per 2.4.2, that requires at least half the maximum transmit emphasis as specified in the relevant clause or IA, with no receiver filtering or equalisation to produce an open eye.

   — Using this channel the transmitter shall be then optimally adjusted and the resulting eye measured (see Appendix 2.E.7 for a suggested method).

   — Using this channel the statistical eye shall then be calculated, as per Annex 2.C.5, using the maximum defined transmit jitter and the actual transmitter's amplitude and emphasis.

If the transmit jitter or transmit eye mask is additionally defined then the following steps shall also be made to identify which transmitters are to be considered compliant:

1. The high frequency transmit jitter shall be within that specified (see Appendix 2.E.1 for suggested methods)
2. The specified transmit eye mask shall not be violated (see Appendix 2.E.7 for a suggested method), after adjusting the horizontal time positions for the measured time with a confidence level of 3 sigma (see Appendix 2.F.3 for a suggested method)

2.4.4 Receiver Compliance

The following step shall be made to identify which receivers are to be considered compliant.

1. The DUT shall be measured to have a BER[1] better than specified for a stressed signal (see Appendix 2.E.4.3 for a suggested method) with a confidence level of three sigma (see Appendix 2.F.2 for a suggested method), given:

   — The defined sinusoidal jitter mask for total and relative wander as per Annex 2.A.1 and Annex 2.A.2, with a high frequency total/relative wander and a maximum total/relative wander as defined in the Implementation Agreement

1. if the defined measurement BER is different to system required BER, adjustments to applied stressed eye TJ are necessary

— The specified amount of High Probability Jitter and Gaussian jitter.

— A stress channel or filter as identified by the methods of 2.4.2. If the optional transmit filter of Appendix 2.E.4.3 is not included then no transmitter emphasis shall be enabled in the reference transmitter. If the transmitter filter of Appendix 2.E.4.3 is present then the standard reference transmitter (as used in channel compliance) shall be used. The transmit filter characteristics (e.g. emphasis settings) shall be set in accordance with the optimised values resulting when the methods of 2.4.2 are applied.

— An additive crosstalk signal of amplitude such that the resulting statistical eye, given the channel, jitter and crosstalk, is as close as feasible in amplitude when compared to the defined minimum amplitude for channel compliance

2.5 Method E

The following sub-clause defines the Interoperability methodology for interfaces where a simple receiver equalization may be used to improve the margin of the link and transparent applications may be used and the receiver eye is still open to within the BER of interest.

2.5.1 Defined Test Patterns

The following pattern shall be used for the testing jitter tolerance and output jitter compliance

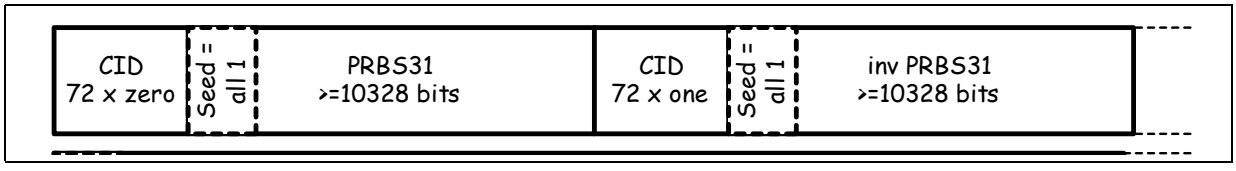
- A free running PRBS31 polynomial

when used in transparent applications the additional test pattern defined in 2.5.1.1 must be additionally tested.

2.5.1.1 CID Jitter Tolerance Pattern

- The pattern is inverting to exercise possible weaknesses in rise and fall time symmetry
- 72 bits are defined for the Consecutive Identical Digits (CID) which aligns to [22.] recommendation
- The length of the PRBS31 is defined as greater than or equal to 10328
- The pattern is based on transition density comparisons between various PRBS patterns and a 3 sigma worst case analysis of a scrambled OC-768 frame.

Figure 2-2. CID Jitter Tolerance Pattern



2.5.2 Channel Compliance

The following steps shall be made to identify which channels are to be considered compliant.

1. The forward channel and significant crosstalk channels shall be measured using a Network analyzer for the maximum baud rate that the channel is to operate at shall be used (see Appendix 2.E.6 for a suggested method)
2. An effective transmit filter as defined by the reference transmitter shall be used
3. An amplitude as defined by the reference transmitter shall be used
4. A transmitter jitter distribution (see Annex 2.C.4) as defined by the reference transmitter shall be used
5. A transmitter return loss as defined by the reference transmitter shall be used
6. All defined reference receivers
7. A sampling point as defined by the reference receiver shall be used
8. A receiver return loss as defined by the reference receiver shall be used
9. The opening of the eye shall be calculated using Statistical Eye Analysis methods, as per Annex 2.C.5, and confirmed to be within the requirements at the required BER of the Implementation Agreement for both receiver types, usually:

   — Amplitude at the zero time offset sampling point

   — Time jitter measured at the zero amplitude sampling point
10. Any parameters that have degrees of freedom e.g. filter coefficients, shall be optimised against the amplitude, at the zero phase offset, as generated by the Statistical Eye Output. e.g. by sweeping all degrees of freedom and selecting the parameters giving the maximum amplitude.

2.5.3 Transmitter Compliance

The following steps shall be made to identify whether a transmitter is considered compliant.

1. the high frequency transmit jitter shall be within that specified (see Appendix 2.E.1 for suggested methods)

   • for jitter transparent applications the bandwidth of any defined Golden PLL should be adjusted according to the specific Implementation Agreement e.g. 8MHz for ITU
2. Specifically for “transparent ITU application egress transmitters” the transmit peak to peak jitter and optionally rms jitter with the defined bandwidth shall be less than that specified (see Appendix 2.E.1.2 for suggested methods)
3. Specifically for “transparent ingress transmitters” the defined jitter transfer mask shall be less than that specified (see Appendix 2.E.5 for suggested methods)

- an applied sinusoidal jitter conforming to the defined jitter tolerance mask for this line interface

4. the specified transmit eye mask is not violated (see Appendix 2.E.7 for a suggested method), after adjusting the horizontal time positions for the measured time and a confidence level of 3 sigma (see Appendix 2.F.3 for a suggested method of calculating Q given a measurement population)
5. the total wander is less than that specified (see Appendix 2.E.2 for a suggested method)

2.5.4 Receiver Compliance

The following steps shall be made to identify whether a receiver is considered compliant.

1. The DUT shall be measured to have a BER[1] better than specified for a stressed signal (see Appendix 2.E.4.2 for a suggested method) with a confidence level of three sigma (see Appendix 2.F.2. for a suggested method) given

- for non-transparent applications, the defined sinusoidal jitter mask for relative and total wander as per Annex 2.A.1 and Annex 2.A.2, with a high frequency total/ relative wander and a maximum total/relative wander as defined in the Implementation Agreement
- for transparent application, the defined appropriate sinusoidal jitter mask for the specific optical standard
- the high frequency jitter should be calibrated by either
  - applying the maximum specified amount of receiver High Probability Jitter and Gaussian jitter[2] including CBHPJ

or

  - applying the maximum specified amount of receiver High Probability Jitter and Gaussian jitter[3] excluding CBHPJ
  - cascading with a compliance channel or filter as identified by 2.5.2.
  - applying an additive crosstalk signal of amplitude such that the resulting statistical eye, given the channel, jitter and crosstalk, is as close as feasible in amplitude when compared to the defined minimum amplitude for channel compliance

1. if the defined measurement BER is different to system required BER, adjustments to applied stressed eye TJ are necessary
2. for jitter “transparent application ingress receivers” the bandwidth of any defined Golden PLL for the calibration of the HPJ and GJ should be adjusted according to the specification Implementation Agreement e.g. 8MHz for ITU
3. for jitter “transparent application ingress receivers” the bandwidth of any defined Golden PLL for the calibration of the HPJ and GJ should be adjusted according to the specification Implementation Agreement e.g. 8MHz for ITU

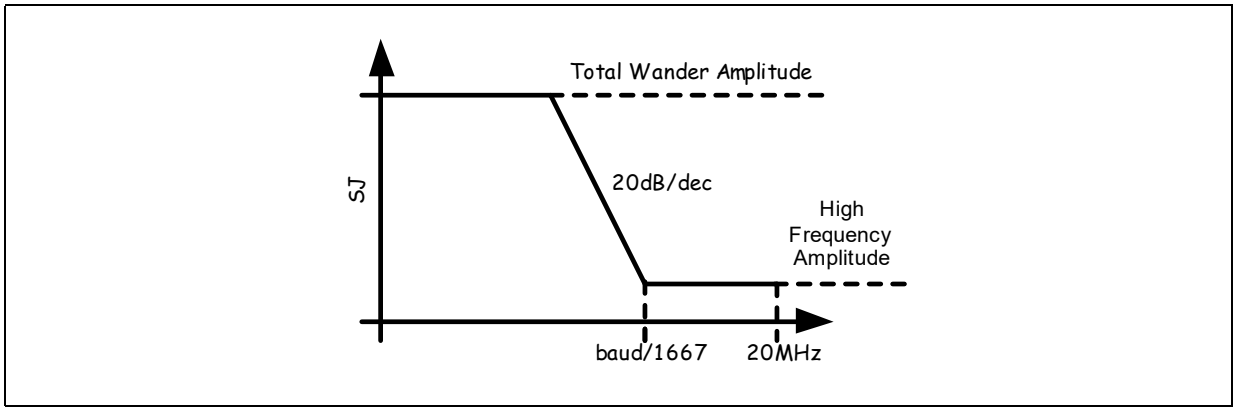
2.A Annex - Masks

2.A.1 Annex - Total Wander Mask

Total wander specifications should be considered as accumulated low frequency jitter. As modern CDRs are digitally based they show a corner tracking frequency plus slew limitation which has been guaranteed, therefore for jitter tolerance testing the total wander needs to be spectrally defined to ensure correct operation.

To this end, for jitter tolerance testing, the wander is considered a sinusoidal jitter source as shown below.

Figure 2-3. Total Wander Mask

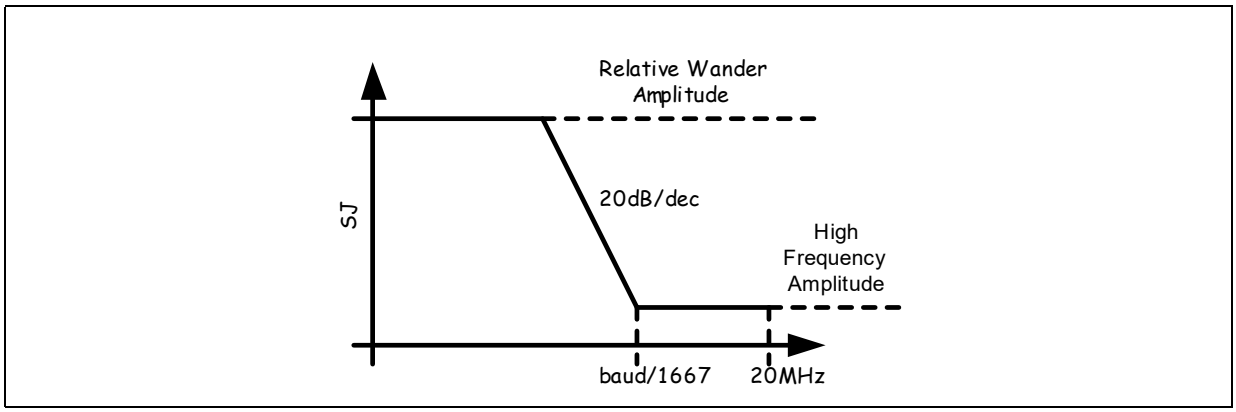


At higher frequency this jitter source is used to ensure margin in the high frequency jitter tolerance of the receiver. At lower frequencies the higher SJ should then be tracked by the CDR.

2.A.2 Annex - Relative Wander Mask

Specifically for interfaces defining relative wander, Figure 2-4 is also defined in terms of a sinusoidal jitter source as shown below.

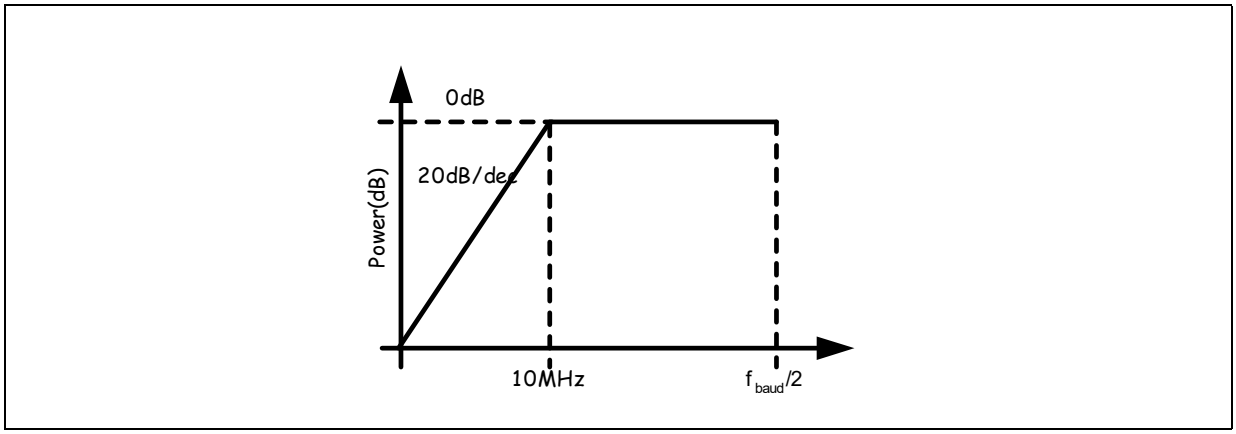
Figure 2-4. Relative Wander Mask



2.A.3 Annex - Random Jitter Mask

To ensure that the random jitter modulation of stressed signals is above the CDR bandwidth and therefore untracked, the following filter mask shall be applied where necessary.

Figure 2-5. Random Jitter Spectrum



2.B Annex - Pulse Response Channel Modelling

This annex shall describe the theoretical background for channel modelling

2.B.1 Annex - Generating a Pulse Response

Given the spectral transfer function as per Chapter 2.E.6 the pulse response of the channel can be calculated using tools such as Matlab.

The Pulse Response of the channel is the received pulse for an ideal square wave and is calculated by either

- convolving the pulse with the impulse response of the channel or
- multiplying the Fourier spectrum of the ideal transmitted square wave with the channel response and taking the inverse Fourier transform,

$$t_{step} = \frac{1}{f_{max}}$$

$$t = t_{step} \cdot n$$

$$n = [1,P]$$

$$tx(t) = H(0) \cdot H(t_{period} - t)$$

$$rx(\omega) = tx(\omega) \cdot Tr(\omega)$$

$$rx(t) = ifft(rx(\omega))$$

where

f_{max} is difference between the maximum positive and minimum negative frequency

P is the number of equally space points in the frequency array

$tx(t)$ is the transmit signal pulse

$tx(\omega)$ is the transmit signal pulse in the frequency domain

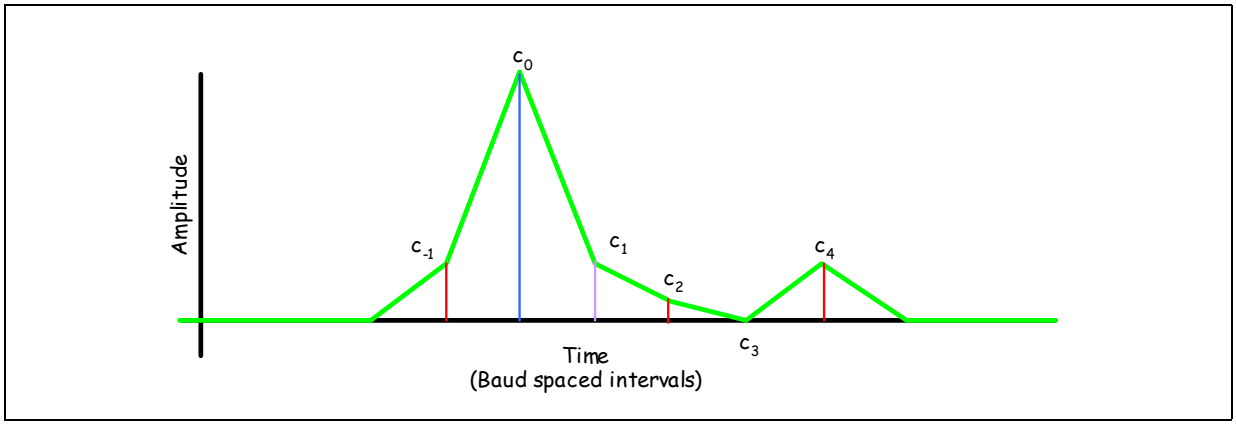
$Tr(\omega)$ is the transfer function of the channel

$rx(t)$ is the resulting pulse response of the channel

2.B.2 Annex - Basic Pulse Response Definitions

A receive pulse response as calculated above can be graphically represented, Figure 2-6.

Figure 2-6. Graphical Representation of Receiver Pulse



Cursors are defined as being the amplitude of the received pulse at symbol spaces from the maximum signal energy at c_0, and extend to infinity in both negative and positive time. The exact position of c_0 is arbitrary and is defined specifically by the various methodologies.

A precursor is defined as a cursor that occurs before the occurrence of the main signal c_0, i.e. c_n where n<0, usually convergences to zero within a small number of bits

A post cursor is defined as a cursor that occurs after the occurrence of the main signal c_0, i.e. c_n where n>0, and usually convergences to zero within twice the propagation time of the channel.

Given a deterministic data stream travelling across the channel, the superposition of the channel pulses give rise to Inter-Symbol Interference (ISI). This ISI has a maximum occurring for a worst case pattern, which for a channel response where all cursors are positive would be a single *1* or *0* in the middle of a long run of *0*s or *1*s respectively. This maximum is referred to Total Distortion

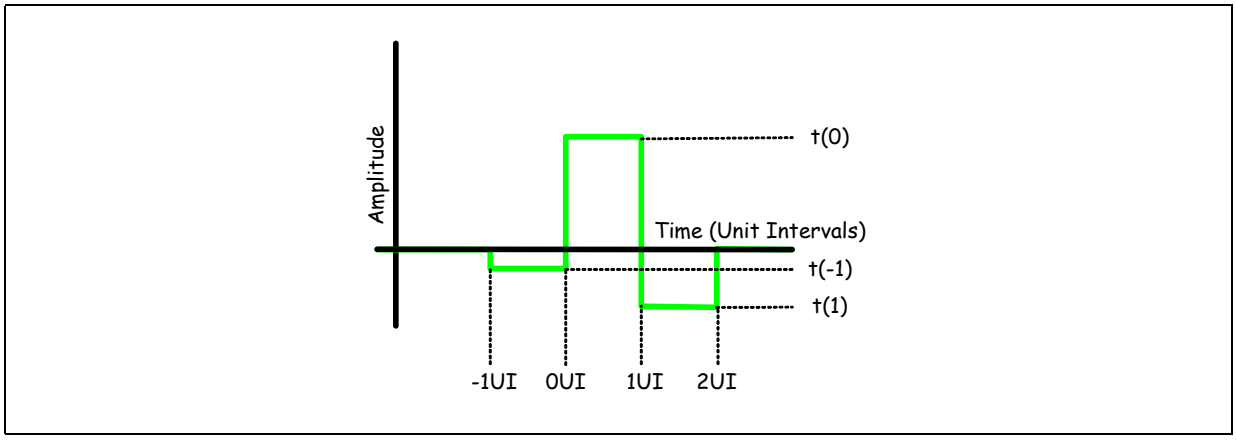
$$\Theta = \sum_{(n=-\infty),(n\neq 0)}^{n=\infty} |c_n|$$

Due to ISI an enclosure in the time domain also occurs which can be determined by either running exhaustive simulations or simulations with determined worst case patterns. For the case where the ISI is so large that the eye is closed, Inherent Channel Jitter has no meaning.

2.B.3 Annex - Transmitter Pulse Definition

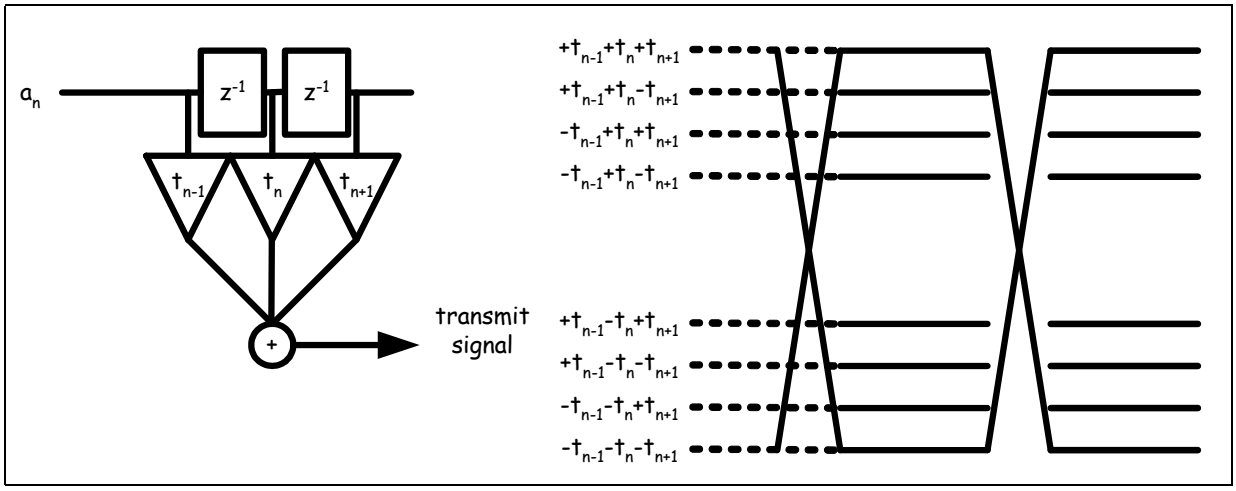
A transmitter is defined by its ability to generate a transmit pulse. A single *1* transmit symbol has different amplitudes at symbol space intervals, t_n, where post taps have n>0, and pre-taps have n<0.

Figure 2-7. Transmit Pulse



When a pulse train is transmitted the exact transmitted amplitude is therefore the superposition of the pulses from the previous and *to be* transmitted pulses, so as in a FIR filter.

Figure 2-8. Transmitter FIR Filter Function



This superposition can be understood by referring to the amplitudes depicted for various bit sequences in Figure 2-8.

The transmit emphasis can be defined to have certain limits of maximum transmit amplitude or ratios of emphasis as defined below

$$P_{post} = \frac{t_1}{t_0}$$

$$E = 20\log\frac{1 + P_{post}}{1 - P_{post}}$$

$$\sum |t_n| < T_\text{Vdiff}$$

where

P_{post} is the first coefficient of the transmit FIR

E is the emphasis of the transmit emphasis

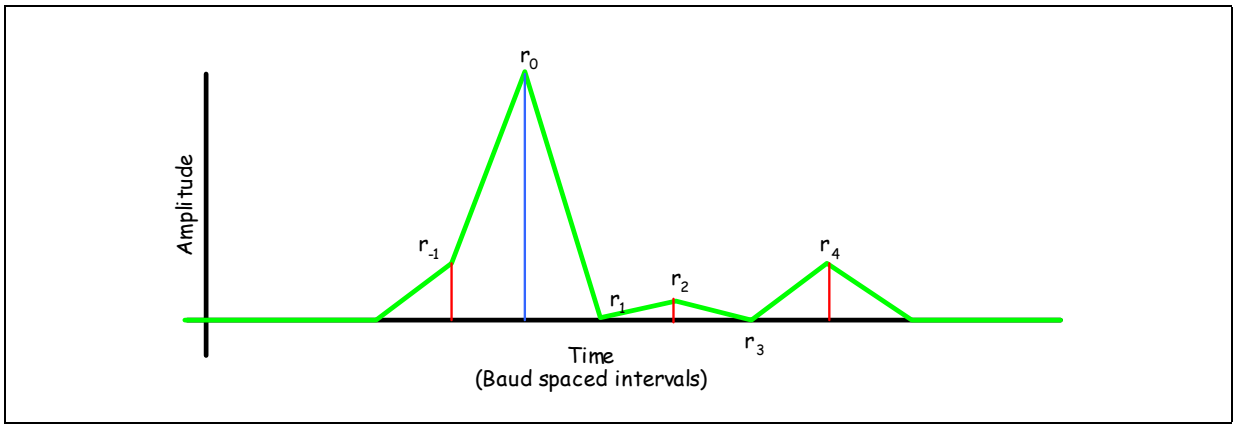
T_Vdiff is the maximum transmit amplitude

2.B.4 Annex - Receiver Pulse Response

Given an emphasized transmitter the pulse response of the receiver should be recalculated using the emphasized transmit pulse as opposed to a simple NRZ pulse.

the receiver pulse cursors are then defined as follows

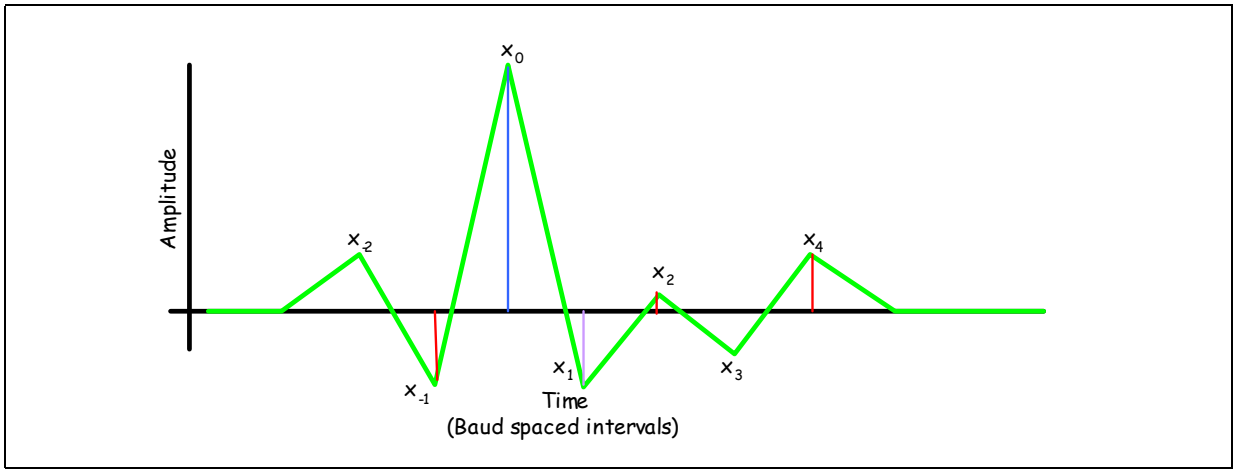
Figure 2-9. Receiver Pulse Definition



2.B.5 Annex - Crosstalk Pulse Response

The crosstalk pulse response is analogous to the receiver pulse response as defined in Annex 2.B.4 but using the crosstalk channel, i.e. NEXT or FEXT network analysis measurement.. The transmit signal as seen in the system should be used for the

Figure 2-10. Crosstalk Pulse Definition



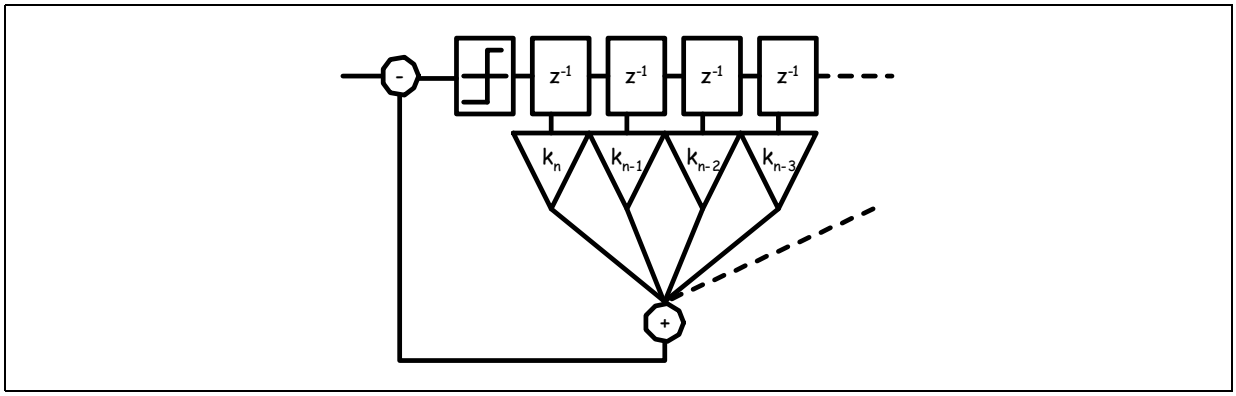
calculation of the resulting crosstalk pulse response, e.g.an emphasized transmitter from above, or XAUI transmit NRZ pulse.

The Crosstalk pulse response is then defined as above, as being a set of cursors x_n usually oscillatory in form. The position of x_0 is defined as being at the maximum amplitude of the pulse response.

2.B.6 Annex - Decision Feedback Equalizer

The following filter function can be used to verify the capability of the channel to be used in such an application.

Figure 2-11. Decision Feedback Equalizer



The value of the coefficients are calculated directly from the channel pulse response or the receiver pulse using an emphasized transmitter.

$k_n = c_n\big|_{n=[1,m]}$ for unemphasized transmitters, or

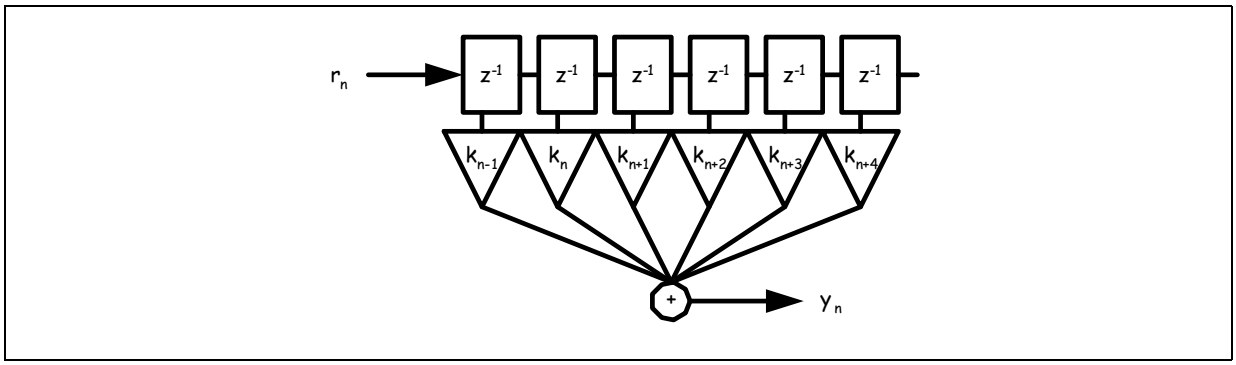
$k_n = r_n\big|_{n=[1,m]}$ for emphasized transmitters

This equalizer is capable of equalizing a finite number of post cursors, whose individual values may be limited.

2.B.7 Annex - Time Continuous Transverse Filter

A.k.a. Feed forward Filter, Finite Input Response or Comb Structure, the Transverse Filter, Figure 2-12 consists of a finite number of coefficients, k. The sum of the continuous value of symbol spaced delayed samples multiplied by these coefficients then gives the resulting signal.

Figure 2-12. Feed Forward Filter



2.B.7.1 Annex - Time Continuous Zero-Pole Equalizer adaption

The pole-zero algorithm takes the SDD21 magnitude response for the through channel and inverts it to produce a desired CTE filter response curve. From a set of initial conditions for 3 poles and 3 zeros, the squared differences are minimized between the CTE response and the inverse channel response curve. The minimization is done using a simplex method, specifically the Nelder-Mead Multidimensional Unconstrained Non-Linear Minimization Method. The Nelder-Mead method provides a local minimization of the square of the difference between the two curves by descending along the gradient of the difference function. Once the optimization result is obtained, it is compared to a specified threshold. If the threshold exceeds the target tolerance, an incrementally offset seed point is generated from a 6-dimensional grid of seed points, and the process is iterated until the correct curve is obtained within the target tolerance.

2.B.8 Annex - Time Continuous Zero/Pole

The Zero/Pole Filter is defined, in the frequency domain by

$$H(f) = \frac{p}{z} \cdot \frac{(z + j2\pi f)}{(p + j2\pi f)}$$

and consists of a single zero, z, and single pole, p.

2.B.9 Annex - Degrees of Freedom

2.B.9.1 Annex - Receiver Sample Point

A receiver shall be allowed to either position the centre sampling point fully independently to the signal transitions or exactly in between the mean crossover of the receiver signal.

2.B.9.2 Annex - Transmit Emphasis

Transmit emphasis and receiver filter coefficients must be optimised with the defined resolution to give the best achievable results. Unless otherwise stated it shall be assumed that the coefficients are defined using floating point variables.

2.C Annex - Jitter Modelling

This annex describes the theoretical background of the methodology used for jitter budgeting and jitter measurement. To avoid fundamental issues with the addition of jitter using the dual Dirac model through a bandlimited channel, a fundamental methodology call “stateye” is defined in Annex 2.C.5, which uses only convolution of the jitter distribution for the calculation of the jitter at the receiver.

2.C.1 Annex - High Frequency Jitter vs. Wander

Jitter is defined as the deviation of the signal transition from an origin, usually its mean. This deviation has an amplitude and an associated spectrum. High frequency jitter is defined by a 1st order high pass phase filter with a corner frequency equal to the ideal CDR bandwidth. The low frequency Jitter or Wander is defined by a 1st order low pass phase filter with a corner frequency equal to the bandwidth.

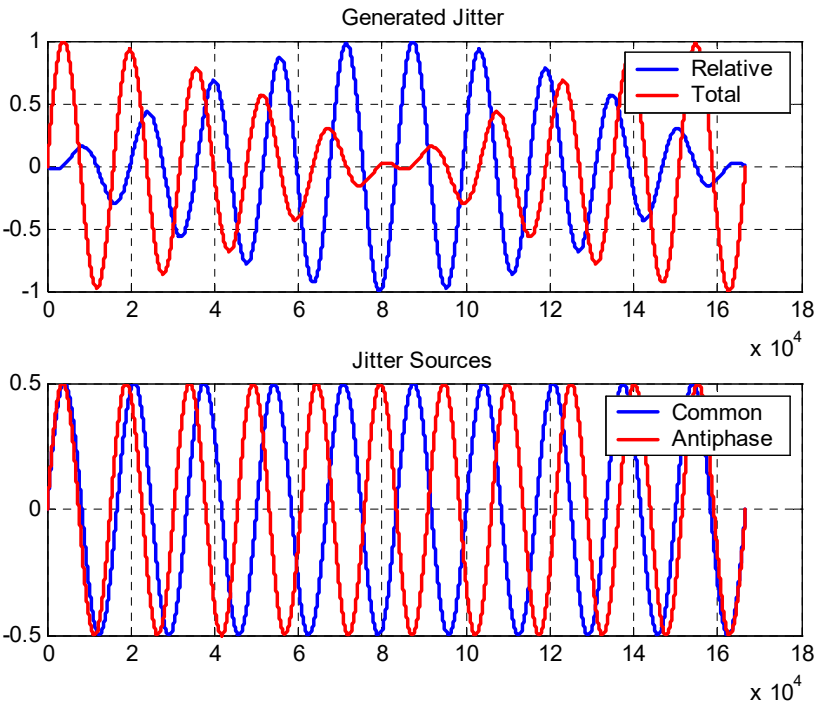
2.C.2 Annex - Total Wander vs. Relative Wander

Generation of Total and Relative Wander can be achieved using a “Common” and “AntiPhase” Sinusoidal Source, where the total and relative wander are then related as defined below.

$$A_{total} = A_{common} + A_{antiphase}$$
$$A_{relative} = 2A_{antiphase}$$

By adding sinusoidal frequencies of slightly differing frequencies the maximum total and relative wander is achieved at various phase relationships, Figure 2-13.

Figure 2-13. Generation of Total and Relative Wander



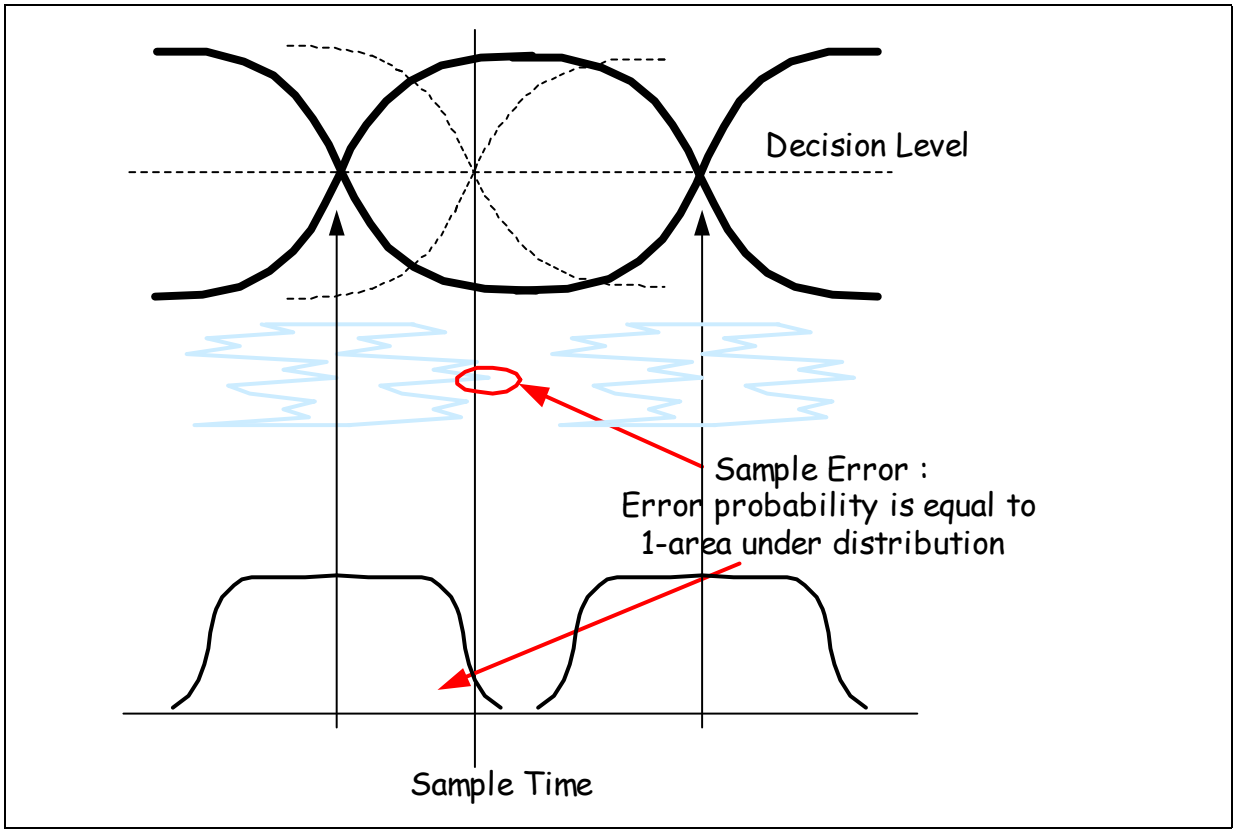
2.C.3 Annex - Correlated vs. Uncorrelated Jitter

If a correlation exists between the amplitude of the jitter and the current, past and future signal level of a data channel, this type of jitter is deemed correlated. Typically this is encountered when band limitation and inter-symbol interference occurs. Due to amplitude to phase conversion of the ISI, a jitter is observed which has a direct correlation to the data pattern being transmitted.

2.C.4 Annex - Jitter Distributions

High frequency is traditionally measured and described using probability density functions, Figure 2-14 (bottom) which describe the probability of the data signal crossing a decision threshold.

Figure 2-14. Jitter Probability Density Function



The low probability part of the jitter distribution can be described by two components, mathematically described below.

2.C.4.1 Annex - Unbounded and Bounded Gaussian Distribution

We define a Unbounded Gaussian distribution function in terms of sigma as below.

$$GJ(\tau, \sigma) = \frac{1}{\sqrt{2\pi}} \cdot \frac{1}{\sigma} \cdot e^{-\frac{\tau^2}{2\sigma^2}}$$

For every offset τ, there exists a finite and non-zero probability.

2.C.4.2 Annex - Bounded Gaussian Distribution

We define a Bounded Gaussian Distribution function[1] in terms of sigma and a maximum value as below.

$$GJ(\tau, \sigma) = \begin{cases} \frac{1}{\sqrt{2\pi}} \cdot \frac{1}{\sigma} \cdot e^{\frac{\tau^2}{2\sigma^2}} & \text{if } \tau \le \tau_{max} \\ 0 & \text{if } \tau > \tau_{max} \end{cases}$$

For random processes consisting of a finite number of random variables there exists a finite non-zero probability only if $\tau \le \tau_{max}$. For example a bandlimited channel is bounded but shows a Gaussian Distribution below its maximum. See Annex 2.C.4.8 for an explanation concerning extrapolation.

2.C.4.3 Annex - High Probability Jitter

We define a dual Dirac distribution function for a High Probability jitter (W) as below

$$HPJ(\tau, W) = \frac{\delta(\tau - \frac{W}{2})}{2} + \frac{\delta(\tau + \frac{W}{2})}{2}$$

2.C.4.4 Annex - Total Jitter

We define the convolution of the High Probability and Gaussian jitter as being the total jitter and define it as below.

$$TJ(\tau, W, \sigma) = \frac{1}{2\sqrt{2\pi}} \cdot \frac{1}{\sigma} \cdot \left[e^{-\frac{\delta\left(\tau - \frac{W}{2}\right)^2}{2\sigma^2}} + e^{-\frac{\delta\left(\tau + \frac{W}{2}\right)^2}{2\sigma^2}} \right]$$

1. Due to its bounded nature the function does not comply with the requirement that the integral of the PDF from minus infinity to infinity is one. This small inaccuracy is recognized and accepted in this context.

2.C.4.5 Annex - Probability Distribution Function vs. Cumulative Distribution Function

An example of the convolution of GJ (magenta), HPJ (green) to give TJ (red) can be seen Figure 2-15. When integrating the probability distribution functions, same colors, we obtain the cumulative distribution function or half the bathtub, Figure 2-16.

Figure 2-15. Example of Total Jitter PDF

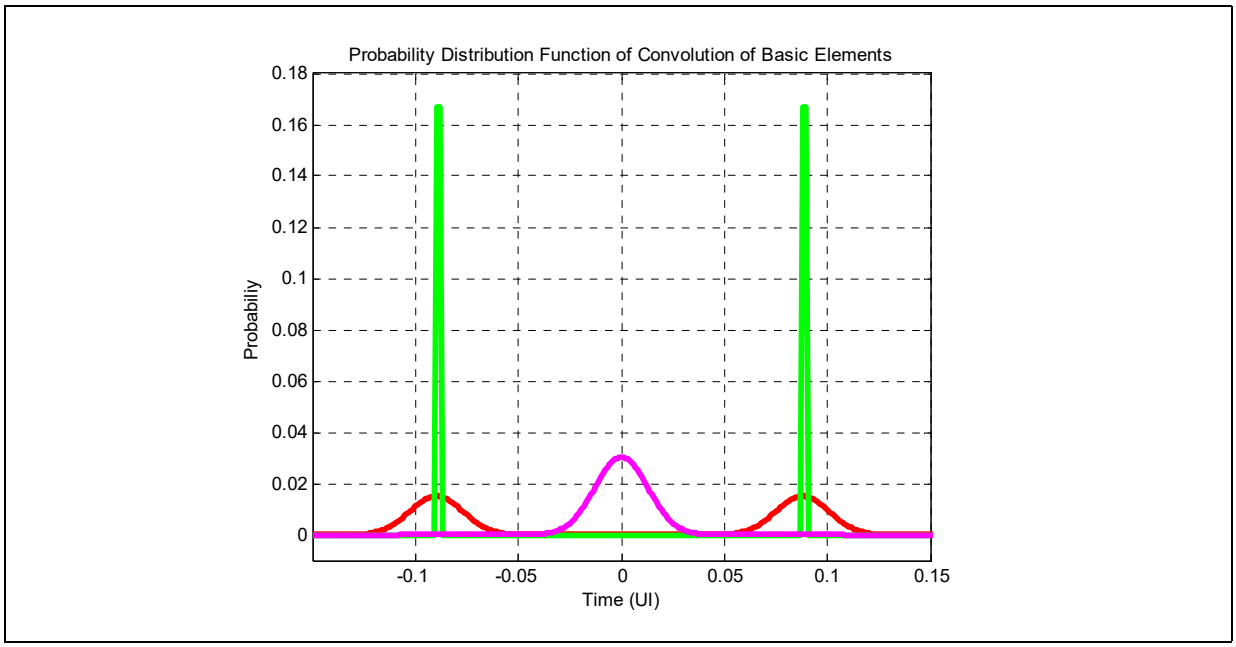
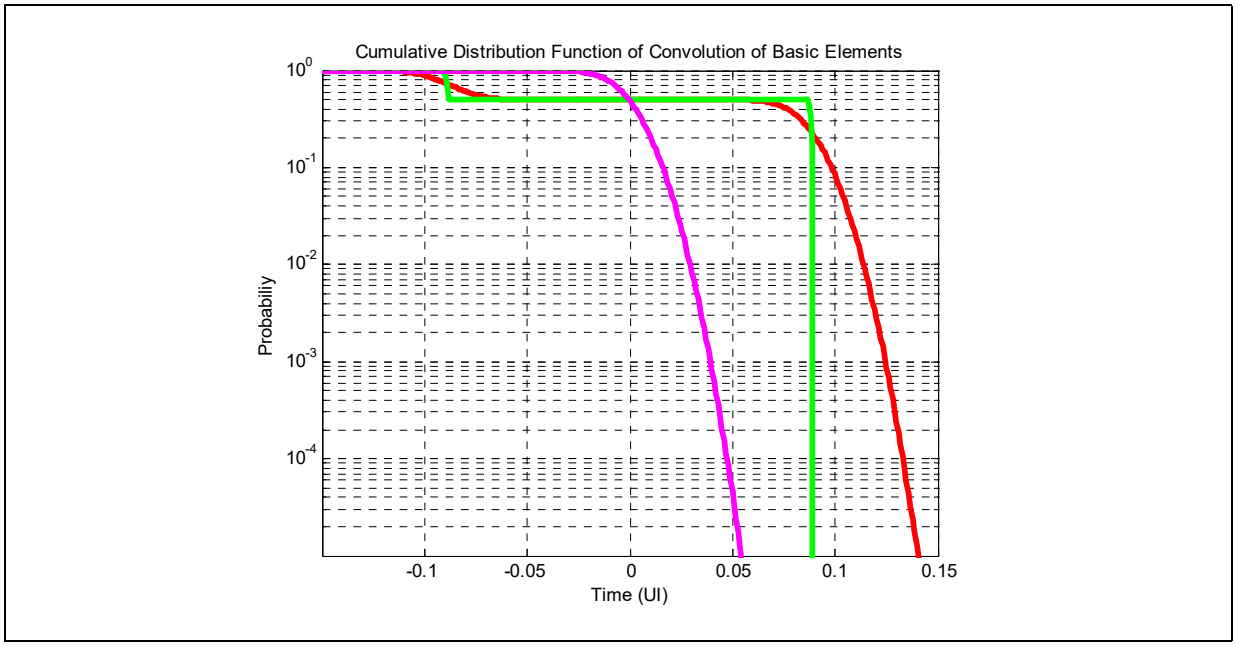


Figure 2-16. Example of Total Jitter CDF



2.C.4.6 Annex - BathTub

Given a measured bathtub curve consisting of measured BER for various sampling offsets, the defined Gaussian and High Probability Distributions can be used to describe the important features of the distribution.

Initially the BER axis should be converted to Q as defined below, e.g. a BER of 10^{-12} is a Q=7.04, and a BER of 10^{-15} a Q=7.94.[1]

$$Q = \sqrt{2} \cdot erf^{-1}(2 \cdot (1 - BER) - 1)$$

where

$erf^{-1}(x)$ is the inverse function of the error function $erf(x)$ and

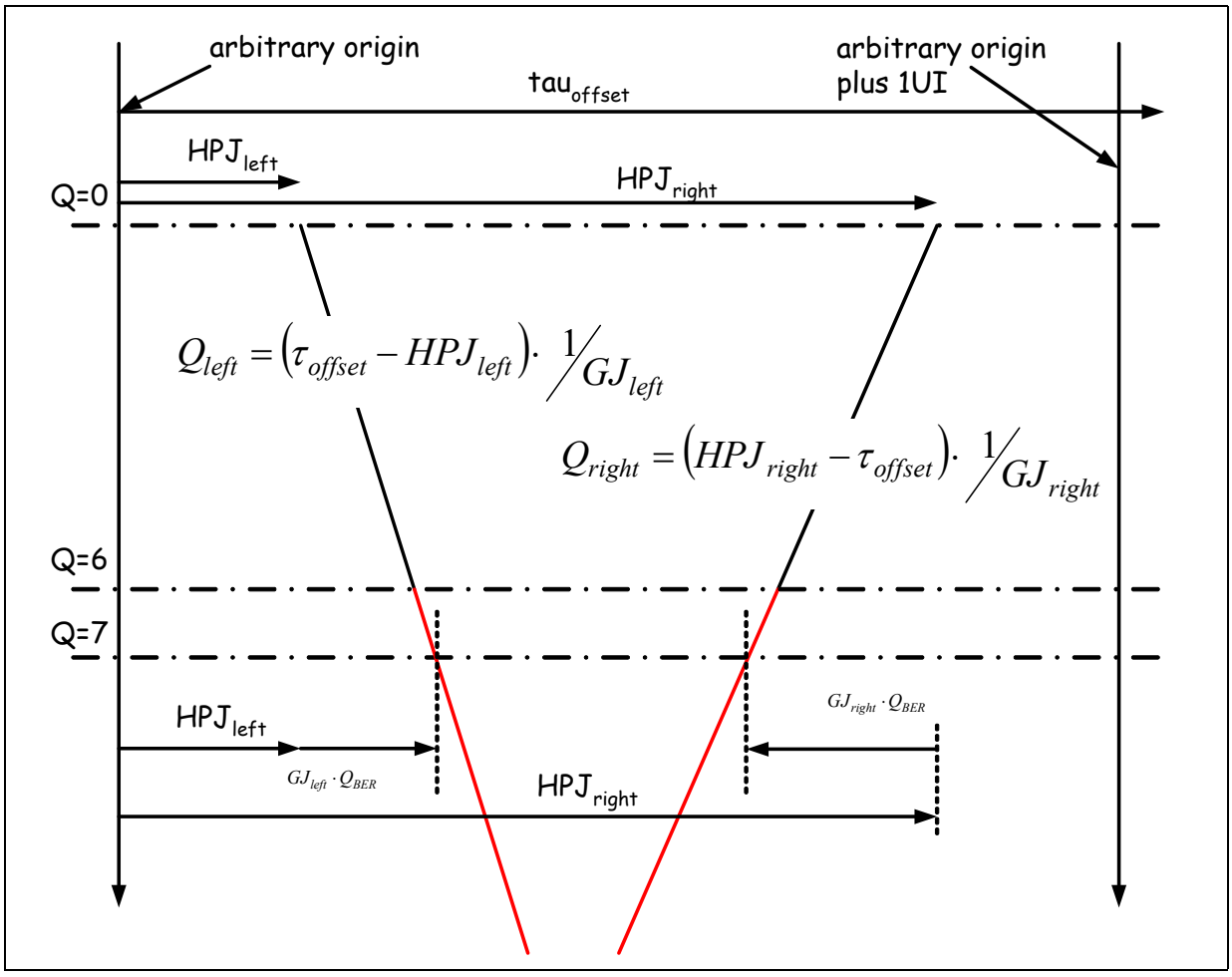
$$erf(z) = \frac{2}{\sqrt{\pi}} \cdot \int_0^z e^{-t^2} dt$$

Note: this conversion from BER to Q is only valid given a large time offset from the optimal sampling point. The use of the nomenclature BER in this reference should therefore be carefully used. Any accurate prediction of the BER towards the centre of the eye should be done using Marcum's Q function, and is outside the scope of this document.

1. It is assumed that when measuring the jitter bathtub that the left and right parts of the bathtub are independent to each other, e.g. the tail of the right hand part of the bathtub and negligible effect on the left hand side of the bathtub.

By linearising the bathtub, Figure 2-17, we can describe the function of the left and

Figure 2-17. Bathtub Definition



right hand linear parts of the bathtub in terms of an offset (HPJ) and gradient (1/GJ)

$$Q_{left}(\tau_{offset}) = (\tau_{offset} - HPJ_{left}) \cdot \frac{1}{GJ_{left}}$$

$$Q_{right}(\tau_{offset}) = (HPJ_{left} - \tau_{offset}) \cdot \frac{1}{GJ_{right}}$$

The conversion to a linearised bathtub from a measurement should be calculated using a polynomial fit algorithm for parts of the measurement made at low BERs or high Q.

2.C.4.7 Annex - Specification of GJ and HPJ

In Implementation Agreements the left and right hand terms are combined to give a single definition as below.

$$HPJ_{total} = 1 - (HPJ_{right} - HPJ_{left})$$

$$GJ_{total} = GJ_{left} \cdot Q_{BER} + GJ_{right} \cdot Q_{BER} = 2Q_{BER} \cdot GJ_{rms}$$

$$GJ_{rms} = \frac{GJ_{left} + GJ_{right}}{2}$$

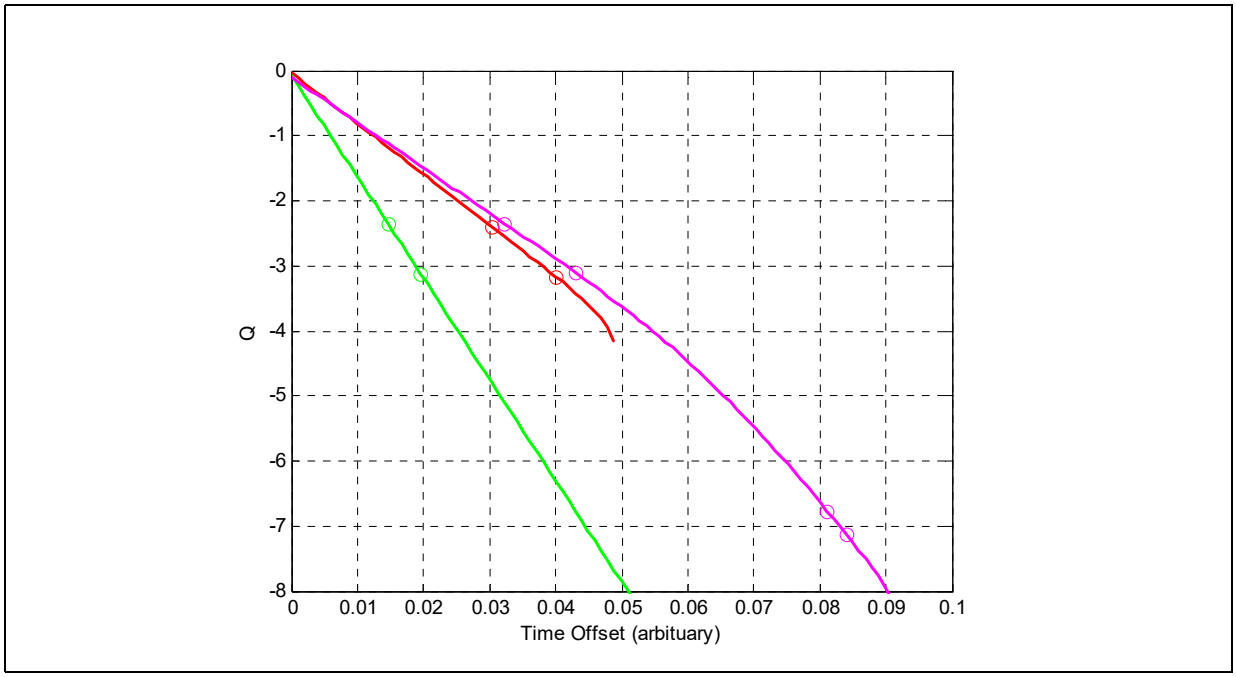
$$J_{total} = GJ_{total} + HPJ_{total}$$

where Q_{BER} is the Q for the BER of interest, e.g Q=7.04 for a $BER = 10^{-12}$

2.C.4.8 Annex - Example of Bounded Gaussian

Assuming that the Cumulative Distribution Function of the jitter could be measured to the probabilities shown, Figure 2-18 shows an example of when a jitter should be classified as Correlated High Probability or Correlated Bounded Gaussian..

Figure 2-18. Example of Bounded Gaussian



The convolution of a true Unbounded Gaussian Jitter (green) with a Bounded Gaussian Jitter (Red) can be seen (Magenta). It can be clearly seen and measured that at a Q of -3 the Bounded Jitter is still Gaussian and the resulting convolution can be calculated

using RMS addition. Below a Q of -5 the Bounding effect can be seen, and if we linearize the Bathtub we measure a non-zero High Probability Jitter and Gaussian component.

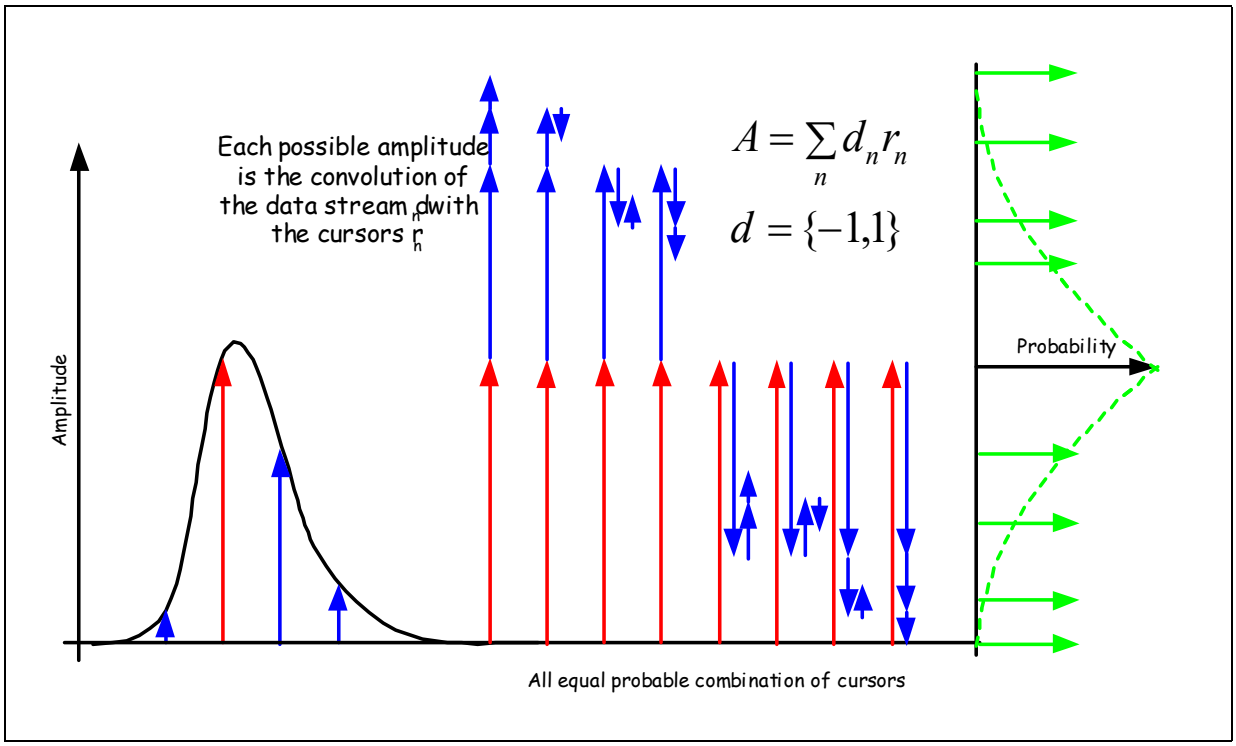
2.C.5 Annex - Statistical Eye Methodology

The following section describes the fundamental underlying the StatEye methodology. For a golden implementation please refer to the scripts on the OIF website, which are published separately, and to the appropriate appendix in this document for the compliance template.

2.C.5.1 Annex - Derivation of Cursors and Calculation of PDF

The Statistical Eye Methodology uses a channel pulse response and crosstalk pulse response in conjunction with a defined sampling jitter to generate an equivalent eye which represents the eye opening as seen by the receiver for a given probability of occurrence.

Figure 2-19. Statistics of Pulse Response Cursor

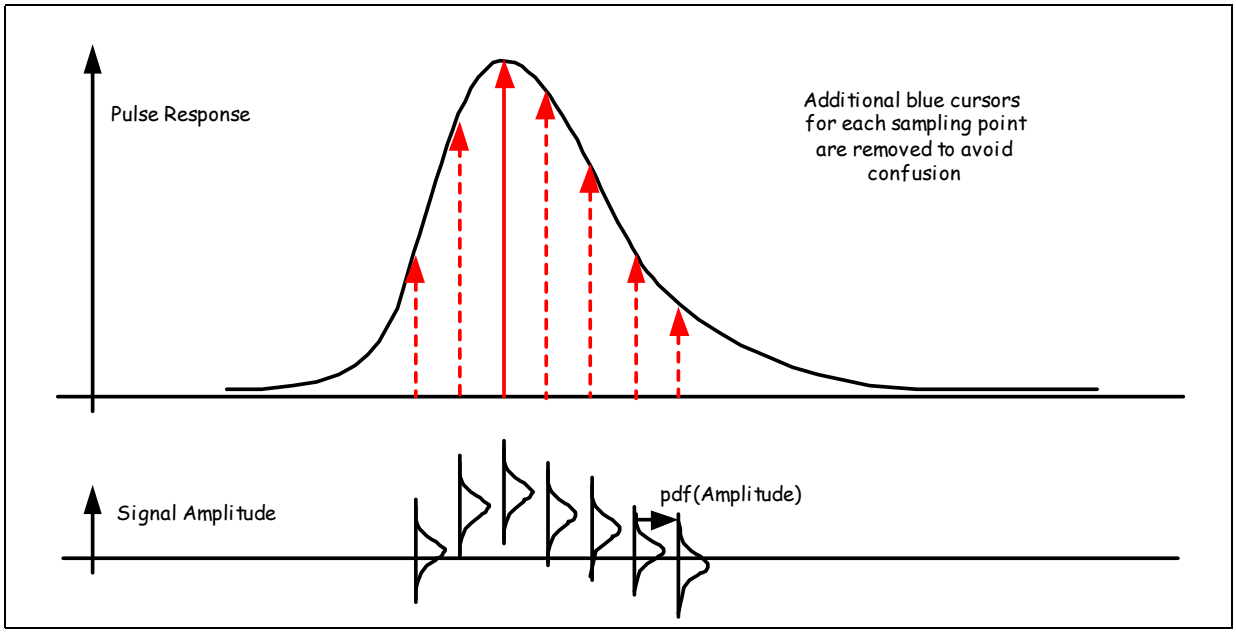


Given a pulse response (black left), Figure 2-19, we locate c_0 at an arbitrary point (red arrow), and measure the symbol space cursors (blue arrows)

Given a DFE the post cursors should be adjusted by negating the measured post cursors by the appropriate static coefficient of the DFE, up to the maximum number of cursors specified.

According to the exact data pattern these cursors superimpose to Inter-symbol Interference. Each possible combination of these cursors is calculated and from these combinations a histogram is generated to form the probability density function (PDF) (green).

Figure 2-20. Variation of the c0 sampling time



By varying the reference sampling point for c0, Figure 2-20, the previous function is repeated and family of conditional PDFs build up, which can be represented mathematically below.

Given,

$r_n(\tau)$ are the cursors of the pulse response at sampling τ

e_b is the ideal static equalization coefficients of the b tap DFE

$c(\tau)$ is the set of equalization cursors at sampling τ

$\delta(\tau) = \lim_{\varepsilon \to 0} \varepsilon |x|^{\varepsilon - 1}$ is the Dirac or delta function

$d_{n,\,b}$ are all the possible combinations of the data stream and is either 1 or 0

$p(ISI, \tau)$ is the probability density function of the ISI for a given sample time

$$c(\tau) = \left[r_{-\frac{m}{2}}(\tau) \ \ldots \ r_{-1}(\tau) \ r_1(\tau) - e_1 \ \ldots \ r_b(\tau) - e_b \ r_{b+1}(\tau) \ \ldots \ r_{\frac{m}{2}}(\tau) \right]$$

$$d = \begin{bmatrix} d_{1,\,1} & d_{1,\,\ldots} & d_{1,\,m} \\ d_{\ldots,\,1} & d_{\ldots,\,\ldots} & d_{\ldots,\,m} \\ d_{2^m,\,1} & d_{2^m,\,\ldots} & d_{2^m,\,m} \end{bmatrix}$$

$$n = \sum_{b\,=\,[1,m]} d_{n,\,b} \cdot 2^{b-1} + 1$$

$$p(ISI, \tau) = \frac{1}{2^m} \sum_{n\,=\,[1,2^m]} \delta(c(\tau) \cdot (2d_n' - 1) - ISI)$$

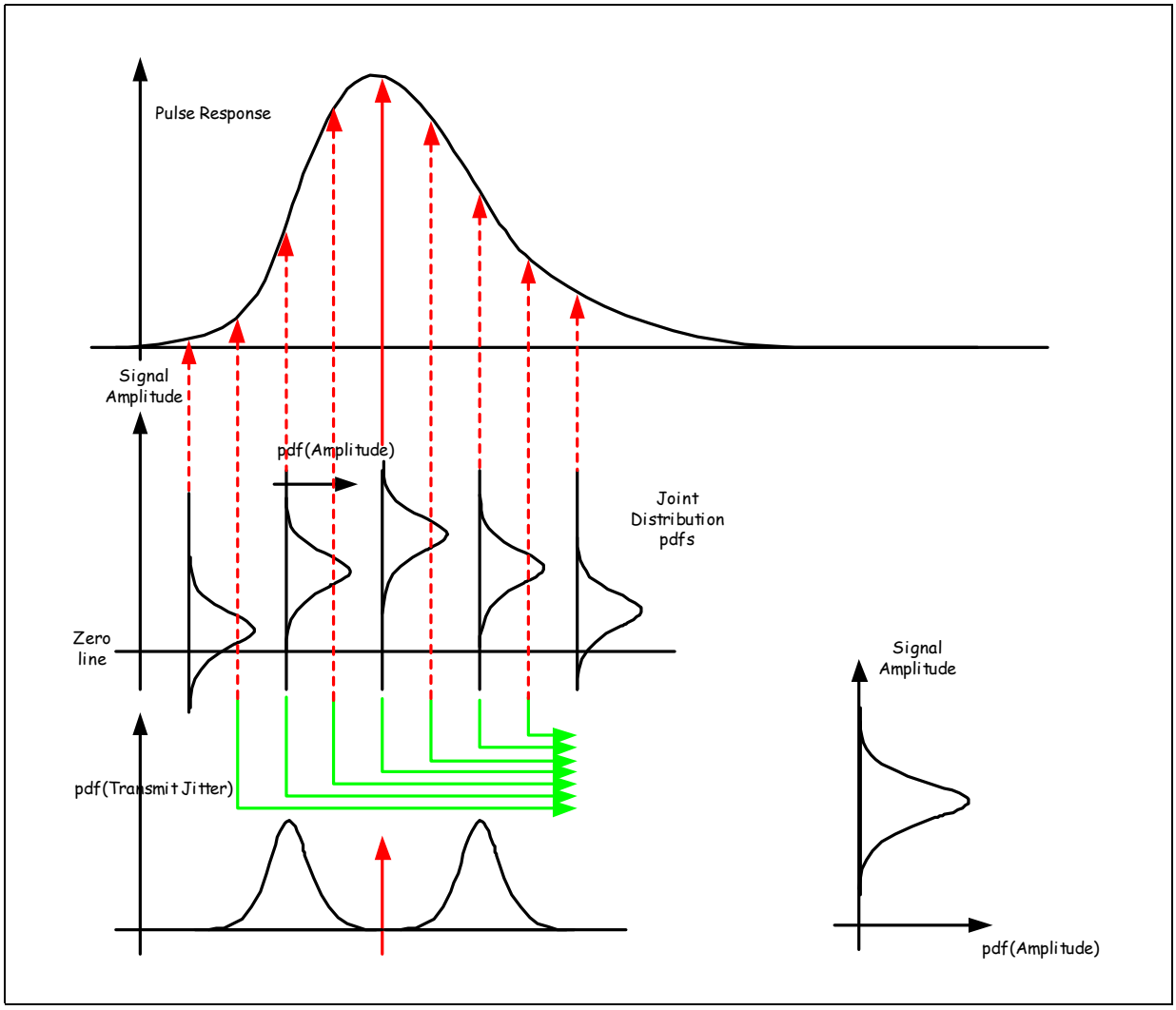
A similar family of PDFs are generated for the crosstalk pulse response and any other aggressors in the system using the cursor set below, noting that the entire pulse response is used

$$c(\tau) = \left[r_{-\frac{m}{2}}(\tau) \ \ldots \ r_{-1}(\tau) \ r_0(\tau) \ r_1(\tau) \ \ldots \ r_{\frac{m}{2}}(\tau) \right]$$

2.C.5.2 Annex - Inclusion of Sampling Jitter

In a real system the sampling point c0 is defined by the CDR and is jittered, for the sake of standardization, by the transmitter. This jitter has a probability density function which is centered at the receiver CDR sampling point and defines the probability of each of the previous conditional PDFs occurring[1].

Figure 2-21. Varying the Receiver Sampling Point



By multiplying each of the conditional PDFs by its associated sampling jitter probability and summing their results together, the joint probability density function at the given receiver CDR sample point can be calculated, Figure 2-21.

1. Currently DCD effects are not taken into account

Given,

$p_{jitter}(\tau, w, \sigma)$ is the dual Dirac probability density function of the sampling jitter in the system, as defined in Annex 2.C.4.4

$p_{crosstalk}(ISI, \tau)$ is the probability density function of the crosstalk

$p_{forward}(ISI, \tau)$ is the probability density function of the ISI of the forward channel

$a \otimes b$ is the convolution operative

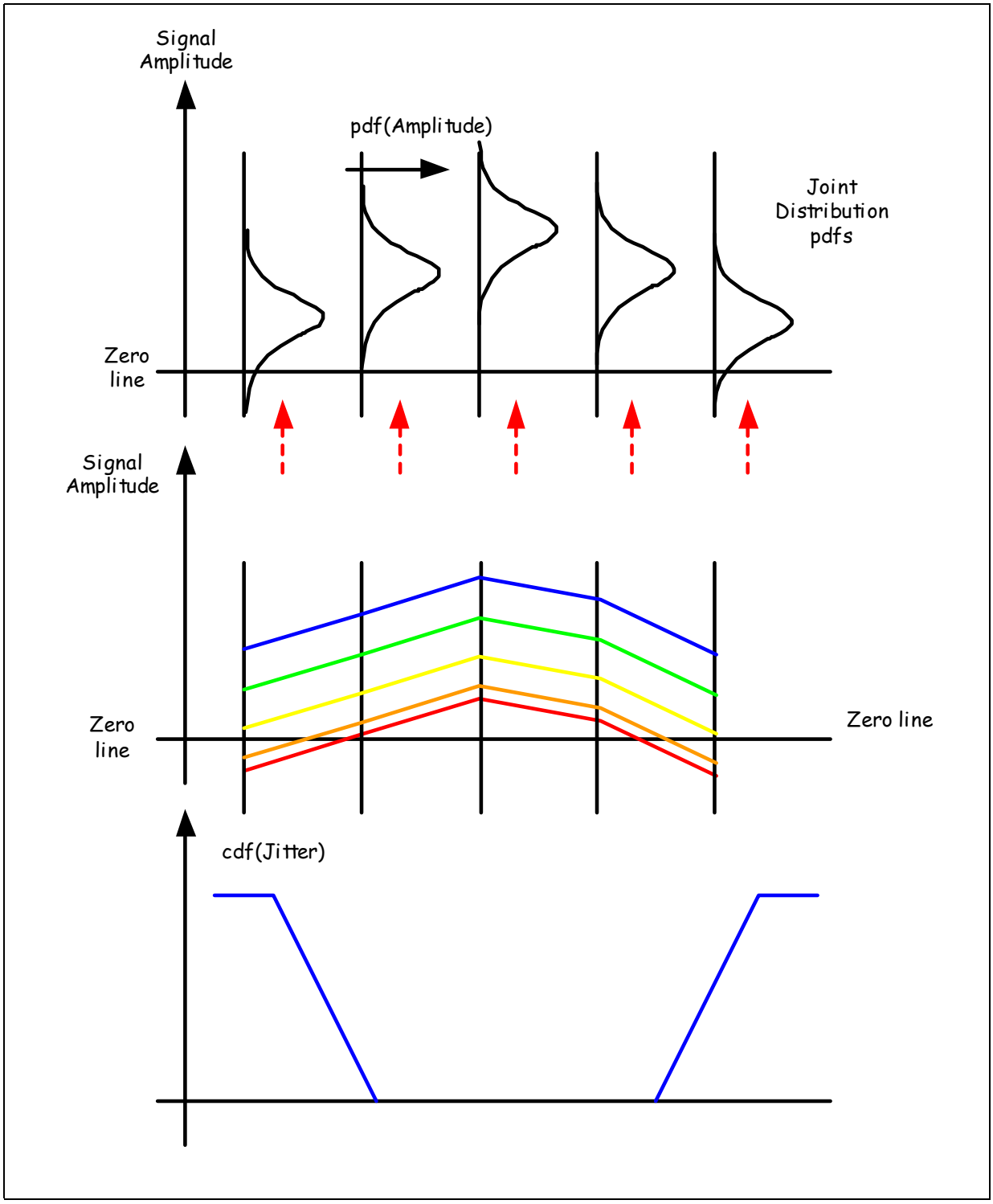
$$p_{average}(ISI, \tau) =$$

$$\int_{-\infty}^{\infty} \{[p_{crosstalk}(ISI, \tau + \upsilon + w) \otimes p_{forward}(ISI, \tau + \upsilon)] \cdot p_{jitter}(\upsilon, w, \sigma)\} d\upsilon$$

2.C.5.3 Annex - Generation of Statistical Eye

By varying the receiver CDR sampling point a new joint probability density function, Figure 2-21 can be generated.

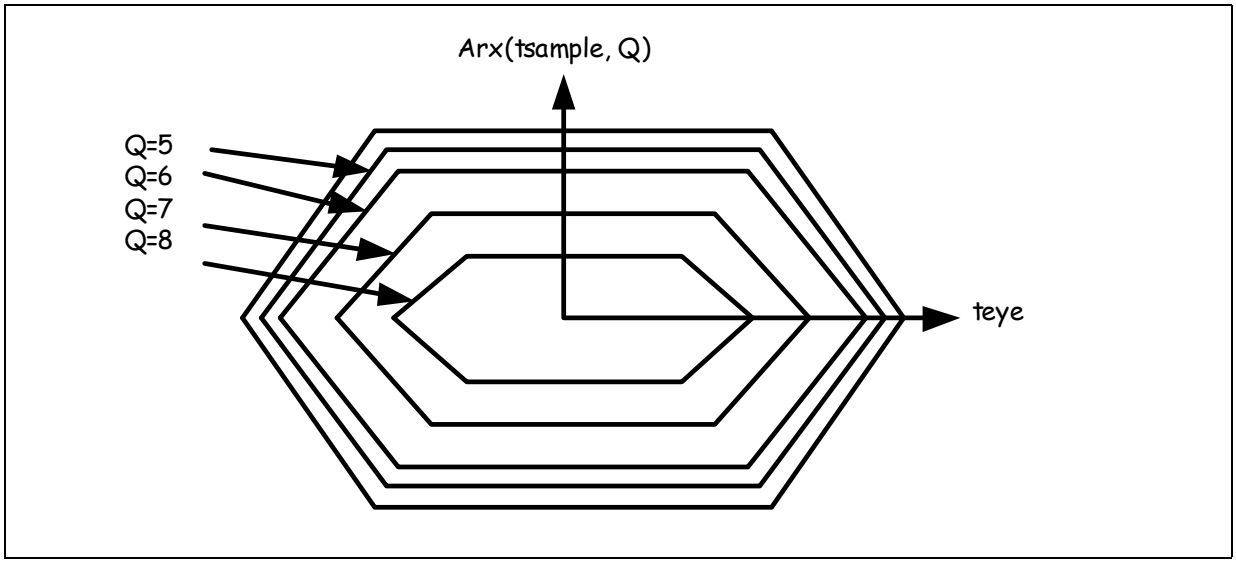
Figure 2-22. Generation of the Data Eye and Bathtub



By integrating the Joint Probability Density Function to give the Cumulative Distribution function, and creating a contour plot an equivalent of the receiver eye can be generated which shows the exact probability of obtaining a given amplitude, Figure 2-22, this equivalent eye is termed the statistical eye, Figure 2-23

By only plotting the probability against time by cutting the statistical Eye along the decision threshold axis, a bathtub of the jitter can be generated,Figure 2-22.

Figure 2-23. Statistical Eye



2.D Annex - Definition of CEI Test Patterns

2.D.1 Annex - PRBS31

The pattern is a free running PRBS31 polynomial in accordance with [21.]. The sequence is generated using taps 28 and 31.

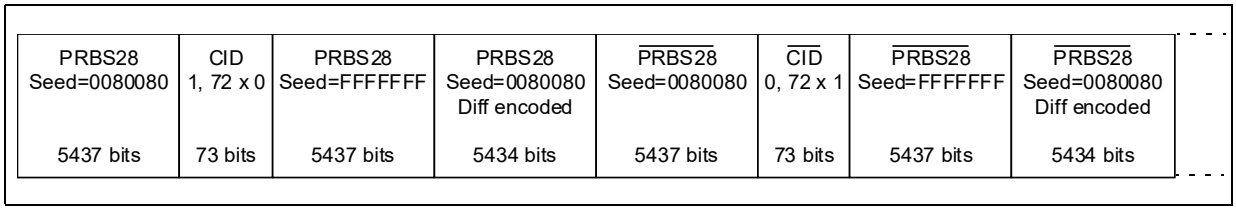
2.D.2 Annex - Short Stress Pattern Random (SSPR)

The SSPR pattern was chosen to have baseline wander and timing content that are at least as stressful as 10,000 years of random binary.

- The baseline wander was assessed with a cut-off frequency of baudrate/10,000.
- The clock content was assessed with a corner frequency of baudrate/1667.
- The period of 10,000 years was chosen on the basis of random binary exceeding the baseline wander timing content limits of the short pattern once in 10 years in a network containing 1000 random streams.

The SSPR pattern is defined as:

Figure 2-24. Short Stress Pattern Random (SSPR)



- Total length 32,762 bits
- All 2^{28}-1 PRBS28 sequences are generated using taps 25 and 28
- Block 1 is 5437 bits of PRBS28 seed = 0x0080080 and begins with 8 x 0, 1, 11 x 0, 1, 12 x 0, 1...
- Block 2 is 1 followed by 72 x 0
- Block 3 is 5437 bits of PRBS28 seed = 0xFFFFFFF and begins with 28 x 1, 25 x 0, 3 x 1, 22 x 0...
- Block 4 takes the same sequence as block 1 (omitting the last 3 bits) and encodes it as follows:
  - — A zero causes a change of output
  - — A one causes no change of output
  - — The output before the first bit is assumed to have been zero
  - — This block begins 10101010010101010101101010101011011010...
- Blocks 5 to 8 are the inverse of blocks 1 to 4 respectively.

Under some circumstances (e.g. to accommodate the restrictions of some pieces of test equipment) it may be desirable to modify this short pattern to have a total length of 32,768 bits (2^{15}) rather than 32,762 bits. To make use of this option, the differentially encoded blocks (blocks 4 and 8) should be extended by 3 bits making these blocks 5437 bits long.

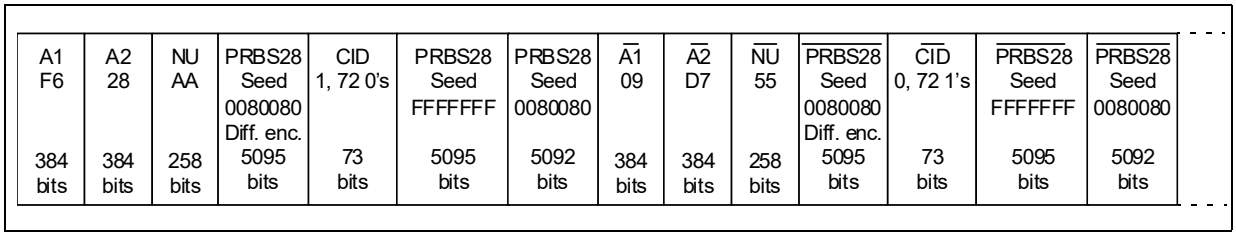
2.D.3 Annex - Short Stress Pattern SDH 16 (SSPS-16)

The SSPS-16 pattern was chosen to have baseline wander and timing content that are at least as stressful as 10,000 years of STM-16 framed random binary.

- The baseline wander was assessed with a cut-off frequency of baud/10,000.
- The clock content was assessed with a corner frequency of baudrate/1667.
- The period of 10,000 years was chosen on the basis of STM-16 framed random binary exceeding the baseline wander and timing content limits of the short pattern once in 10 years in a network containing 1000 STM-16 framed streams.

The SSPS-16 pattern is defined as:

Figure 2-25. Short Stress Pattern SDH 16 (SSPS-16)



- Total length 32,762 bits
- All 2^{28}-1 PRBS28 sequences are generated using taps 25 and 28
- Block 1 is A1 (11110110) repeated 48 times to give 384 bits
- Block 2 is A2 (00101000) repeated 48 times to give 384 bits
- Block 3 is the National Use bits and consists of 1010 repeated for 258 bits
- Block 4 takes 5095 bits of PRBS28 seed = 0x0080080 and encodes it as follows:
  - — A zero causes a change of output
  - — A one causes no change of output
  - — The output before the first bit is assumed to have been zero
  - — This block begins 10101010010101010101101010101011011010 ...
- Block 5 is 1 followed by 72 x 0
- Block 6 is 5095 bits of PRBS28 seed = 0xFFFFFFF and begins 28 x 1, 25 x 0, 3 x 1, 22 x 0 …
- Block 7 is 5092 bits of PRBS28 seed = 0x0080080 and begins with 8 x 0, 1, 11 x 0, 1, 12 x 0, 1 …

- Blocks 8 to 14 are the inverse of 1 to 7 respectively.

Under some circumstances (e.g. to accommodate the restrictions of some pieces of test equipment) it may be desirable to modify this short pattern to have a total length of 32,768 bits (2^{15}) rather than 32,762 bits. To make use of this option, the last block in each half (blocks 7 and 14) should be extended by 3 bits making these blocks 5095 bits long.

2.D.4 Annex - Short Stress Pattern SDH 64 (SSPS-64)

The SSPS-64 pattern was chosen to have baseline wander and timing content that are at least as stressful as 10,000 years of STM-64 framed random binary.

- The baseline wander was assessed with a cut-off frequency of baud/10,000.
- The clock content was assessed with a corner frequency of baudrate/1667.
- The period of 10,000 years was chosen on the basis of STM-64 framed random binary exceeding the baseline wander and timing content limits of the short pattern once in 10 years in a network containing 1000 STM-64 framed streams.

The SSPS-64 pattern is defined as:

Figure 2-26. Short Stress Pattern SDH 64 (SSPS-64)

A1 F6 1536 bits	A2 28 1536 bits	NU AA 1026 bits	PRBS28 Seed 0080080 Diff. enc. 4071 bits	CID 1, 72 0's 73 bits	PRBS28 Seed FFFFFFF 4071 bits	PRBS28 Seed 0080080 4068 bits	$\overline{A1}$ 09 1536 bits	$\overline{A2}$ D7 1536 bits	$\overline{NU}$ 55 1026 bits	$\overline{PRBS28}$ Seed 0080080 Diff. enc. 4071 bits	$\overline{CID}$ 0, 72 1's 73 bits	$\overline{PRBS28}$ Seed FFFFFFF 4071 bits	$\overline{PRBS28}$ Seed 0080080 4068 bits

- Total length 32,762 bits
- All 2^{28}-1 PRBS28 sequences are generated using taps 25 and 28
- Block 1 is A1 (11110110) repeated 192 times to give 1536 bits
- Block 2 is A2 (00101000) repeated 192 times to give 1536 bits
- Block 3 is the National Use bits and consists of 1010 repeated for 1026 bits
- Block 4 takes 4071 bits of PRBS28 seed = 0x0080080 and encodes it as follows:
  - — A zero causes a change of output
  - — A one causes no change of output
  - — The output before the first bit is assumed to have been zero
- This block begins 10101010010101010101101010101011011010...
- Block 5 is 1 followed by 72 x 0
- Block 6 is 4071 bits of PRBS28 seed = 0xFFFFFFF and begins 28 x 1, 25 x 0, 3 x 1, 22 x 0 …

- Block 7 is 4068 bits of PRBS28 seed = 0x0080080 and begins with 8 x 0, 1, 11 x 0, 1, 12 x 0, 1 …
- Blocks 8 to 14 are the inverse of 1 to 7 respectively.

Under some circumstances (e.g. to accommodate the restrictions of some pieces of test equipment) it may be desirable to modify this short pattern to have a total length of 32,768 bits (2^{15}) rather than 32,762 bits. To make use of this option, the last block in each half (blocks 7 and 14) should be extended by 3 bits making these blocks 4071 bits long.

2.D.5 Annex - Use of CEI Test Patterns

The Test patterns required for the various electrical interfaces covered by CEI are specified in Table 2-1.

Table 2-1. Use of CEI Test Patterns

Electrical Requirement	"Method"	IA	Data	Test Patterns	
				Mandatory	Recommended
CEI Clause 4 (SxI-5)	A	SFI-4.2	Scrambled	PRBS31 or SSPR	
		Other	Scrambled	PRBS31 or SSPR	
		SPI-5	Scrambled	PRBS31 or SSPR	
		SFI-5.1	Partially scrambled	PRBS31 or SSPR	SSPR
		SFI-5.1s	Partially scrambled	PRBS31 or SSPR	SSPS-16
CEI Clause 5 (TFI-5)	B	TFI-5	Scrambled	PRBS31 or SSPR	
			Partially scrambled	PRBS31 or SSPR	SSPS-16
CEI Clause 6 (CEI-6G-SR)	B	TDM-P	Scrambled	PRBS31 or SSPR	
		CEI-P	Scrambled	PRBS31 or SSPR	
		Other	Scrambled	PRBS31 or SSPR	
		Other	Partially scrambled	PRBS31 or SSPR	SSPS-16
CEI Clause 7 (CEI-6G-LR)	D	TDM-P	Scrambled	PRBS31 or SSPR	
		CEI-P	Scrambled	PRBS31 or SSPR	
		Other	Scrambled	PRBS31 or SSPR	
		Other	Partially scrambled	PRBS31 or SSPR	SSPS-16
CEI Clause 8 (CEI-11G-SR)	E	TDM-P	Scrambled	PRBS31 or SSPR	
		CEI-P	Scrambled	PRBS31 or SSPR	
		SFI5.2	Scrambled	PRBS31 or SSPR	
		Other	Scrambled	PRBS31 or SSPR	
		Other	Partially scrambled	PRBS31 or SSPR	SSPS-64
CEI Clause 9 (CEI-11G-LR/MR)	E for 11G-MR	TDM-P	Scrambled	PRBS31 or SSPR	
		CEI-P	Scrambled	PRBS31 or SSPR	
	C&D without Tx emphasis for 11G-LR	Other	Scrambled	PRBS31 or SSPR	
		Other	Partially scrambled	PRBS31 or SSPR	SSPS-64

Table 2-1. Use of CEI Test Patterns

Electrical Requirement	"Method"	IA	Data	Test Patterns	
				Mandatory	Recommended
CEI Clause 10 (CEI-28G-SR)	C	Other	Scrambled	PRBS9 for DDJ & Tx emphasis, otherwise SSPR	
CEI Clause 11 (CEI-25G-LR)	D	Other	Scrambled	PRBS9 for DDJ & Tx emphasis, otherwise SSPR	
CEI Clause 13 (CEI-28G-VSR)	-	Other	Scrambled	PRBS9 for eye, otherwise PRBS31	
CEI Clause 14 (CEI-28G-MR)	C	Other	Scrambled	PRBS9 for DDJ & Tx emphasis, otherwise SSPR	
CEI Clause 16 (CEI-56G-VSR-PAM4)	-	Other	Scrambled	For PAM-4 see Appendix 16.C.3	
CEI Clause 17 (CEI-56G-MR-PAM4)	-	Other	Scrambled	For PAM-4 see Appendix 16.C.3	
CEI Clause 18 (CEI-56G-USR-NRZ)	E	Other	Scrambled	PRBS9 for DDJ, otherwise SSPR	
CEI Clause 19 (CEI-56G-XSR-NRZ)	E	Other	Scrambled	PRBS9 for DDJ, otherwise SSPR	
CEI Clause 20 (CEI-56G-XSR-PAM4)	-	Other	Scrambled	For PAM-4 see Appendix 16.C.3	
CEI Clause 21 (CEI-56G-LR-PAM4)	-	Other	Scrambled	For PAM-4 see Appendix 16.C.3	
CEI Clause 22 (CEI-56G-LR-ENRZ)	-	Other	Scrambled	For ENRZ see Appendix 22.A.5	
CEI Clause 24 (CEI-112G-XSR-PAM4)	-	Other	Scrambled	For 112G PAM-4 see Appendix 16.C.3, Appendix 25.G	
CEI Clause 25 (CEI-112G-VSR-PAM4)	-	Other	Scrambled	For 112G PAM-4 see Appendix 16.C.3, Appendix 25.G	
CEI Clause 26 (CEI-112G-MR-PAM4)	-	Other	Scrambled	For 112G PAM-4 see Appendix 16.C.3, Appendix 25.G	
CEI Clause 27 (CEI-112G-LR-PAM4)	-	Other	Scrambled	For 112G PAM-4 see Appendix 16.C.3, Appendix 25.G	
CEI Clause 28 (CEI-112G-XSR+-PAM4)	-	Other	Scrambled	For 112G PAM-4 see Appendix 16.C.3, Appendix 25.G	

2.D.6 Annex - Text Definitions of Patterns

Below are definitions of the patterns described in Annex 2.D.2, Annex 2.D.3 and Annex 2.D.4 as hexadecimal digits with the most significant bit of each digit transmitted first. Since these patterns are 32,762 bits long (which is not divisible by 4), the two least significant bits of the last digit shown are not included in the sequence.

Short Stress Pattern Random (SSPR)

```
008008004804802082081249248800000C8000068800032C8001A48800C80C8068868832CB2C
9A49248480000A080005A480028808016C8480A08A085A4DA4A882081EC9248E88000FAC8007
2C8803E48C81CC0E88FAC7ACF2CFACB64B2C90412481248008800804C8048228820936C92408
0800448480260A081165A489A4880C480C86E0868B1E4B2D3EC1244C8C80628E88376FAC98C1
2C85EC848AA88A0DFECDA6208A09724DA42E020855E124AFAE801D2DA80F440E875647ABDE47
AF52C7AD5C4FAC7BE32CFA4FA4B283281269A68812492C8800048C80020E880127AC8081AC88
48CC8CA0EA8E9A7BEFA49A492804800682080329248 1A60008C96004E826023A91613EE1A68C
9EC92E868805AB2C828F24896F600C214606D2B7630470C7B27F6FA218412B2DA48724080BE0
44854E260AF3F165D6C7A4B60FA810672E8935E5AC09AC8CC44C8EAE628FBDD76F2536C160C8
0CA668869952CB253C4920CDE0026A2E0113B5E098E1AE45FECDC6A08A3F3A4DBC6E8205F1A9
22A7CE03799BE18B544EDD1F63835E47F99AC78354CFB99F2B27566721DE55E2F2CFAF564B2D
5E41247AC4807ACE083ACBE49EC94C068832C32C9A4DA48482080A092485A4000A884005ECA4
02A898417EC5A4A88E881ECFAC8E8B2C8FAD248F2C400F64E407443C43D65DE5D64B2CB64124
904480012608008164804 8A40820D8449261A60016C9600A082605A491628801A76C80C9C088
687C4CB2B9E292776F601CC1460FACB7672C90C5E4816EAC08A1BCC4DAC5AE20CE8DF26BAE26
136DF1688027A2C811AB4889CF10CC7B796AFA0B23D2A523D478C3D77BEDD6CA483609809864
5845B469A681724928AE0006DDE003032E01B1A5E0C3C8AE6DD8DDD031E3351BEFA9DC492E73
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FC13C851C8D8ADF8E1DC23FEF3D3C096D4DC420723E523E3CCC3CFDAADDB10FC303971DB1F2F
F03E65071CD4D3FFA724C029E02C166E14CA51EB298DEB265E2B214AF722B1D4E373F73F8EC4
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Short Stress Pattern SDH 16 (SSPS-16)

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2828282828282828282828282828282828282828AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA
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```
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Short Stress Pattern SDH 64 (SSPS-64)

F6F6F6

```
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6C6FE2EF0EF0A68868A6D34D26FB6DBEEDFFFB67DFFDFA6DFEDD6FDF7C8
```

2.E Appendix - Lab Setups

All methodology described in this Appendix is only relevant for verification of low level CDR functionality, and does not cover any required tests for protocol compliance e.g. deskew. The methodology is based on the assumption that either an integrated BERT is present in the DUT or a loop or functionality for the attachment of external equipment.

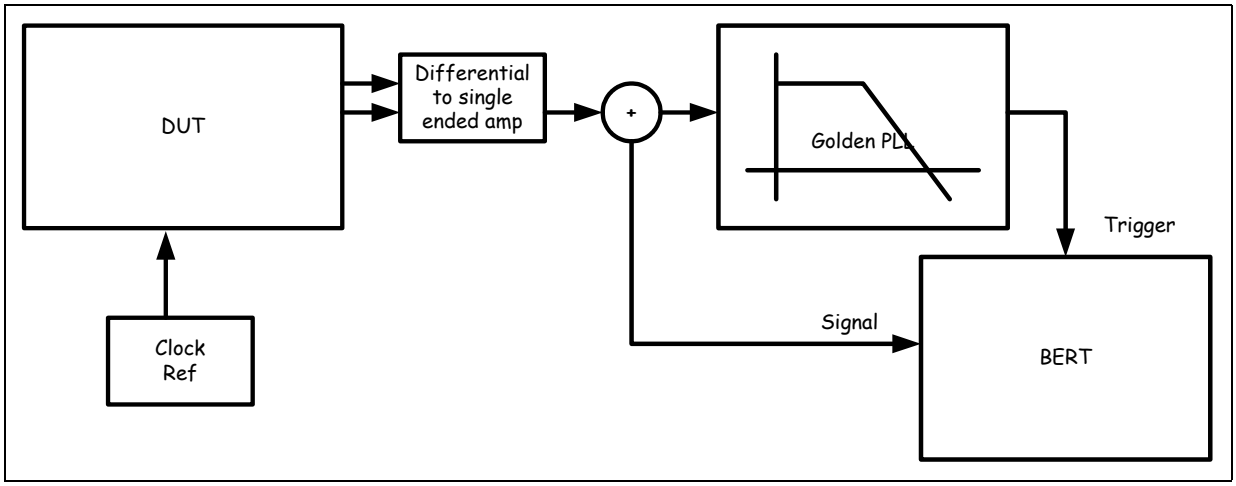
2.E.1 High Frequency Transmit Jitter Measurement

The following sub-clause describes various methods for measuring high frequency jitter, which depending upon the baud rate can be applied for various levels of accuracy.

2.E.1.1 BERT Implementation

Referring to Figure 2-27, this sub-clause describes test methodology based on bathtub extraction, which relies on equipment being available for the given baud rate.

Figure 2-27. BERT with Golden PLL



- This same methodology can be used by equalized transmitters, by initially turning the equalization off, or by performing the measurement at the output of a **Stress Channel**.
- The transmitter under test shall transmit the specified data pattern, while all other signals are active.
  - The other channels can transmit the same pattern if they have at least a 16 bit offset with the channel under test.
  - All links within a device under test to be active in both transmit and receive directions, and receive links are to use asynchronous clocks with respect to transmit links (to maximum allowed ppm. offset as specified in the protocol specifications).
- The data should be differentially analysed using an external differential amp or differential input BERT and Golden PLL.

— Use of single ended signals will give an inaccurate measurement and should not be used.

— The use of a balun will most likely degrade the signal integrity and is only recommended for 3Gsym/s signalling when the balun is linear with a return loss of better than -15dB until three times the baud rate.

- Inherent bandwidth of clock reference inputs of BERT should be verified e.g. in the case of parBERTs. Additional bandwidth limitation of the BERT will lead to inaccurate results.
- The use of a Golden PLL is required to eliminate inherent clock content (Wander) in transmitted data signals for long measurement periods.

  — The Golden PLL should have at maximum a bandwidth of baud rate over 1667, with a maximum of 20dB/dec rolloff, until at least baud rate over 16.67, with no peaking around the corner frequency.
- The output jitter for the DUT is not defined as the contributed jitter from the DUT but as the total output jitter including the contributions from the reference clock. To this end, the reference clock of the DUT should be verified to have a performance similar to the real application.
- a confidence level of three sigma should be guaranteed in the measurement of BER for the Bathtub as per Appendix 2.F.2.[1]
- The High Probability and Gaussian Jitter components should be extracted from the bathtub measurement using the methodology defined in Annex 2.C.4.6.
- If not defined the maximum Gaussian jitter is equal to the maximum total jitter minus the actual High Probability jitter.

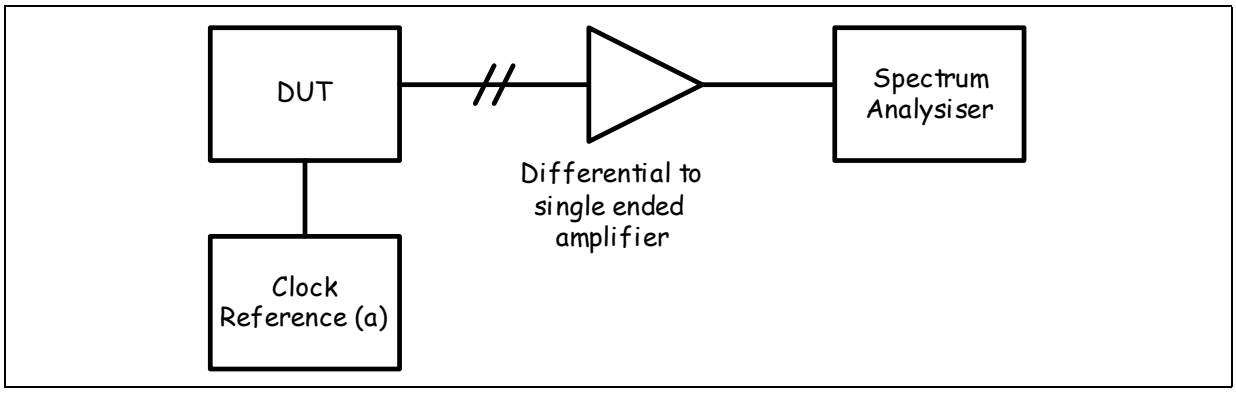
2.E.1.2 Spectrum analyzer and Oscilloscope Methodology

Bandlimited[2] Unbounded Gaussian Noise

Referring to Figure 2-28, bandlimited or high frequency Gaussian noise can be measured at the transmitter of the DUT accurately using a high frequency 101010 pattern and measuring the spectral power[3].

1. It is assumed due to the magnitude of jitter present at the transmitter that the left and right hand parts of the bathtub are independent to each other
2. Normal CEI application will integrate from the defined ideal CDR bandwidth to infinity, while some CEI-11G-SR application will integrate over a specific band
3. The spectral power should be measured using averaging

Figure 2-28. Spectral Measurement Setup[a]



a.The clock reference is such that its power noise represents the typical power noise of the reference in the system

The spectral power is calculating by integrating over the frequency band of interest and converting into time jitter.

$$\tau_{rms} = \frac{1}{2\pi}\sqrt{2 \cdot \int_{f_1/100}^{100f_2} \left| \frac{1/f_1 \cdot j \cdot f}{(1 + j \cdot f/f_1)(1 + j \cdot f/f_2)} \right| \cdot 10^{\frac{P(f)}{10}}}$$

where

τ_{rms} is the time jitter

$P(f)$ is the measured spectral power for 1Hz Bandwidth

It should be noted that the measured Gaussian noise for a driver can usually be considered equivalent to that derived from a full bathtub jitter distribution.

Bandlimited 60 second Total Jitter Measurements

In certain CEI-11G-SR applications total jitter measurements of 60 seconds are required. The Gaussian jitter, as measured above, should be multiplied by a Q of 6.96[1]. If spurs are present in the spectrum then these must be converted to time jitter separately using an inverse of the Bessel function as per Figure 2-29, which describes the power spectrum for a given phase modulated signal.

where

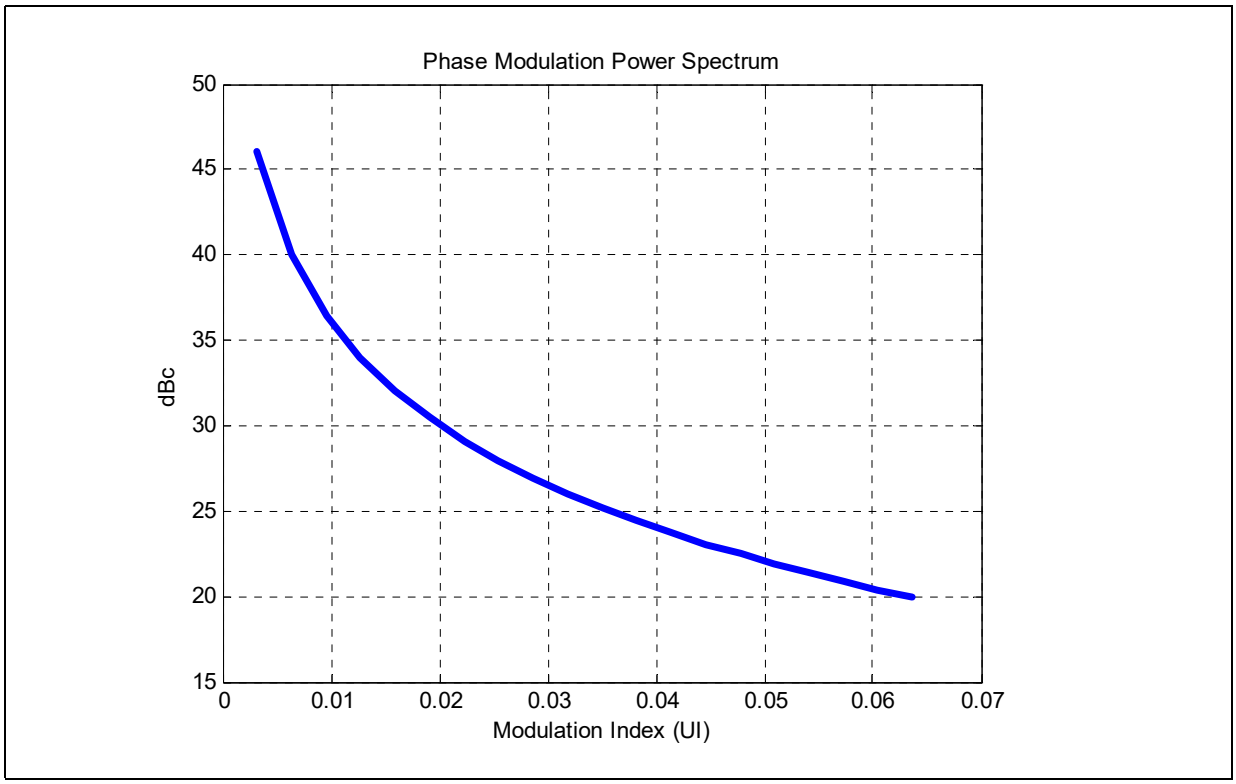
$F(P_n)$ is the inverse spectral SSB power to time modulation (below)

1. Traditional measurements are performed for 60 seconds using a demodulator and performing a real time peak to peak measurement of the jitter. Given this, the number of bits transmitter across the link in 60 seconds is calculated and the associated three sigma confidence level, peak to peak multiplication factor, Q, for the random jitter.

$$\tau_{pkpk} = 2Q\tau_{rms} + \sum_{n} F(P_n)$$

P_n is the relative SSB power of a spur

Figure 2-29. Single Side Band Relative Power Spectrum for Phase Modulated Signal



Uncorrelated High Probability Jitter

After measuring the Gaussian Jitter, as above, an oscilloscope measurement, as per Appendix 2.E.7, of the peak to peak jitter should be performed using a 101010 pattern.

The Uncorrelated High Probability Jitter is then calculated by removing the accumulated Unbounded Gaussian jitter.

$$\tau_{UBHJ} = \tau_{pkpk} - 2Q\tau_{rms}$$

using a Q calculated for a 3 sigma confidence level[1] as per Appendix 2.F.3.

1. It is recommended that enough samples on the oscilloscope should be made such that Q>4

Total High Probability Jitter

After measuring the Unbounded Gaussian Jitter, as above, an oscilloscope measurement, as per Appendix 2.E.7, of the peak to peak jitter should be performed using the standard pattern e.g. PRBS31.

The Total High Probability Jitter is then calculated by removing the accumulated Gaussian jitter.

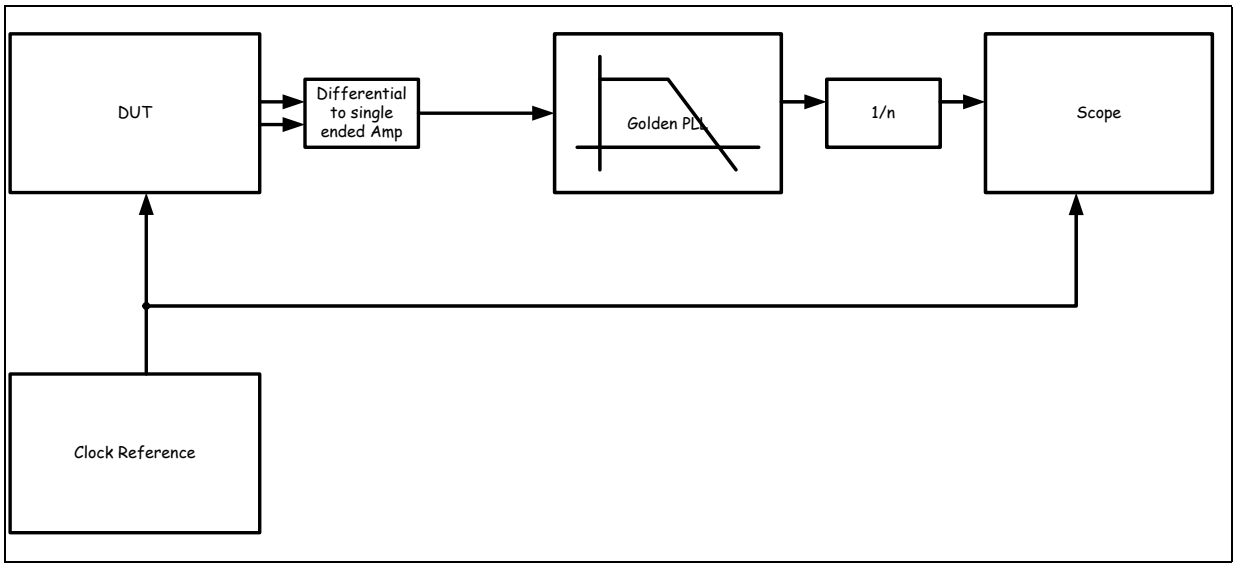
$$\tau_{HPJ} = \tau_{pkpk} - 2Q\tau_{rms}$$

using a Q calculated for a 3 sigma confidence level[1] as per Appendix 2.F.3.

2.E.2 Total Transmit Wander Measurement

This sub-clause describes the total transmit wander of a simple non-equalized transmitter as depicted below

Figure 2-30. Transmit Wander Lab Setup



- The transmitter under test shall transmit the specified data pattern, while all other signals are active.
  - The other channels can transmit the same pattern if they have at least a 16 bit offset with the channel under test.
  - All lanes to be active in both transmit and receive directions, and opposite ends of the link, i.e. transmit to receiver, are to use asynchronous clocks (to maximum allowed ppm. offset as specified in the protocol specifications).
- The transmitter can be tested single ended as high frequency jitter components are filtered by the Golden PLL

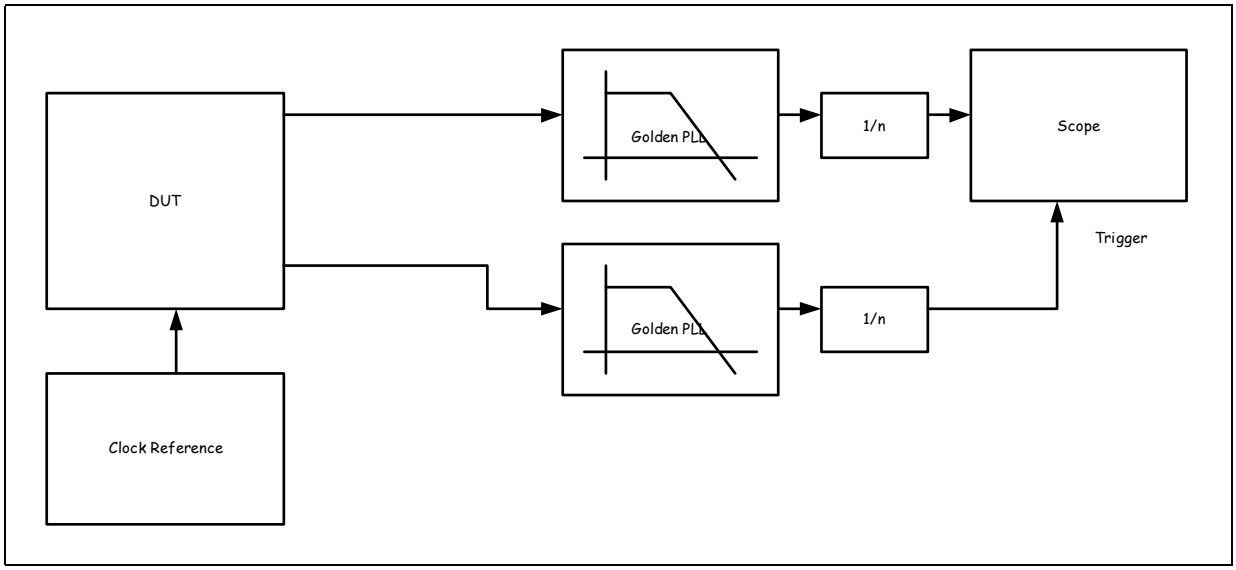
1. It is recommended that enough samples on the oscilloscope should be made such that Q>4

- Temperature and Supply Voltage should be cycled with a rate slower than baud rate over 166700Hz during test to exercise any delay components in the DUT.
- The inherent clock wander in signal shall be extracted using Golden PLL and divided, by the 1/n block, such as to limit the measured wander to 1UI at the divided frequency, and thus allowing it to be measured on an oscilloscope.
  - The Golden PLL should have at a minimum bandwidth of baud rate over 1667, with a maximum of 20dB/dec rolloff, until at least baud rate over 16.67, and is suggested to have no peaking around the corner frequency.
- The peak to peak total wander of the extracted clock should be measured using a scope trigger by the reference clock. The measured peak to peak wander should be verified to be bounded by repeating the measurement for ever increasing periods of time until the measurement is constant.

2.E.3 Relative Transmit Wander Measurement

This sub-clause describes specifically for SxI-5 interfaces, where limitations are defined in terms of relative wander between data lane and clocks, whose relative wander can be measured as depicted below.

Figure 2-31. Relative Wander Lab Setup



- The transmitter under test shall transmit the specified data pattern, while all other signals are active.
  - The other channels can transmit the same pattern if they have at least a 16 bit offset with the channel under test.
  - All lanes to be active in both transmit and receive directions, and opposite ends of the link, i.e. transmit to receiver, are to use asynchronous clocks (to maximum allowed ppm. offset as specified in the protocol specifications).
- The transmitters can be tested single ended as high frequency jitter components are filtered by the Golden PLL

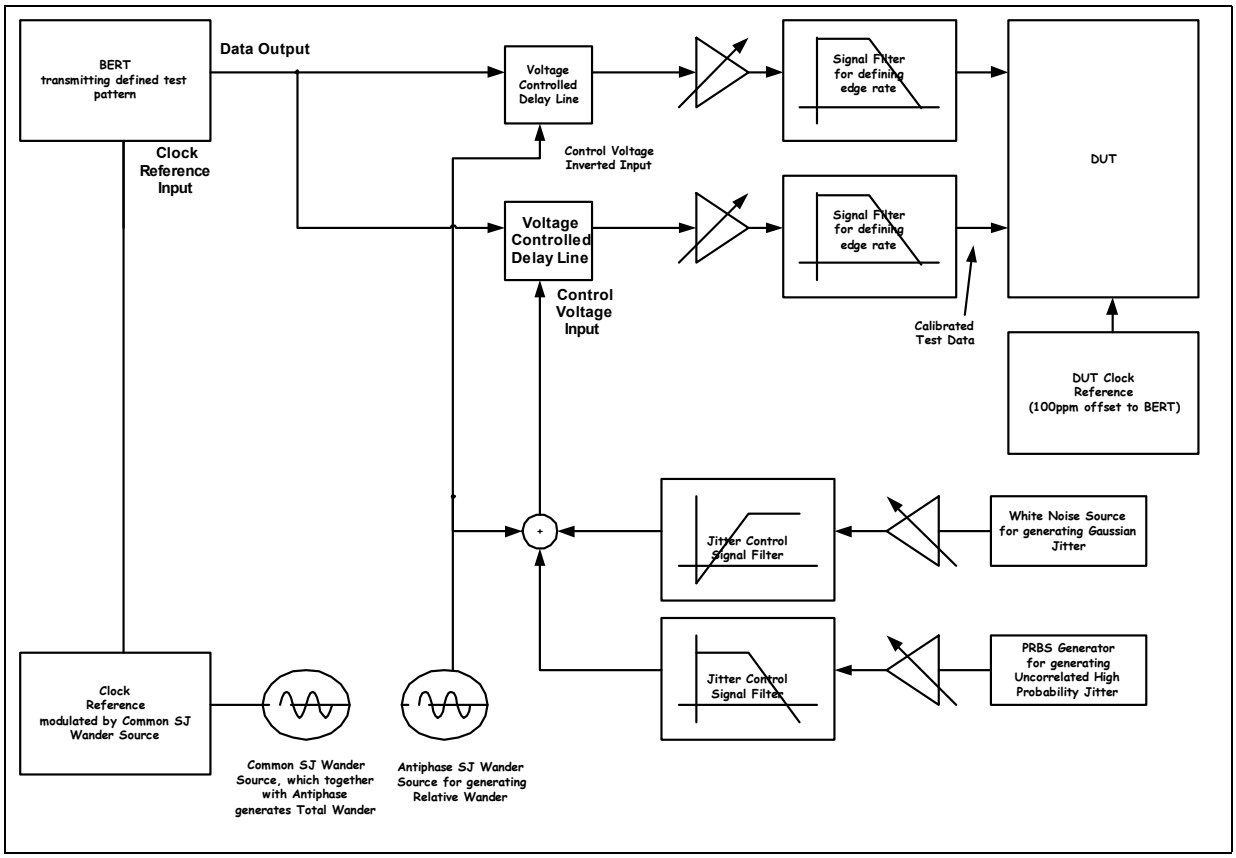
- Temperature and Supply Voltage should be cycled with a rate slower than baud rate over 166700Hz during test to exercise any delay components in the DUT.
- The inherent clock wander in each signal shall be extracted using Golden PLL and divided, by the 1/n block, such as to limit the measured wander to 1UI at the divided frequency, and thus allowing it to be measured on an oscilloscope.
  - The Golden PLL should have at a minimum bandwidth of baud rate over 1667, with a maximum of 20dB/dec rolloff, until at least baud rate over 16.67, and is suggested to have no peaking around the corner frequency.
- The peak to peak relative wander between the extracted clocks should be measured using a scope trigger by one of the extracted clocks. The measured peak to peak wander should be verified to be bounded by repeating the measurement for ever increasing periods of time until the measurement is constant.

2.E.4 Jitter Tolerance

2.E.4.1 Jitter Tolerance with Relative Wander Lab Setup

The following sub-clause describes the required jitter tolerance methodology for devices where Relative Wander is applicable e.g. SxI.5 and where no receive equalization is implemented.

Figure 2-32. Jitter Tolerance with Relative Wander Lab Setup



General

- The transmitter under test shall transmit the specified data pattern, while all other signals are active.
  - The other channels can transmit the same pattern if they have at least a 16 bit offset with the channel under test.
  - All lanes to be active in both transmit and receive directions, and opposite ends of the link, i.e. transmit to receiver, are to use asynchronous clocks (to maximum allowed ppm. offset as specified in the protocol specifications).
- The Device Under Test (DUT) shall be tested using an internal BERT or loop to have the defined BER performance
- The confidence level of the BER measurement should be at least three sigma as per Appendix 2.F.2.

Synchronization

- All lanes are to be active in both transmit and receive direction.
- All reference clocks should have the maximum offset frequency, with respect to each other, as defined in the implementation agreement.

Jitter

- The applied calibrated test signal shall have applied a calibrated amount of HF GJ and HPJ
- The jitter control signal for generating High Probability Jitter should be filtered using at least a first order low pass filter with a corner frequency between 1/20 - 1/10 of the baud rate of the PRBS generator to ensure that high frequency components are removed. The distribution of the jitter after the filter must be reasonably even, symmetrical, and large spikes should be avoided. The order of the PRBS polynomial may be between 7 and 11, inclusive, to allow flexibility in meeting this objective. The rate of the PRBS generator should be between 1/10 - 1/3 of the data rate of the DUT being tested, and their rates must be not harmonically related. The upper -3 dB frequency of the filtered HPJ should be at least 1/100 of the data rate of the DUT being tested to represent transmitter jitter that is above the tracking frequencies of the DUT's CDR. Calibration of HPJ must be done with a golden PLL in place. Once these objectives are achieved, there is no need to vary these settings; any combination of settings that meets all the objectives is satisfactory.
- The jitter control signal for generating Unbounded Gaussian Jitter shall be filtered as per Figure 2-5 using the “Jitter Control Signal Filter”. However, the upper frequency of the Gaussian jitter spectrum will be, acceptably, limited by the bandwidth of the voltage controlled delay line. The crest factor of the White Noise generator should be better than 18dB.
- The calibrated test signal shall have a calibrated amount of Total Wander and Relative Wander as compared to the *used* clock by using the Common SJ Wander and Antiphase SJ Sources with 1% frequency offsets. (Note the use of the inverted input to the uppermost delay line), as per Annex 2.C.2

- The amplitude of the Total Wander and Relative Wander is defined by the sinusoidal masks defined in Annex 2.A.1 and Annex 2.A.2 with the specified amplitudes from the implementation agreement.
- Wander should be applied
  - — from a frequency equivalent to 1UI of Total Jitter up to 20MHz modulation frequency
  - — at a maximum of 2MHz frequency steps above the corner frequency
  - — at a maximum of 200kHz frequency steps below the corner frequency.

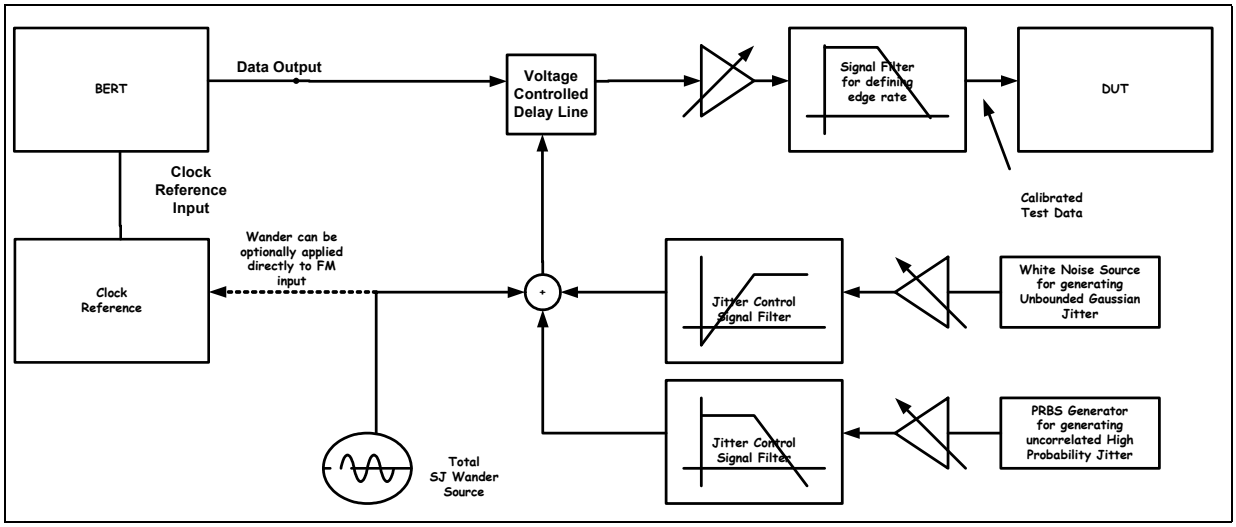
Amplitude

- The calibrated data signals should be filtered using a single pole low pass filter with a corner frequency of 0.7 times the baud rate, to define the edge rate.
- The amplitude of signal should be adjusted such that it *just passes* the defined receiver data eye sensitivity.
- For testing of DC coupled receivers either a pattern generator capable of generating differential signals and setting the common mode should be used or a combined AC coupled signal together with a biased-T. Using this setup the common mode should be varied between the defined maximum and minimum.

2.E.4.2 Jitter Tolerance with no Relative Wander Lab Setup

The following sub-clause describes the required jitter tolerance methodology for devices where Relative Wander is not applicable and no receive equalization is implemented.

Figure 2-33. Jitter Tolerance with no Relative Wander

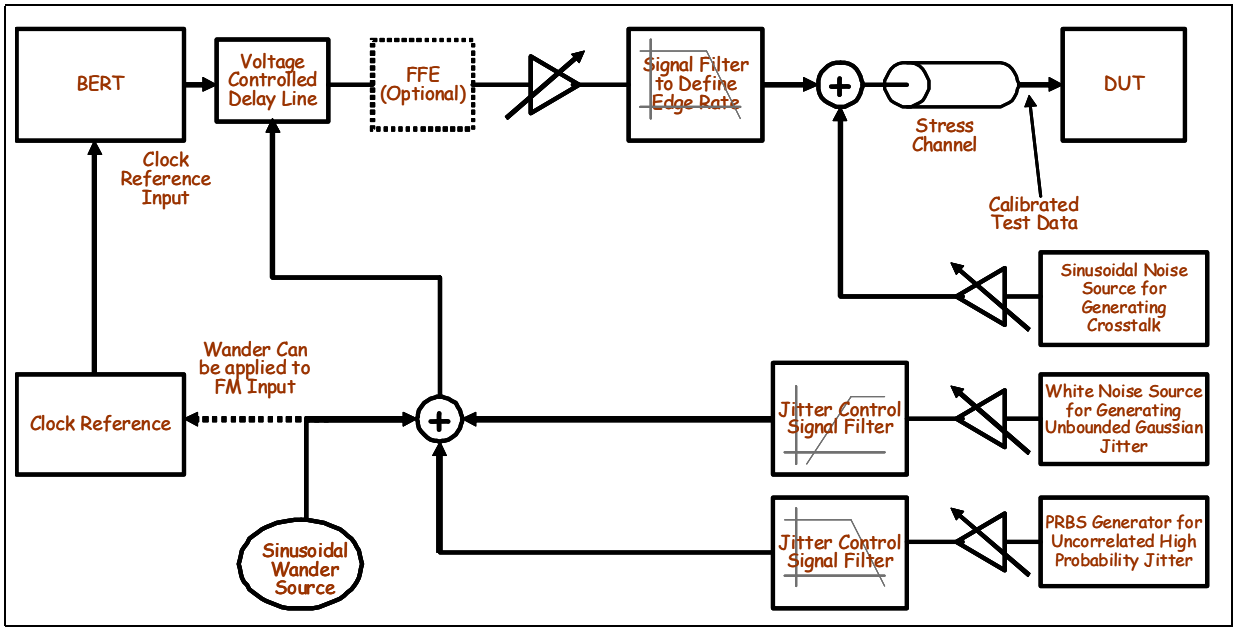


Referring to Figure 2-33, the DUT shall be tested as per the description in Appendix 2.E.4.1, omitting any requirements relating to relative wander and where only Total Wander is applied via the SJ Source shown.

2.E.4.3 Jitter Tolerance with Defined ISI and no Relative Wander

The following sub-clause describes the required jitter tolerance methodology for devices where Relative Wander is not applicable e.g. SxI.5 and where receive equalization is implemented and the performance of the equalization must be verified.

Figure 2-34. Jitter Tolerance with Defined ISI



Referring to Figure 2-34, the DUT shall be tested as per the description in Appendix 2.E.4.1, omitting any requirements relating to relative wander, and additionally

- The transmit jitter and amplitude shall be initially calibrated as per Appendix 2.E.1 at the output of the delay line.
- The stress channel shall have the characteristics specified in the relevant test method.
- The use of a Transmit Equalizing Filter (FFE) is optional. If it is included then its characteristics should be adjusted in accordance with the relevant test method.
- The defined amount of uncorrelated additive noise shall be applied via a sinusoidal source differentially to the signal. The frequency used shall be between 100MHz and the lesser of 1/4 the data rate and 2GHz. There is no need to sweep the frequency.

2.E.5 Jitter Transfer

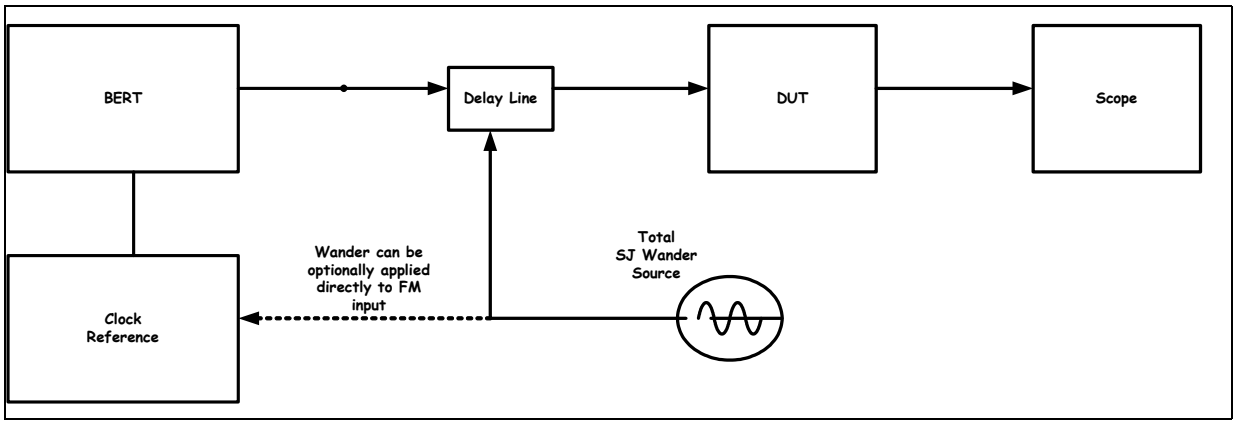
This section describes how jitter transfer relevant interfaces can be tested for compliance, e.g. CEI-11-SR-Transparent, SxI-5. Referring to Figure 2-35

- The BERT shall generate a data pattern as defined by the IA
- The jitter present before the delay line should be minimized as much as possible so as to maximize any transfer bandwidth function of the DUT

- A sinusoidal jitter should be applied following the same defined SJ mask as used for jitter tolerance, with the same resolution as described in Appendix 2.E.4.

The peak to peak jitter for a 60 second period measured on the scope should be compared before and after the application of the sinusoidal jitter. The ratio of the difference to the jitter applied is then defined as the jitter transfer function.

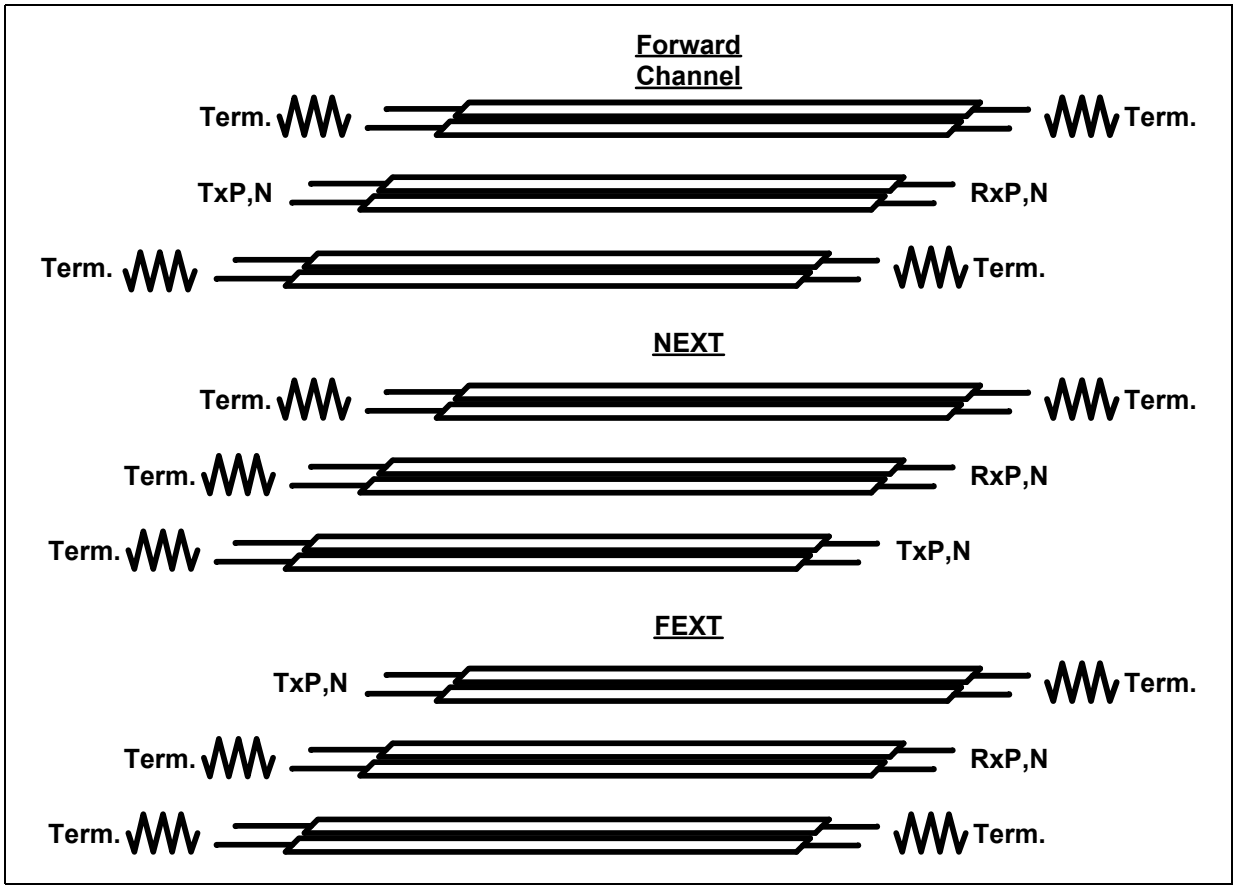
Figure 2-35. Jitter Transfer Lab Setup



2.E.6 Network Analysis Measurement

To enable accurate analysis of a channel the following methodology should be followed for the measurement and calculation of the effective channel transfer function.

Figure 2-36. S-parameter Port definitions



- Figure 2-36 shows an overview of the termination and port definitions typically used when measuring the forward channel and NEXT/FEXT crosstalk aggressors
- The intermediate frequency (IF) bandwidth should be set to a maximum of 300 Hertz with 100 Hertz preferred. The launch power shall be specified to the highest available leveled output power not to exceed 0 dBm.[1]
- Either direct differential measurements of the channel S21 and S11 should be performed or multiple single ended measurements from which the differential modes should be calculated.[2]
- Linear frequency steps of the measurements shall be no larger than 12.5MHz.
- A frequency range from no higher than 100MHz to no lower than three times the fundamental frequency should be measured.

1. Please refer to Agilent PLTS data sheet #5989-0271EN, and Agilent TDR Users Guide #54753-97015, section 2.2
2. Special care must be taken when performing multiple single ended measurements if the system is tightly coupled

- Extrapolation towards DC should be performed linearly on magnitude part with the phase being extrapolated to zero at DC, i.e. only a real part is present at DC.
- The channel response of the channel should be calculated by cascading the complete 4 port S-parameter matrix with a worst case transmitter and receiver. The transmitter/receiver should be described as a parallel R and C, where R is the defined maximum allowed DC resistance of the interface and C is increased until the defined maximum Return Loss at the defined frequency is reached.
- Any defined effective transmit or receiver filters should also be cascaded with the channel response
- The time resolution should be increased by resampling the impulse response in the time domain
- If required interpolation of the frequency domain should be performed on the magnitude and unwrapped phase components of the channel response

$$Tr(\omega) = \begin{bmatrix} 1 & 1 \\ 1 & Tx_{22}(\omega) \end{bmatrix} \otimes \begin{bmatrix} S_{11}(\omega) & S_{21}(\omega) \\ S_{12}(\omega) & S_{22}(\omega) \end{bmatrix} \otimes \begin{bmatrix} Rx_{11}(\omega) & 1 \\ 1 & 1 \end{bmatrix}$$

where

$S_{m,n}$ is the measured 4 port differential data of the channel

Tx_{22} is the transmitter return loss

Rx_{11} is the receiver return loss

$Tr(\omega)$ is the receiver return loss

converting the original frequency range to time domain, we obtain

$$i(t_m) = ifft(Tr(\omega))$$

where

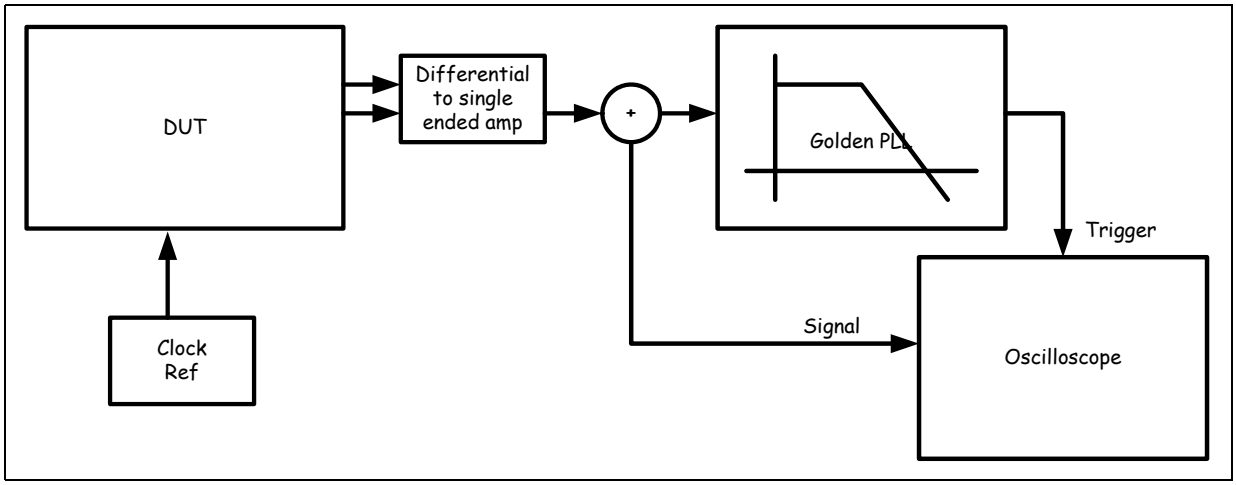
$$\omega = [-\frac{3}{4}f_{baud}, \frac{3}{4}f_{baud}]$$

2.E.7 Eye Mask Measurement Setup

The measurement of an eye mask is defined by the various Implementation Agreements in terms of a polygon for the probability of the required Bit Error Rate. This polygon may have to be altered given that the sample population of the scope is limited

and must be adjusted as per Appendix 2.F.3. For the measurement of the signal the laboratory setup shown in Figure 2-37 should be used, including the recommendations list in Appendix 2.E.1.

Figure 2-37. Eye Mask Measurement with Golden PLL



2.F Appendix - BER Adjustment Methodology

2.F.1 Extrapolation of Correlated Bounded Gaussian Jitter to low BERs

For IAs with BER requirements of 1×10^{-15} or lower, measurements to that level are very time consuming (or rely on averaging multi-links), hence more practical to only take measurements to Qs around 7 (BER around 1×10^{-12}).

Bathtub Measurements

CBGJ can appear as either GJ or CBHPJ depending upon the Q at which it is linearised.

If HPJ and GJ are measured using a bathtub there is no knowledge as to if the GJ is UUGJ or CBGJ. For system budgeting it is recommended that the bathtub GJ should be assumed to be all UUGJ.

If combined spectral, oscilloscope methods are used then UUGJ, UBHPJ and CBHPJ can be estimated. It is not possible to estimate the CBGJ as it has already become bounded and appears as CBHPJ. For system budgeting it is recommended that this peak value is valid for the extrapolated Q of interest.

2.F.2 Confidence Level of Errors Measurement

Assuming that a link, with a given BER, can be modelled as a Bernoulli random process, the following statistics can be assumed.

Given,

p is the probability of error

$q = (1-p)$ is the probability of not erroring

n is the number of bits received and measured

then,

$m = np$ is the expected number of errors received

$\sigma = \sqrt{npq}$ is the sigma of the variation of the number of errors received

As an example process, for a 3 sigma confidential level

$$p = 10^{-12}$$

$$n = 100 \cdot 10^{12}$$

$$m = 100$$

$$\sigma = 10$$

$$m\Big|_{max}^{min} = [m + Q\sigma]\Big|_{Q=-3}^{Q=3}$$

$$m\Big|_{max}^{min} = \begin{matrix} 70 \\ 130 \end{matrix}$$

To assess the accuracy of such a measurement an equivalent process with a higher BER can be calculated that would show the same limit of error for the same confidence level and measured number of bits.

$$m\Big|_{max} = E[m] - Q\sigma$$

$$m\Big|_{max} = np - Q\sqrt{npq}$$

$$m\Big|_{max} = np - Q\sqrt{np(1-p)}$$

Solving the quadratic equation for p

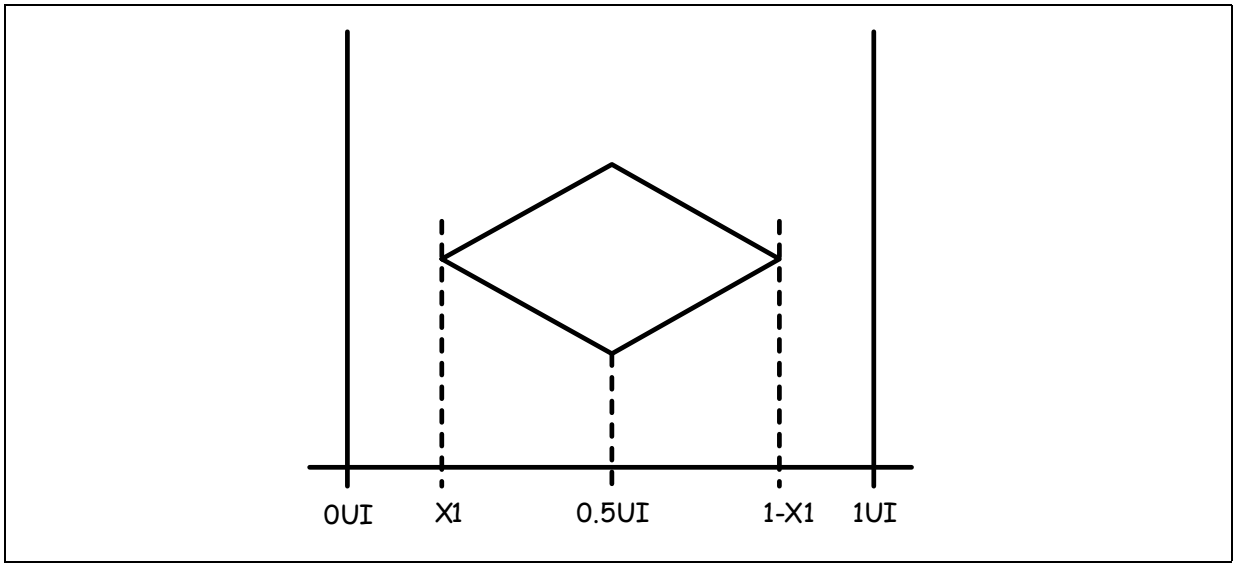
$$p = 1.69 \times 10^{-12}$$

2.F.3 Eye Mask Adjustment for Sampling Oscilloscopes

In all Interoperability Agreement the data mask is defined for the bit error rate of the link. Given that this bit error rate is very small, typical oscilloscope measurement will not sample enough points to be able to verify compliance to these mask.

2.F.3.1 Theory

Figure 2-38. Example Data Mask



Given an example eye mask, Figure 2-38, the extremes of the mask, X1 are defined as a linear addition of a Gaussian and High Probability jitter component.

$$X1 = \frac{HPJ}{2} + Q \cdot GJ_{rms}$$

where

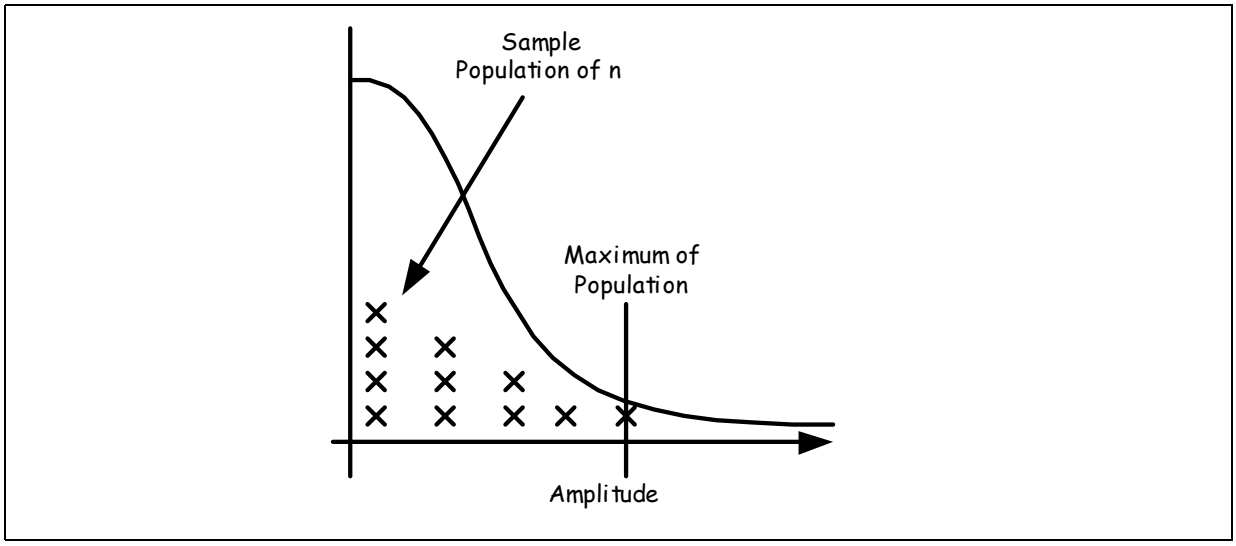
HPJ is the high probability jitter

GJ_{rms} is the gaussian distributed jitter

Q is the GJ multiplication factor

Given a low sample population and the requirements for mask verification to achieve a hit or no-hit result, X1 must be adjusted according to the sample population and the confidence level that a particular peak to peak is achieved., Given a random process

Figure 2-39. Example Data Mask



the probability of measuring a particular maximum amplitude on an oscilloscope, requires one sample to lie on the maximum and all other samples to lie below this value. Referring this all to a half Gaussian distribution and a population of n, there are n different ways this can occur,

$$P(x_m) = nQ(x_m)\left(\int_0^{x_m} Q(x)dx\right)^{n-1}$$

where

x_m is the random variable of the maximum amplitude measured

x is the random variable of the underlying random jitter process

$Q(x)$ is the Q function of the Normal probability density function

n is the sample population

$P(x_m)$ is a probability density function

The equation above is solved and the probability of attaining a given maximum (normalized to the sigma) for various populations plotted, Figure 2-40.

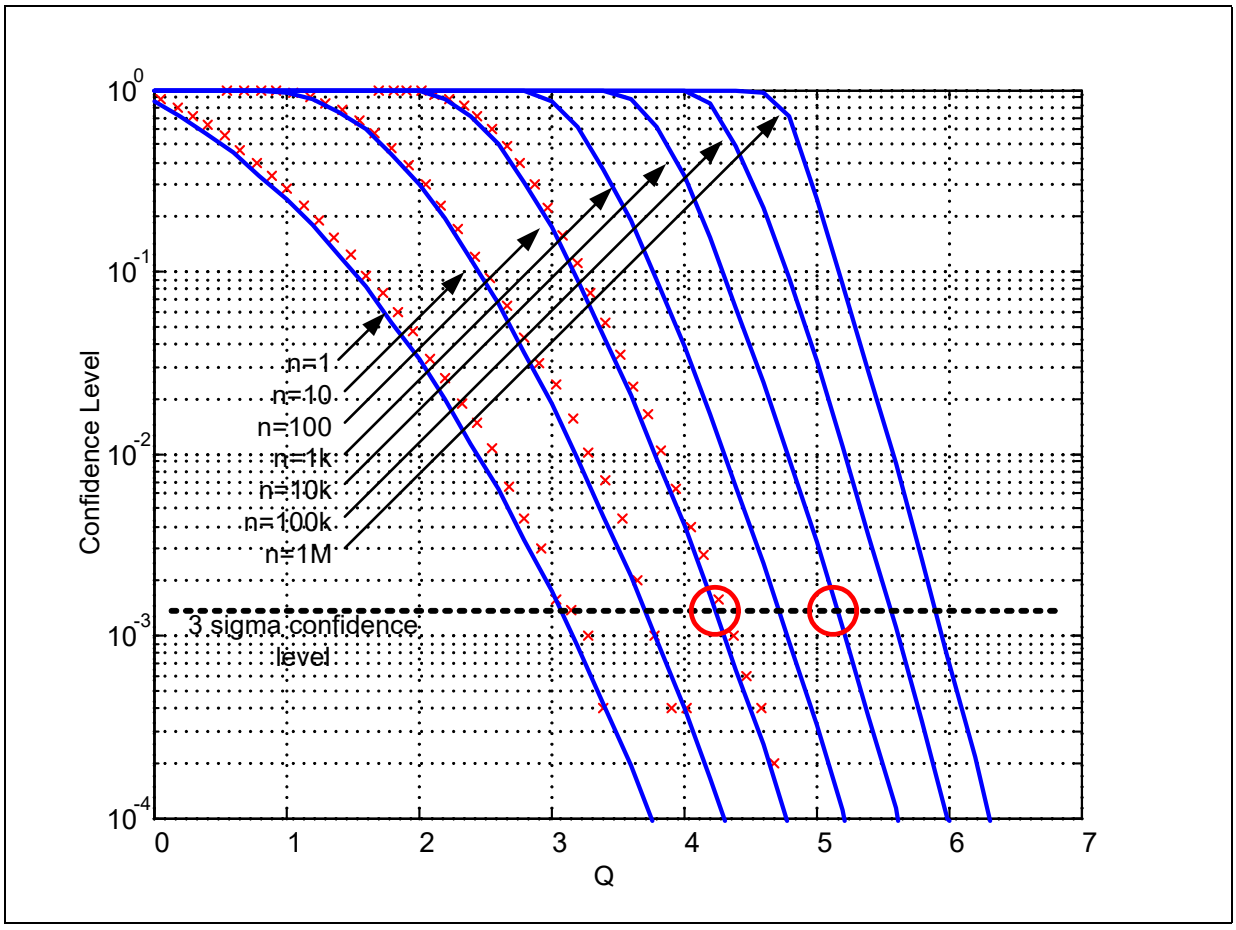
2.F.3.2 Usage

Given a known sampling population, n, calculated from the measurement time, average transition density and sampling/collection frequency of the oscilloscope the three sigma confidence level (i.e. 1.3×10^{-3}) of the measured Gaussian jitter peak value can be read from Figure 2-40. This value should be multiplied by 2 to give the full peak to peak value of the random jitter.

The three sigma confidence level should be understood as ensuring that 99.96% of all good devices do not violate the eye mask. To limit the number of bad devices that also pass the eye mask it is strongly recommended that the sample population be chosen as to give a Q larger than 5.

e.g. referring to the red circled intersections Figure 2-40, if we calculate that the sample population for an oscilloscope was 100 i.e. n=100, then for a 3 sigma confidence this equals a Q of 4.2. As the recommended Q value is 5 we should increase the sample population to 10k to give a Q of 5.2.

Figure 2-40. Cumulative Distribution Function of Maximum Amplitude



3 Common Electrical Specification

3.1 Introduction

This clause specifies electrical parameters and attributes common to all links defined in clause 1. In the event of a difference between an individual clause and these general requirements, the respective individual clause shall prevail.

3.2 General requirements

3.2.1 Data Patterns

This IA does not have any requirements for specific data patterns (i.e. 8B/10B, 64/66B, SONET scrambling, stream cipher, raw data, etc.), however the following requirements are necessary to insure proper operation. If all of these conditions are not met, then the link may not work to the full distance, or meet the BER, or in fact work at all.

- Average transition density needs to converge to 0.5 over a long period (>10^9 bits), but can in the extreme be between 0.45 and 0.55 over a 30,000 bit period with a probability of at least one minus the BER ratio (1-10^{-15} with a test requirement to verify 1-10^{-12})
- Average DC balance needs to converge to 0.5 over a long period (>10^9 bits), but can in the extreme be between 0.45 and 0.55 over a 30,000 bit period with a probability of at least one minus the BER ratio (1-10^{-15} with a test requirement to verify 1-10^{-12}).
- Probability of run lengths over 10 to be proportional to 2^{-N} for N-like bits in a row ($N \geq 10$). Hence, a run length of 40 bits would occur with a max probability of 2^{-40}.
- If a fixed block coding scheme is used (e.g. 8B/10B, SONET), the raw data must be scrambled before coding or the coded data must be scrambled prior to transmission. This is to prevent the so called worst case patterns (e.g. CJPAT-like patterns).

SONET can be viewed as a coding scheme that can create worst case patterns (via the un-encoded overhead bytes). Two such cases would be the A1/A2 pattern and the Z0 byte that can be anything (each unscrambled byte is repeated N times in an OC-N stream [N = 3, 12, 48, 192]).

3.2.2 Signal Levels

The signal is a low swing differential interface. This implies that the receiver has a wide common mode range (within the max. absolute input voltages). All devices must support load type 0 defined in Table 3-1, SR devices can optionally support any/all of the other 3 load types while LR devices can optionally support load type 1.

Table 3-1. Definition of load types

Characteristic	Load Type 0	Load Type 1	Load Type 2	Load Type 3	Unit
R_Zvtt	>1k	<30	<30	<30	Ω
Nominal Vtt	undefined	1.2	1.0	0.8	V

This type of differential interface allows for interoperability between components operating from different supply voltages and different I/O types (CML, LVDS-like, PECL, etc.). Low swing differential signaling provides noise immunity and improved electromagnetic interference (EMI). Differential signal swings are defined in following sections and depend on several factors such as transmitter pre-equalization, receiver equalization and transmission line losses.

3.2.3 Bit Error Ratio

The link will operate with a Bit Error Ratio (BER) of 10^{-15} (with a test requirement to verify 10^{-12} - see Clause 2 for more information on the jitter model and how to measure BER)

3.2.4 Ground Differences

The maximum ground difference between the driver and the receiver shall be ±50mV for SR links and ±100mV for LR links. This will affect the absolute maximum voltages at compliance point 'R'. If driver and receiver are on the same PCB with no intervening connectors, then the ground difference is approximately 0 mV.

3.2.5 Cross Talk

Cross talk arises from coupling within the connectors, on the PCB, the package and the die. Cross talk can be categorized as either Near-End or Far-End Cross talk (NEXT and FEXT). In either of these categories, the amount of cross talk is dependent upon signal amplitudes, signal spectrum, and trace/cable length. There can be many aggressor channels onto one victim channel, however typically only a few are dominant.

Further consideration of Crosstalk can be found in Appendix 3.A.4.

3.2.6 Driver Test Load

All driver characteristics should be implemented and measured to a differential impedance of 100Ω±1% at DC with a return loss of better than 20dB from baud rate divided by 1667 to 1.5 times the baud rate, unless otherwise noted.

3.2.7 Driver Lane-to-Lane Skew

While the protocol layer will control some of the lane to lane skew, the electrical level is allowed up to 500ps of lane-to-lane skew caused by the driver circuitry and associated routing. Hence, the total output (i.e. measured) lane-to-lane skew is to be specified in the protocol standards with this 500ps taken into account. The driver lane-to-lane skew is only for the Serdes TX and does not include any effects of the channel.

3.2.8 Input Lane-to-Lane Skew

While the protocol layer will control the maximum amount of lane to lane skew that is allowed, it must allow for up to 1000ps of skew caused by the driver & receiver circuitry and associated routing (that is 500ps for the driver and 500ps for the Rx). The input lane-to-lane skew does not include any skew effects of the channel.

3.2.9 Driver Short Circuit Current

The max DC current into or out of the driver pins when either shorted to each other or to ground shall be ±100mA when the device is fully powered up. From a hot swap point of view, the ±100mA limit is only valid after 10 μs

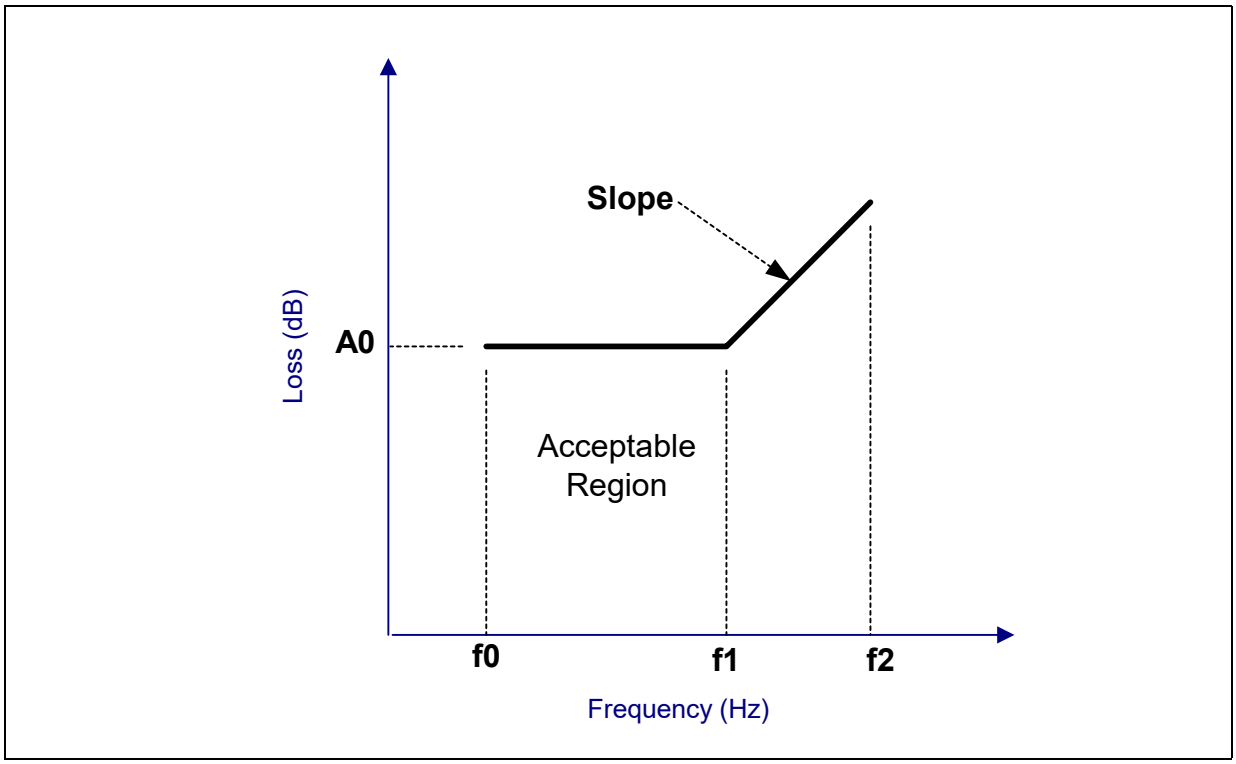
3.2.10 Differential Resistance and Return Loss, Driver and Receiver

The DC differential resistance shall be between 80 and 120Ω.

The differential return loss shall be better than A0 from f0 to f1 and better than A0 + Slope*log10(f/f1) where f is the frequency from f1 to f2. See Figure 3-1 for definitions. Differential return loss is measured at compliance points T and R. If AC coupling is used, then all components (internal or external) are to be included in this requirement. The reference impedance for the differential return loss measurements is 100Ω.

Common mode return loss measurement shall be better than -6dB between a minimum frequency of 100MHz and a maximum frequency of 0.75 times the baud rate. The reference impedance for the common mode return loss is 25Ω.

Figure 3-1. Driver and Input Differential Return Loss



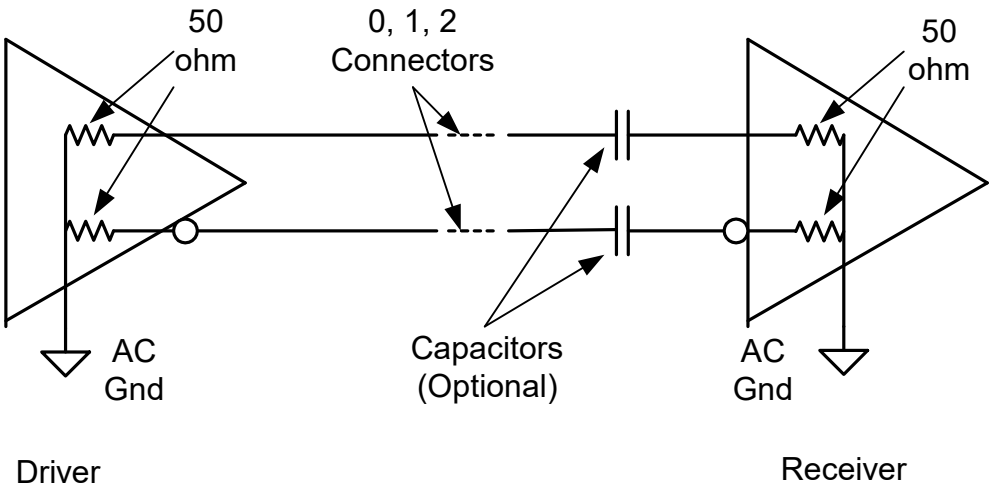
3.2.11 Baud Rate Tolerance

The range of operating Baud rates is defined specifically for each interface in the specific clauses. Each CEI interface is required to operate asynchronously with a tolerance of +/-100ppm from the nominal baud rate.

3.2.12 Termination and DC Blocking

Each link requires a nominal 100Ω differential source termination at the driver and a nominal 100Ω differential load termination at the receiver. The terminations shall provide both differential and common mode termination to effectively absorb differential or common mode noise and reflections. Receivers and transmitters shall support AC coupling and may also optionally support DC coupling. AC Coupled receivers require a differential termination >1kΩ at DC (by blocking capacitors in or near receivers as shown in Figure 3-2 or by circuit means within the receiver). DC Coupled Devices shall meet additional electrical parameters T_Vcm, R_Vrcm, R_Vtt, R_Zvtt. All termination components are included within the Rx and TX blocks as shown in the reference model as defined in Section 1.8.

Figure 3-2. Termination Example



3.A Appendix - Transmission Line Theory and Channel Information

3.A.1 Transmission Lines Theory

The performance of a high frequency transmission line is strongly affected by impedance matching, high frequency attenuation and noise immunity.

It is possible to design a high frequency transmission line using only a single conductor. Nevertheless most high frequency signals use differential transmission lines (i.e. a pair of coupled conductors carrying signals of opposite polarity). Although differential signaling appears wasteful of both pins and signal traces it results in much better noise immunity. Differential signals produce less conducted noise because the opposite power and ground current flows cancel each other both in the line driver and in the transmission line. Differential signals produce less radiated noise because over a modest distance the opposite fields induced by the opposite currents cancel each other. Differential signals are less susceptible to noise because most sources of noise (common mode noise) tend to affect both signal lines identically, producing a variation in common mode voltage but not in differential voltage.

3.A.1.1 Impedance Matching.

The AC impedance of a single conductor is determined by the trace geometry, distance to the nearest AC ground plane(s) and the dielectric constant of the material between the trace and the ground plane(s). If the distance between the signal trace and the nearest ground plane is significantly less than the distance to other signal traces the signal trace will behave as a single-ended transmission line. Its AC impedance does not vary with signal polarity although it may vary with frequency due to the properties of the dielectric material. This impedance is often called single ended impedance, Zse.

The AC impedance, Z of a differential transmission line is affected by the configuration of the pair of conductors and the relationship between their signal polarities, in addition to the trace geometry, distance to the nearest AC ground plane(s) and the dielectric constant of the material between the trace and the ground plane(s). If the paired conductors are close enough to interact (coupled), then the impedance for signals of opposite polarity (odd mode impedance, Zodd) will be lower than the impedance for signals of the same polarity (even mode impedance, Zeven).

If there is minimal coupling between the paired conductors then Zodd = Zeven = Zse. Coupled transmission lines always produce Zodd < Zse < Zeven. The following equations relate effective differential impedance, *zdiff* to common mode impedance, *Zcm* and single ended impedance, *Zse* to even and odd mode impedances:

$$Zdiff = 2Zodd \qquad Zcm = \frac{Zeven}{2} \qquad Zse = \frac{Zeven + Zodd}{2}$$

Most differential data signals are designed with *zdiff* = 100Ω and 25Ω < *Zcm* < 50Ω.

There is a trade-off in the choice of *Zcm*. With *Zcm* = 25Ω (no coupling) may reduce conducted noise for transmission lines with inadequate AC or DC grounding. *Zcm* = 50Ω (close coupling) may reduce radiated noise (crosstalk) which is more critical in backplanes. However close coupling requires careful ground construction to control common mode noise.

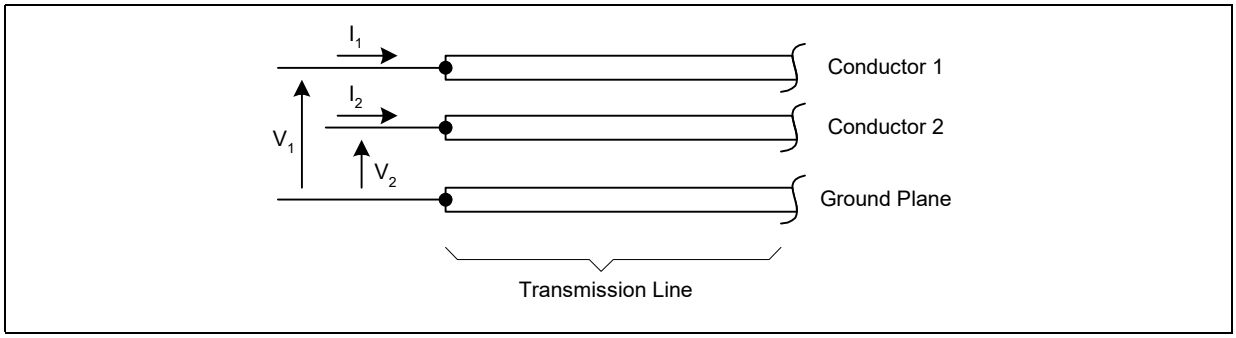
The reader may wonder why common mode impedance is meaningful in a differential transmission system. In a perfectly constructed system only odd mode (opposite polarity) signals propagate. However imperfections in the transmission system cause differential to common mode conversion. Once converted into common mode the energy may convert back to differential mode by the same imperfections. Thus, these imperfections convert some of the signal energy from opposite polarities to the same polarity and back.

The two main sources of mode conversion are impedance mismatches which cause part of the energy to be reflected, and differential skew which causes variations in forward signal propagation delay between the individual paths of the differential pair. Impedance mismatches typically occur at boundaries between transmission line segments, including wire bonds, solder joints, connectors, vias and trace-to-via transitions. Often ignored sources of impedance mismatches at these boundaries are discontinuities within the AC ground itself as well as asymmetric coupling between the individual traces and the AC ground. Differential skew can occur at these same boundaries and also due to mismatched trace lengths in device packages and in PCBs.

3.A.1.2 Impedance Definition Details

Differential transmission lines consist of two conductors and a ground plane. The voltage-current relationships at one end of this line can be formulated in terms of a two-port as in Figure 3-3.

Figure 3-3. Transmission Line as 2-port



The voltage current relationships are:

$$V_1 = Z_{11}I_1 + Z_{12}I_2 \qquad V_2 = Z_{21}I_1 + Z_{22}I_2$$

If the line is infinitely long or perfectly terminated, then these four impedance values are the characteristic impedance of the line. The characteristic impedance is a 2 x 2 matrix:

$$\hat{Z}_c = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}$$

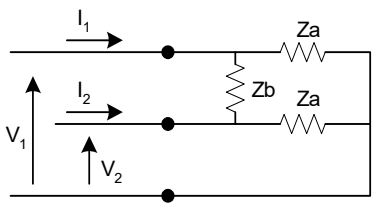
Generally, all four of the matrix entries are complex. But, at frequencies of interest, the inductance and capacitance per unit length dominate so that all four quantities are approximately real, positive numbers. For engineering purposes it is common to speak of the impedances as though they are resistances, with no imaginary part; keeping in mind that the imaginary part exists. Since the line is passive and symmetric, we have $Z_{11} = Z_{22}$ and $Z_{12} = Z_{21}$ so that the line is described by just two impedance values. If the line is to be perfectly terminated, then we must create a network that is equivalent to $\hat{Z}_c$. That is, we need a 3-terminal (2 nodes + ground) network that presents the same values of Z_{11} and Z_{12} as the line. A T or pi network could be used. The pi network is shown in Figure 3-4, along with the impedance values in terms of Z_{11} and Z_{12}.

.

Figure 3-4. PI Network Termination

$$Za = Z_{11} + Z_{12} \qquad Zb = \frac{Z_{11}^{\,2} - Z_{12}^{\,2}}{Z_{12}}$$

$$Zodd = \frac{ZaZb}{2Za + Zb} = Z_{11} - Z_{12} \qquad Zeven = Za = Z_{11} + Z_{12}$$



The odd and even mode impedances, *Zodd* and *Zeven*, are other impedance definitions that are more descriptive referring to the polarity of the signal propagating the differential pair. In the case of opposite signal polarity in the two lines of the signal pair the odd mode impedance is used. In the case of same signal polarity the even mode is used. *Zodd* and *Zeven* are measured as shown in Figure 3-5.

Figure 3-5. Measurement of Zodd, Zeven

Zodd Zeven

$$V = V_1 = -V_2 \; V = V_1 = V_2$$

$$I = I_1 = -I_2 \; I = I_1 = I_2$$

$$Zodd = \frac{V}{I} \; Zeven = \frac{V}{I}$$

Odd mode impedance is the impedance measured when the two halves of the line are driven by equal voltage or current sources of opposite polarity. Even mode impedance is the impedance measured when the two halves of the line are driven by equal voltage or current sources of the same polarity. In this specification the differential mode impedance, *Zdiff* and the common mode impedance, *Zcm* are used. The relationship to even and odd mode impedances is given as:

$$Zdiff = 2Zodd \qquad Zcm = \frac{Zeven}{2} \qquad Zse = \frac{Zeven + Zodd}{2}$$

From the above equations we see that *Zeven* is always greater than *Zodd* by $2Z_{12}$, where Z_{12} is a measure of the amount of coupling between the lines. This means that *Zeven* is larger than *Zodd* for coupled transmission lines.

3.A.2 Density considerations

The preceding section showed that, for two idealized forms of termination, *Zodd* is correctly terminated but *Zeven* is not. The first illustrated case, using a 50 ohm resistor (or its equivalent) from either terminal to ground (or to AC ground), has become relatively standard. Because it has *ZoddT* = *ZevenT* = 50 ohm, it provides correct differential termination and is often close to providing correct common-mode termination.

By increasing the conductor spacing in the transmission line we can decrease Zeven (decrease Z_{12}) and bring it closer to 50 ohm. But dense backplanes require a large number of transmission lines per unit cross-sectional area of the printed circuit board. This means that the two printed circuit traces comprising the differential transmission line are forced close together, which increases Z_{12}. The backplane design is therefore, a compromise between the desire for high density of transmission lines and a desire for correct common-mode termination.

Transmission lines act as low-pass filters due to skin effect and dielectric absorption. As the density of transmission lines increases, both the series resistance per unit length and the parallel conductance per unit length increase. This, in turn, results in greater attenuation at a given frequency. Thus, high speed backplane design is not just a compromise between density and common-mode matching. There is also a compromise between density and attenuation.

3.A.3 Common-Mode Impedance and Return Loss

It is demonstrated above that increasing the density of transmission lines in a backplane results in higher common-mode impedance, which is known as interference and for high amplitudes the receiver is likely to be disrupted.

Common-mode interference arises from several sources. Among them are:

1. Imperfections in driver circuits.
2. A difference in length between the two conductors of the transmission line
3. Imperfections in impedance matching across board boundaries connectors and vias causing mode conversion, differential to Common mode
4. EMI.

The interference resulting from the driver probably has a spectrum that is the same as or similar to that of the signal. EMI arising from coupling into the printed circuit traces should be small, assuming that coupled stripline is used. However, connector pins may be exposed. EMI may have frequency components that are well below signal frequencies, which means that it won't necessarily be attenuated to the extent that signals are. But, at the same time, the lower frequencies are probably poorly coupled into the backplane circuit.

Earlier, two ideal forms of termination were presented based on either one or two resistors. These ideal terminating devices are helpful in examining the relationship between the parameters of the transmission line versus those of the device. Real devices, however, are not simple resistances. They contain parasitic components and a non-ideal path from package pins to die. There may also be a need to AC-couple the terminations.

The most that we can do in this situation is to make the package and the die appear as close to ideal as possible over as much of the signal spectrum as possible. The extent of the deviation from ideal is specified and measured as a function of frequency. The preferred measures are S_{11} (single-ended return loss) or S_{DD11} (differential return loss) as functions of frequency. (Sometimes S_{22} or S_{DD22} are used to indicate an output.) Ideally these return losses are 0 (no reflection) over the frequency range of interest. In dB this is -∞.

Note: Sometimes a return loss is specified as a positive number, it being understood that this still refers to the log of a reflection coefficient in the range of 0 to 1.

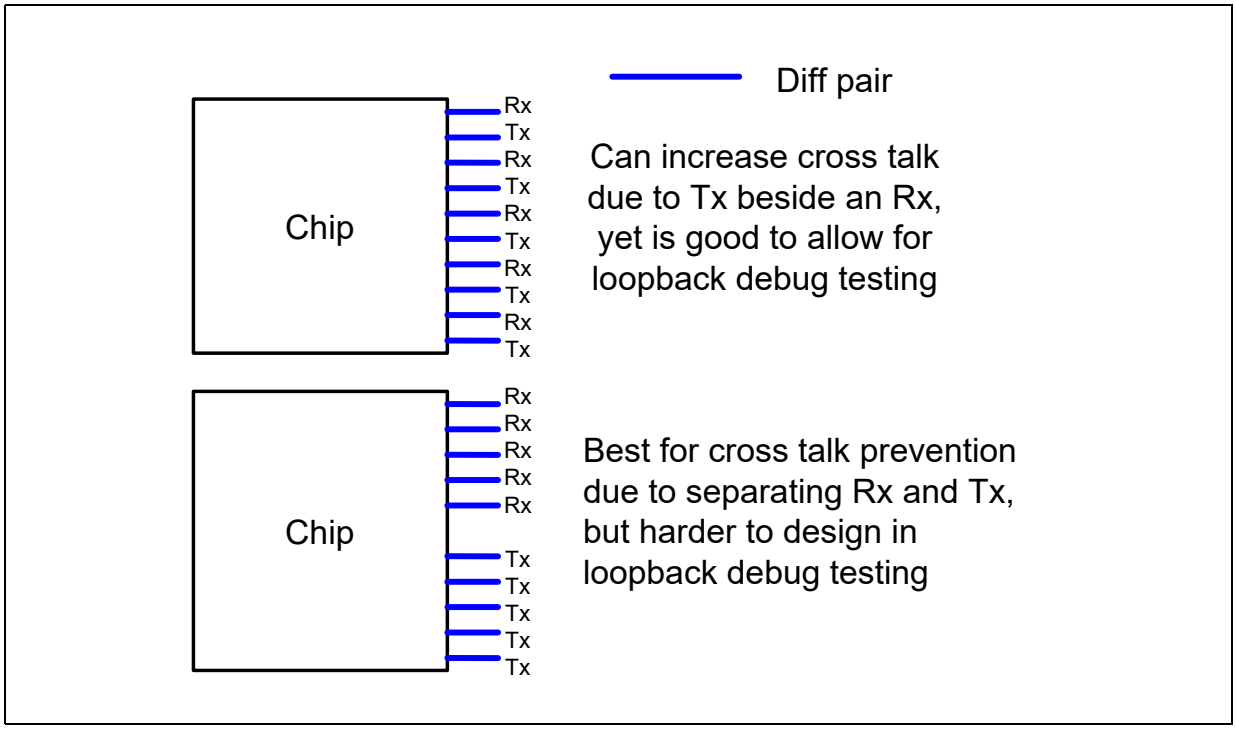
3.A.4 Crosstalk Considerations.

This IA assumes that the dominant cross talk can come from aggressors other than the transmitter associated with the receiver. Hence NEXT cancellation is not useful.

Crosstalk between CEI channels should be minimized by good design practices. This includes the pin-out arrangement to the driving/receiving IC's, connectors and backplane tracking.

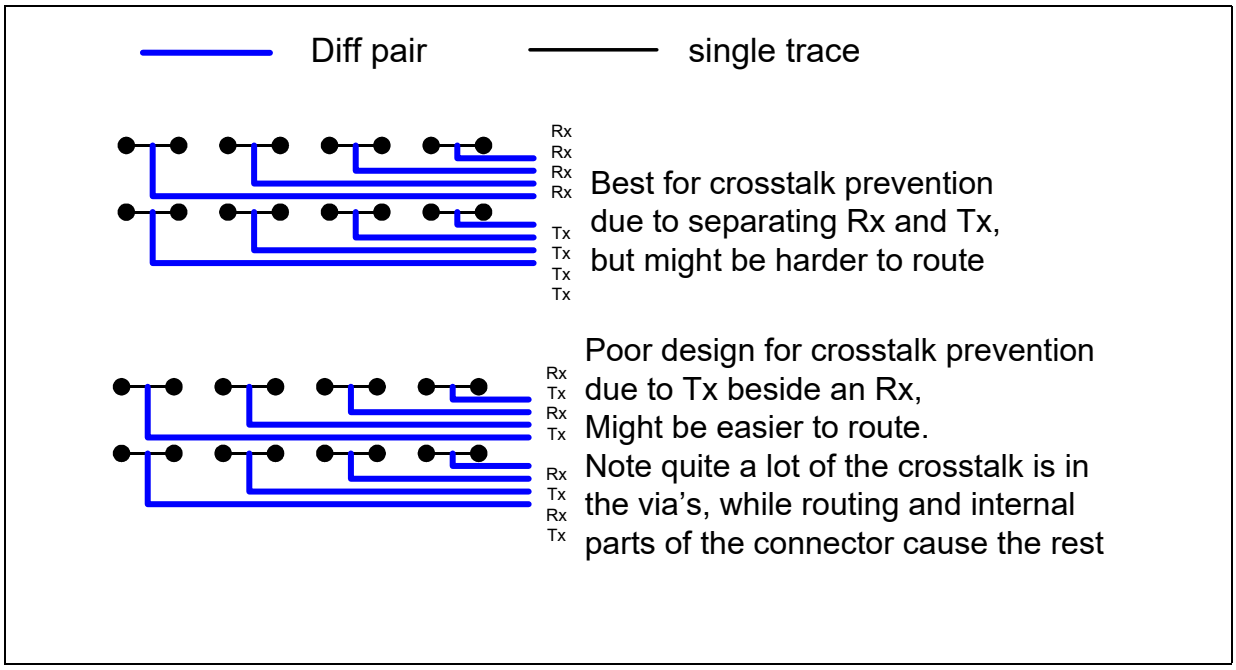
Optimum arrangement for minimising crosstalk between channels at IC pins is illustrated in Figure 3-6 below. Crosstalk between channels can be reduced by grouping TX and RX pins and avoiding close proximity between individual TX and Rx pins. This practice will minimize coupling of noise from TX drivers into RX inputs.

Figure 3-6. Minimisation of crosstalk at IC pins.



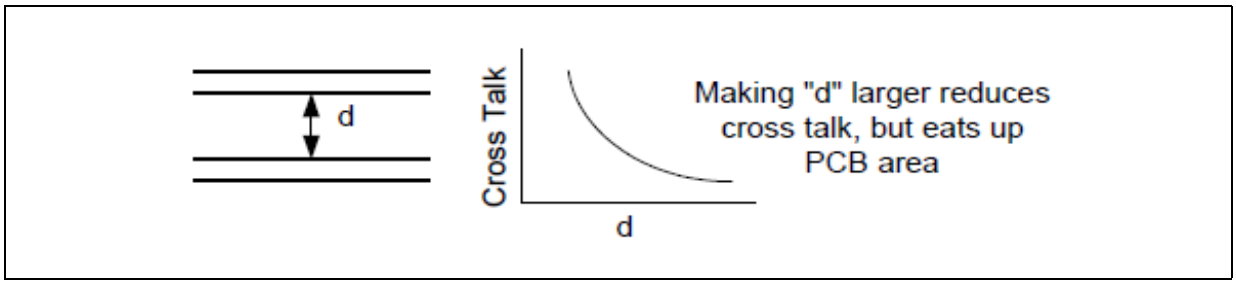
Crosstalk at connector pins can be minimized by careful optimisation of connections as shown in Figure 3-7 below.

Figure 3-7. Minimisation of crosstalk at connector pins



Crosstalk between channels over a backplane can be minimized by careful arrangement of tracking, avoiding coupling of noise into RX inputs and increasing spacing "d" between channels as far as possible as shown in Figure 3-8 below.

Figure 3-8. Minimisation of crosstalk over backplane



3.A.5 Equation based Channel Loss by curve fit.

This section describes a technique with specific limitations. It does not include any phase data for the SDD21, and includes no return loss information about SDD11 or SDD22, neither phase nor magnitude, information that is critical for the evaluation of a specific topology's performance. The above proposed statistical-eye characterization includes these effects by including the full 4-port S-parameter measurements. The following method is included for information only and is believed to be of relevance to the overall understanding of the channel transfer loss.

One way to specify the channel loss is to have an average or worst case "curve" fit to several real channels. This method includes effects of real vias and connectors. This method typically uses the equation below:

$$Att = -20\log(e)\left(a_1\sqrt{f} + a_2 f + a_3 f^2\right)$$

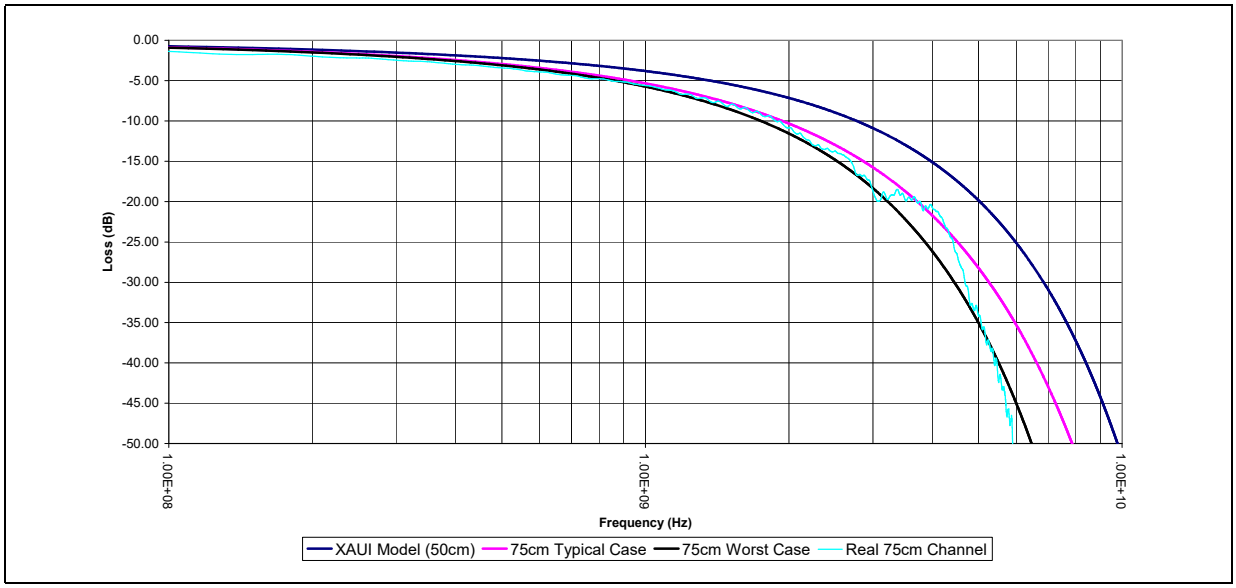
Where f is frequency in Hz, a_1, a_2, & a_3 are the curve fit coefficients and Att is in dB.

Table 3-2 gives some examples of these coefficients and Figure 3-9 plots them along with the PCB model and a real 75cm backplane (with 5cm paddle cards on both ends). These examples are representative for CEI-6G-LR applications but do not represent specifications that a CEI link are to comply with.

Table 3-2. Curve fit Coefficients

	a_1	a_2	a_3
XAUI [19] (50cm)	6.5e-6	2.0e-10	3.3e-20
75cm [24] "Worse"	6.5e-6	3.9e-10	6.5e-20
75cm [24] "Typical"	6.0e-6	3.9e-10	3.5e-20

Figure 3-9. Equation based Channel Loss curves



4 SxI-5, SFI-4.2, SFI-5.1 & SPI-5.1 Interfaces

4.1 Introduction

This clause details the requirements for the SxI-5 electrical interface (which includes the following three OIF Implementation Agreements SFI-4.2, SFI-5.1 and SPI-5.1).

4.2 General Requirements

This clause uses “Method A” of the Jitter and Interoperability Methodology section.

4.2.1 Channel Compliance

As per 2.1.2, with the following reference transmitter and reference receiver (note these conditions do not specify any required implementation but rather indicate a methodology for testing channel compliance), and shall meet the received eye mask as specified in [13], [10], [11] or [12] as required.

Also refer to Appendix 3.A for more information on the channel characteristics.

Reference Transmitter:

1. No emphasis
2. A concatenated first order low pass transmit filter with 0.75 times baud rate
3. An amplitude equal to the defined minimum transmit amplitude in the specific Implementation Agreement
4. A jitter distribution equal to the defined maximum allowed transmit jitter in the specific Implementation Agreement
5. Worst case transmitter return loss described as a parallel RC elements, see 2.E.6.

Reference Receiver:

1. No sampling jitter
2. No equalisation
3. A sampling point defined at the midpoint between the average zero crossings of the differential signal
4. Worst case receiver return loss described as a parallel RC elements, see 2.E.6.
5. A BER as per [13].

4.3 Electrical Characteristics

Refer to [13] for detailed information on SxI-5, [10] for detailed information on SFI-4.2, [11] for detailed information on SFI-5.1 and [12] for detailed information on SPI-5.1.

Note these implementation agreements require that one drop the high frequency jitter tolerance number by 0.1UI for the addition of the sinusoidal jitter.

4.A Appendix - StatEye.org Template

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5 TFI-5 Interface

5.1 Introduction

This clause details the requirements for the TFI-5 electrical interface.

5.2 General Requirements

This clause uses “Method B” of the “Jitter and Interoperability Methodology” section.

5.2.1 Channel Compliance

As per 2.2.2, with the following reference transmitter and reference receiver (note these conditions do not specify any required implementation but rather indicate a methodology for testing channel compliance), and shall meet the received eye mask as specified in [4].

Also refer to Appendix 3.A for more information on the channel characteristics.

Reference Transmitter:

1. A single post tap transmitter, with ≤ 3dB of emphasis and infinite precision accuracy.
2. A maximum amplitude equal to the defined minimum transmit amplitude in the specific Implementation Agreement
3. A jitter distribution equal to the defined maximum allowed transmit jitter in the specific Implementation Agreement
4. At the maximum baud rate as defined by the specific Implementation Agreement
5. Worst case transmitter return loss described as a parallel RC elements, see 2.E.6.
6. A concatenated first order low pass transmit filter with 0.75 times baud rate.

Reference Receiver:

1. No sampling jitter
2. No equalisation
3. A sampling point defined at the midpoint between the average zero crossings of the differential signal
4. Worst case receiver return loss described as a parallel RC elements, see 2.E.6.
5. A BER as per [4].

5.3 Electrical Characteristics

Refer to [4] for detailed information on TFI-5.

Note this implementation agreement requires that one drop the high frequency jitter tolerance number by 0.1UI for the addition of the sinusoidal jitter.

5.A Appendix - StatEye.org Template

```
%%%
```

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%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% set the de-emphasis of 4-point transmit pulse
% the de-emphasis run if param.txpre = [] and param.txpost = []

param.txdeemphasis = [1 1 1 1];            % de-emphasis is off

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% set the data coding changing the transmit pulse spectrum
% the coding run if param.txpre = [] and param.txpost = []

param.datacoding = 1;        % the coding is off

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% set PAM amplitude and rate

param.PAM = 2;              % PAM is switched off

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% the rx sample point does not need to be changed as it is
% automatically adjusted by the optimisation scripts.
% The number of DFE taps should be set, however, the initial
% conditions are irrelevant.

param.rxsample                    = -0.1;

% no DFE
param.dfe                         = [];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% sampling jitter in HPJpp and GJrms is defined here

param.txdj                        = 0.175;
param.txrj                        = 0.175/(2*7.04);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% the following options are not yet implemented and should
% not be changed

param.user                        = [0.0];
param.useuser                     = 'no';
param.usesymbol                   = '';
param.xtAmp                       = 1.0;
```

```
%%%
```

6 CEI-6G-SR Short Reach Interface

6.1 Introduction

This clause details the requirements for the CEI-6G-SR short-reach high speed electrical interface between nominal baud rates of 4.976Gsym/s to 6.375Gsym/s using NRZ coding (hence 1 bit per symbol at the electrical level). A compliant device must meet all of the requirements listed below. The electrical interface is based on high speed, low voltage logic with nominal differential impedance of 100Ω. Connections are point-to-point balanced differential pair and signaling is unidirectional.

The electrical IA is based on loss & jitter budgets and defines the characteristics required to communicate between a CEI-6G-SR driver and a CEI-6G-SR receiver using copper signal traces on a printed circuit board. The characteristic impedance of the signal traces is nominally 100Ω differential. These characteristics are normative for the devices and informative for the channel. Rather than specifying materials, channel components, or configurations, the IA focuses on effective channel characteristics. Hence a short length of poorer material should be equivalent to a longer length of premium material. A 'length' is effectively defined in terms of its attenuation rather than physical length.

Short reach CEI-6G-SR devices from different manufacturers shall be inter-operable.

6.2 Requirements

1. Support serial baud rate from 4.976Gsym/s to 6.375Gsym/s.
2. Capable of low bit error rate (required BER of 10^{-15}).
3. Capable of driving 0 – 200mm of PCB and up to 1 connector.
4. Shall support AC coupled operation and optionally DC-coupled operation.
5. Shall allow multi-lanes (1:N).
6. Shall support hot plug.

6.3 General Requirements

This clause uses "Method B" of the Jitter and Interoperability Methodology section.

6.3.1 Data Patterns

Please refer to 3.2.1

6.3.2 Signal levels

Please refer to 3.2.2 and 6.4.1.

6.3.3 Signal Definitions

Please refer to 1.A

6.3.4 Bit Error Ratio

Please refer to 3.2.3

6.3.5 Ground Differences

Please refer to 3.2.4

6.3.6 Cross Talk

Please refer to 3.2.5

6.3.7 Channel Compliance

As per 2.2.2, with the following reference transmitter and reference receiver (note these conditions do not specify any required implementation but rather indicate a methodology for testing channel compliance), and shall meet the received eye mask as specified in Figure 1-5 and Table 6-8.

Also refer to Appendix 3.A for more information on the channel characteristics.

Reference Transmitter:

1. A single post tap transmitter, with ≤ 3dB of emphasis and infinite precision accuracy.
2. A transmit amplitude of 400mVppd
3. Additional Uncorrelated Bounded High Probability Jitter of 0.15UIpp (emulating part of the Tx jitter)
4. Additional Uncorrelated Unbounded Gaussian Jitter of 0.15UIpp (emulating part of the Tx jitter)
5. A Tx edge rate filter: simple 20dB/dec low pass at 75% of baud rate, this is to emulate a Tx -3dB bandwidth at $^{3}/_{4}$ baud rate.
6. At the maximum baud rate that the channel is to operate at or 6.375Gsym/s which ever is the lowest.
7. Worst case transmitter return loss described as a parallel RC elements, see 2.E.6.

Reference Receiver:

1. No Rx equalization and the Rx bandwidth is assumed to be infinite.
2. Worst case receiver return loss described as a parallel RC elements, see 2.E.6.
3. A BER as per 6.3.4.
4. A sampling point defined at the midpoint between the average zero crossings of the differential signal

6.4 Electrical Characteristics

The electrical interface is based on high speed, low voltage logic with nominal differential impedance of 100Ω. Connections are point-to-point balanced differential pair and signaling is unidirectional.

6.4.1 Driver Characteristics

The key driver characteristics are summarized in Table 6-1 and Table 6-2 while the following sub-clauses fully detail all the requirements.

Table 6-1. CEI-6G-SR Transmitter Output Electrical Specifications

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	T_Baud	See 6.4.1.2	4.976		6.375	Gsym/s
Output Differential voltage (into floating load Rload=100Ω)	T_Vdiff	See 6.4.1.3	400		750	mVppd
Differential Resistance	T_Rd	See 6.4.1.5	80	100	120	Ω
Recommended output rise and fall times (20% to 80%)	T_tr, T_tf	See 6.4.1.4	30			ps
Differential Output Return Loss (100MHz to 0.75*T_Baud)	T_SDD22	See 6.4.1.5			-8	dB
Differential Output Return Loss (0.75*T_Baud to T_Baud)						
Common Mode Return Loss (100MHz to 0.75 *T_Baud)	T_SCC22	See 6.4.1.5			-6	dB
Transmitter Common Mode Noise	T_Ncm				5% of T_Vdiff	mVppd

NOTES:
1. For all Load Types: R_Rdin = 100Ω± 20Ω. For Vcm definition, see Figure 1-1
2. Load Type 0 with min T_Vdiff, AC-Coupling or floating load.
3. For Load Types 1 through 3: R_Zvtt ≤ 30Ω; Vtt is defined for each load type as follows: Load Type 1 R_Vtt = 1.2V +5%/-8%; Load Type 2 R_Vtt = 1.0V +5%/-8%; Load Type 3 R_Vtt = 0.8V +5%/-8%.
4. DC Coupling compliance is optional (Type 1 through 3). Only Transmitters that support DC coupling are required to meet this parameter. It is acceptable for a Transmitter to restrict the range of T_Vdiff in order to comply with the specified T_Vcm range. For a Transmitter which supports multiple T_Vdiff levels, it is acceptable for a Transmitter to claim DC Coupling Compliance if it meets the T_Vcm ranges for at least one of its T_Vdiff setting as long as those setting(s) that are compliant are indicated.
5. Simple CML Transmitters designed using Vdd ≥ 1.2V may still claim DC compliance if this parameter is not met.
6. Simple CML Transmitters designed using Vdd ≤ 0.8V may still claim DC compliance if this parameter is not met.

Table 6-1. CEI-6G-SR Transmitter Output Electrical Specifications

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Output Common Mode Voltage See Note 1, 3, 4 Also see 3.2.2	T_Vcm	Load Type 0 Note 2	0.0		1.8	V
		Load Type 1 Note 6	735		1135	mV
		Load Type 2	550		1060	mV
		Load Type 3 Note 5	490		850	mV

NOTES:
1. For all Load Types: R_Rdin = 100Ω± 20Ω. For Vcm definition, see Figure 1-1
2. Load Type 0 with min T_Vdiff, AC-Coupling or floating load.
3. For Load Types 1 through 3: R_Zvtt ≤ 30Ω; Vtt is defined for each load type as follows: Load Type 1 R_Vtt = 1.2V +5%/-8%; Load Type 2 R_Vtt = 1.0V +5%/-8%; Load Type 3 R_Vtt = 0.8V +5%/-8%.
4. DC Coupling compliance is optional (Type 1 through 3). Only Transmitters that support DC coupling are required to meet this parameter. It is acceptable for a Transmitter to restrict the range of T_Vdiff in order to comply with the specified T_Vcm range. For a Transmitter which supports multiple T_Vdiff levels, it is acceptable for a Transmitter to claim DC Coupling Compliance if it meets the T_Vcm ranges for at least one of its T_Vdiff setting as long as those setting(s) that are compliant are indicated.
5. Simple CML Transmitters designed using Vdd ≥ 1.2V may still claim DC compliance if this parameter is not met.
6. Simple CML Transmitters designed using Vdd ≤ 0.8V may still claim DC compliance if this parameter is not met.

Table 6-2. CEI-6G-SR Transmitter Output Jitter Specifications

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Uncorrelated High Probability Jitter	T_UHPJ	See 6.4.1.8			0.15	UIpp
Duty Cycle Distortion	T_DCD	See 6.4.1.8			0.05	UIpp
Total Jitter	T_TJ	See 6.4.1.8			0.30	UIpp
Eye Mask	T_X1	See 6.4.1.8			0.15	UI
Eye Mask	T_X2	See 6.4.1.8			0.40	UI
Eye Mask	T_Y1	See 6.4.1.8	200			mV
Eye Mask	T_Y2	See 6.4.1.8			375	mV

NOTES:

6.4.1.1 Driver Test Load

Please refer to 3.2.6

6.4.1.2 Driver Baud Rate

All devices shall work from 4.976Gsym/s to the maximum baud rate specified for the device, with the baud rate tolerance as per 3.2.11. Note that implementation of specific protocols will define the operating baud rate without affecting CEI compliance.

6.4.1.3 Driver Amplitude and Swing

Driver differential output amplitude shall be between 400 to 750mVppd either with or without any transmit emphasis. Absolute driver output voltage shall be between -0.1V and 1.9V with respect to local ground. See Figure 1-1 for an illustration of absolute driver output voltage limits and definition of differential peak-to-peak amplitude.

6.4.1.4 Driver Rise and Fall Times

The recommended minimum differential rise and fall times are 30ps as measured between the 20% and 80% of the maximum measured levels; the maximum differential rise and fall times are defined by the Tx eye diagram (Figure 1-4 and Table 6-4). Shorter rise and fall times may result in excessive high frequency components and increase EMI and cross talk.

6.4.1.5 Driver Resistance and Return Loss

As per 3.2.10, with the following parameters.

Table 6-3. CEI-6G-SR Driver Return Loss Parameters

Parameter	Value	Units
A0	-8	dB
f0	100	MHz
f1	$T_\text{Baud} \times \frac{3}{4}$	Hz
f2	T_Baud	Hz
Slope	16.6	dB/dec

6.4.1.6 Driver Lane-to-Lane Skew

Please refer to 3.2.7

6.4.1.7 Driver Short Circuit Current

Please refer to 3.2.9

6.4.1.8 Driver Template and Jitter

As per 2.2.3 for a BER as per 6.3.4, the driver shall satisfy both the near-end and far-end eye template and jitter requirements as given in Figure 1-4, Table 6-4, Figure 1-5 and Table 6-8 either with or without any transmit emphasis.

The maximum near-end duty cycle distortion (T_DCD) shall be less than 0.05UIpp.

It should be noted that it is assumed the Uncorrelated High Probability Jitter component of the driver jitter is not Inter-symbol Interference (ISI). This is only assumed from a receiver point of view and does not in any way put any restrictions on the real driver HPJ.

Table 6-4. CEI-6G-SR Near-End (Tx) Template Intervals

Characteristics	Symbol	Near-End Value	Units
Eye Mask	T_X1	0.15	UI
Eye Mask	T_X2	0.40	UI
Eye Mask	T_Y1	200	mV
Eye Mask	T_Y2	375	mV
Uncorrelated Bounded High Probability Jitter	T_UBHPJ	0.15	UIpp
Duty Cycle Distortion	T_DCD	0.05	UIpp
Total Jitter	T_TJ	0.30	UIpp

6.4.1.9 Driver Training Pattern

There is no requirement at the electrical level for a training pattern, however there may be a training pattern requirement(s) at the protocol level.

6.4.2 Receiver Characteristics

The key receiver characteristics are summarized in Table 6-5 and Table 6-6 while the following sub-clauses fully detail all the requirements.

Table 6-5. CEI-6G-SR Receiver Electrical Input Specifications

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Rx Baud Rate	R_Baud	See 6.4.2.1	4.976		6.375	Gsym/s
Input Differential voltage	R_Vdiff	See 6.4.2.3	125		750	mVppd
Differential Resistance	R_Rdin	See 6.4.2.7	80	100	120	Ω
Bias Voltage Source Impedance (load types 1 to 3)	R_Zvtt	See Note 1			30	Ω
Differential Input Return Loss (100MHz to 0.75*R_Baud)	R_SDD11	See 6.4.2.7			-8	dB
Differential Input Return Loss (0.75*R_Baud to R_Baud))						
Common mode Input Return Loss (100MHz to 0.75 *R_Baud)	R_SCC11	See 6.4.2.7			-6	dB

NOTES:
1. DC Coupling compliance is optional. For Vcm definition, see Figure 1-1
2. Receiver is required to implement at least one of specified nominal R_Vtt values, and typically implements only one of these values. Receiver is only required to meet R_Vrcm parameter values that correspond to R_Vtt values supported.
3. Input common mode voltage for AC-coupled or floating load input with min T_Vdiff,
4. For floating load, input resistance must be ≥ 1kΩ.

Table 6-5. CEI-6G-SR Receiver Electrical Input Specifications

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Termination Voltage Note 1, 2	R_Vtt	R_Vtt floating, Note 4	Not Specified			V
		R_Vtt = 1.2V Nominal	1.2 - 8%		1.2 + 5%	V
		R_Vtt = 1.0V Nominal	1.0 - 8%		1.0 + 5%	V
		R_Vtt = 0.8V Nominal	0.8 - 8%		0.8 + 5%	V
Input Common Mode Voltage Note 1, 2	R_Vrcm	R_Vtt floating, Note 3, 4	-0.05		1.85	V
		R_Vtt = 1.2V Nominal	720		R_Vtt - 10	mV
		R_Vtt = 1.0V Nominal	535		R_Vtt + 125	mV
		R_Vtt = 0.8V Nominal	475		R_Vtt + 105	mV
Wander divider (in Figure 2-30 & Figure 2-31)	n			10		

NOTES:
1. DC Coupling compliance is optional. For Vcm definition, see Figure 1-1
2. Receiver is required to implement at least one of specified nominal R_Vtt values, and typically implements only one of these values. Receiver is only required to meet R_Vrcm parameter values that correspond to R_Vtt values supported.
3. Input common mode voltage for AC-coupled or floating load input with min T_Vdiff,
4. For floating load, input resistance must be ≥ 1kΩ.

Table 6-6. CEI-6G-SR Receiver Input Jitter Tolerance Specifications

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Bounded High Probability Jitter	R_BHPJ	See 6.4.2.8			0.45	UIpp
Sinusoidal Jitter, maximum	R_SJ-max	See 6.4.2.8			5	UIpp
Sinusoidal Jitter, High Frequency	R_SJ-hf	See 6.4.2.8			0.05	UIpp
Total Jitter (Does not include Sinusoidal Jitter)	R_TJ	See 6.4.2.8			0.60	UIpp
Eye Mask	R_X1	See 6.4.2.8			0.30	UI
Eye Mask	R_Y1	See 6.4.2.8			62.5	mV
Eye Mask	R_Y2	See 6.4.2.8			375	mV

NOTES:

6.4.2.1 Input Baud Rate

All devices shall work from 4.976Gsym/s to the maximum baud rate specified for the device, with the baud rate tolerance as per 3.2.11. Note that implementation of specific protocols will define the operating baud rate without affecting CEI compliance.

6.4.2.2 Reference Input Signals

Reference input signals to the receiver have the characteristics determined by compliant driver. The reference input signal must satisfy the transmitter near-end template and jitter given in Figure 1-4 and Table 6-4, as well as the far-end eye template and jitter given in Figure 1-5 and Table 6-8, with the differential load impedance of 100Ω ±1% at DC with a return loss of better than 20dB from baud rate divided by 1667 to 1.5 times the baud rate. Note that the input signal might not meet either of these templates when the actual receiver replaces this load.

6.4.2.3 Input Signal Amplitude

The receiver shall accept differential input signal amplitudes produced by compliant transmitters connected without attenuation to the receiver. This may be larger than the 750mVppd maximum of the driver due to output/input impedances and reflections.

The minimum input amplitude is defined by the far-end driver template, the actual receiver input impedance and the loss of the actual PCB. Note that the far-end driver template is defined using a well controlled load impedance, however the real receiver is not, which can leave the receiver input signal smaller than the minimum 125mVppd.

6.4.2.4 Absolute Input Voltage

The absolute voltage levels with respect to the receiver ground at the input of the receiver are dependent on the driver implementation, the inter-ground difference, whether the receiver is AC or DC coupled, and (in the case of DC coupling load types 1 to 3) the nominal R_Vtt supported by the receiver. The voltage levels at the input of a DC coupled receiver shall be consistent with R_Vrcm and R_Vdiff values defined in Table 6-5.

The voltage levels at the input of an AC coupled receiver (if AC coupling is done within the receiver) or at the Tx side of the external AC coupling cap (if AC coupling is done externally) shall be between -0.15 to 1.95V with respect to local ground.

6.4.2.5 Input Common Mode Impedance

The input common mode impedance (R_Zvtt) at the input of the receiver is dependent on whether the receiver is AC or DC coupled. The value of R_Zvtt as measured at the input of an AC coupled receiver is undefined. The value of R_Zvtt as measured at the input of a DC coupled receiver is defined as per Table 6-5.

If AC coupling is used, it is to be considered part of the receiver for the purposes of this specification unless explicitly stated otherwise. It should be noted that various methods for AC coupling are allowed (for example, internal to the chip or done externally). See also 3.2.12 for more information.

6.4.2.6 Input Lane-to-Lane Skew

Please refer to 3.2.8

6.4.2.7 Input Resistance and Return Loss

Please refer to 3.2.10 with the following parameters.

Table 6-7. CEI-6G-SR Input Return Loss Parameters

Parameter	Value	Units
A0	-8	dB
f0	100	MHz
f1	$R_Baud \times \frac{3}{4}$	Hz
f2	R_Baud	Hz
Slope	16.6	dB/dec

6.4.2.8 Input Jitter Tolerance

As per 2.2.4, the receiver shall tolerate at least the far-end eye template and jitter requirements as given in Figure 1-5 and Table 6-8 with an additional SJ with any frequency and amplitude defined by the mask of Figure 2-4 where the minimum & maximum total wander amplitude are 0.05UIpp & 5UIpp respectively. This additional SJ component is intended to ensure margin for wander, hence is over and above any high frequency jitter from Table 6-8.

Table 6-8. CEI-6G-SR Far-End (Rx) Template Intervals

Characteristics	Symbol	Far-End Value	Units
Eye Mask	R_X1	0.30	UI
Eye Mask	R_Y1	62.5	mV
Eye Mask	R_Y2	375	mV
Uncorrelated Bounded High Probability Jitter	R_UBHPJ	0.15	UIpp
Correlated Bounded High Probability Jitter	R_CBHPJ	0.30	UIpp
Total Jitter (Does not include Sinusoidal Jitter)	R_TJ	0.60	UIpp

6.A Appendix - Link and Jitter Budgets

The primary intended application is as a point-to-point interface of up to approximately 200mm (≈8”) and up to one connector between integrated circuits using controlled impedance traces on low-cost printed circuit boards (PCBs). Informative loss and jitter budgets are presented in Table 6-9 (see also Appendix 3.A for more information) to demonstrate the feasibility of legacy FR4 epoxy PCB’s. The jitter budget is given in Table 6-10. The performance of an actual transceiver interconnect is highly dependent on the implementation.

Table 6-9. CEI-6G-SR Informative Loss, Skew and Jitter Budget

	Loss (dB)	**Differential Skew (ps)**	Bounded High Probability **(UIpp)**	**TJ (UIpp)**
Driver	0	15	0.15	0.30
Interconnect (with Connector)	6.6	25	0.15	0.15
Other	3.5		0.15	0.15
Total	10.1	40	0.45	0.60

Table 6-10. CEI-6G-SR High Frequency Jitter Budget

CEI-6G-SR	Uncorrelated Jitter		Correlated Jitter		Total Jitter				Amplitude	
	Unbounded Gaussian	High Probability	Bounded Gaussian	Bounded High Probability	Gaussian	Sinusoidal	Bounded High Probability	Total		
Abbreviation	**UUGJ**	**UHPJ**	**CBGJ**	**CBHPJ**	**GJ**	**SJ**	**HPJ**	**TJ**	**k**	
Unit	UIpp	UIpp	UIpp	UIpp	UIpp	UIpp	UIpp	UIpp		mVppd
Transmitter	**0.150**	**0.150**		**-0.200 See 1**	**0.150**		**-0.050**	**0.100**		**400.0**
Channel				0.500						
Receiver Input	**0.150**	**0.150**	**0.000**	**0.300**	**0.150**		**0.450**	**0.600**	**0.25**	**125**
Clock + Sampler	0.150	0.100		0.100						-50.0
Budget	**0.212**	**0.250**	**0.000**	**0.400**	**0.212**	**0.050**	**0.650**	**0.912**	**0.13**	**75.0**

NOTES:
1. Due to transmitter emphasis, it reduces the ISI as seen at the receiver. Thus this number is negative

6.B Appendix - StatEye.org Template

```
%%%
```

```
1
2  % set the de-emphasis of 4-point transmit pulse
3  % the de-emphasis run if param.txpre = [] and param.txpost = []
4
5  param.txdeemphasis = [1 1 1 1];          % de-emphasis is off
6
7  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
8
9  % set the data coding changing the transmit pulse spectrum
10 % the coding run if param.txpre = [] and param.txpost = []
11
12 param.datacoding = 1;       % the coding is off
13
14 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
15
16 % set PAM amplitude and rate
17
18 param.PAM = 2;             % PAM is switched off
19
20 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
21
22 % the rx sample point does not need to be changed as it is
23 % automatically adjusted by the optimisation scripts.
24 % The number of DFE taps should be set, however, the initial
25 % conditions are irrelevant.
26
27 param.rxsample                  = -0.1;
28
29 % no DFE
30 param.dfe                       = [];
31
32 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
33
34 % sampling jitter in HPJpp and GJrms is defined here
35
36 param.txdj                      = 0.15;
37 param.txrj                      = 0.15/(2*7.94);
38
39 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
40
41 % the following options are not yet implemented and should
42 % not be changed
43
44 param.user                      = [0.0];
45 param.useuser                     = 'no';
46 param.usesymbol                    = '';
47 param.xtAmp                      = 1.0;
48
49 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
param.TransmitAmplitude = 0.400; % mVppdif
param.MinEye            = 0.125; % mVppdif

param.Q                 = 2*7.94;
param.maxDJ             = 0.30;
param.maxTJ             = 0.60;
```

7 CEI-6G-LR Long Reach Interface

7.1 Introduction

This clause details the requirements for the CEI-6G-LR long-reach high speed electrical interface between nominal baud rates of 4.976Gsym/s to 6.375Gsym/s using NRZ coding (hence 1 bit per symbol at the electrical level). A compliant device must meet all of the requirements listed below. The electrical interface is based on high speed, low voltage logic with nominal differential impedance of 100Ω. Connections are point-to-point balanced differential pair and signaling is unidirectional.

The electrical IA is based on loss & jitter budgets and defines the characteristics required to communicate between a CEI-6G-LR driver and a CEI-6G-LR receiver using copper signal traces on a printed circuit board. The characteristic impedance of the signal traces is nominally 100Ω differential. These characteristics are normative for the devices and informative for the channel. Rather than specifying materials, channel components, or configurations, the IA focuses on effective channel characteristics. Hence a short length of poorer material should be equivalent to a longer length of premium material. A 'length' is effectively defined in terms of its attenuation rather than physical length.

Long reach CEI-6G-LR devices from different manufacturers shall be inter-operable.

7.2 Requirements

1. Support serial baud rate from 4.976Gsym/s to 6.375Gsym/s.
2. Capable of low bit error rate (required BER of 10^{-15}).
3. Capable of driving 0 – 1m of PCB (such as IEEE 802.3 XAUI/TFI-5 compliant backplane) and up to 2 connector.
4. Shall support AC coupled operation and optionally DC-coupled operation.
5. Shall allow multi-lanes (1:N).
6. Shall support hot plug.

7.3 General Requirements

This clause uses "Method D" of the Jitter and Interoperability Methodology section.

7.3.1 Data Patterns

Please refer to 3.2.1

7.3.2 Signal levels

Please refer to 3.2.2 and 7.4.1.

7.3.3 Signal Definitions

Please refer to 1.A

7.3.4 Bit Error Ratio

Please refer to 3.2.3

7.3.5 Ground Differences

Please refer to 3.2.4

7.3.6 Cross Talk

Please refer to 3.2.5

7.3.7 Channel Compliance

As per 2.4.2, with the following reference transmitter and reference receiver (note these conditions do not specify any required implementation but rather indicate a methodology for testing channel compliance), and shall meet the equalized eye mask as specified in Figure 1-5 and Table 7-1. However for the case of a short reach Tx talking to a long reach Rx, the Rx needs to meet all requirements as given in 6.3.7 and 6.4.2.

Also refer to Appendix 3.A for more information on the channel characteristics.

Reference Transmitter:

1. Either a single pre or post tap transmitter, with ≤ 6dB of emphasis, with infinite precision accuracy.
2. A transmit amplitude of 800mVppd.
3. Additional Uncorrelated Bounded High Probability Jitter of 0.15UIpp (emulating part of the Tx jitter)
4. Additional Uncorrelated Unbounded Gaussian Jitter of 0.15UIpp (emulating part of the Tx jitter)
5. A Tx edge rate filter: simple 40dB/dec low pass at 75% of baud rate, this is to emulate both Rx and Tx -3dB bandwidths at $^{3}/_{4}$ baud rate.
6. At the maximum baud rate that the channel is to operate at or 6.375Gsym/s which ever is lowest
7. Worst case transmitter return loss described as a parallel RC elements, see 2.E.6.

Reference Receiver:

1. Rx equalization: 5 tap DFE, with infinite precision accuracy and having the following restriction on the coefficient values:

   Let W[N] be sum of DFE tap coefficient weights from taps N through M where

   N = 1 is previous decision (i.e. first tap)
   M = oldest decision (i.e. last tap)
   R_Y2 = T_Y2 = 400mV
   Y = min(R_X1, (R_Y2 - R_Y1) / R_Y2) = 0.30
   Z = $^2/_3$ = 0.66667

   Then $W[N] \leq Y * Z^{(N - 1)}$

   For the channel compliance model the number of DFE taps (M) = 5. This gives the following maximum coefficient weights for the taps:

   W[1] ≤ 0.3000 (sum of taps 1 to 5)
   W[2] ≤ 0.2000 (sum of taps 2 to 5)
   W[3] ≤ 0.1333 (sum of taps 3 to 5)
   W[4] ≤ 0.0889 (sum of taps 4 and 5)
   W[5] ≤ 0.0593 (tap 5)

   Notes:
   - These coefficient weights are absolute assuming a T_Vdiff of 1Vppd
   - For a real receiver the restrictions on tap coefficients would apply for the actual number of DFE taps implemented (M)
2. Worst case receiver return loss described as a parallel RC elements, see 2.E.6.
3. A BER as per 3.2.3.

Table 7-1. CEI-6G-LR Receiver Equalization Output Eye Mask

Parameter	Symbol	Max	Units
Eye mask	R_X1	0.3	UI
Eye mask	R_Y1	50	mV
Bounded High Probability Jitter	R_BHPJ	0.325	UI

7.4 Electrical Characteristics

The electrical interface is based on high speed, low voltage logic with nominal differential impedance of 100Ω. Connections are point-to-point balanced differential pair and signaling is unidirectional.

7.4.1 Driver Characteristics

The key driver characteristics are summarized in Table 7-2 and Table 7-3 while the following sub-clauses fully detail all the requirements.

Table 7-2. CEI-6G-LR Transmitter Output Electrical Specifications

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	T_Baud	See 7.4.1.2	4.976		6.375	Gsym/s
Output Differential voltage (into floating load Rload=100Ω)	T_Vdiff	See 7.4.1.3 & Note 1	800		1200	mVppd
Differential Resistance	T_Rd	See 7.4.1.5	80	100	120	Ω
Recommended output rise and fall times (20% to 80%)	T_tr, T_tf	See 7.4.1.4	30			ps
Differential Output Return Loss (100MHz to 0.75*T_Baud)	T_SDD22	See 7.4.1.5			-8	dB
Differential Output Return Loss (0.75*T_Baud to T_Baud)						
Common Mode Return Loss (100MHz to 0.75 *T_Baud)	T_S11	See 7.4.1.5			-6	dB
Transmitter Common Mode Noise	T_Ncm				5% of T_Vdiff	mVppd
Output Common Mode Voltage See Notes 2, 3 & 4 See also 3.2.2	T_Vcm	Load Type 0 See Note 2	100		1700	mV
		Load Type 1 See Note 3 & 4	630		1100	mV

NOTES:
1. The Transmitter must be capable of producing a minimum T_Vdiff greater than or equal to 800 mVppd. In applications where the channel is better than the worst case allowed, a Transmitter device may be provisioned to produce T_Vdiff less than this minimum value, but greater than or equal to 400 mVppd, and is still compliant with this specification.
2. Load Type 0 with min T_Vdiff, AC-Coupling or floating load.
3. For Load Type 1: R_Zvtt ≤ 30Ω; T_Vtt & R_Vtt = 1.2V +5%/-8%
4. DC Coupling compliance is optional (Load Type 1). Only Transmitters that support DC coupling are required to meet this parameter.

Table 7-3. CEI-6G-LR Transmitter Output Jitter Specifications

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Uncorrelated High Probability Jitter	T_UHPJ	See 7.4.1.8			0.15	UIpp
Duty Cycle Distortion	T_DCD	See 7.4.1.8			0.05	UIpp
Total Jitter	T_TJ	See 7.4.1.8			0.30	UIpp
Eye Mask	T_X1	See 7.4.1.8			0.15	UI
Eye Mask	T_X2	See 7.4.1.8			0.50	UI
Eye Mask	T_Y1	See 7.4.1.8	400			mV
Eye Mask	T_Y2	See 7.4.1.8			600	mV
NOTES:						

7.4.1.1 Driver Test Load

Please refer to 3.2.6

7.4.1.2 Driver Baud Rate

All devices shall work from 4.976Gsym/s to the maximum baud rate specified for the device, with the baud rate tolerance as per 3.2.11. Note that implementation of specific protocols will define the operating baud rate without affecting CEI compliance.

7.4.1.3 Driver Amplitude and Swing

Driver differential output amplitude shall be able to drive between 800 to 1200mVppd either with or without any transmit emphasis. However, for the case of this transmitter talking to a short reach receiver, the differential output amplitude shall be between 400 to 750mVppd either with or without any transmit emphasis. DC referenced logic levels are not defined since the receiver must have high common mode impedance at DC. However, absolute driver output voltage shall be between -0.1 V and 1.9 V with respect to local ground. See Figure 1-1 for an illustration of absolute driver output voltage limits and definition of differential peak-to-peak amplitude.

7.4.1.4 Driver Rise and Fall Times

The recommended minimum differential rise and fall time is 30ps as measured between the 20% and 80% of the maximum measured levels; the maximum differential rise and fall times are defined by the Tx eye diagram (Figure 1-4 and Table 7-5). Shorter rise and falls may result in excessive high frequency components and increase EMI and cross talk.

7.4.1.5 Output Resistance and Return Loss

Please refer to 3.2.10 with the following parameters.

Table 7-4. CEI-6G-LR Driver Return Loss Parameters

Parameter	Value	Units
A0	-8	dB
f0	100	MHz
f1	$T_\mathrm{Baud} \times \frac{3}{4}$	Hz
f2	R_Baud	Hz
Slope	16.6	dB/dec

7.4.1.6 Driver Lane-to-Lane Skew

Please refer to 3.2.7

7.4.1.7 Driver Short Circuit Current

Please refer to 3.2.9

7.4.1.8 Driver Template and Jitter

As per 2.4.3 for a BER as per 7.3.4, the driver shall satisfy both the near-end eye template & jitter requirements as given in Figure 1-4, Table 7-5 either with or without any transmit emphasis.

The maximum near-end duty cycle distortion (T_DCD) shall be less than 0.05UIpp.

It should be noted that it is assumed the Uncorrelated High Probability Jitter component of the driver jitter is not Inter-symbol Interference (ISI). This is only assumed from a receiver point of view so that a receiver can't equalize it and does not in any way put any restrictions on the real driver HPJ.

Table 7-5. CEI-6G-LR Near-End Template Intervals

Characteristics	Symbol	Near-End Value	Units	Comments
Eye Mask	T_X1	0.15	UI	
Eye Mask	T_X2	0.50	UI	
Eye Mask	T_Y1	400	mV	For connection to short reach Rx
		400		For connection to long reach Rx
Eye Mask	T_Y2	375	mV	For connection to short reach Rx
		600		For connection to long reach Rx
Uncorrelated Bounded High Probability Jitter	T_UBHPJ	0.15	UIpp	
Duty Cycle Distortion	T_DCD	0.05	UIpp	
Total Jitter	T_TJ	0.30	UIpp	

7.4.1.9 Driver Training Pattern

The driver is required to repeatedly transmit a "training pattern". This pattern may be needed by the receiver to aid in its power up adaptive process. The pattern is at least 384 bits long and is explained in Table 7-6. However it should be noted that other data (i.e. framing bits) may be present between the repeated groups of 384 bits.

Table 7-6. CEI-6G-LR Training Pattern

Pattern (in Hex)	Purpose
00 FF 00 FF 00 FF	48 bits - f/16 square wave
00 80 00	24 bits - positive impulse with 12 leading and trailing zeros
55 55 55 55 55 55	48 bits - f/2 square wave
FF EF FF	24 bits - negative impulse with 12 leading and trailing ones
00 FF 00 FF 00 FF	48 bits - f/16 square wave
At least 192 random or pseudo-random bits	Approximation of normal randomized data patterns (see 3.2.1)

The means to indicate to the driver when it has to send or stop the training pattern is beyond the scope of this IA.

Note there may well be other training pattern(s) requirements at the protocol level.

7.4.2 Receiver Characteristics

The key receiver characteristics are summarized in Table 7-7 while the following sub-clauses fully detail all the requirements.

Table 7-7. CEI-6G-LR Receiver Electrical Input Specifications

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Rx Baud Rate	R_Baud	See 7.4.2.1	4.976		6.375	Gsym/s
Input Differential voltage	R_Vdiff	See 7.4.2.3			1200	mVppd
Differential Resistance	R_Rdin	See 7.4.2.7	80	100	120	Ω
Bias Voltage Source Impedance (load type 1)	R_Zvtt	See Note 1			30	Ω
Differential Input Return Loss (100MHz to 0.75*R_Baud)	R_SDD11	See 7.4.2.7			-8	dB
Differential Input Return Loss (0.75*R_Baud to R_Baud))						
Common Mode Input Return Loss (100MHz to 0.75 *R_Baud)	R_SCC11	See 7.4.2.7			-6	dB
Input Common Mode Voltage See Notes: 1, 2 & 3	R_Vfcm	Load Type 0 See Note 2	0		1800	mV
		Load Type 1 Notes: 1 & 3	595		R_Vtt - 60	mV
Wander divider (in Figure 2-30 & Figure 2-31)	n			10		

NOTES:
1. DC Coupling compliance is optional (Load Type 1). Only receivers that support DC coupling are required to meet this parameter.
2. Load Type 0 with min T_Vdiff, AC-Coupling or floating load. For floating load, input resistance must be ≥ 1kΩ
3. For Load Type 1: T_Vtt & R_Vtt = 1.2V +5%/-8%.

7.4.2.1 Baud Rate

All devices shall work from 4.976Gsym/s to the maximum baud rate specified for the device, with the baud rate tolerance as per 3.2.11. Note that implementation of specific protocols will define the operating baud rate without affecting CEI compliance.

7.4.2.2 Reference Input Signals

Reference input signals to the receiver have the characteristics determined by compliant driver. The reference input signal must satisfy the transmitter near-end template and jitter given in Figure 1-4 and Table 7-5, as well as the far-end eye jitter given in Table 7-10, with the differential load impedance of 100Ω ±1% at DC with a return loss of better than 20dB from baud rate divided by 1667 to 1.5 times the baud rate. Note that the input signal might not meet either of these requirements when the actual receiver replaces this load.

7.4.2.3 Input Signal Amplitude

The receiver shall accept differential input signal amplitudes produced by compliant transmitters connected without attenuation to the receiver. This may be larger than the 1200mVppd maximum of the driver due to output/input impedances and reflections.

The minimum input amplitude is defined by the far-end driver template, the actual receiver input impedance and the loss of the actual PCB. Note that the far-end driver template is defined using a well controlled load impedance, however the real receiver is not, which can leave the receiver input signal smaller than expected.

7.4.2.4 Absolute Input Voltage

The absolute voltage levels with respect to the receiver ground at the input of the receiver are dependent on the driver implementation and the inter-ground difference.

The voltage levels at the input of an AC coupled receiver (if the effective AC coupling is done within the receiver) or at the Tx side of the external AC coupling cap (if AC coupling is done externally) shall be between -0.2 to 2.0V with respect to local ground.

7.4.2.5 Input Common Mode Impedance

The input common mode impedance (R_Zvtt) at the input of the receiver is dependent on whether the receiver is AC or DC coupled. The value of R_Zvtt as measured at the input of an AC coupled receiver is undefined. The value of R_Zvtt as measured at the input of a DC coupled receiver is defined as per Table 7-7.

If AC coupling is used, it is to be considered part of the receiver for the purposes of this specification unless explicitly stated otherwise. It should be noted that various methods for AC coupling are allowed (for example, internal to the chip or done externally). See also 3.2.12 for more information.

7.4.2.6 Input Lane-to-Lane Skew

Please refer to 3.2.8

7.4.2.7 Input Resistance and Return Loss

Please refer to 3.2.10 with the following parameters.

Table 7-8. CEI-6G-LR Input Return Loss Parameters

Parameter	Value	Units
A0	-8	dB
f0	100	MHz
f1	$R_Baud \times \frac{3}{4}$	Hz
f2	R_Baud	Hz
Slope	16.6	dB/dec

7.4.2.8 Jitter Tolerance

As per 2.4.4, the receiver shall tolerate at least the far-end jitter requirements as given in Table 7-1 in combination with any compliant channel, as per 7.3.7, with an additional SJ with any frequency and amplitude defined by the mask of Figure 2-4 where the minimum & maximum total wander amplitude are 0.05UIpp & 5UIpp respectively. This additional SJ component is intended to ensure margin for wander, hence is over and above any high frequency jitter from Table 7-1.

7.A Appendix - Link and Jitter Budgets

The primarily intended application is as a point-to-point interface of up to approximately 1m (≈40") and up to two connector between integrated circuits using controlled impedance traces on low-cost printed circuit boards (PCBs). Informative loss and jitter budgets are presented in Table 7-9 (see also Appendix 3.A for more information) to demonstrate the feasibility of legacy FR4 epoxy PCB's. The jitter budget is given in Table 7-10. The performance of an actual transceiver interconnect is highly dependent on the implementation.

Table 7-9. CEI-6G-LR Informative Loss, Skew and Jitter Budget

	Loss (dB)	**Differential Skew (ps)**	Bounded High Probability **(UIpp)**	**TJ (UIpp)**
Driver	0	15	0.15	0.30
Interconnect (with Connector)	15.9	25	0.35	0.513
Other	4.5		0.10	0.262
Total	20.4	40	0.60	0.875

Table 7-10. CEI-6G-LR High Frequency Jitter Budget

CEI-6G-LR	Uncorrelated Jitter		Correlated Jitter		Total Jitter				Amplitude	
	Unbounded Gaussian	High Probability	Bounded Gaussian	Bounded High Probability	Gaussian	Sinusoidal	Bounded High Probability	Total		
Abbreviation	**UUGJ**	**UHPJ**	**CBGJ**	**CBHPJ**	**GJ**	**SJ**	**HPJ**	**TJ**	**k**	
Unit	UIpp	UIpp	UIpp	UIpp	UIpp	UIpp	UIpp	UIpp		mVppd
Transmitter	**0.150**	**0.150**			**0.150**		**0.150**	**0.300**		**800.0**
Channel			0.230	0.525						
Receiver Input	**0.150**	**0.150**	**0.230**	**0.525**	**0.275**		**0.675**	**0.950**	**0.00**	**0.0 See 2**
Equalizer				-0.350 See 1						
Post Equalization	**0.150**	**0.150**	**0.230**	**0.175**	**0.275**		**0.325**	**0.60**	**0.20**	**100.0**
DFE Penalties				0.100					-0.08	-45.0
Clock + Sampler	0.150	0.100		0.100						-45.0
Budget	**0.212**	**0.250**	**0.230**	**0.375**	**0.313**	**0.050**	**0.625**	**0.988**	**0.06**	**10.0**

NOTES:
1. Due to receiver equalization, it reduces the ISI as seen inside the receiver. Thus this number is negative.
2. It is assumed that the eye is closed at the receiver, hence receiver equalization is required as indicated below.

7.B Appendix - StatEye.org Template

```
%%%
```

```
1
2  % set the de-emphasis of 4-point transmit pulse
3  % the de-emphasis run if param.txpre = [] and param.txpost = []
4
5  param.txdeemphasis = [1 1 1 1];            % de-emphasis is off
6
7  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
8
9  % set the data coding changing the transmit pulse spectrum
10 % the coding run if param.txpre = [] and param.txpost = []
11
12 param.datacoding = 1;        % the coding is off
13
14 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
15
16 % set PAM amplitude and rate
17
18 param.PAM = 2;              % PAM is switched off
19
20 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
21
22 % the rx sample point does not need to be changed as it is
23 % automatically adjusted by the optimisation scripts.
24 % The number of DFE taps should be set, however, the initial
25 % conditions are irrelevant.
26
27 param.rxsample                    = -0.1;
28
29 param.dfe                         = [0.3 0.1 0.1 0.1 0.1];
30
31 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
32
33 % sampling jitter in HPJpp and GJrms is defined here
34
35 param.txdj                        = 0.15;
36 param.txrj                        = 0.15/(2*7.94);
37
38 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
39
40 % the following options are not yet implemented and should
41 % not be changed
42
43 param.user                        = [0.0];
44 param.useuser                       = 'no';
45 param.usesymbol                     = '';
46 param.xtAmp                       = 1.0;
47
48 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
49
```

```
param.TransmitAmplitude = 0.800; % mVppdif
param.MinEye            = 0.100; % mVppdif

param.Q                 = 2*7.94;
param.maxDJ             = 0.325;
param.maxTJ             = 0.60;
```

8 CEI-11G-SR Short Reach Interface

This clause details the requirements for the CEI-11G-SR short-reach high speed electrical interface between nominal baud rates of 9.95 Gsym/s to 11.2 Gsym/s using NRZ coding. A compliant device must meet all of the requirements listed below. The electrical interface is based on high speed, low voltage logic with nominal differential impedance of 100 Ω. Connections are point-to-point balanced differential pair and signaling is unidirectional.

The electrical IA is based on loss & jitter budgets and defines the characteristics required to communicate between a CEI-11G-SR driver and a CEI-11G-SR receiver using copper signal traces on a printed circuit board. The characteristic impedance of the signal traces is nominally 100 Ω differential. These characteristics are normative for the devices and informative for the channel. Rather than specifying materials, channel components, or configurations, the IA focuses on effective channel characteristics. Hence a short length of poorer material should be equivalent to a longer length of premium material. A 'length' is effectively defined in terms of its attenuation rather than physical length.

Short reach CEI-11G-SR devices from different manufacturers shall be inter-operable.

8.1 Requirements

1. Support serial data rate from 9.95 Gsym/s to 11.2 Gsym/s.
2. Capable of low bit error rate (required BER[1] of 10^{-15}).
3. Capable of driving 0 – 200 mm of PCB and up to 1 connector.
4. Shall support AC-coupled and optionally DC-coupled operation.
5. Shall allow multi-lanes (1 to n).
6. Shall support hot plug.

8.2 General Requirements

This clause uses "Method E" of the Jitter and Interoperability Methodology section.

8.2.1 Data Patterns

Please refer to 3.2.1

1. If optical components are included, i.e XFP modules, the BER is constrained by the optical specification.

8.2.2 Signal levels

Please refer to 3.2.2

8.2.3 Signal Definitions

Please refer to 1.A

8.2.4 Bit Error Ratio

Please refer to 3.2.3[1]

8.2.5 Ground Differences

Please refer to 3.2.4

8.2.6 Cross Talk

Please refer to 3.2.5

8.2.7 Channel Compliance

As per 2.5.2, with the following reference transmitter and reference receivers (note these conditions do not specify any required implementation but rather indicate a methodology for testing channel compliance), and shall meet the receive eye mask as specified in Figure 1-5 and Table 8-5 when:

a. Using reference receiver A and Electrical Characteristic R_X1 less R_SJ-hf in Table 8-5

b. Using reference receiver B and Electrical Characteristic R_X1LessCBHPJ in Table 8-5

Also refer to Appendix 3.A for more information on the channel characteristics.

Reference Transmitter:

1. A transmitter with no emphasis
2. A transmit amplitude of both 360 mVppd and 770 mVppd
3. Additional Uncorrelated Bounded High Probability Jitter of 0.15 UIpp (emulating part of the Tx jitter)
4. Additional Uncorrelated Unbounded Gaussian Jitter of 0.15UIpp (emulating part of the Tx jitter)
5. At the maximum baud rate that the channel is to operate at or 11.2Gsym/s which ever is the lowest.

1. If optical components are included, i.e XFP modules, the BER is constrained by the optical specification.

6. A Tx edge rate filter: simple 20dB/dec low pass at 75% of baud rate, this is to emulate a Tx -3dB bandwidth at $^3/_4$ baud rate.
7. Worst case transmitter return loss described as a parallel RC elements, see 2.E.6.

Reference Receiver A:

1. No Rx equalization and the Rx bandwidth is assumed to be infinite.
2. Worst case receiver return loss described as a parallel RC elements, see 2.E.6.
3. A BER[1] as per 3.2.3.
4. A wander divider (n in Figure 2-30 & Figure 2-31) equal to 10
5. A sampling point defined at the midpoint between the average zero crossings of the differential signal

Reference Receiver B[2]:

1. A receiver with a single zero single pole filter (as per Annex 2.B.8) and the Rx bandwidth is assumed to be infinite.
2. Worst case receiver return loss described as a parallel RC elements, see 2.E.6.
3. A BER[1] as per 3.2.3.
4. A wander divider (n in Figure 2-30 & Figure 2-31) equal to 10
5. A sampling point defined at the midpoint between the average zero crossings of the differential signal

8.3 Electrical Characteristics

The electrical signaling is based on high speed low voltage logic with a nominal differential impedance of 100 Ω.

All devices shall work from 9.95Gsym/s to the maximum baud rate specified for the device, with the baud rate tolerance as per 3.2.11. Note that implementation of specific protocols will define the operating baud rate without affecting CEI compliance.

8.3.1 Driver Characteristics

The driver electrical specifications at compliance point T are given in tableTable 8-1. As per 2.4.3, the driver shall satisfy both the near-end and far-end eye template and jitter requirements as given in Figure 1-4, Table 8-2, Figure 1-5 and Table 8-5. It is assumed

1. If optical components are included, i.e XFP modules, the BER is constrained by the optical specification.
2. Reference receiver B allows compliance to XFP Rev. 3.1 (10 gigabit Small form factor Pluggable Module) April 25th 2003

that the UBHPJ component of the driver jitter is not Inter-symbol Interference (ISI), hence it cannot be equalized in the receiver. To attenuate noise and absorb even/odd mode reflections, the source must provide a common mode return path.

For termination and DC-blocking information, please refer to 3.2.12

Table 8-1. Transmitter Electrical Output Specification.

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	T_Baud		9.95		11.2	Gsym/s
Output Differential Voltage	T_Vdiff		360		770	mVppd
Differential Resistance	T_Rd		80	100	120	Ω
Differential Termination Resistance Mismatch	T_Rdm				5	%
Output Rise and Fall Time (20% to 80%)	T_tr, T_tf		24			ps
Differential Output Return Loss	T_SDD22	See 8.3.1.3				dB
Common mode Output Return Loss	T_SCC22	See 8.3.1.3			-6	dB
Transmitter Common Mode Noise	T_Ncm				15	mVrms
Output Common Mode Voltage Note 1, 3, 4	T_Vcm	Load Type 0 Note 2	0.05		3.55	V
		Load Type 1 Note 6	735		1135	mV
		Load Type 2	550		1060	mV
		Load Type 3 Note 5	490		850	mV

NOTES:
1. For Load Types 1, 2 and 3: R_Rdin = 100 ohms ± 20 ohms, R_Zvtt ≤ 30 ohms. For Vcm definition, see Figure 1-1
2. Load Type 0, AC-Coupling or floating load, R_Rdin = 100 ohms ± 20 ohms.Number includes ground difference
3. For Load Types 1 through 3: Vtt is defined for each load type as follows: Load Type 1 R_Vtt = 1.2V +5% / -8%; Load Type 2 R_Vtt = 1.0V +5% / -8%; Load Type 3 R_Vtt = 0.8V +5% / -8%.
4. DC Coupling compliance is optional (Type 1 through 3). Only Transmitters that support DC coupling are required to meet this parameter. It is acceptable for a Transmitter to restrict the range of T_Vdiff in order to comply with the specified T_Vcm range. For a Transmitter which supports multiple T_Vdiff levels, it is acceptable for a Transmitter to claim DC Coupling Compliance if it meets the T_Vcm ranges for at least one of it's T_Vdiff setting as long as those setting(s) are that are compliant are indicated
5. Simple CML Transmitters designed using Vdd ≥ 1.2V may still claim DC compliance if this parameter is not met.
6. Simple CML Transmitters designed using Vdd ≤ 0.8V may still claim DC compliance if this parameter is not met.

Table 8-2. Transmitter Output Jitter Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Uncorrelated Bounded High Probability Jitter	T_UBHPJ				0.15	UIpp
Uncorrelated Unbounded Gaussian Jitter	T_UUGJ	Note 1			0.15	UIpp
Total Jitter	T_TJ				0.30	UIpp
Eye Mask	T_X1				0.15	UI
Eye Mask	T_X2				0.4	UI
Eye Mask	T_Y1		180			mV
Eye Mask	T_Y2				385	mV

NOTES:
1. BER=10^{-15}, Q=7.94

8.3.1.1 Driver Baud Rate

All devices shall work from 9.95Gsym/s to the maximum baud rate specified for the device, with the baud rate tolerance as per 3.2.11.

8.3.1.2 Driver Test Load

Please refer to 3.2.6.

8.3.1.3 Driver Resistance and Return Loss

Please refer to 3.2.10 with the following parameters..

Table 8-3. Driver Return Loss Parameters

Parameter	Value	Units
A0	-8	dB
f0	100	MHz
f1	$T_\text{Baud} \times \frac{3}{4}$	Hz
f2	$T_\text{Baud} \times \frac{3}{2}$	Hz
Slope	16.6	dB/dec

8.3.1.4 Driver Lane-to-Lane Skew

Please refer to 3.2.7

8.3.1.5 Driver Short Circuit Current

Please refer to 3.2.9

8.3.2 Receiver Characteristics

Receiver electrical specifications are given in Table 8-4 and measured at compliance point R. To dampen noise sources and absorption of both even and odd mode reflections, the source in addition to improve differential termination must provide a common mode return path. Jitter specifications at reference R are listed in Table 8-5 and the compliance mask is shown in Figure 1-5.

As per 2.2.4, the receiver shall tolerate at least the far-end eye template and jitter requirements as given in Figure 1-5 and Table 8-5 with an additional SJ with any frequency and amplitude defined by the mask of Figure 2-4 where the maximum total wander amplitude is 5UIpp. This additional SJ component is intended to ensure margin for wander.

For termination and DC-blocking information, please refer to 3.2.12.

Table 8-4. Receiver Electrical Input Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	R_Baud		9.95		11.2	Gsym/s
Input Differential Voltage	R_Vdiff		110		1050	mVppd
Differential Input Resistance	R_Rdin		80	100	120	Ω
Receiver Common Mode Noise	R_Ncm				25	mVrms
Input Resistance Mismatch	R_Rm				5	%
Differential Input Return Loss	R_SDD11	See 8.3.2.3				dB
Common mode Return Loss	R_SCC11	See 8.3.2.3			-6	dB
Differential to Common mode input conversion	R_SCD11	See 8.3.2.3			-12	dB
Termination Voltage Note 1, 2	R_Vtt	R_Vtt floating, Note 3	Not Specified			V
		R_Vtt = 1.2V Nominal	1.2 - 8%		1.2 + 5%	V
		R_Vtt = 1.0V Nominal	1.0 - 8%		1.0 + 5%	V
		R_Vtt = 0.8V Nominal	0.8 - 8%		0.8 + 5%	V
Input Common Mode Voltage Note 1, 2	R_Vrcm	R_Vtt floating, Note 3	0		3.60	V
		R_Vtt = 1.2V Nominal	720		R_Vtt -10	mV
		R_Vtt = 1.0V Nominal	535		R_Vtt +125	mV
		R_Vtt = 0.8V Nominal	475		R_Vtt +105	mV

NOTES:
1. DC Coupling compliance is optional. Only Receivers which support DC coupling are required to meet this parameter. For Vcm definition, see Figure 1-1
2. Receiver is required to implement at least one of specified nominal R_Vtt values, and typically implements only one of these values. Receiver is only required to meet R_Vrcm parameter values that correspond to R_Vtt values supported.
3. Input common mode voltage for AC-coupled or floating load input.

Table 8-5. Receiver Input Jitter Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Uncorrelated Bounded High Probability Jitter	R_UBHPJ				0.25	UIpp
Correlated Bounded High probability Jitter	R_CBHPJ				0.20	UIpp
Gaussian Jitter (UUGJ + CBGJ)	R_GJ	Note 2			0.20	UIpp

NOTES:
1. TJ includes high frequency sinusoidal jitter. The receiver must tolerate the total deterministic and random jitter with addition of the sinusoidal jitter. For transparent applications the specified jitter tolerance mask replace R_SJ.
2. BER=10^{-15}, Q=7.94

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Sinusoidal Jitter, Maximum	R_SJ-max	See 2.2.4			5	UIpp
Sinusoidal Jitter, High Frequency	R_SJ-hf	See 2.2.4			0.05	UIpp
Total Jitter, including R_SJ-hf	R_TJ	Note 1			0.70	UIpp
Total Jitter excl. Correlated High Probability Jitter	R_TJLess CHPJ				0.50	UIpp
Eye Mask incl. Correlated High Probability. Jitter	R_X1				0.35	UI
Eye mask excl. Correlated High Probability Jitter	R_X1Less CHPJ				0.25	
Eye Mask	R_Y1		55			mV
Eye Mask	R_Y2				525	mV

NOTES:
1. TJ includes high frequency sinusoidal jitter. The receiver must tolerate the total deterministic and random jitter with addition of the sinusoidal jitter. For transparent applications the specified jitter tolerance mask replace R_SJ.
2. BER=10^{-15}, Q=7.94

.

8.3.2.1 Input Baud Rate

All devices shall work from 9.95Gsym/s to the maximum baud rate specified for the device, with the baud rate tolerance as per 3.2.11.

8.3.2.2 Reference Input Signals

Reference input signals to the receiver shall have the characteristics determined by a compliant driver. The reference input signal must satisfy the transmitter near-end template and jitter given in Figure 1-4 and Table 8-2, as well as the far-end eye template and jitter given in Figure 1-5 and Table 8-5, with the differential load impedance of 100Ω ±1% at DC and a return loss of better than 20dB from baud rate over 1667 to 1.5 times the baud rate. Note that the input signal might not meet either of these templates when the actual receiver replaces this load.

8.3.2.3 Input Resistance and Return Loss

Please refer to 3.2.10 with the following parameters.

Table 8-6. Driver Return Loss Parameters

Parameter	Value	Units
A0	-8	dB
f0	100	MHz
f1	$R_\text{Baud} \times \frac{3}{4}$	Hz
f2	$R_\text{Baud} \times \frac{3}{2}$	Hz
Slope	16.6	dB/dec

SCD11 relates to the conversion of Differential to Common mode and the associated generation of EMI. The common mode reference impedance is 25Ω, measurement range is f0 to f1 of Table 8-6.

8.3.2.4 Input Lane-to-Lane Skew

Please refer to *3.2.8*

8.4 Specifications for Jitter-transparent applications

The CEI interface for short reach may be used for applications where connected elements are transparent to other clock domains with requirements to jitter performance that in some implementations may interfere with the CEI jitter requirements. Consider a situation using the CEI reference model, Figure 1-6, where the Ingress Transmitter T_I does not filter the jitter from the adjacent clock domain with a low frequency low pass filter and the Egress Receiver R_E likewise pass the CEI channel jitter unfiltered to the adjacent clock domain. In this case the requirements to handle the combined jitter of the CEI interface and the adjacent clock domain is evident. In the Ingress direction the unfiltered Jitter from the input to the Ingress Transmitter will be superimposed to the jitter of the Transmitter, link and Receiver. In the Egress direction the jitter of the Transmitter, Link and Receiver will be passed beyond the Egress Receiver R_E into the adjacent clock domain. The following sections specify the requirements to devices intended for use in transparent applications. The requirements have an effect on the previously defined channel, transmitter, and receiver compliance testing and must be carefully understood, please refer to 2.5 for further details.

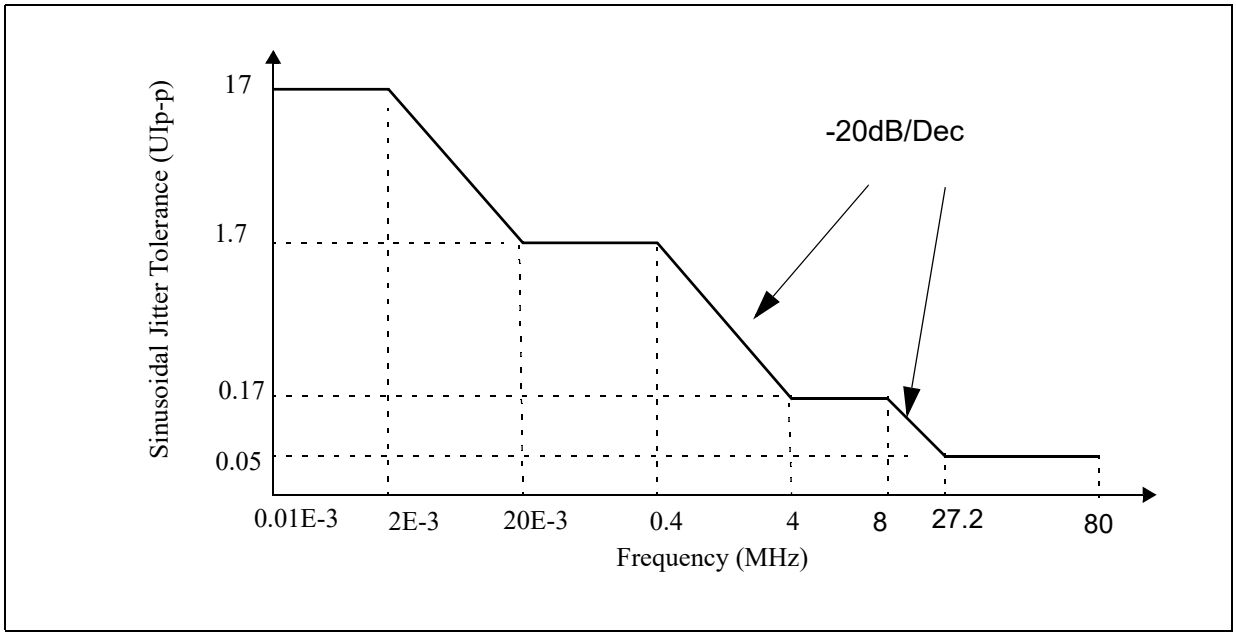
8.4.1 Jitter Requirements for Transparent Applications in Telecom systems

Telecom systems are Sonet as defined by ANSI: T1.105.03-2003 and Telcordia: GR-253, SDH systems as defined by ITU-T: G.783, G.812, G.813, G.825 and OTN systems as defined by ITU-T: G.8251 (for OTN jitter).

Currently there are discrepancies between Telcordia GR-253 and ITU-T G.783. This IA is compliant to both with respect to jitter transfer and aligned with ITU-T G.783 with respect to jitter generation

8.4.1.1 Sinusoidal Jitter tolerance mask for Ingress direction, CEI receiver at reference point R_I.

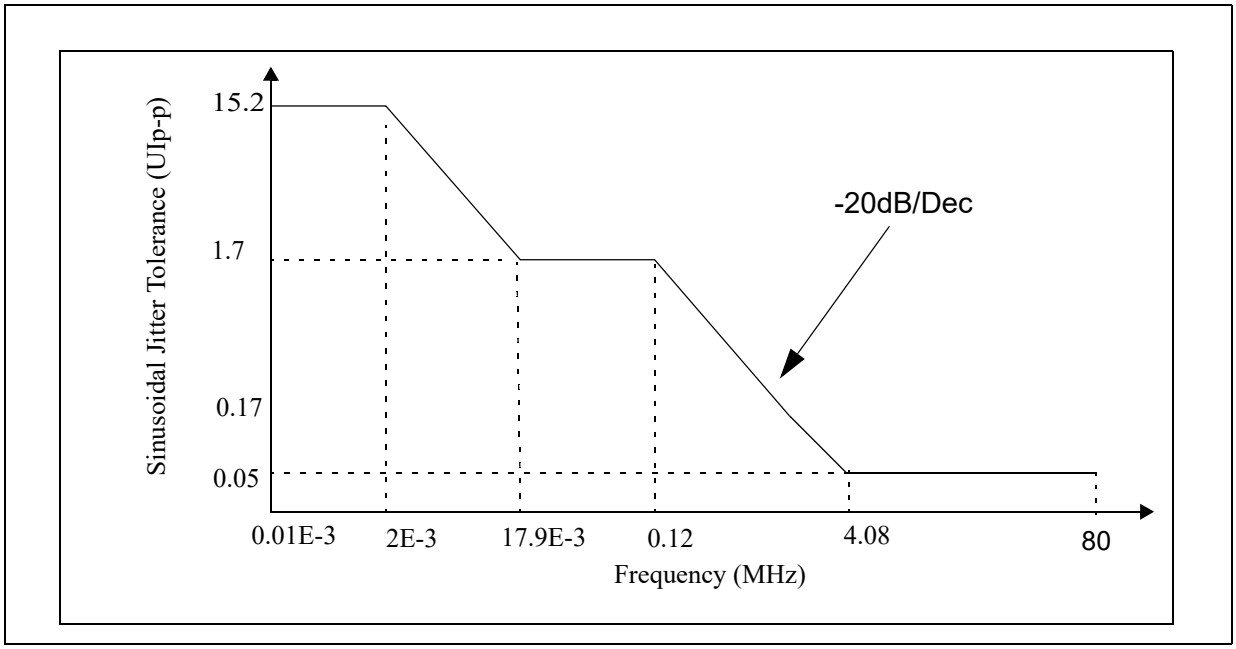
Figure 8-1. Jitter Ingress Receiver Input Telecom Sinusoidal Jitter



The Sinusoidal Jitter mask is aligned with the Telecom requirements for the Input Jitter Tolerance at the Signal Conditioner input and a required maximum loop BW of 8MHz in the case of a simple PLL based Signal Conditioner. Margins are added to the jitter amplitude to allow for added jitter by the signal conditioner and the CEI interconnect. This margin is not intended to alter in any way the telecom network limits as specified by ANSI/ITU-A but is required to assure the limits to be met by an Ingress CEI receiver that needs to tolerate the combined telecom network maximum jitter and CEI channel maximum jitter.

8.4.1.2 Sinusoidal Jitter tolerance mask for Egress direction, CEI receiver at reference point R_E.

Figure 8-2. Jitter Egress Receiver Input Telecom Sinusoidal Jitter



The Sinusoidal Jitter mask is aligned with the Telecom requirements for the Input Jitter of an Ingress Signal Conditioner with additional margin for the signal transfer to the Egress path in accordance with 8.4.1.3. This implies a required minimum loop BW of 4MHz in the case of a simple PLL based Signal Conditioner. The low frequency amplitude is required for tolerance testing only and does not reflect a valid condition during operation.

8.4.1.3 Telecom Jitter transfer

Jitter transfer specifications are necessary to constrain the Peaking and Bandwidth transfer function of the elements in a telecom system due to the synchronous timing of network elements. Measurements as per Annex 2.E.5. The following specifications assume an overall transfer -3dB bandwidth (20db/dec) limited to 120kHz by circuits outside the scope of this IA.

Table 8-7. Telecom Signal Conditioner, Egress direction

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Jitter Transfer Bandwidth	BW	Data see 1			8	MHz
Jitter Peaking		Frequency <120kHz			0.03	dB
		Frequency >120kHz			1	dB
NOTES: 1. PRBS 2^{31}-1, OC-192/SDH-64 Sinusoidal Jitter Tolerance Mask						

Table 8-8. Telecom Signal Conditioner, Ingress Direction

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Jitter Transfer Bandwidth	BW	Data, see 1			8	MHz
Jitter Peaking		Frequency <120kHz			0.03	dB
		Frequency >120kHz			1	dB
NOTES: 1. PRBS 2^{31}-1, OC-192/SDH-64 Sinusoidal Jitter Tolerance Mask						

8.4.1.4 Telecom Jitter Generation for Egress Direction

The Jitter generation measured at the Egress output of the Jitter Transparent Element is the sum of the jitter at the Egress Driver Output (reference point T_E in Figure 1-6), the CEI channel and the Jitter Transparent Element in which the CEI receiver R_E (Figure 1-6) resides. The maximum allowed Jitter Generation at the output of the Jitter Transparent Element is allocated in Table 8-9.

Table 8-9. Telecom Egress Jitter Generation budget

	Measurement range		Budget allocation
	Lower Frequency	Upper Frequency	
Egress driver	TE Egress output lower measurement limit	Signal conditioner max transfer bandwidth	42.5%
Egress channel	TE Egress output lower measurement limit	Signal conditioner max transfer bandwidth	7.5%
Egress TE, signal conditioner and path to Egress output	TE Egress output lower measurement limit	TE Egress output upper measurement limit	50%

Informative values for the Egress Driver is given in Table 8-10 based on current telecom recommendations...

Table 8-10. Telecom Egress Driver Jitter Generation

	TE Output Specified Range	Measurement Range	Method	Value	Unit
Telcordia GR-253	50kHz - 80MHz	50kHz - 8MHz	not specified, note 1	6.5	mUIrms
	50kHz - 80MHz	50kHz - 8MHz	not specified, note 1	43	mUIpp
ITU-T G.783	20kHz - 80MHz	20kHz - 8MHz	60 sec	129	mUIpp
	4MHz - 80MHz	4MHz - 8MHz	60 sec	43	mUIpp

NOTES:
1. The ITU-T specifications are applicable, Telcordia plans to align GR-253 those specifications when/if GR-253 is reissued

The measurement range corresponds to the transfer bandwidth as stated in Table 8-7.

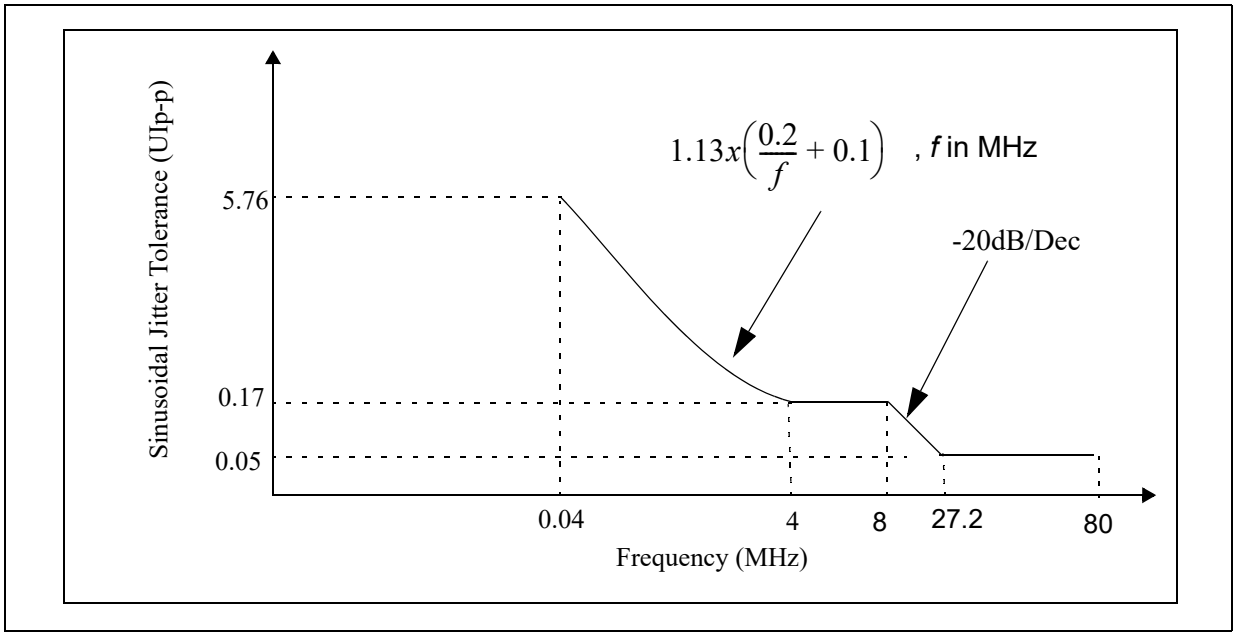
8.4.2 Jitter Requirements for Transparent Applications in Datacom systems

Datacom systems are 10GE as defined by IEEE 802.3ae-2002and the 10GFC as defined by INCITS, T11.2.

8.4.2.1 Sinusoidal Jitter tolerance mask for Ingress direction, CEI Receiver at reference point D

.

Figure 8-3. Jitter Ingress Receiver Input Datacom Sinusoidal Jitter



The Sinusoidal Jitter mask is aligned with the Datacom requirements for the Input Jitter Tolerance at the Signal Conditioner input and a required maximum loop BW of 8MHz in the case of a simple PLL based Signal Conditioner. Margins are added to the jitter amplitude to allow for added jitter by the signal conditioner and the CEI interconnect.

8.4.2.2 Datacom Jitter transfer

The jitter transparent Signal Conditioner of the Ingress and Egress directions need to be specified to constrain the overall signal jitter transferred to the receive end of the CEI channel and for the Egress direction further onto the transmit side of the signal conditioner.

Table 8-11. Datacom Signal Conditioner Egress direction

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Jitter Transfer Bandwidth	BW	Data see 1			8	MHz
Jitter Peaking		Frequency >50kHz			1	dB
NOTES: 1. Based on IEEE 802.3ae-2002 Clause 52 Sinusoidal Jitter Tolerance Mask, figure 52-4						

Table 8-12. Datacom Signal Conditioner Ingress Direction

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Jitter Transfer Bandwidth	BW	Data, see 1			8	MHz
Jitter Peaking		Frequency >50kHz			1	dB
NOTES: 1. Based on IEEE 802.3ae-2002 Clause 52 Sinusoidal Jitter Tolerance Mask, figure 52-4						

8.4.3 Jitter Transparency compliance nomenclature

For compliance to Jitter-transparent applications transmitters and receivers shall be identified as shown in table

Table 8-13. Datacom Signal Conditioner Ingress Direction

Characteristic	Symbol
Telecom Receiver, Ingress	**CEI 11GSR - TR(I)**
Telecom Transmitter, Ingress	**CEI 11GSR - TT(I)**
Telecom Receiver, Egress	**CEI 11GSR - TR(E)**
Telecom Transmitter, Egress	**CEI 11GSR - TT(E)**
Datacom Receiver, Ingress	**CEI 11GSR - DR(I)**
NOTES:	

Table 8-13. Datacom Signal Conditioner Ingress Direction

Characteristic	Symbol
Datacom Transmitter, Ingress	**CEI 11GSR - DT(I)**
Datacom Receiver, Egress	**CEI 11GSR - DR(E)**
Datacom Transmitter, Egress	**CEI 11GSR - DT(E)**
NOTES:	

8.A Appendix - Informative Jitter Budget

The Jitter Budget is presented in Table 8-14. Contributors in the 'Source' column should not exceed the value of the 'Value' column.

Table 8-14. Informative Jitter Budget

Source	Uncorrelated Jitter		Correlated Jitter		Total Jitter				Amplitude	
	Unbounded Gaussian	Bounded High Prob.	Bounded Gaussian	Bounded High Prob.	Gaussian	Sinusoidal	High Prob.	Total		
Abbreviation	**UUGJ**	**UBHPJ**	**CBGJ**	**CBHPJ**					**k**	
Unit	UIpp	UIpp	UIpp	UIpp	UIpp	UIpp	UIpp	UIpp		mVppd
Transmitter	**0.150**	**0.150**			**0.150**		**0.150**	**0.300**		**360**
Channel		0,100	0,132	0.200		0,050				
Receiver Input	**0.150**	**0.250**	**0,132**	**0.200**	**0.200**	**0,050**	**0.450**	**0.650**	**0.31**	**110**
Equalizer				-0.200						
Post Equalizer	**0.150**	**0.250**	**0,132**	**0.000**	**0.200**	**0,050**	**0.250**	**0.450**	**0.31**	**110**
Clock & Sampler	0.150	0.100		0.100						-50
Budget with Equalizer	**0.212**	**0.350**	**0,132**	**0.100**	**0.250**	**0.050**	**0.450**	**0.750**		**60**
Budget without equalizer	**0.212**	**0.350**	**0,132**	**0.300**	**0.250**	**0.050**	**0650**	**0.950**		**60**
Note: Values in yellow are specified values from Table 8-2 and Table 8-5										

8.B Appendix - StatEye.org Template[1]

```
%%%
```

```
param.vstep = [0.1 0.05 0.025];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% set the de-emphasis of 4-point transmit pulse
% the de-emphasis run if param.txpre = [] and param.txpost = []

param.txdeemphasis = [1 1 1 1]; % de-emphasis is off

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% set the data coding changing the transmit pulse spectrum
% the coding run if param.txpre = [] and param.txpost = []

param.datacoding = 1; % the coding is off

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% set PAM amplitude and rate

param.PAM = 2; % PAM is switched off

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% the rx sample point does not need to be changed as it is
% automatically adjusted by the optimisation scripts.
% The number of DFE taps should be set, however, the initial
% conditions are irrelevant.

param.rxsample = -0.1;

param.dfe = [];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% sampling jitter in HPJpp and GJrms is defined here

param.txdj = 0.15;
param.txrj = 0.15/(2*7.94);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% the following options are not yet implemented and should
% not be changed

param.user = [0.0];
param.useuser = 'no';
param.usesymbol = '';
param.xtAmp = 1.0;
```

%%%

9 CEI-11G-LR/MR Long/Medium Reach Interface

This clause details the requirements for the CEI-11G-LR and CEI-11G-MR high speed electrical interface between nominal baud rates of 9.95 Gsym/s to 11.2 Gsym/s using NRZ coding. A compliant device must meet all of the requirements listed below. The electrical interface is based on high speed, low voltage logic with nominal differential impedance of 100 Ω. Connections are point-to-point balanced differential pair and signaling is unidirectional.

The electrical IA is based on loss and jitter budgets and defines the characteristics required to communicate between a CEI-11G-LR driver and a CEI-11G-LR receiver and between a CEI-11G-MR driver and a CEI-11G-MR receiver, using copper signal traces on a printed circuit board. The characteristic impedance of the signal traces is nominally 100 Ω differential. Rather than specifying materials, channel components or configurations, the IA focuses on effective channel characteristics. Hence a short length of poorer material should be equivalent to a longer length of premium material. A length is effectively defined in terms of its attenuation and phase response rather than its physical length.

CEI-11G-LR as well as CEI-11G-MR devices from different manufacturers shall be inter-operable.The CEI-11GLR/MR channel is tested to insure compliance using the statEye scripts. The transmitter is specified in terms of its ability to pre-equalize the transmit signal and the receiver must work to the given BER using a compliant driver and channel.

The primary focus of the CEI-11G-LR implementation agreement will be for non-legacy applications, optimized for overall cost-effective system performance including total power dissipation. Future clauses may address schemes otherwise optimized.

This clause also provides for a CEI-11G-MR low power option. The CEI-11G-MR option is based upon the following:

- A channel compliance specification is defined in this clause for CEI-11G-MR which is more stringent than that of CEI-11G-LR.
- CEI-11G-MR uses the same Transmitter device as is specified for CEI-11G-LR, making use of certain features otherwise defined as optional.
- CEI-11G-MR uses a Receiver device that is similar to the device specified for CEI-11G-SR in Clause 8, but with extended T_Vdiff range. Relevant specifications for this receiver device are incorporated by reference to Clause 8.

9.1 Requirements

1. Support NRZ coded serial data rate from 9.95 Gsym/s to 11.2 Gsym/s.
2. Capable of low bit error rate (required BER < 10^{-15}).
3. Capable of driving 0 — 1 meter (39 inches) of PCB and up to 2 connectors.
4. Capable of driving 0 — 600 mm of PCB and up to 2 connectors for low-power applications.
5. Shall support AC-coupled and optionally DC-coupled operation.
6. Shall allow multi-lanes (1 to n).
7. Shall support hot plug.

9.2 General Requirements

9.2.1 Data Patterns

See 3.2.1

9.2.2 Signal Levels

See 3.2.2

9.2.3 Signal Definitions

See 1.A

9.2.4 Bit Error Ratio

See 3.2.3

9.2.5 Ground Differences

See 3.2.4

9.2.6 Cross Talk

See 3.2.5

9.2.7 Channel Compliance

9.2.7.1 CEI-11G-LR Channel Compliance

A forward channel and associated dominant crosstalk channels are deemed compliant if for the specified reference transmitter and both the specified reference receivers, the signal conforms to the defined eye mask and does not exceed the defined jitter using the “Statistical Eye” methodology defined in 2.C

Reference Transmitter:

1. Maximum Transmit Pulse, as per 2.E.7, of T_Vdiff min. of Table 9-1
2. A TX edge rate filter simple 40dB/dec low pass at 75% of Baud Rate
3. Effective Driver UUGJ, UBHPJ and DCD as in Table 9-3
4. Equalizing Filter with 2 tap baud spaced emphasis no greater than a total of 6dB with finite resolution no better than 1.5dB.
5. Worst case Transmitter return loss described as a parallel RC element, see 2.E.6
6. Maximum baud rate that the channel is to operate at or 11.2 Gsym/sec whichever is the lowest, see 9.3.1.1

Reference Receiver A:

1. 4-tap baud spaced Non-Linear Discrete Inverse Channel Filter (DFE), with infinite precision accuracy and having the following restrictions:

   Let W[N] be sum of DFE tap coefficient weights from taps N through M where

   N = 1 is previous decision (i.e. first tap)
   M = 4
   R_Y2 = T_Y2 = 400mV
   Y = min(R_X1, (R_Y2 - R_Y1) / R_Y2) = 0.2625
   $Z = {}^{2}/_{3} = 0.66667$

   Then $W[N] \leq Y * Z^{(N - 1)}$

   For the channel compliance model the number of DFE taps (M) = 4. This gives the following maximum coefficient weights for the taps:

   $W[1] \leq 0.2625$ (sum of absolute value of taps 1 and2)
   $W[2] \leq 0.1750$ (sum of absolute value of taps 2, 3 and 4)
   $W[3] \leq 0.1167$ (sum of absolute value of taps 3 and 4)
   $W[4] \leq 0.0778$ (sum of absolute value of tap 4)

   Notes:
   - Coefficient weights are absolute, assuming a T_Vdiff of 1Vppd

- For a real receiver the restrictions on tap coefficients would apply for the actual number of DFE taps implemented (M)
- LMS, Least Mean Squared Adaptation Algorithm.

2. Worst case Receiver return loss described as a parallel RC, see 2.E.6

Resulting Eye Mask of either receiver:

Table 9-1. CEI-11G-LR Receiver Equalization Output Eye Mask

Parameter	Symbol	Max	Units
Eye mask	R_X1	0.2625	UI
Eye mask	R_Y1	50	mV
Correlated Bounded High Probability Jitter, pre-equalizer	R_CBHPJ	0.40	UIpp
Correlated Bounded High Probability Jitter, post-equalizer	R_CBHPJ	0.10	UIpp
Uncorrelated Bounded High Probability Jitter	R_UBHPJ	0.15	UIpp
Uncorrelated Unbounded Gaussian Jitter	R_UUGJ	0.15	UIpp
Quality of signal (SNR in real number)	Q	7.94	

9.2.7.2 CEI-11G-MR Channel Compliance

As per 2.5.2, with the following reference transmitter and reference receiver (note these conditions do not specify any required implementation but rather indicate a methodology for testing channel compliance), and shall meet the receive eye mask as specified in Figure 1-5 and Table 9-9 when using electrical characteristic R_X1 less R_SJ-hf in Table 9-9.

Reference Transmitter as defined in “Reference Transmitter” in Section 9.2.7.1.

Reference Receiver as defined in “Reference Receiver A” in Section 8.2.7.

9.3 Electrical Characteristics, CEI-11G-LR and CEI-11G-MR

The electrical signaling is based on high speed low voltage logic with a nominal differential impedance of 100 Ω.

9.3.1 Driver Characteristics

For termination and DC-blocking information, please refer to 8.2.7

Table 9-2. Transmitter Output Electrical Specifications

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	T_Baud		9.95		11.2	Gsym/s
Output Differential Voltage	T_Vdiff	Pre-emphasis off or Tx Filter Applied, see note 1	800		1200	mVppd
Differential Output Impedance	T_Rd		80	100	120	Ω
Differential Termination Impedance Mismatch	T_Rm				10	%
Output Rise and Fall Time (20% to 80%)	T_tr, T_tf		24			ps
Differential Output Return Loss	T_SDD22	See 9.3.1.3				
Common Mode Return Loss	T_SCC22	See 9.3.1.3			-6	dB
Transmitter Common Mode Noise	T_Ncm				5% of T_Vdiff	mVppd
Output Common Mode Voltage See Notes 2, 3 & 4	T_Vcm	Load Type 0 See Note 2	100		1700	mV
		Load Type 1 See Note 3 & 4	630		1100	mV

NOTES:
1. In applications where the channel is better than the worst case allowed, a transmitter device may be provisioned to produce T_Vdiff less than this minimum value but ≥360mVppd and be compliant with this specification.
2. Load Type 0 with min. T_Vdiff, AC-Coupling or floating load.
3. For Load Type 1: R_Zvtt ≤ 30Ω; T_Vtt & R_Vtt = 1.2V +5%/-8%
4. DC Coupling compliance is optional (Load Type). Only Transmitters that support DC coupling are required to meet this parameter.

Table 9-3. Transmitter Output Jitter Specifications

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Uncorrelated Unbounded Gausian Jitter	T_UUGJ	See 9.3.1.6, Note 1			0.15	UI_{PP}
Uncorrelated Bounded High Probability Jitter	T_UBHPJ	See 9.3.1.6, Note 1			0.15	UI_{PP}
Duty Cycle Distortion (component of UBHPJ)	T_DCD	See 9.3.1.6			0.05	UI_{PP}
Total Jitter	T_TJ	See 9.3.1.6			0.30	UI_{PP}
Eye Mask	T_X1	See 9.3.1.6			0.15	UI
Eye Mask	T_X2	See 9.3.1.6			0.50	UI
Eye Mask	T_Y1	See 9.3.1.6 Note 3	400			mV
Eye Mask	T_Y2	See 9.3.1.6			600	mV

NOTES:
1. UBHPJ is composed of DCD, inter-symbol-interference (ISI), and Sinusoidal Jitter.
2. Except for amplitude, the CEI-11G+ long-reach driver electrical specifications of Table 9-3 are intended to be the same as for CEI-11G+ short-reach
3. The minimum value for channel compliance is 300mV and not 180mV. The 180mV is to allow lower power for channels that are better than the worst case channels allowed

9.3.1.1 Driver Baud Rate

All devices shall work from 9.95Gsym/s to the maximum baud rate specified for the device, with the baud rate tolerance as per 3.2.12. Note that implementation of specific protocols will define the operating baud rate without affecting CEI compliance.

9.3.1.2 Driver Amplitude and Swing

Driver differential output amplitude shall be able to drive between 800 to 1200mVppd either with or without any transmit emphasis. However, for the case of this transmitter talking to a short reach receiver, the differential output amplitude shall be between 380 to 770mVppd either with or without any transmit emphasis. DC referenced logic levels are not defined since the receiver must have high common mode impedance at DC. However, absolute driver output voltage shall be between -0.1 V and 1.9 V with respect to local ground. See Figure 1-1 for an illustration of absolute driver output voltage limits and definition of differential peak-to-peak amplitude.

9.3.1.3 Driver Resistance and Return Loss

Please refer to 3.2.10 with the following parameters.

Table 9-4. Driver Return Loss Parameters

Parameter	Value	Units
A0	-8	dB
f0	100	MHz
f1	$T_\text{Baud} \times \frac{3}{4}$	Hz
f2	T_Baud	Hz
Slope	16.6	dB/dec

9.3.1.4 Driver Lane-to-Lane Skew

Please refer to 3.2.7

9.3.1.5 Driver Short Circuit Current

Please refer to 3.2.9

9.3.1.6 Driver Template and Jitter

As per 2.2.3 for a BER as per 9.2.4, the driver shall satisfy the eye template and jitter requirements as given in Figure 1-4.

9.3.2 CEI-11G-LR Receiver Characteristics

This section defines receiver characteristics for CEI-11G-LR receivers. Receiver characteristics for CEI-11G-MR receivers are defined in 9.3.3.

Receiver electrical specifications are given in Table 9-5 and measured at compliance point R. For termination and DC-blocking information, please refer to 3.2.12

Table 9-5. CEI-11G-LR Receiver Electrical Specifications

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud rate	R_Baud		9.95		11.2	GSym/s
Input Differential Voltage	R_Vdiff	Note 1			1200	mVppd
Differential Input Impedance	R_Rdin		80	100	120	Ω
Input Impedance Mismatch	R_Rm				10	%
Differential Input Return Loss	R_SDD11	See 9.3.2.3				
Common Mode Input Return Loss	R_SCC11	Below 10 GHz			-6	dB
Input Common Mode Voltage See Notes: 2, 3 & 4	R_Vcm	Load Type 0 See Note 3	0		1800	mV
		Load Type 1 See Notes 2, 4	595		R_Vtt - 60	mV
Wander Divider	n	See Note 5		10		

NOTES:
1. The long-reach receiver shall have a differential input voltage range sufficient to accept a signal produced at point R by the combined transmitter and channel. The channel response shall include the worst case effects of the return losses at the transmitter and receiver.
2. DC Coupling compliance is optional (Load Type 1). Only receivers that support DC coupling are required to meet this parameter.
3. Load Type 0 with min. T_Vdiff, AC-Coupling or floating load. For floating load, input resistance must be ≥ 1kΩ
4. For Load Type 1: T_Vtt & R_Vtt = 1.2V +5%/-8%.
5. Used in Statistical Eye script, must be set to 10

Table 9-6. CEI-11G-LR Receiver Input Jitter Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Sinusoidal Jitter, Maximum	R_SJ-max	See 2.5.4, note 1, 2			5	UIpp
Sinusoidal Jitter, High Frequency	R_SJ-hf	See 2.5.4, note 1, 2			0.05	UIpp

NOTES:
1. The Receiver shall tolerate the sum of these jitter contributions: Total Driver jitter from Table 9-2;Sinusoidal jitter as defined in Table 9-6;The effects of a channel compliant to the Channel Characteristics (9.2.7).
2. The receiver must tolerate the total deterministic and random jitter with addition of the sinusoidal jitter.

9.3.2.1 Input Baud Rate

All devices shall work from 9.95 Gsym/s to the maximum baud rate specified for the device, with the baud rate tolerance as per 3.2.11. Note that implementation of specific protocols will define the operating baud rate without affecting CEI compliance.

9.3.2.2 Absolute Input Voltage

The absolute voltage levels with respect to the receiver ground at the input of the receiver are dependent on the driver implementation and the inter-ground difference.

The voltage levels at the input of an AC coupled receiver (if the effective AC coupling is done within the receiver) or at the Tx side of the external AC coupling cap (if AC coupling is done externally) shall be between -0.2 to 2.0V with respect to local ground.

9.3.2.3 Input Resistance and Return Loss

Please refer to 3.2.10 with the following parameters.

Table 9-7. Driver Return Loss Parameters

Parameter	Value	Units
A0	-8	dB
f0	100	MHz
f1	$R_\text{Baud} \times \frac{3}{4}$	Hz
f2	R_Baud	Hz
Slope	16.6	dB/dec

9.3.2.4 Input Signal Amplitude

The receiver shall accept differential input signal amplitudes produced by compliant transmitters connected without attenuation to the receiver. This may be larger than the 1200 mVppd maximum of the driver due to output/input impedances and reflections.

The minimum input amplitude is defined by the far-end driver template, the actual receiver input impedance and the loss of the actual PCB. Note that the far-end driver template is defined using a well controlled load impedance, however the real receiver is not, which can leave the receiver input signal smaller than expected.

9.3.2.5 Input Lane-to-Lane Skew

Please refer to 3.2.8

9.3.3 CEI-11G-MR Receiver Characteristics

This section defines receiver characteristics for CEI-11G-MR receivers. Receiver characteristics for CEI-11G-LR receivers are defined in 9.3.2.

Receiver electrical specifications are given in Table 9-8 and measured at compliance point R. Jitter specifications at reference R are listed in Table 9-9 and the compliance mask is shown in Figure 1-5.

For termination and DC-blocking information, please refer to 3.2.12.

Table 9-8. CEI-11G-MR Receiver Electrical Specifications

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud rate	R_Baud		9.95		11.2	GSym/s
Input Differential Voltage	R_Vdiff	Note 1	110		1200	mVppd
Differential Input Impedance	R_Rdin		See R_Rdin in Table 8-4			Ω
Input Impedance Mismatch	R_Rm		See R_Rm in Table 8-4			%
Differential Input Return Loss	R_SDD11	See 9.3.2.3	See R_SDD11 in Table 8-4			
Common Mode Input Return Loss	R_SCC11	Below 10 GHz	See R_SCC11 in Table 8-4			dB
Input Common Mode Voltage	R_Vcm	Note 2	See R_Vcm in Table 9-5			mV
Wander Divider	n	See Note 5	See n in Table 9-5			

NOTES:
1. The medium-reach receiver shall have a differential input voltage range sufficient to accept a signal produced at point R by the combined transmitter and channel. The channel response shall include the worst case effects of the return losses at the transmitter and receiver.
2. DC Coupling compliance is optional (Load Type 1). Only receivers that support DC coupling are required to meet this parameter.

Table 9-9. CEI-11G-MR Receiver Input Jitter Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Uncorrelated Bounded High Probability Jitter	R_UBHPJ		see R_UBHPJ in Table 8-5			UIpp
Correlated Bounded High probability Jitter	R_CBHPJ		see R_CBHPJ in Table 8-5			UIpp
Gaussian Jitter (UUGJ + CBGJ)	R_GJ	Note 2	see R_GJ in Table 8-5			UIpp
Sinusoidal Jitter, Maximum	R_SJ-max	See 2.2.4	see R_SJmax in Table 8-5			UIpp
Sinusoidal Jitter, High Frequency	R_SJ-hf	See 2.2.4	see R_SJ-hf in Table 8-5			UIpp
Total Jitter, including R_SJ-hf	R_TJ	Note 1	see R_TJ in Table 8-5			UIpp
Eye Mask incl. Correlated High Probability. Jitter	R_X1		see R_X1 in Table 8-5			UI
Eye Mask	R_Y1		see R_GJ in Table 8-5			mV
Eye Mask	R_Y2				600	mV

NOTES:
1. TJ includes high frequency sinusoidal jitter. The receiver must tolerate the total deterministic and random jitter with addition of the sinusoidal jitter. For transparent applications the specified jitter tolerance mask replace R_SJ.
2. BER=10^{-15}, Q=7.94

.

9.3.3.1 Input Baud Rate

Refer to 8.3.2.

9.3.3.2 Reference Input Signals

Reference input signals to the receiver shall have the characteristics determined by a compliant driver. The reference input signal must satisfy the transmitter near-end template and jitter given in Figure 1-4 and Table 9-3, as well as the far-end eye template and jitter given in Figure 1-5 and Table 9-9, with the differential load impedance of 100 ohms +/- 1% at DC and a return loss of better than 20dB from baud rate over 1667 to 1.5 times the baud rate. Note that the input signal might not meet either of these templates when the actual receiver replaces this load.

9.3.3.3 Input Resistance and Return Loss

Please refer to 3.2.10 with the parameters shown in Table 8-6.

9.3.3.4 Input Lane-to-Lane Skew

Please refer to 3.2.8

9.A Appendix - Informative Jitter Budgets

9.A.1 Informative Jitter Budget for Long Reach

The following table is an informative jitter budget for long reach. It includes the specified transmit jitter and an estimate of receiver jitter. A receiver may trade its ability to equalize against its own internal jitter; possibly leading to different numbers than are shown here. The receiver must tolerate sinusoidal jitter in addition to jitter contained in this table.

Although only total jitter (TJ) and Uncorrelated Bounded High Probability Jitter (UBHPJ) are normative to the specification, a realistic jitter budget must account for Uncorrelated Unbounded Gaussian Jitter (UUGJ) of both the Receiver and Transmitter as well as Correlated Bounded Gaussian Jitter of the Channel. A budget based entirely on Uncorrelated bounded high Probability Jitter would be overly pessimistic or would unfairly burden the equalization.

Table 9-10. CEI-11G-LR Informative Jitter Budget

Source	Uncorrelated Jitter		Correlated Jitter		Total Jitter				Amplitude	
	Unbounded Gaussian	Bounded High Prob.	Bounded Gaussian	Bounded High Prob.	Gaussian	Sinusoidal	High Prob.	Total		
Abbreviation	**UUGJ**	**UBHPJ**	**CBGJ**	**CBHPJ**					**k**	
Unit	UIpp	UIpp	UIpp	UIpp	UIpp	UIpp	UIpp	UIpp		mVppd
Transmitter	**0.150**	**0.150**			**0.150**		**0.150**	**0.300**		**800**
Channel			0.230	0.400						
Receiver Input	**0.150**	**0.150**	**0.230**	**0.400**	**0.275**		**0.550**	**0.825**	**0**	**0** See 2
Equalizer				-0.300 See 1						
Post Equalizer	**0.150**	**0.150**	**0.230**	**0.100**	**0.275**		**0.250**	**0.525**	**0.25**	**100**
DFE Penalties				0.100						-45
Clock & Sampler	0.150	0.100		0.100						-45
Budget	**0.212**	**0.250**	**0.230**	**0.300**	**0.313**	**0.050**	**0.550**	**0.913**	**0.13**	**10**

Note:
1. Due to receiver equalization, it reduces the ISI as seen inside the receiver. Thus this number is negative.
2. It is assumed that the eye is closed at the receiver, hence receiver equalization is required.
3. Values in yellow are specified values fromTable 9-5and Table 9-6

9.A.2 Informative Jitter Budget for Medium Reach

The following table is an informative jitter budget for medium reach. It includes the specified transmit jitter and an estimate of receiver jitter. A receiver may trade its ability to equalize against its own internal jitter; possibly leading to different numbers than are shown here. The receiver must tolerate sinusoidal jitter in addition to jitter contained in this table.

Although only total jitter (TJ) and Uncorrelated Bounded High Probability Jitter (UBHPJ) are normative to the specification, a realistic jitter budget must account for Uncorrelated Unbounded Gaussian Jitter (UUGJ) of both the Receiver and Transmitter as well as Correlated Bounded Gaussian Jitter of the Channel. A budget based entirely on Uncorrelated bounded high Probability Jitter would be overly pessimistic or would unfairly burden the equalization.

Table 9-11. CEI-11G-MR Informative Jitter Budget

Source	Uncorrelated Jitter		Correlated Jitter		Total Jitter				Amplitude	
	Unbounded Gaussian	Bounded High Prob.	Bounded Gaussian	Bounded High Prob.	Gaussian	Sinusoidal	High Prob.	Total		
Abbreviation	**UUGJ**	**UBHPJ**	**CBGJ**	**CBHPJ**					**k**	
Unit	UIpp	UIpp	UIpp	UIpp	UIpp	UIpp	UIpp	UIpp		mVppd
Transmit equalizer				-0.200						
Transmitter	**0.150**	**0.150**		**-0.200**	**0.150**		**-0.050**	**0.100**		**800**
Channel		0.100	0.132	0.400		0.0				
Receiver Input	**0.150**	**0.250**	**0.132**	**0.200**	**0.200**	**0.050**	**0.450**	**0.700**	**0**	**110**
Clock & Sampler	0.150	0.100		0.100						-45
Budget	**0.212**	**0.350**	**0.132**	**0.300**	**0.250**	**0.050**	**0.650**	**0.950**	**0.13**	**10**

Note:
1. Due to receiver equalization, it reduces the ISI as seen inside the receiver. Thus this number is negative.
2. Values in yellow are specified values fromTable 9-8and Table 9-9

9.B Appendix - StatEye.org templates

9.B.1 StatEye.org templates for CEI-11G-LR, reference receiver A

```
%%%
```

```
param.vstep                    = [0.1 0.05 0.025];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% set the de-emphasis of 4-point transmit pulse
% the de-emphasis run if param.txpre = [] and param.txpost = []

param.txdeemphasis = [1 1 1 1];          % de-emphasis is off

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% set the data coding changing the transmit pulse spectrum
% the coding run if param.txpre = [] and param.txpost = []

param.datacoding = 1;       % the coding is off

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% set PAM amplitude and rate

param.PAM = 2;            % PAM is switched off

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% the rx sample point does not need to be changed as it is
% automatically adjusted by the optimisation scripts.
% The number of DFE taps should be set, however, the initial
% conditions are irrelevant.

param.rxsample                 = -0.1;

param.dfe                      = [0.3 0.1 0.1 0.1];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% The CTE shall be controlled.

param.cte = 0; % CTE setting “0” = off; “1” = on;
param.ctethresh = 0; % max gain;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% sampling jitter in HPJpp and GJrms is defined here

param.txdj                     = 0.15;
param.txrj                     = 0.15/(2*7.94);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
% the following options are not yet implemented and should
% not be changed

param.user                  = [0.0];
param.useuser                 = 'no';
param.usesymbol                 = '';
param.xtAmp                  = 1.0;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

param.TransmitAmplitude = 0.800; % mVppdif
param.MinEye          = 0.100; % mVppdif

param.Q             = 2*7.94;
param.maxDJ           = 0.275;
param.maxTJ           = 0.525;
```

9.B.2 StatEye.org Templates for CEI-11G-LR, reference receiver B

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% example template for setting up a standard, i.e. equaliser
% jitter and return loss

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

param.version = [param.version '_v1.0'];

% these are internal variables and should not be changed

param.scanResolution            = 0.01;
param.binsize                = 0.0005;
param.points                 = 2^13;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% set the transmitter and baud rate. The tx filter has two
% parameters defined for the corner frequency of the poles

param.bps                   = 11.1e9;
param.bitResolution             = 1/(3*param.bps);
param.txFilter              = 'twopole';
param.txFilterParam             = [0.75 0.75];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% set the return loss up. The return loss can be turned off
```

```
% using the appropriate option

param.returnLoss                = 'on';
param.cpad                      = 0.60;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% set the transmitter emphasis up. Some example setting are
% included which can be uncommented

% single tap emphasis
param.txpre                     = [-0.1];
param.signal                    = 1.0;
param.txpost                    = [-0.1];
param.vstart                    = [-0.3 -0.3];
param.vend                      = [+0.0 +0.0];
param.vstep                     = [0.1 0.05 0.025];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% set the de-emphasis of 4-point transmit pulse
% the de-emphasis run if param.txpre = [] and param.txpost = []

param.txdeemphasis = [1 1 1 1];          % de-emphasis is off

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% set the data coding changing the transmit pulse spectrum
% the coding run if param.txpre = [] and param.txpost = []

param.datacoding = 1;       % the coding is off

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% set PAM amplitude and rate

param.PAM = 2;            % PAM is swithed off

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% the rxsample point does not need to be changed as it is
% automatically adjusted by the optimisation scripts.
% The number of DFE taps should be set, however, the initial
% conditions are irrelevant.

param.rxsample                  = -0.1;

param.dfe                       = [];
```

```
%%%
```

```
param.scanResolution          = 0.01;
param.binsize                 = 0.0005;
param.points                  = 2^13;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% set the transmitter and baud rate. The tx filter has two
% parameters defined for the corner frequency of the poles

param.bps                     = 11.1e9;
param.bitResolution           = 1/(3*param.bps);
param.txFilter                = 'twopole';
param.txFilterParam           = [0.75 0.75];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% set the return loss up. The return loss can be turned off
% using the appropriate option

param.returnLoss              = 'on';
param.cpad                    = 0.60;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% set the transmitter emphasis up. Some example setting are
% included which can be uncommented

% single tap emphasis
param.txpre                   = [-0.1];
param.signal                  = 1.0;
param.txpost                  = [-0.1];
param.vstart                  = [-0.3 -0.3];
param.vend                    = [+0.0 +0.0];
param.vstep                   = [0.1 0.05 0.025];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% set the de-emphasis of 4-point transmit pulse
% the de-emphasis run if param.txpre = [] and param.txpost = []

param.txdeemphasis = [1 1 1 1];          % de-emphasis is off

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% set the data coding changing the transmit pulse spectrum
% the coding run if param.txpre = [] and param.txpost = []

param.datacoding = 1;       % the coding is off
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
% set PAM amplitude and rate

param.PAM = 2;              % PAM is swithed off

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% the rxsample point does not need to be changed as it is
% automatically adjusted by the optimisation scripts.
% The number of DFE taps should be set, however, the initial
% conditions are irrelevant.

param.rxsample                  = -0.1;

param.dfe                       = [];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% The CTE shall be controlled.

param.cte = 0; % CTE setting “0” = off; “1” = on;
param.ctethresh = 0; % max gain;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% sampling jitter in HPJpp and GJrms is defined here

param.txdj                      = 0.15;
param.txrj                      = 0.15/(2*7.94);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% the following options are not yet implemented and should
% not be changed

param.user                      = [0.0];
param.useuser                   = ’no’;
param.usesymbol                 = ’’;
param.xtAmp                     = 1.0;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

param.TransmitAmplitude = 0.800; % mVppdif
param.MinEye          = 0.100; % mVppdif

param.Q             = 2*7.94;
param.maxDJ           = 0.275;
param.maxTJ           = 0.525;
```

10 CEI-28G-SR Short Reach Interface

This clause details the requirements for the CEI-28G-SR short reach high speed electrical interface between nominal baud rates of 19.90 Gsym/s and 28.05 Gsym/s using NRZ coding. A compliant device shall meet all of the requirements listed below. The electrical interface is based on high speed, low voltage logic. Connections are point-to-point balanced differential pairs and signaling is unidirectional.

The electrical IA is based on loss and jitter budgets and defines the characteristics required to communicate between a CEI-28G-SR transmitter and a CEI-28G-SR receiver using copper signal traces on a printed circuit board. The characteristic impedance of the signal traces is nominally 100 Ω differential. A 'length' is effectively defined in terms of its attenuation and phase response rather than its physical length. Refer to Section 10.2.6 for channel requirements.

Short reach CEI-28G-SR devices from different manufacturers shall be interoperable.

10.1 Requirements

1. Support serial baud rates within the range from 19.90 Gsym/s to 28.05 Gsym/s.
2. Capable of low bit error ratio (10^{-15}, with a test requirement to verify 10^{-12}).
3. Capable of driving up to 300 mm of PCB and up to 1 connector.
4. Shall support AC-coupled operation
5. Shall allow multi-lanes (1 to n).
6. Shall support hot plug.

10.2 General Requirements

10.2.1 Data Patterns

Please refer to Section 3.2.1

10.2.2 Signal levels

Please refer to Section 3.2.2. All transmitter and receiver devices shall support "Load Type 0". Other load types are not supported by this clause.

10.2.3 Signal Definitions

Please refer to Section 1.A

10.2.4 Bit Error Ratio

Please refer to Section 3.2.3

10.2.5 Ground Differences

Please refer to Section 3.2.4

10.2.6 Channel Compliance

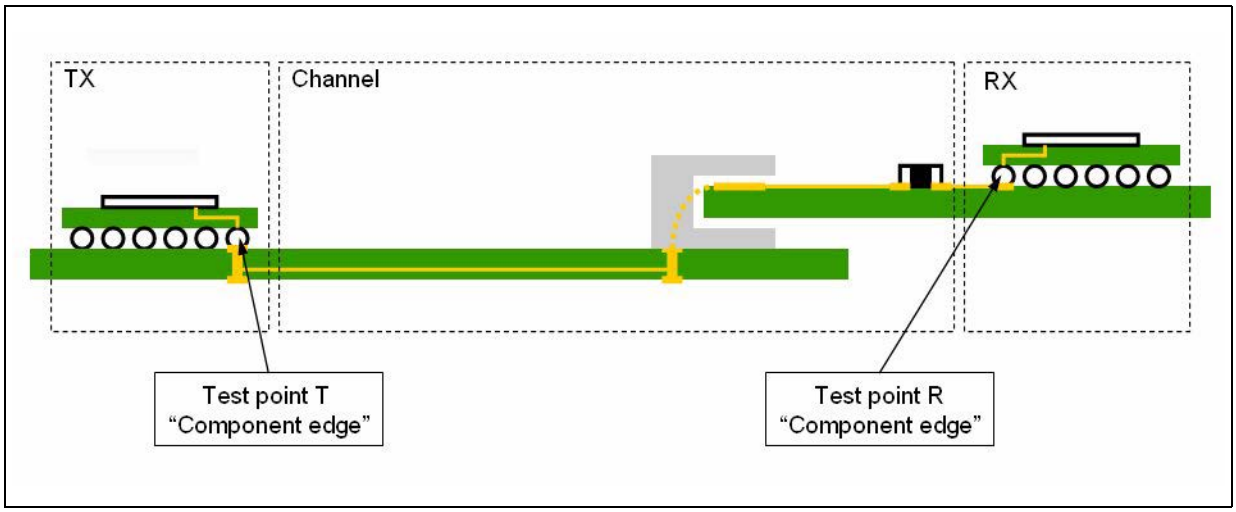
A forward channel and associated dominant crosstalk channels are deemed compliant if the channel characteristics conform to the requirements in this section.

10.2.6.1 Reference Model

The channel consists of PCB traces, vias, and 0 or 1 connector. The reference PCB trace differential impedance is 100Ω.

Figure 10-1 shows a diagram of test points on an example board.

Figure 10-1. CEI-28G-SR Reference Model



Note: Test points differ from definitions in Section 1.8, as DC blocking capacitors, if physically located outside of the package, are part of the channel.

Measured at these test points, several channel characteristics are parametrized. Port definitions noted in Figure 2-33 allow proper measurement of the parameters in Table 10-1 used for calculation of the channel parameters found in Table 10-2.

Table 10-1. Measured Channel Parameters

Symbol	Description
$IL(f)$	Differential insertion loss, -SDD21 magnitude (dB)
$RL_1(f)$	Differential input return loss, -SDD11 magnitude (dB)
$RL_2(f)$	Differential output return loss, -SDD22 magnitude (dB)
$NEXT_m(f)$	Differential near-end crosstalk loss (m^{th} aggressor), -SDD21 magnitude (dB)
$FEXT_n(f)$	Differential far-end crosstalk loss (n^{th} aggressor), -SDD21 magnitude (dB)

Table 10-2. Calculated Channel Parameters

Symbol	Description
$IL_{fitted}(f)$	Fitted insertion loss (dB)
$ILD(f)$	Insertion loss deviation (dB)
$ICN(f)$	Integrated crosstalk noise (mV, RMS)
FOM_{ILD}	RMS value of the insertion loss Deviation (dB)

10.2.6.2 Insertion Loss

Channel insertion losses, including PCB traces and connectors, shall comply with the limits specified by equations (10-1), (10-2) and plotted in Figure 10-2. Note that the variable f_b is the maximum baud rate to be supported by the channel under test (19.90 Gsym/s $\le f_b \le$ 28.05 Gsym/s).

Table 10-3. Channel Insertion Loss Frequency Range

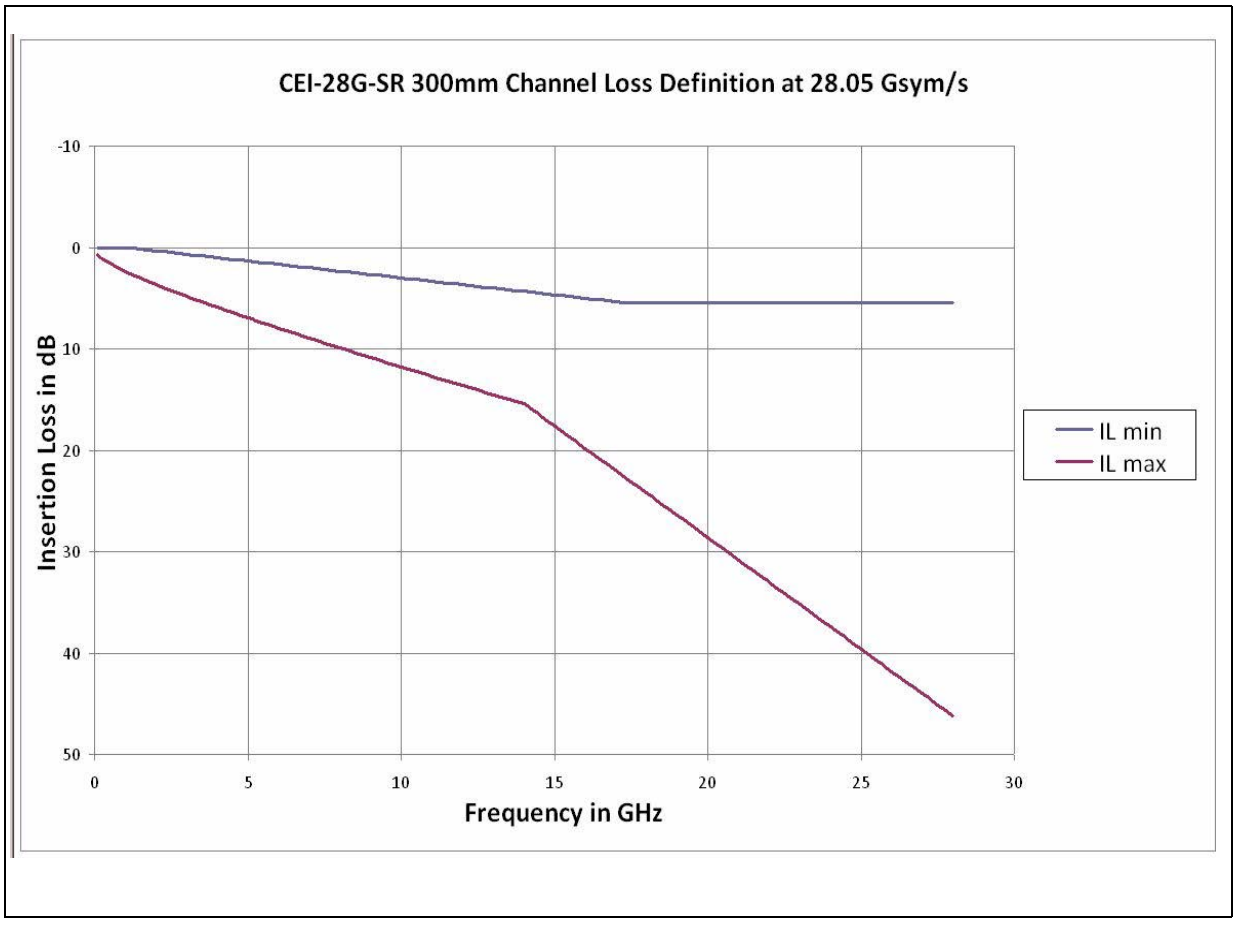
Parameter	Value	Units
fmin	50	MHz
fmax	f_b	GHz

$$IL_{max} = \begin{cases} 0.1188 + 1.54\sqrt{\frac{f \times 28.05}{f_b}} + 0.68\frac{f \times 28.05}{f_b}, & f_{min} \le f < \frac{f_b}{2} \\ -15.43 + 2.2\frac{f \times 28.05}{f_b}, & \frac{f_b}{2} \le f \le f_b \end{cases} \quad (10\text{-}1)$$

$$IL_{min} = \begin{cases} 0, & f_{min} \le f \le 1GHz \\ \frac{1}{3}(f-1), & 1GHz < f \le 17.5GHz \\ 5.5, & 17.5GHz < f \le f_b \end{cases} \quad (10\text{-}2)$$

Note: f in (10-1) and (10-2) is in GHz.

Figure 10-2. CEI-28G-SR Normative Channel Insertion Loss at 28.05 Gsym/s



10.2.6.3 Fitted insertion loss

For fitted insertion loss definitions, please refer to Section 12.2.1.1

The channel shall meet the insertion loss requirements defined in Table 10-4. Note that the variable f_b is the maximum baud rate to be supported by the channel under test.

Table 10-4. Channel fitted insertion loss characteristics

Parameter	Units	Value	
		Min.	Max.
Minimum frequency, f_{ILmin}	GHz	0.05	-
Maximum frequency, f_{ILmax}	GHz	-	f_b
Fitted Insertion loss at Nyquist	dB	-	15.42
Fitted insertion loss, a_0	dB	-1	1.5
Fitted insertion loss, a_1	dB	0	9.533
Fitted insertion loss, a_2	dB	0	30.855
Fitted insertion loss, a_4	dB	0	14.162

10.2.6.4 Insertion loss deviation (ILD)

The insertion loss deviation *ILD* is the difference between the measured insertion *IL* and the fitted insertion loss IL_{fitted} as defined in (10-3).

$$ILD = IL - IL_{fitted} \tag{10-3}$$

The insertion loss deviation ILD shall be within the region defined by (10-4) and (10-5) where f_b is the maximum baud rate to be supported by the channel under test and f_{ILmin} and f_{ILmax} are given in Table 10-4.

$$ILD \geq ILD_{min} = \begin{Bmatrix} -1.0 - 12.0(f/f_b) & f_{ILmin} \leq f < f_b/4 \\ -4.0 & f_b/4 \leq f \leq (3/4)f_{ILmax} \end{Bmatrix} \tag{10-4}$$

$$ILD \leq ILD_{max} = \begin{Bmatrix} 1.0 + 12.0(f/f_b) & f_{ILmin} \leq f < f_b/4 \\ 4.0 & f_b/4 \leq f \leq (3/4)f_{ILmax} \end{Bmatrix} \tag{10-5}$$

FOM_{ILD}, a figure of merit for the channel, is calculated as indicated below. In OIF-CEI-03.0 and OIF-CEI-03.1, FOM_{ILD} was called ILD_{rms}.

Define the weight at each frequency *f* using equation (10-6) below.

$$W(f) = \sin c^2(f/f_b)\left[\frac{1}{1+(f/f_t)^4}\right]\left[\frac{1}{1+(f/f_r)^8}\right] \tag{10-6}$$

Note that -3 dB transmit filter bandwidth f_t is inversely proportional to the minimum 20 to 80% rise and fall times *T_tr and T_tf*. The constant of proportionality is 0.2365 (e.g. T_tr x f_t = 0.2365), where T_tr is in nano seconds and f_t is in GHz. In addition, f_r is the -3 dB reference receiver bandwidth, which should be set at (3/4)f_b, where f_b is the maximum baud rate to be supported by the channel.

$$FOM_{ILD} = \sqrt{\frac{\sum W(f) \times ILD(f)^2}{N}} \quad (10\text{-}7)$$

where N is the number of frequency points, the summation is done over the frequency range of ILD and FOM_{ILD} shall be less than 0.3dB for valid channels.

10.2.6.5 Channel differential return loss

Channel differential return loss shall be bounded by:

- RL(f) >= 12 dB for $f_{min} < f \leq f_b/4$ (10-8)
- RL(f) >= 12 dB - 15 $Log_{10}(4f/f_b)$ for $f_b/4 < f < f_b$ (10-9)

Note: f_{min} is as defined in Table 10-3

10.2.6.6 Channel integrated crosstalk noise

Using the Integrated crosstalk noise method of Section 12.2.1.2 and the parameters of Table 10-5, the total integrated crosstalk noise for the channel shall be less than the value specified by Equation (10-10) and illustrated in Figure 10-3.

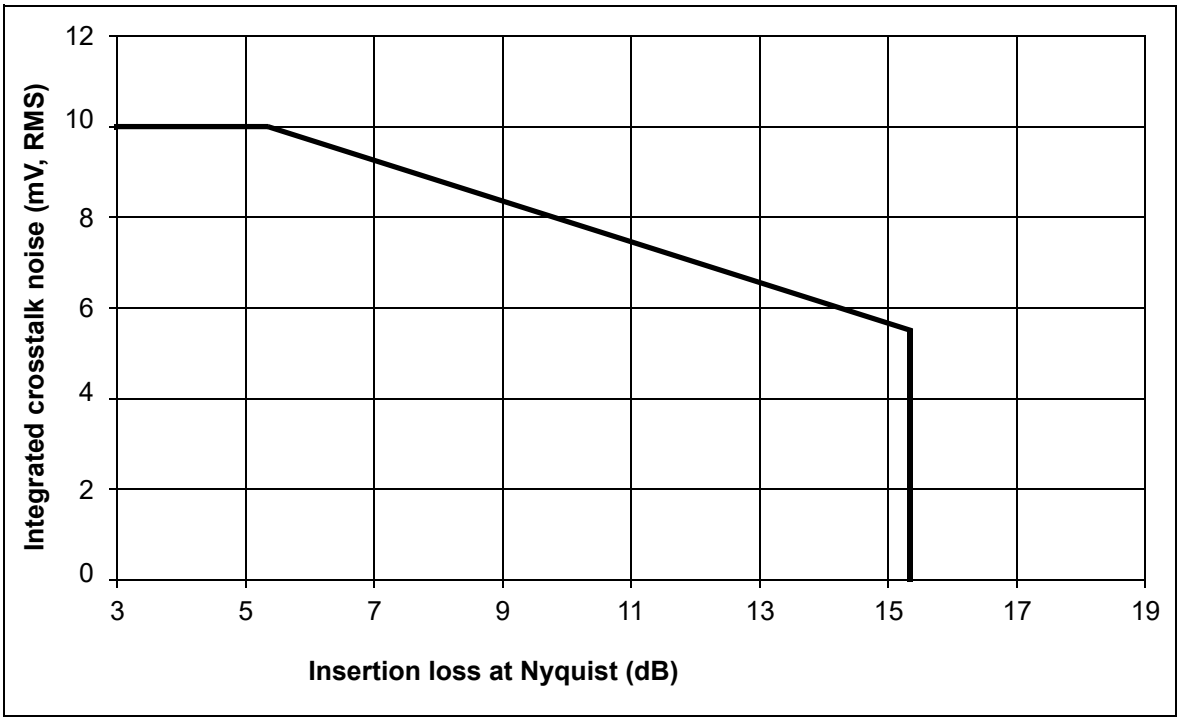
Table 10-5. Channel integrated crosstalk aggressor parameters

Parameter	Symbol	Value	Units
Baud rate	f_b	max. Baud Rate sup. by Channel	Gsym/s
Near-end aggressor peak to peak differential output amplitude	A_{nt}	1200	mVppd
Far-end aggressor peak to peak differential output amplitude	A_{ft}	1200	mVppd
Near-end aggressor 20 to 80% rise and fall times	T_{nt}	8	ps
Far-end aggressor 20 to 80% rise and fall times	T_{ft}	8	ps

$$\begin{aligned} \sigma_x \leq \sigma_{x,\,max} &= 10\ (mV, RMS) && for && 3\,dB < IL \leq 5.3\ dB \\ 0 &= 12.4 - 0.45\,IL\ (mV, RMS) && for && 5.3\,dB < IL \leq 15.42\ dB \end{aligned} \quad (10\text{-}10)$$

In Equation (10-10), the *IL* denotes the value of the channel insertion loss in dB at 1/2 · baud rate (NRZ).

Figure 10-3. Illustration integrated crosstalk noise limits



10.3 Electrical Characteristics

The electrical signaling is based on high speed low voltage logic with a nominal differential impedance of 100 Ω.

All devices shall work within the range from 19.90 Gsym/s to 28.05 Gsym/s as specified for the device, with the baud rate tolerance as per Section 3.2.11. Note that implementation of specific protocols will define the operating baud rate without affecting CEI compliance.

10.3.1 Transmitter Characteristics

The transmitter electrical specifications at compliance point T are given in Table 10-6. The transmitter shall satisfy jitter requirements specified in Table 10-7. Jitter is measured as specified in Section 2.3.3, for a BER as specified in Section 10.2.4. It is assumed that the UBHPJ component of the transmitter jitter is not data-dependent jitter (DDJ) from the receiver view point, hence it cannot be equalized in the receiver. To attenuate noise and absorb even/odd mode reflections, the transmitter shall satisfy the Common Mode Output Return Loss requirement of Table 10-6.

Link budgets in this document assume adaptive TX FIR equalization that is part of the system management function. The specific implementation is outside the scope of this document.

Table 10-6. Transmitter Electrical Output Specification.

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	T_Baud		19.90		28.05	Gsym/s
Output Differential Voltage	T_Vdiff	Emphasis off. See Note 4	800		1200	mVppd
Differential Resistance	T_Rd		80	100	120	Ω
Differential Termination Resistance Mismatch (see Table 1-2)	T_Rdm				10	%
Output Rise and Fall Time (20% to 80%)	T_tr, T_tf	Emphasis off. See Note 2	8			ps
Common Mode Noise	T_Ncm	Note 3			12	mVrms
Differential Output Return Loss	T_SDD22	See Section 10.3.1.3				dB
Common Mode Output Return Loss	T_SCC22	Below 10 GHz			-6	dB
		10 GHz to baud rate			-4	
Output Common Mode Voltage	T_Vcm	Load Type 0 See Note 1	-100		1700	mV

NOTES:
1. Load Type 0 with min. T_Vdiff, AC-Coupling or floating load.
2. The transmitter under test is preset such that C0 is its maximum value (C0_max) and all other coefficients are zero. The 20% and 80% values are of the steady state one and zero. The max value is limited by the linear fit pulse peak value in Table 10-11.
3. Measurement procedure is defined in Section 12.3.
4. T_Vdiff is two times the steady-state value V_f as defined in Section 10.3.1.6.2. The value is given as differential p-p voltage.

Table 10-7. Transmitter Output Jitter Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Uncorrelated Unbounded Gaussian Jitter	T_UUGJ				0.15	UI_{PP}
Uncorrelated Bounded High Probability Jitter	T_UBHPJ	Note 2			0.15	UI_{PP}
Even-Odd Jitter (component of UBHPJ)	T_EOJ	Note 3			0.035	UI_{PP}
Total Jitter	T_TJ	Note 1			0.28	UI_{PP}

NOTES:
1. T_TJ includes all of the jitter components measured without any transmit equalization.
2. Measured with all possible values of transmitter equalization, excluding DDJ as defined in Section 12.1.1.
3. included in T_UBHPJ

10.3.1.1 Transmitter Baud Rate

All devices shall work within the range from 19.90 Gsym/s to 28.05 Gsym/s as specified for the device, with the baud rate tolerance as per Section 3.2.11. Note that implementation of specific protocols will define the operating baud rate without affecting CEI compliance.

10.3.1.2 Transmitter Amplitude and Swing

Transmitter differential output amplitude shall be able to drive between 800 to 1200 mVppd with transmit emphasis disabled. The absolute transmitter output voltage shall be between -0.3V and 1.9 V with respect to local ground. Transmitter differential output amplitude shall additionally adhere to the requirements in Section 10.3.1.6.

10.3.1.3 Transmitter Resistance and Return Loss

Please refer to Section 3.2.10 with the following parameters.

Table 10-8. Transmitter Differential Return Loss Parameters

Parameter	Value	Units
A0	-12	dB
f0	50	MHz
f1	0.1714 x T_Baud	Hz
f2	T_Baud	Hz
Slope	12.0	dB/dec

10.3.1.4 Transmitter Lane-to-Lane Skew

Please refer to Section 3.2.7

10.3.1.5 Transmitter Short Circuit Current

Please refer to Section 3.2.9

10.3.1.6 Transmitter output waveform requirements

The transmitter shall include an equalizer defined as:

$$H(Z) = C_{-1} + C_0 z^{-1} + C_1 z^{-2} \quad (10\text{-}11)$$

10.3.1.6.1 Summary of requirements

The normalized amplitudes of the coefficients of the transmitter equalizer (computed per 10.3.1.6.2) shall meet the requirements in Table 10-9.

Table 10-9. Coefficient range and step size

Coefficient	Normalized Amplitude		Normalized Step Size (%)
	Min (%)	Max (%)	
C_{-1}	-10	0	1.25 to 5
C_1	-25	0	1.25 to 5
C_0	40	100	1.25 to 5

The amplitude of a coefficient can be computed by multiplying its normalized amplitude by v_f, which is defined in equation (10-12). "min" is defined as the minimum normalized amplitude of the coefficient that must be supplied by the transmitter to be compliant. "max" is defined as the maximum normalized amplitude of the coefficient that must be supplied by the transmitter to be compliant.

In addition:

a) $|C_{-1}|+|C_0|+|C_1|$, the peak output voltage shall not exceed 1200 mVppd.

b) $C_{-1} + C_0 + C_1$, the steady-state output voltage shall be greater than or equal to 140 mVppd.

10.3.1.6.2 Process to compute coefficients

The coefficients of the transmitter equalizer shall be determined from the measured waveform during TX compliance test using the process described below.

1. The transmitter under test is preset such that C_0 is its maximum value (C_{0_max}) and all other coefficients are zero.

2. Capture at least one complete cycle of the test pattern PRBS9 at T [T is defined as the test point at the output of transmitter package] per 10.3.1.6.3.

3. Compute the linear fit to the captured waveform per 10.3.1.6.4.

4. Define t_x to be the time where the rising edge of the linear fit pulse, p, from step 3 crosses 50% of its peak amplitude.

5. Sample the linear fit pulse, p, at symbol-spaced intervals relative to the time $t_0 = t_x + 0.5$ UI, interpolating as necessary to yield the sampled pulse p_i.

6. Use p_i to compute the vector of coefficients, w, of a T_N_w-tap symbol-spaced transversal filter that equalizes for the transfer function from the transmit function to T per 10.3.1.6.5.

The parameters of the pulse fit and the equalizing filter are given in Table 10-10.

Table 10-10. Linear fit pulse and equalizing filter parameters

Parameter	Value (UI)
Linear fit pulse length T_N_p	8
Linear fit pulse delay T_D_p	2
Equalizer length T_N_w	8
Equalizer delay T_D_w	2

The differential zero to peak output voltage at T in the steady state, v_f, is estimated by equation (10-12).

$$v_f = \frac{1}{M} \cdot \sum_{k=1}^{M \cdot T_Np} p(k) \qquad (10\text{-}12)$$

In (10-12), p is the linear fit pulse from step 3 and M is the number of samples per symbol as defined in 10.3.1.6.3. The peak value of the linear fit pulse from step 3, p_{max}, shall satisfy the requirements of Table 10-11.The RMS value of the error between the linear fit and measured waveform from step 3, σ_e, shall satisfy the requirements of Table 10-11.

Table 10-11. Transmitter output waveform requirements

Parameter	Condition	Units	
Steady state output voltage, 2 x v_f	max	mVppd	1200
Steady state output voltage, 2 x v_f	min	mVppd	800
Linear fit pulse peak, p_{max}	min	-	0.80 x v_f
RMS error, σ_e	max	-	0.027 x v_f

For each configuration of the transmit equalizer:

7. Configure the transmitter under test as required.

8. Capture at least one complete cycle of the test pattern PRBS9 at T.

9. Compute the linear fit to the captured waveform per 10.3.1.6.4.

10. Define t_x to be the time where the rising edge of the linear fit pulse, p, from step 3 crosses 50% of its peak amplitude.

11. Sample the linear fit pulse, p, at symbol-spaced intervals relative to the time $t_0 = t_x + 0.5$ UI, interpolating as necessary to yield the sampled pulse p_i.

12. Equalize the sampled pulse, p_i, using the coefficient vector, w, computed in step 6 per 10.3.1.6.5 to yield the equalized pulse q_i.

The RMS value of the error between the linear fit and measured waveform from step 9, σ_e, shall satisfy the requirements of Table 10-11.

The normalized amplitude of coefficient C_{-1} is the value of q_i at time $t_0 + (T_D_w - 1)$ UI.
The normalized amplitude of coefficient C_0 is the value of q_i at time $t_0 + T_D_w$ UI.
The normalized amplitude of coefficient C_1 is the value of q_i at time $t_0 + (T_D_w + 1)$ UI.

10.3.1.6.3 Waveform acquisition

The transmitter under test repetitively transmits the specified test pattern. The waveform shall be captured with an effective sample rate that is M times the signaling rate of the transmitter under test. The value of M shall be an integer not less than 7. Averaging multiple waveform captures is recommended.

The captured waveform shall represent an integer number of repetitions of the test pattern totaling N bits. Hence the length of the captured waveform should be $M \cdot N$ samples. The waveform should be aligned such that the first M samples of waveform correspond to the first bit of the test pattern, the second M samples to the second bit, and so on.

10.3.1.6.4 Linear fit to the waveform measured at T

Given the captured waveform $y(k)$ and corresponding aligned symbols $x(n)$ derived from the procedure defined in 10.3.1.6.2, define the M-by-N waveform matrix Y as shown in (10-13).

$$Y = \begin{bmatrix} y(1) & y(M+1) & \cdots & y(M(N-1)+1) \\ y(2) & y(M+2) & \cdots & y(M(N-1)+2) \\ \vdots & \vdots & \cdots & \vdots \\ y(M) & y(2M) & \cdots & y(MN) \end{bmatrix} \quad (10\text{-}13)$$

Rotate the symbols vector *x* by the specified pulse delay D_p to yield x_r.

$$x_r = \begin{bmatrix} x(T_D_p+1) & x(T_D_p+2) & \cdots & x(N) & x(1) & \cdots & x(T_D_p) \end{bmatrix} \quad (10\text{-}14)$$

Define the matrix *X* to be an *N*-by-*N* matrix derived from x_r as shown in (10-15).

$$X = \begin{bmatrix} x_r(1) & x_r(2) & \cdots & x_r(N) \\ x_r(N) & x_r(1) & \cdots & x_r(N-1) \\ \vdots & \vdots & \cdots & \vdots \\ x_r(2) & x_r(3) & \cdots & x_r(1) \end{bmatrix} \quad (10\text{-}15)$$

Define the matrix X_1 to be the first T_N_p rows of *X* concatenated with a row vector of 1's of length *N*. The *M*-by-(T_N_p + 1) coefficient matrix, *P*, corresponding to the linear fit is then defined by (10-16).

$$P = YX_1^{\mathrm{T}}(X_1X_1^{\mathrm{T}})^{-1} \quad (10\text{-}16)$$

In (10-16) the superscript "T" denotes the matrix transpose operator.

$$E = PX_1 - Y = \begin{bmatrix} e(1) & e(M+1) & \cdots & e(M(N-1)+1) \\ e(2) & e(M+2) & \cdots & e(M(N-1)+2) \\ \vdots & \vdots & \cdots & \vdots \\ e(M) & e(2M) & \cdots & e(MN) \end{bmatrix} \quad (10\text{-}17)$$

The error waveform, *e(k)*, is then read column-wise from the elements of *E*.

Define P_1 to be a matrix consisting of the first T_N_p columns of the matrix *P* as shown in (10-18).

$$P_1 = \begin{bmatrix} p(1) & p(M+1) & \cdots & p(M(T_N_p - 1)+1) \\ p(2) & p(M+2) & \cdots & p(M(T_N_p - 1)+2) \\ \vdots & \vdots & \cdots & \vdots \\ p(M) & p(2M) & \cdots & p(MT_N_p) \end{bmatrix} \quad (10\text{-}18)$$

The linear fit pulse response, *p(k)*, is then read column-wise from the elements of P_1.

10.3.1.6.5 Removal of the transfer function between the transmit function and T

Rotate sampled pulse response p_i by the specified equalizer delay T_D_w to yield p_r as shown in (10-19).

$$p_r = \left[p_i(T_D_w + 1) \quad p_i(T_D_w + 2) \quad \cdots \quad p_i(T_N_p) \quad p_i(1) \quad \cdots \quad p_i(T_D_w) \right] \quad (10\text{-}19)$$

Define the matrix P_2 to be a T_N_p-by-T_N_p matrix derived from pr as shown in (10-20).

$$P_2 = \begin{bmatrix} p_r(1) & p_r(T_N_p) & \cdots & p_r(2) \\ p_r(2) & p_r(1) & \cdots & p_r(3) \\ \vdots & \vdots & \cdots & \vdots \\ p_r(T_N_p) & p_r(T_N_p - 1) & \cdots & p_r(1) \end{bmatrix} \quad (10\text{-}20)$$

Define the matrix P_3 to be the first T_N_w rows of P_2. Define a unit pulse column vector x_p of length T_N_p. The value of element $x_p(T_D_p + 1)$ is 1 and all other elements have a value of 0. The vector of filter coefficients w that equalizes p_i is then defined by (10-21).

$$w = (P_3^{\mathrm{T}} P_3)^{-1} P_3^{\mathrm{T}} x_p \quad (10\text{-}21)$$

Given the column vector of equalizer coefficients, w, the equalized pulse response q_i is determined by (10-22).

$$q_i = P_3 w \quad (10\text{-}22)$$

10.3.2 Receiver Characteristics

A compliant receiver shall operate at the specified BER with the worst case combination of a compliant transmitter and a compliant channel.

Receiver electrical specifications are given in Table 10-12 and measured at compliance point R. To dampen noise sources and absorption of both even and odd mode reflections, the receiver shall satisfy the Common Mode Input Return Loss requirement of Table 10-12. Jitter specifications at reference R are listed in Table 10-13.

Table 10-12. Receiver Electrical Input Specifications

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud rate	R_Baud		19.90		28.05	GSym/s
Input Differential Voltage	R_Vdiff	Note 1			1200	mVppd
Differential Input Impedance	R_Rdin		80	100	120	Ω
Input Impedance Mismatch	R_Rm				10	%
Differential Input Return Loss	R_SDD11	See 10.3.2.3				
Common Mode Input Return Loss	R_SCC11	Below 10 GHz			-6	dB
		10GHz to baud rate			-4	
Input Common Mode Voltage	R_Vcm	Load Type 0 See Note 2	-200		1800	mV

NOTES:
1. The receiver shall have a differential input voltage range sufficient to accept a signal produced at point R by the combined transmitter and channel. The channel response shall include the worst case effects of the return losses at the transmitter and receiver.
2. Load Type 0 with min. T_Vdiff, AC-Coupling or floating load. For floating load, input resistance shall be ≥ 1kΩ

Table 10-13. Receiver Input Jitter Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Sinusoidal Jitter, Maximum	R_SJ-max	See Section 2.3.4, note 1			5	UIpp
Sinusoidal Jitter, High Frequency	R_SJ-hf	See Section 2.3.4, note 1			0.05	UIpp

NOTES:
1. The Receiver shall tolerate the sum of these jitter contributions: Total transmitter jitter from Table 10-7;Sinusoidal jitter as defined in Table 10-13;The effects of a channel compliant to the Channel Characteristics (Section 10.2.6).

10.3.2.1 Input Baud Rate

All devices shall work within the range from 19.90 Gsym/s to 28.05 Gsym/s as specified for the device, with the baud rate tolerance as per Section 3.2.11.

10.3.2.2 Reference Input Signals

The receiver shall accept differential input signal amplitudes produced by a compliant transmitter connected with the minimum attenuation specified in Figure 10-2 to the receiver. This may be larger than the 1200 mVppd maximum of the transmitter due to output/input impedances and reflections.

The minimum input amplitude is defined by the minimum transmitter amplitude, the actual receiver input impedance and the loss of the actual PCB. Note that the minimum transmitter amplitude is defined using a well controlled load impedance, however the real receiver is not, which can leave the receiver input signal smaller than expected. Additionally it will be determined by the environmental noise inside and outside the receiver.

10.3.2.3 Input Resistance and Return Loss

Please refer to Section 3.2.10 with the following parameters.

Table 10-14. Receiver Differential Return Loss Parameters

Parameter	Value	Units
A0	-12	dB
f0	50	MHz
f1	0.1714 x R_Baud	Hz
f2	R_Baud	Hz
Slope	12.0	dB/dec

10.3.2.4 Input Lane-to-Lane Skew

Please refer to Section 3.2.8.

10.3.2.5 Absolute Input Voltage

The absolute voltage levels with respect to the receiver ground at the input of the receiver are dependent on the transmitter implementation and the inter-ground difference. The voltage levels at the input of an AC coupled receiver (if the effective AC coupling is done within the receiver) or at the TX side of the external AC coupling cap (if AC coupling is done externally) shall be between -0.3 to 2.0V with respect to local ground.

11 CEI-25G-LR Long Reach Interface

This clause details the requirements for the CEI-25G-LR long reach high speed electrical interface between nominal baud rates of 19.90 Gsym/s and 25.80 Gsym/s using NRZ coding. A compliant device shall meet all of the requirements listed below. The electrical interface is based on high speed, low voltage logic. Connections are point-to-point balanced differential pairs and signaling is unidirectional.

The electrical IA is based on loss and jitter budgets and defines the characteristics required to communicate between a CEI-25G-LR transmitter and a CEI-25G-LR receiver using copper signal traces on a printed circuit board. The characteristic impedance of the signal traces is nominally 100 Ω differential. A 'length' is effectively defined in terms of its attenuation and phase response rather than its physical length. Refer to Section 11.2.6 for transmission line guidelines to meet the channel requirements.

Long reach CEI-25G-LR devices from different manufacturers shall be interoperable.

11.1 Requirements

1. Support serial baud rates within the range from 19.90 Gsym/s to 25.80 Gsym/s.
2. Capable of low bit error ratio (10^{-15}, with a test requirement to verify 10^{-12}).
3. Capable of driving up to 686 mm of PCB and up to 2 connectors.
4. Shall support AC-coupled operation.
5. Shall allow multi-lanes (1 to n).
6. Shall support hot plug.

11.2 General Requirements

11.2.1 Data Patterns

Please refer to Section 3.2.1

11.2.2 Signal levels

Please refer to Section 3.2.2. All transmitter and receiver devices shall support "Load Type 0". Other load types are not supported by this clause.

11.2.3 Signal Definitions

Please refer to Section 1.A

11.2.4 Bit Error Ratio

Please refer to Section 3.2.3

11.2.5 Ground Differences

Please refer to Section 3.2.4

11.2.6 Channel Compliance

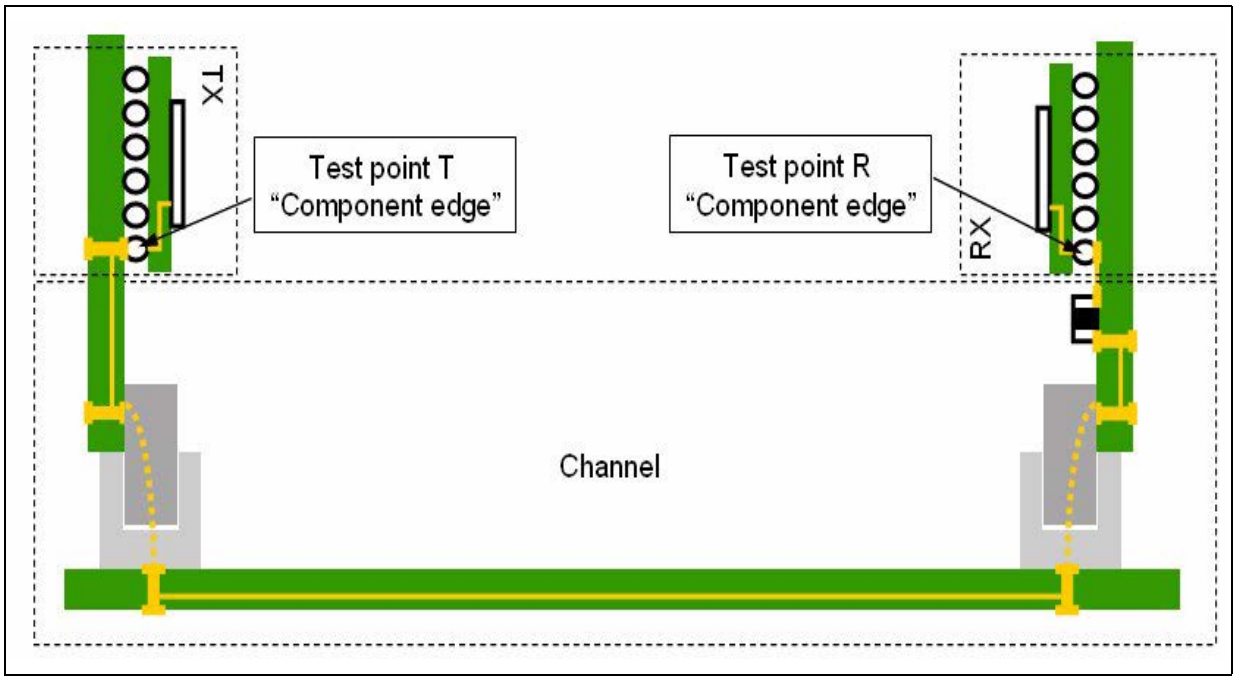
A forward channel and associated dominant crosstalk channels are deemed compliant if the channel characteristics conform to the requirements in this section.

11.2.6.1 Reference Model

The channel consists of PCB traces, vias, and up to 2 connectors. The reference PCB trace differential impedance is 100Ω.

Figure 11-1 shows a diagram of test points on an example board.

Figure 11-1. CEI-25G-LR Reference Model



Note: Test points differ from definitions in Section 1.8, as DC blocking capacitor, if physically located outside of the package, is part of the channel.

Measured at these test points, several channel characteristics are parametrized. Port definitions as noted in Figure 2-33 allow proper measurement of the parameters in Table 11-1 used for calculation of the channel parameters found in Table 11-2.

Table 11-1. Measured Channel Parameters

Symbol	Description
$IL(f)$	Differential insertion loss, -SDD21 magnitude (dB)
$RL_1(f)$	Differential input return loss, -SDD11 magnitude (dB)
$RL_2(f)$	Differential output return loss, -SDD22 magnitude (dB)
$NEXT_m(f)$	Differential near-end crosstalk loss (m^{th} aggressor), -SDD21 magnitude (dB)
$FEXT_n(f)$	Differential far-end crosstalk loss (n^{th} aggressor), -SDD21 magnitude (dB)

Table 11-2. Calculated Channel Parameters

Symbol	Description
$IL_{fitted}(f)$	Fitted insertion loss (dB)
$ILD(f)$	Insertion loss deviation (dB)
$ICN(f)$	Integrated crosstalk noise (mV, RMS)
FOM_{ILD}	RMS value of the insertion loss Deviation (dB)

11.2.6.2 Insertion Loss

Channel insertion losses, including PCB traces and connectors, shall comply with the limits specified by equations (11-1), (11-2) and plotted in Figure 11-2. Note that the variable f_b is the maximum baud rate to be supported by the channel under test (19.90 Gsym/s $\le f_b \le$ 25.80 Gsym/s).

Table 11-3. Channel Insertion Loss Frequency Range

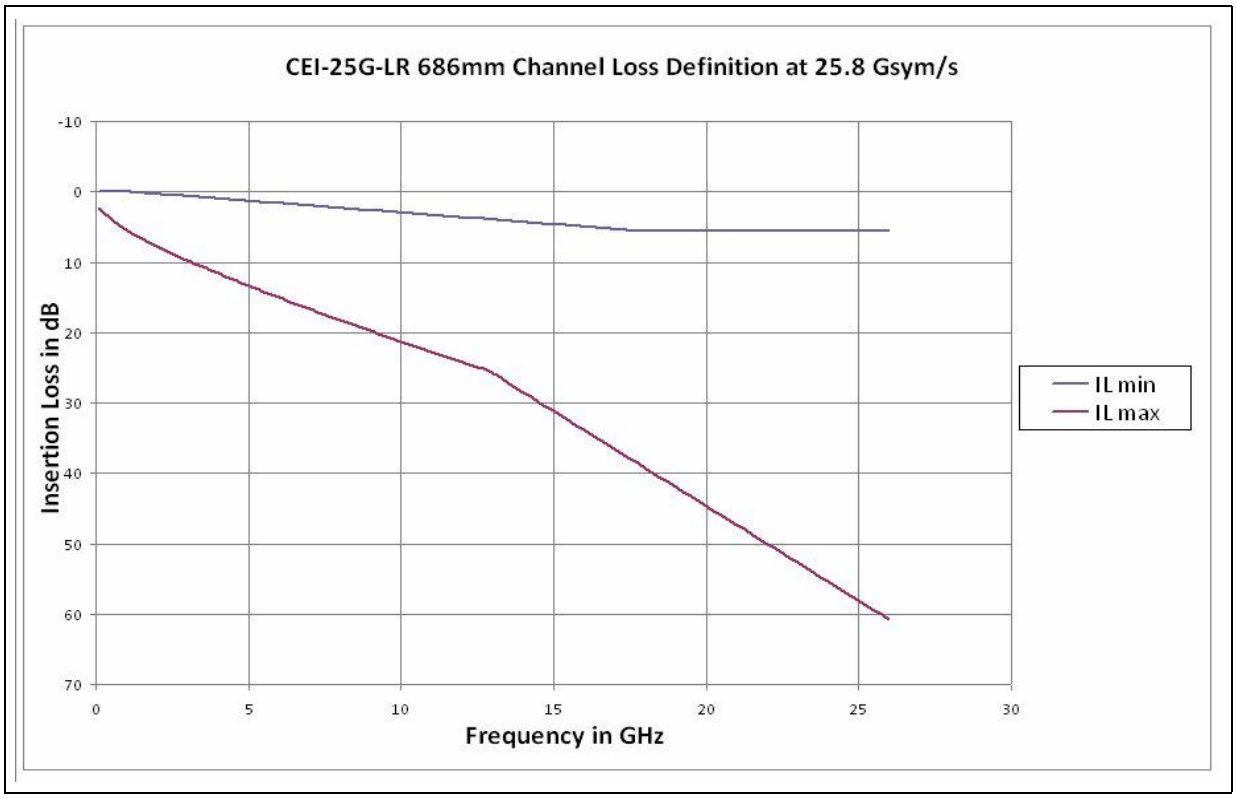
Parameter	Value	Units
fmin	50	MHz
fmax	**f_b**	GHz

$$IL_{max} = \begin{cases} 1.083 + 3.35\sqrt{\frac{f \times 25.8}{f_b}} + 0.96\frac{f \times 25.8}{f_b}, & f_{min} \le f < \frac{f_b}{2} \\ -9.25 + 2.694\frac{f \times 25.8}{f_b}, & \frac{f_b}{2} \le f \le f_b \end{cases} \quad (11\text{-}1)$$

$$IL_{min} = \begin{pmatrix} 0, & f_{min} \le f \le 1\,GHz \\ \frac{1}{3}(f-1), & 1\,GHz < f \le 17.5\,GHz \\ 5.5, & 17.5\,GHz < f \le f_b \end{pmatrix} \quad (11\text{-}2)$$

Note: f in (11-1) and (11-2) is in GHz.

Figure 11-2. CEI-25G-LR Normative Channel Insertion Loss at 25.80 Gsym/s.



11.2.6.3 Fitted insertion loss

For fitted insertion loss definitions, please refer to Section 12.2.1.1

The channel shall meet the insertion loss requirements defined in Table 11-4. Note that the variable f_b is the maximum baud rate to be supported by the channel under test.

Table 11-4. Channel fitted insertion loss characteristics

Parameter	Units	Value	
		Min.	Max.
Minimum frequency, f_{ILmin}	GHz	0.05	-
Maximum frequency, f_{ILmax}	GHz	-	f_b
Fitted Insertion loss at Nyquist	dB	-	25.5
Fitted insertion loss, a_0	dB	-1	2.0
Fitted insertion loss, a_1	dB	0	20.317
Fitted insertion loss, a_2	dB	0	51.6
Fitted insertion loss, a_4	dB	0	25.294

11.2.6.4 Insertion loss deviation (ILD)

The insertion loss deviation *ILD* is the difference between the measured insertion *IL* and the fitted insertion loss IL_{fitted} as defined in (11-3).

$$ILD = IL - IL_{fitted} \tag{11-3}$$

The insertion loss deviation ILD shall be within the region defined by (11-4) and (11-5) where f_b is the maximum baud rate to be supported by the channel under test and f_{ILmin} and f_{ILmax} are given in Table 11-4.

$$ILD \geq ILD_{min} = \begin{Bmatrix} -1.0 - 12.0(f/f_b) & f_{ILmin} \leq f < f_b/4 \\ -4.0 & f_b/4 \leq f \leq (3/4)f_{ILmax} \end{Bmatrix} \tag{11-4}$$

$$ILD \leq ILD_{max} = \begin{Bmatrix} 1.0 + 12.0(f/f_b) & f_{ILmin} \leq f < f_b/4 \\ 4.0 & f_b/4 \leq f \leq (3/4)f_{ILmax} \end{Bmatrix} \tag{11-5}$$

FOM_{ILD}, a figure of merit for the channel, is calculated as indicated below. In OIF-CEI-03.0 and OIF-CEI-03.1, FOM_{ILD} was called ILD_{rms}.

Define the weight at each frequency *f* using equation (11-6) below.

$$W(f) = \sin c^2(f/f_b)\left[\frac{1}{1+(f/f_t)^4}\right]\left[\frac{1}{1+(f/f_r)^8}\right] \tag{11-6}$$

Note that -3 dB transmit filter bandwidth f_t is inversely proportional to the minimum 20 to 80% rise and fall times *T_tr and T_tf*. The constant of proportionality is 0.2365 (e.g. T_tr x f_t = 0.2365), where T_tr is in nano seconds and f_t is in GHz. In addition, f_r is the -3 dB reference receiver bandwidth, which should be set at (3/4)f_b, where f_b is the maximum baud rate to be supported by the channel.

$$FOM_{ILD} = \sqrt{\frac{\sum W(f) \times ILD(f)^2}{N}} \quad (11\text{-}7)$$

where N is the number of frequency points, the summation is done over the frequency range of ILD and FOM_{ILD} shall be less than 0.3dB for valid channels.

11.2.6.5 Channel Return Loss

Channel Return Loss shall be bounded by:

- RL(f) >= 12 dB for $f_{min} < f \leq f_b/4$
- RL(f) >= 12 dB - 15 $Log_{10}(4f/f_b)$ for $f_b/4 < f < f_b$ (11-8)

(11-9)

Note: f_{min} is as defined in Table 11-3

11.2.6.6 Channel integrated crosstalk noise

Using the Integrated crosstalk noise method of Section 12.2.1.2 and the parameters of Table 11-5, the total integrated crosstalk noise for the channel shall be less than the value specified by Equation (11-10) and illustrated in Figure 11-3.

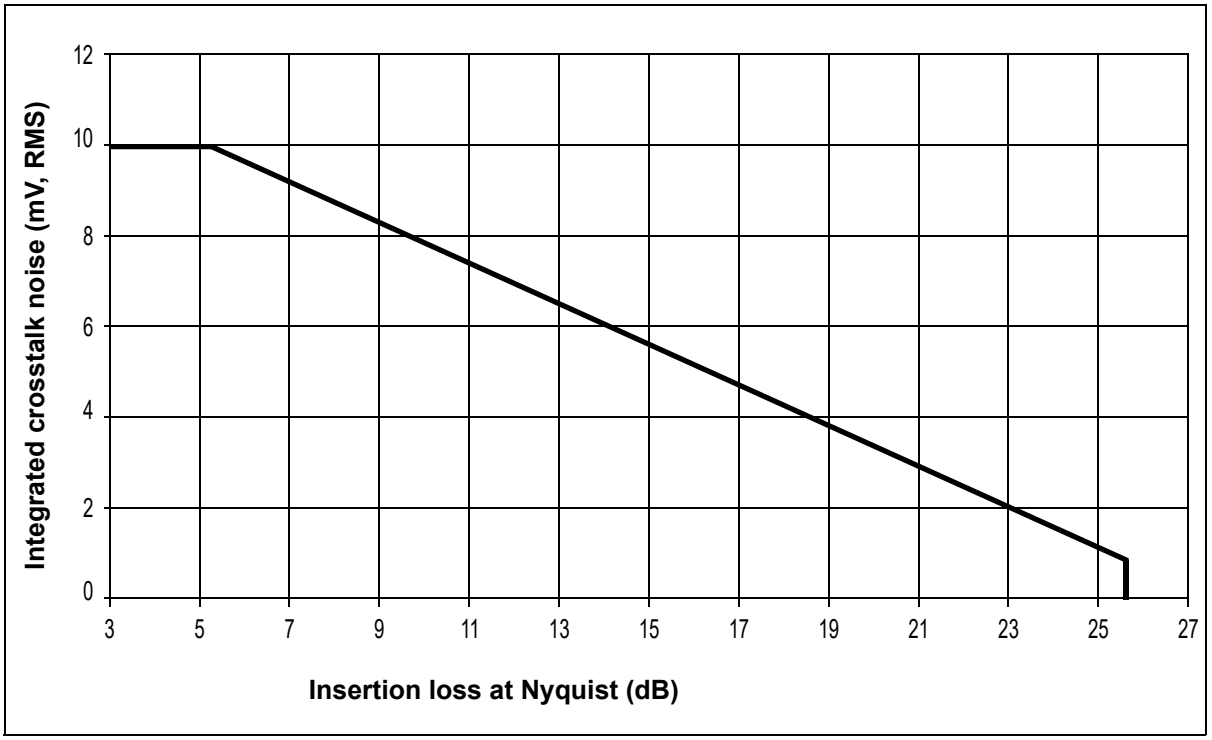
Table 11-5. Channel integrated crosstalk aggressor parameters

Parameter	Symbol	Value	Units
Baud rate	f_b	max. Baud Rate sup. by Channel	Gsym/s
Near-end aggressor peak to peak differential output amplitude	A_{nt}	1200	mVppd
Far-end aggressor peak to peak differential output amplitude	A_{ft}	1200	mVppd
Near-end aggressor 20 to 80% rise and fall times	T_{nt}	8	ps
Far-end aggressor 20 to 80% rise and fall times	T_{ft}	8	ps

$$\begin{aligned} \sigma_x \leq \sigma_{x,\,max} &= 10\ (mV, RMS) && for && 3\,dB < IL \leq 5.3\ dB \\ 0 &= 12.4 - 0.45\,IL\ (mV, RMS) && for && 5.3\,dB < IL \leq 25.5\ dB \end{aligned} \quad (11\text{-}10)$$

In Equation (11-10), the *IL* denotes the value of the channel insertion loss in dB at 1/2 · baud rate (NRZ).

Figure 11-3. Illustration integrated crosstalk noise limits



11.3 Electrical Characteristics

The electrical signaling is based on high speed low voltage logic with a nominal differential impedance of 100 Ω.

All devices shall work within the range from 19.90 Gsym/s to 25.80 Gsym/s as specified for the device, with the baud rate tolerance as per Section 3.2.11. Note that implementation of specific protocols will define the operating baud rate without affecting CEI compliance.

11.3.1 Transmitter Characteristics

The transmitter electrical specifications at compliance point T are given in Table 11-6. The transmitter shall satisfy jitter requirements specified in Table 11-7. Jitter is measured as specified in Section 2.4.3, for a BER as specified in Section 11.2.4. It is assumed that the UBHPJ component of the transmitter jitter is not data-dependent jitter (DDJ) from the receiver view point, hence it cannot be equalized in the receiver. To attenuate noise and absorb even/odd mode reflections, the transmitter shall satisfy the Common Mode Output Return Loss requirement of Table 11-6.

Link budgets in this document assume adaptive TX FIR equalization that is part of the system management function. The specific implementation is outside the scope of this document.

Table 11-6. Transmitter Electrical Output Specification.

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	T_Baud		19.90		25.80	Gsym/s
Output Differential Voltage	T_Vdiff	Emphasis off. See Note 4.	800		1200	mVppd
Differential Resistance	T_Rd		80	100	120	Ω
Differential Termination Resistance Mismatch (see Table 1-2)	T_Rdm				10	%
Output Rise and Fall Time (20% to 80%)	T_tr, T_tf	Emphasis off. See Note 2.	8			ps
Common Mode Noise	T_Ncm	See Note 3.			12	mVrms
Differential Output Return Loss	T_SDD22	See Section 11.3.1.3				dB
Common Mode Output Return Loss	T_SCC22	Below 10 GHz			-6	dB
		10 GHz to baud rate			-4	
Output Common Mode Voltage	T_Vcm	Load Type 0 See Note 1	-100		1700	mV

NOTES:
1. Load Type 0 with min. T_Vdiff, AC-Coupling or floating load.
2. The transmitter under test is preset such that C0 is its maximum value (C0_max) and all other coefficients are zero. The 20% and 80% values are of the steady state one and zero. The max value is limited by the linear fit pulse peak value in Table 11-11.
3. Measurement procedure is defined in Section 12.3.
4. T_Vdiff is two times the steady-state value V_f as defined in Section 11.3.1.6.2. The value is given as differential p-p voltage.

Table 11-7. Transmitter Output Jitter Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Uncorrelated Unbounded Gaussian Jitter	T_UUGJ				0.15	UI_{PP}
Uncorrelated Bounded High Probability Jitter	T_UBHPJ	Note 2			0.15	UI_{PP}
Even-Odd Jitter (component of UBHPJ)	T_EOJ	Note 3			0.035	UI_{PP}
Total Jitter	T_TJ	Note 1			0.28	UI_{PP}

NOTES:
1. T_TJ includes all of the jitter components measured without any transmit equalization.
2. Measured with all possible values of transmitter equalization, excluding DDJ as defined in Section 12.1.1.
3. included in T_UBHPJ

11.3.1.1 Transmitter Baud Rate

All devices shall work within the range from 19.90 Gsym/s to 25.80 Gsym/s as specified for the device, with the baud rate tolerance as per Section 3.2.11. Note that implementation of specific protocols will define the operating baud rate without affecting CEI compliance.

11.3.1.2 Transmitter Amplitude and Swing

Transmitter differential output amplitude shall be able to drive between 800 to 1200 mVppd with transmit emphasis disabled. The absolute transmitter output voltage shall be between -0.3V and 1.9 V with respect to local ground. Transmitter differential output amplitude shall additionally adhere to the requirements in Section 11.3.1.6.

11.3.1.3 Transmitter Resistance and Return Loss

Please refer to Section 3.2.10 with the following parameters.

Table 11-8. Transmitter Differential Return Loss Parameters

Parameter	Value	Units
A0	-12	dB
f0	50	MHz
f1	0.1714 x T_Baud	Hz
f2	T_Baud	Hz
Slope	12.0	dB/dec

11.3.1.4 Transmitter Lane-to-Lane Skew

Please refer to Section 3.2.7

11.3.1.5 Transmitter Short Circuit Current

Please refer to Section 3.2.9

11.3.1.6 Transmitter output waveform requirements

The transmitter shall include an equalizer defined as:

$$H(Z) = C_{-1} + C_0 z^{-1} + C_1 z^{-2} \quad (11\text{-}11)$$

11.3.1.6.1 Summary of requirements

The normalized amplitudes of the coefficients of the transmitter equalizer (computed per 11.3.1.6.2) shall meet the requirements in Table 11-9.

Table 11-9. Coefficient range and step size

Coefficient	Normalized Amplitude		Normalized Step Size (%)
	Min (%)	Max (%)	
C_{-1}	-25	0	1.25 to 5
C_1	-25	0	1.25 to 5
C_0	40	100	1.25 to 5

The amplitude of a coefficient can be computed by multiplying its normalized amplitude by v_f, which is defined in equation (11-12). "min" is defined as the minimum normalized amplitude of the coefficient that must be supplied by the transmitter to be compliant. "max" is defined as the maximum normalized amplitude of the coefficient that must be supplied by the transmitter to be compliant.

In addition:

a) $|C_{-1}|+|C_0|+|C_1|$, the peak output voltage shall not exceed 1200 mVppd.

b) $C_{-1} + C_0 + C_1$, the steady-state output voltage shall be greater than or equal to 80 mVppd.

11.3.1.6.2 Process to compute coefficients

The coefficients of the transmitter equalizer shall be determined from the measured waveform during TX compliance test using the process described below.

1. The transmitter under test is preset such that C_0 is its maximum value (C_{0_max}) and all other coefficients are zero.

2. Capture at least one complete cycle of the test pattern PRBS9 at T [T is defined as the test point at the output of transmitter package] per 11.3.1.6.3.

3. Compute the linear fit to the captured waveform per 11.3.1.6.4.

4. Define t_x to be the time where the rising edge of the linear fit pulse, p, from step 3 crosses 50% of its peak amplitude.

5. Sample the linear fit pulse, p, at symbol-spaced intervals relative to the time $t_0 = t_x + 0.5$ UI, interpolating as necessary to yield the sampled pulse p_i.

6. Use p_i to compute the vector of coefficients, w, of a T_N_w-tap symbol-spaced transversal filter that equalizes for the transfer function from the transmit function to T per 11.3.1.6.5.

The parameters of the pulse fit and the equalizing filter are given in Table 11-10.

Table 11-10. Linear fit pulse and equalizing filter parameters

Parameter	Value (UI)
Linear fit pulse length T_N_p	8
Linear fit pulse delay T_D_p	2
Equalizer length T_N_w	8
Equalizer delay T_D_w	2

The differential zero to peak output voltage at T in the steady state, v_f, is estimated by equation (11-12).

$$v_f = \frac{1}{M} \cdot \sum_{k=1}^{M \cdot T_Np} p(k) \qquad (11\text{-}12)$$

In (11-12), p is the linear fit pulse from step 3 and M is the number of samples per symbol as defined in 11.3.1.6.3. The peak value of the linear fit pulse from step 3, p_{max}, shall satisfy the requirements of Table 11-11.The RMS value of the error between the linear fit and measured waveform from step 3, σ_e, shall satisfy the requirements of Table 11-11.

Table 11-11. Transmitter output waveform requirements

Parameter	Condition	Units	
Steady state output voltage, 2 x v_f	max	mVppd	1200
Steady state output voltage, 2 x v_f	min	mVppd	800
Linear fit pulse peak, p_{max}	min	-	0.80 x v_f
RMS error, σ_e	max	-	0.027 x v_f

For each configuration of the transmit equalizer:

7. Configure the transmitter under test as required.

8. Capture at least one complete cycle of the test pattern PRBS9 at T.

9. Compute the linear fit to the captured waveform per 11.3.1.6.4.

10. Define t_x to be the time where the rising edge of the linear fit pulse, p, from step 3 crosses 50% of its peak amplitude.

11. Sample the linear fit pulse, p, at symbol-spaced intervals relative to the time $t_0 = t_x + 0.5$ UI, interpolating as necessary to yield the sampled pulse p_i.

12. Equalize the sampled pulse, p_i, using the coefficient vector, w, computed in step 6 per 11.3.1.6.5 to yield the equalized pulse q_i.

The RMS value of the error between the linear fit and measured waveform from step 9, σ_e, shall satisfy the requirements of Table 11-11.

The normalized amplitude of coefficient C_{-1} is the value of q_i at time $t_0 + (T_D_w - 1)$ UI.
The normalized amplitude of coefficient C_0 is the value of q_i at time $t_0 + T_D_w$ UI.
The normalized amplitude of coefficient C_1 is the value of q_i at time $t_0 + (T_D_w + 1)$ UI.

11.3.1.6.3 Waveform acquisition

The transmitter under test repetitively transmits the specified test pattern. The waveform shall be captured with an effective sample rate that is M times the signaling rate of the transmitter under test. The value of M shall be an integer not less than 7. Averaging multiple waveform captures is recommended.

The captured waveform shall represent an integer number of repetitions of the test pattern totaling N bits. Hence the length of the captured waveform should be $M \cdot N$ samples. The waveform should be aligned such that the first M samples of waveform correspond to the first bit of the test pattern, the second M samples to the second bit, and so on.

11.3.1.6.4 Linear fit to the waveform measured at T

Given the captured waveform $y(k)$ and corresponding aligned symbols $x(n)$ derived from the procedure defined in 11.3.1.6.2, define the M-by-N waveform matrix Y as shown in (11-13).

$$Y = \begin{bmatrix} y(1) & y(M+1) & \cdots & y(M(N-1)+1) \\ y(2) & y(M+2) & \cdots & y(M(N-1)+2) \\ \vdots & \vdots & \cdots & \vdots \\ y(M) & y(2M) & \cdots & y(MN) \end{bmatrix} \quad (11\text{-}13)$$

Rotate the symbols vector *x* by the specified pulse delay D_p to yield x_r.

$$x_r = \begin{bmatrix} x(T_D_p+1) & x(T_D_p+2) & \cdots & x(N) & x(1) & \cdots & x(T_D_p) \end{bmatrix} \quad (11\text{-}14)$$

Define the matrix *X* to be an *N*-by-*N* matrix derived from x_r as shown in (11-15).

$$X = \begin{bmatrix} x_r(1) & x_r(2) & \cdots & x_r(N) \\ x_r(N) & x_r(1) & \cdots & x_r(N-1) \\ \vdots & \vdots & \cdots & \vdots \\ x_r(2) & x_r(3) & \cdots & x_r(1) \end{bmatrix} \quad (11\text{-}15)$$

Define the matrix X_1 to be the first T_N_p rows of *X* concatenated with a row vector of 1's of length *N*. The *M*-by-(T_N_p + 1) coefficient matrix, *P*, corresponding to the linear fit is then defined by (11-16).

$$P = YX_1^{\mathrm{T}}(X_1X_1^{\mathrm{T}})^{-1} \quad (11\text{-}16)$$

In (11-16) the superscript "T" denotes the matrix transpose operator.

$$E = PX_1 - Y = \begin{bmatrix} e(1) & e(M+1) & \cdots & e(M(N-1)+1) \\ e(2) & e(M+2) & \cdots & e(M(N-1)+2) \\ \vdots & \vdots & \cdots & \vdots \\ e(M) & e(2M) & \cdots & e(MN) \end{bmatrix} \quad (11\text{-}17)$$

The error waveform, *e(k)*, is then read column-wise from the elements of *E*.

Define P_1 to be a matrix consisting of the first T_N_p columns of the matrix P as shown in (11-18).

$$P_1 = \begin{bmatrix} p(1) & p(M+1) & \cdots & p(M(T_N_p - 1)+1) \\ p(2) & p(M+2) & \cdots & p(M(T_N_p - 1)+2) \\ \vdots & \vdots & \cdots & \vdots \\ p(M) & p(2M) & \cdots & p(MT_N_p) \end{bmatrix} \quad (11\text{-}18)$$

The linear fit pulse response, *p(k)*, is then read column-wise from the elements of P_1.

11.3.1.6.5 Removal of the transfer function between the transmit function and T

Rotate sampled pulse response p_i by the specified equalizer delay T_D_w to yield p_r as shown in (11-19).

$$p_r = \begin{bmatrix} p_i(T_D_w+1) & p_i(T_D_w+2) & \cdots & p_i(T_N_p) & p_i(1) & \cdots & p_i(T_D_w) \end{bmatrix} \quad (11\text{-}19)$$

Define the matrix P_2 to be a T_N_p-by-T_N_p matrix derived from pr as shown in (11-20).

$$P_2 = \begin{bmatrix} p_r(1) & p_r(T_N_p) & \cdots & p_r(2) \\ p_r(2) & p_r(1) & \cdots & p_r(3) \\ \vdots & \vdots & \cdots & \vdots \\ p_r(T_N_p) & p_r(T_N_p - 1) & \cdots & p_r(1) \end{bmatrix} \quad (11\text{-}20)$$

Define the matrix P_3 to be the first T_N_w rows of P_2. Define a unit pulse column vector x_p of length T_N_p. The value of element $x_p(T_D_p + 1)$ is 1 and all other elements have a value of 0. The vector of filter coefficients w that equalizes p_i is then defined by (11-21).

$$w = (P_3^{\mathrm{T}} P_3)^{-1} P_3^{\mathrm{T}} x_p \quad (11\text{-}21)$$

Given the column vector of equalizer coefficients, w, the equalized pulse response q_i is determined by (11-22).

$$q_i = P_3 w \quad (11\text{-}22)$$

11.3.2 Receiver Characteristics

A compliant receiver shall operate at the specified BER with the worst case combination of a compliant transmitter and a compliant channel.

Receiver electrical specifications are given in Table 11-12 and measured at compliance point R. To dampen noise sources and absorption of both even and odd mode reflections, the receiver shall satisfy the Common Mode Input Return Loss requirement of Table 11-12. Jitter specifications at reference R are listed in Table 11-13.

Table 11-12. Receiver Electrical Input Specifications

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud rate	R_Baud		19.90		25.80	GSym/s
Input Differential Voltage	R_Vdiff	Note 1			1200	mVppd
Differential Input Impedance	R_Rdin		80	100	120	Ω
Input Impedance Mismatch	R_Rm				10	%
Differential Input Return Loss	R_SDD11	See 11.3.2.3				
Common Mode Input Return Loss	R_SCC11	Below 10 GHz			-6	dB
		10GHz to baud rate			-4	
Input Common Mode Voltage	R_Vcm	Load Type 0 See Note 2	-200		1800	mV

NOTES:
1. The receiver shall have a differential input voltage range sufficient to accept a signal produced at point R by the combined transmitter and channel. The channel response shall include the worst case effects of the return losses at the transmitter and receiver.
2. Load Type 0 with min. T_Vdiff, AC-Coupling or floating load. For floating load, input resistance shall be ≥ 1kΩ

Table 11-13. Receiver Input Jitter Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Sinusoidal Jitter, Maximum	R_SJ-max	See Section 2.4.4, note 1			5	UIpp
Sinusoidal Jitter, High Frequency	R_SJ-hf	See Section 2.4.4, note 1			0.05	UIpp

NOTES:
1. The Receiver shall tolerate the sum of these jitter contributions: Total transmitter jitter from Table 11-7;Sinusoidal jitter as defined in Table 11-13;The effects of a channel compliant to the Channel Characteristics (Section 11.2.6).

11.3.2.1 Input Baud Rate

All devices shall work within the range from 19.90 Gsym/s to 25.80 Gsym/s as specified for the device, with the baud rate tolerance as per Section 3.2.11.

11.3.2.2 Reference Input Signals

The receiver shall accept differential input signal amplitudes produced by a compliant transmitter connected with the minimum attenuation specified in Figure 11-2 to the receiver. This may be larger than the 1200 mVppd maximum of the transmitter due to output/input impedances and reflections.

The minimum input amplitude is defined by the minimum transmitter amplitude, the actual receiver input impedance and the loss of the actual PCB. Note that the minimum transmitter amplitude is defined using a well controlled load impedance, however the real receiver is not, which can leave the receiver input signal smaller than expected. Additionally it will be determined by the environmental noise inside and outside the receiver.

11.3.2.3 Input Resistance and Return Loss

Please refer to Section 3.2.10 with the following parameters.

Table 11-14. Receiver Differential Return Loss Parameters

Parameter	Value	Units
A0	-12	dB
f0	50	MHz
f1	0.1714 x R_Baud	Hz
f2	R_Baud	Hz
Slope	12.0	dB/dec

11.3.2.4 Input Lane-to-Lane Skew

Please refer to Section 3.2.8.

11.3.2.5 Absolute Input Voltage

The absolute voltage levels with respect to the receiver ground at the input of the receiver are dependent on the transmitter implementation and the inter-ground difference. The voltage levels at the input of an AC coupled receiver (if the effective AC coupling is done within the receiver) or at the TX side of the external AC coupling cap (if AC coupling is done externally) shall be between -0.3 to 2.0V with respect to local ground.

12 Test Methodologies for CEI Baud Rates above 11G

This test methodology clause defines some common requirements needed for the following variants: CEI-28G-SR, CEI-28G-MR, CEI-25G-LR, CEI-56G-USR, CEI-56G-XSR-NRZ, and CEI-56G-XSR-PAM4.

12.1 TX jitter measurement methodology

- TX jitter measurements are performed using the Short Stress Pattern Random (SSPR) defined in Appendix 2.D.2 of the “Implementation Guide for the Common Electrical Interface 2.0", except for DDJ, which is measured using PRBS9.
- Unless otherwise specified, TX jitter parameters defined in Table 10-7 and 11-7 are measured with TX FIR equalization turned-off and on.
- Jitter distributions are defined in 2.C.4, and are the basis for determining the jitter parameters
- Jitter distributions are measured with any jitter measurement capable instrument (e.g., scope, BERT) referenced to a golden PLL recovery clock timing with its corner frequency set at baud rate/1667.
- T_UUGJ, T_UBHPJ, and T_TJ are derived with the method defined in 2.C.4.6 from the BER CDF. T_UBHPJ is calculated as HPJ_{total} - DDJ.
- T_DCD is defined in Section 1.6, Table 1-3
- T_EOJ is defined in Section 1.6, Table 1-3
- The DDJ difference with TX FIR on and off is defined as:
  diff_DDJ = T_DDJ (FIR on) -T_DDJ (FIR off)
- T_UUGJ, T_UBHPJ, T_TJ, T_DCD, and T_DDJ need to be measured with TX FIR on and off
- diff_DDJ should be subtracted from the T_TJ measured when the FIR is on
- T_UUGJ, T_UBHPJ, T_TJ, and T_DCD measured with FIR on and off should be within the limits as defined in Table 10-7 and 11-7
- The measurement instrument bandwidth should be at least 40 GHz. If the measurement bandwidth affects the result, it can be corrected using post-processing

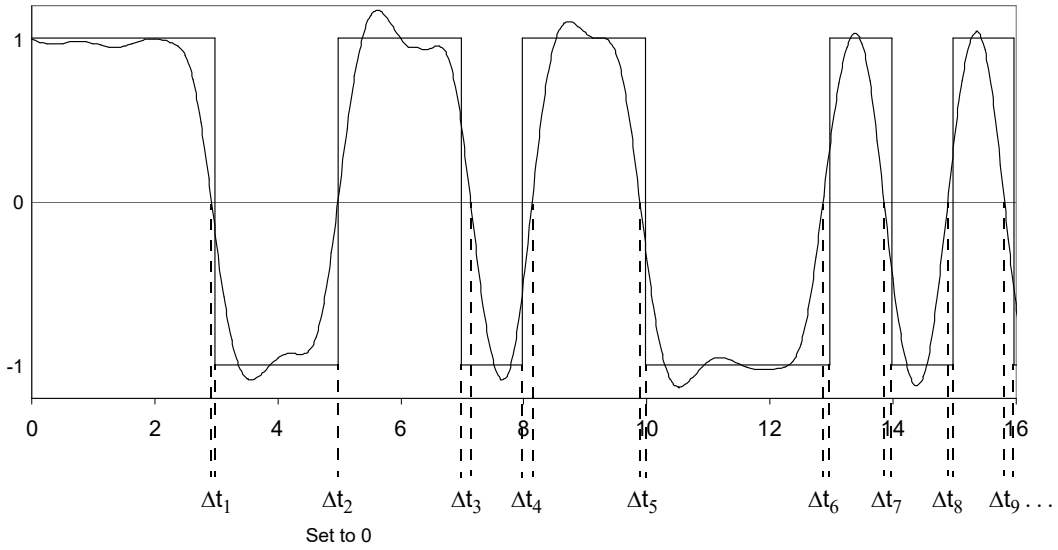
12.1.1 Data Dependent Jitter (DDJ) measurement

A high-resolution oscilloscope, time interval analyzer, or other instrument with equivalent capability may be used to measure DDJ. Establish a crossing level equal to the average value of the entire waveform being measured.

Synchronize the instrument to the pattern repetition frequency and average the waveforms or the crossing times sufficiently to remove the effects of random jitter and noise in the system. The mean time of each crossing is then compared to the expected time of the crossing, and a set of timing variations is determined. DDJ is the range (max-min) of the timing variations. Keep track of the signs (early/late) of the variations. Note, it may be convenient to align the expected time of one of the crossings with the measured mean crossing. All edges of the repeating pattern that have been averaged need to be included in the measurement.

The following Figure 12-1 illustrates the method. The vertical axis is in arbitrary units, and the horizontal axis is plotted in UI. The waveform is AC coupled to an average value of 0, therefore 0 is the appropriate crossing level. The rectangular waveform shows the expected crossing times, and the other is the waveform with jitter that is being measured. Only 16 UI are shown in this example. The waveforms have been arbitrarily aligned with ($\Delta t_2 = 0$) at 5 UI.

Figure 12-1. DDJ Measurement Method



$$DDJ = \max(\Delta t_1, \Delta t_2, \ldots \Delta t_n) - \min(\Delta t_1, \Delta t_2, \ldots \Delta t_n)$$

12.2 Channel compliance methodology

12.2.1 Channel Compliance

A forward channel and associated dominant crosstalk channels are deemed compliant if the channel characteristics conform to the requirements in the relevant clause, using the methodologies described in this section.

12.2.1.1 Fitted insertion loss

The weighted fitted insertion loss IL_{fitted} as a function of frequency f is defined by the equation below.

$$IL_{fitted}(f) = a_0 + a_1\sqrt{\frac{f}{f_b}} + a_2\frac{f}{f_b} + a_4\left(\frac{f}{f_b}\right)^2 \quad (dB) \tag{12-1}$$

Where f_b is the maximum symbol rate to be supported by the channel under test.

Given the channel insertion loss measurement at N uniformly-spaced frequencies f_n spanning f_{ILmin} to f_{ILmax} with a maximum frequency spacing of 10MHz. The coefficients of the fitted insertion loss are computed as follows.

Note: f_{ILmin}, f_{ILmax} are defined in Table 10-4/ 11-4.

Define the weighted frequency matrix F as shown below, where "$mag(IL_f)$" is the magnitude of the measured insertion loss at each frequency point [$mag(IL_{fx}) = 10^{(-IL_{fx}/20)}$]. Note: $mag(IL_f)$ is a real number between 0 and 1.

$$F = \begin{bmatrix} mag(IL_{f_1}) & mag(IL_{f_1})\times\sqrt{\frac{f_1}{f_b}} & mag(IL_{f_1})\times\frac{f_1}{f_b} & mag(IL_{f_1})\times\left(\frac{f_1}{f_b}\right)^2 \\ mag(IL_{f_2}) & mag(IL_{f_2})\times\sqrt{\frac{f_2}{f_b}} & mag(IL_{f_2})\times\frac{f_2}{f_b} & mag(IL_{f_2})\times\left(\frac{f_2}{f_b}\right)^2 \\ \cdots & \cdots & \cdots & \cdots \\ mag(IL_{f_N}) & mag(IL_{f_N})\times\sqrt{\frac{f_N}{f_b}} & mag(IL_{f_N})\times\frac{f_N}{f_b} & mag(IL_{f_N})\times\left(\frac{f_N}{f_b}\right)^2 \end{bmatrix} \tag{12-2}$$

The polynomial coefficients a_0, a_1, a_2, and a_4 are determined using the Equation below.

$$\begin{bmatrix} a_0 \\ a_1 \\ a_2 \\ a_4 \end{bmatrix} = \langle F^T F \rangle^{-1} F^T \left[mag(IL_f) \times IL_f \right] \quad \text{(12-3)}$$

Where T denotes the matrix transpose operator and IL_f is a column vector of the measured insertion loss values, in dB, at each frequency point.

This polynomial fit process is expected to yield values for the coefficients a_0, a_1, a_2, and a_4 that are greater than the minimum and less than the maximum coefficients (as specified in the specific clauses). If any of the coefficients in the equation are below the minimum allowed value they are forced to the minimum value and the fitting process is iterated (see example below). Iteration is done by creating a newIL by subtracting all coefficients below the minimum allowed value from the original IL, removing those coefficients from F and recalculating the remaining coefficients. At the end of the iteration, limit all coefficients to the maximum allowed, followed by a final iteration on any coefficients not previously limited.

For each iteration only one additional coefficient should be forced to a value. If multiple coefficients are below the minimum or above the maximum then the coefficients should be forced to a value in the following order - a4 followed by a1 followed by a2 and last a0.

Example iteration: If a_2 needs to be set to zero, but all other coefficients are within the range, then calculate newIL and solve for a_0, a_1 & a_4 as indicated below.

$$newIL = IL - \left[a_{2_{fixed}} \times \frac{f}{f_b} \right] \quad \text{(12-4)}$$

Define the frequency matrix F as shown below

$$F = \begin{bmatrix} mag(IL_{f_1}) & mag(IL_{f_1}) \times \sqrt{\frac{f_1}{f_b}} & mag(IL_{f_1}) \times \left(\frac{f_1}{f_b}\right)^2 \\ mag(IL_{f_2}) & mag(IL_{f_2}) \times \sqrt{\frac{f_2}{f_b}} & mag(IL_{f_2}) \times \left(\frac{f_2}{f_b}\right)^2 \\ \cdots & \cdots & \cdots \\ mag(IL_{f_N}) & mag(IL_{f_N}) \times \sqrt{\frac{f_N}{f_b}} & mag(IL_{f_N}) \times \left(\frac{f_N}{f_b}\right)^2 \end{bmatrix} \quad (12\text{-}5)$$

The polynomial coefficient a_0, a_1 & a_4 are determined using the Equation below.

$$\begin{bmatrix} a_0 \\ a_1 \\ a_4 \end{bmatrix} = \langle F^T F \rangle^{-1} F^T \left[mag(IL_f) \times IL_f \right] \quad (12\text{-}6)$$

Where T denotes the matrix transpose operator and IL_f is a column vector of the measured insertion loss values, in dB, at each frequency point.

If after this iteration, a_1 is below minimum allowed value, then another newIL is calculated as indicated below.

$$newIL = IL - \left[a_{1_{fixed}} \times \sqrt{\frac{f}{f_b}} + a_{2_{fixed}} \times \frac{f}{f_b} \right] \quad (12\text{-}7)$$

Define the frequency matrix F as shown below

$$F = \begin{bmatrix} mag(IL_{f_1}) & mag(IL_{f_1}) \times \left(\frac{f_1}{f_b}\right)^2 \\ mag(IL_{f_2}) & mag(IL_{f_2}) \times \left(\frac{f_2}{f_b}\right)^2 \\ \cdots & \cdots \\ mag(IL_{f_N}) & mag(IL_{f_N}) \times \left(\frac{f_N}{f_b}\right)^2 \end{bmatrix} \quad (12\text{-}8)$$

The polynomial coefficient a_0 & a_4 are determined using the Equation below.

$$\begin{bmatrix} a_0 \\ a_4 \end{bmatrix} = \langle F^T F \rangle^{-1} F^T \left[mag(IL_f) \times IL_f \right] \quad \text{(12-9)}$$

Where T denotes the matrix transpose operator and IL_f is a column vector of the measured insertion loss values, in dB, at each frequency point.

If after this iteration all values are within range, the calculation is finished.

12.2.1.2 Integrated crosstalk noise

Given multi-disturber near-end crosstalk loss $MDNEXT_{loss}$ and multi-disturber far-end crosstalk loss $MDFEXT_{loss}$ measured over N frequencies f_x spanning 0.05 GHz to f_b (where f_b is the maximum baud rate supported by the channel), with uniform frequency step Δf, the RMS value of the integrated crosstalk noise σ_x shall be calculated as follows.

$MDNEXT_{loss}$ is determined from all individual pair-to-pair differential NEXT loss values using Equation (12-10).

$$MDNEXT_{loss}(f) = -10 \times \log_{10}\left(\sum_{i=0}^{all\ NEXTs} 10^{-(NLi(f))/10} \right) (dB) \quad \text{(12-10)}$$

for 0.05 GHz $\leq f \leq f_b$

where

$MDNEXT_{loss}(f)$	is the MDNEXT loss at frequency f,
$NL_i(f)$	is the NEXT loss at frequency f of pair combination i, in dB,
f	is the frequency in GHz,
i	is all pair-to-pair combinations.

$MDFEXT_{loss}$ is determined from all individual pair-to-pair differential FEXT loss values using Equation (12-11).

$$MDFEXT_{loss}(f) = -10 \times \log_{10}\left(\sum_{i=0}^{all\ FEXTs} 10^{-(NLi(f))/10} \right) (dB) \quad \text{(12-11)}$$

for 0.05 GHz ≤ f ≤ f_b

where

$MDFEXT_{loss}(f)$	is the MDFEXT loss at frequency f,
$NL_i(f)$	is the FEXT loss at frequency f of pair combination i, in dB,
f	is the frequency in GHz,
i	is all pair-to-pair combinations.

Define the weight at each frequency f_n using Equation (12-12) and Equation (12-13).

$$W_{nt}(f) = (A_{nt}^2 / 4f_b)\,\mathrm{sinc}^2(f/f_b)\left[\frac{1}{1+(f/f_{nt})^4}\right]\left[\frac{1}{1+(f/f_r)^8}\right] \quad (12\text{-}12)$$

$$W_{ft}(f) = (A_{ft}^2 / 4f_b)\,\mathrm{sinc}^2(f/f_b)\left[\frac{1}{1+(f/f_{ft})^4}\right]\left[\frac{1}{1+(f/f_r)^8}\right] \quad (12\text{-}13)$$

Note that -3 dB transmit filter bandwidths f_{nt} and f_{ft} are inversely proportional to the 20 to 80% rise and fall times T_{nt} and T_{ft} respectively. The constant of proportionality is 0.2365 (e.g. $T_{nt}\,f_{nt}$ = 0.2365), where T_{nt} is in nano seconds and f_{nt} is in GHz. In addition, f_r is the -3 dB reference receiver bandwidth, which should be set at 3/4 the maximum baud rate specified for the device.

The near-end integrated crosstalk noise σ_{nx} is calculated using Equation (12-14).

$$\sigma_{nx} = \left(2\Delta f \sum_n W_{nt}(f_n)\,10^{-MDNEXT_{loss}(f_n)/10}\right)^{1/2} \quad (12\text{-}14)$$

The far-end integrated crosstalk noise σ_{fx} is calculated using Equation (12-15).

$$\sigma_{fx} = \left(2\Delta f \sum_n W_{ft}(f_n)\,10^{-MDFEXT_{loss}(f_n)/10}\right)^{1/2} \quad (12\text{-}15)$$

The total integrated crosstalk noise σ_x is calculated using Equation (12-16).

$$\sigma_x = \sqrt{\sigma_{nx}^2 + \sigma_{fx}^2} \quad (12\text{-}16)$$

12.3 Common Mode Noise

Common mode noise specification is to be measured using the following test procedure.

The data pattern is normal traffic or a common test pattern. Connect both waveform polarities through a suitable test fixture to a 50 ohm communication analysis oscilloscope system. Waveforms are not triggered (free-run mode). Scope shall have a minimum bandwidth (including probes) of 1.8 times the signaling rate.

No filtering except AC coupling with a high-pass 3dB low frequency not greater than 10MHz.

The two inputs are summed for common mode analysis. Set the horizontal scale for full width to span one UI. Set up a vertical histogram with full display width. Measure the rms value of the histogram. Common mode rms value (*Ncm*) is half the rms value of the histogram.

Follow equation (12-17) below to account for instrumentation noise.

$$T_Ncm(orR_Ncm) = \sqrt{(measured_Ncm)^2 - (instrumentation_noise)^2} \quad (12\text{-}17)$$

13 CEI-28G-VSR Very Short Reach Interface

This clause details the requirements for the CEI-28G-VSR very short reach high speed chip-to-module electrical interface of nominal baud rates of 19.6 Gsym/s to 28.1 Gsym/s. A compliant host or module shall meet all of the relevant requirements listed below. The electrical interface is based on high speed, low voltage logic, and connections are point-to-point balanced differential pairs.

This clause defines the characteristics required to communicate between CEI-28G-VSR drivers and CEI-28G-VSR receivers using copper signal traces on a printed circuit board, a mated connector pair and copper signal traces inside an optical module. These specifications are normative at the test points shown in Figure 13-1. A 'length' is effectively defined in terms of its attenuation and phase response rather than its physical length.

Hosts and modules compliant to CEI-28G-VSR from different manufacturers shall be interoperable.

13.1 Requirements

The objectives and requirements for the CEI-28G-VSR implementation agreement are given by the project definition as follows:

- Support serial baud rates (f_b) within the range from 19.6 Gsym/s to 28.1 Gsym/s as specified for the device using ***NRZ coding***. Note that implementation of specific protocols will define the operating baud rate without affecting CEI compliance.
- Capable of driving up to a minimum of ***100 mm*** of host PCB trace plus one connector and a minimum of **50 mm** of module PCB trace
- Capable of achieving Bit Error Ratio of 10^{-15} or better per lane
- Shall support AC-coupled operation.
- Shall allow multi-lanes (1 to n).
- Shall support hot plug.
- The IA will document the constraints of the chip-to-module application(s) used to derive the channel model specifications
- The IA shall define a compliance test methodology including compliance boards.

13.2 General CEI Requirements

13.2.1 Data Patterns

See 3.2.1.

13.2.2 Signal levels

The CEI-28G-VSR interface uses low swing differential signaling. It is designed to operate with load type 0 from Section 3.2.2 (no other load types are supported).

This type of differential interface allows for interoperability between components operating from different supply voltages and different I/O types (CML, LVDS-like, PECL, etc.). Low swing differential signaling provides noise immunity and improved electromagnetic interference (EMI). Differential signal swings are defined in later sections and depend on several factors: such as transmitter pre-equalization, receiver equalization and transmission line losses.

13.2.3 Signal Definitions

Each signal path, or CEI lane, is a point-to-point connection made up of two complementary signals making a balanced differential pair. This specification allows for bi-directional applications with multiple lanes in each direction.

13.2.4 Bit Error Ratio

See 3.2.3.

13.2.5 Ground Differences

The maximum ground difference between the host and module shall be ±50 mV. This will affect the absolute maximum voltages at the compliance points.

13.3 Electrical Characteristics

Hosts and modules shall meet the appropriate specifications defined in Table 13-1, Table 13-2, Table 13-4, and Table 13-5. Note that the direction of a given lane (host-to-module or module-to-host) will determine which of the listed tables give applicable specifications.

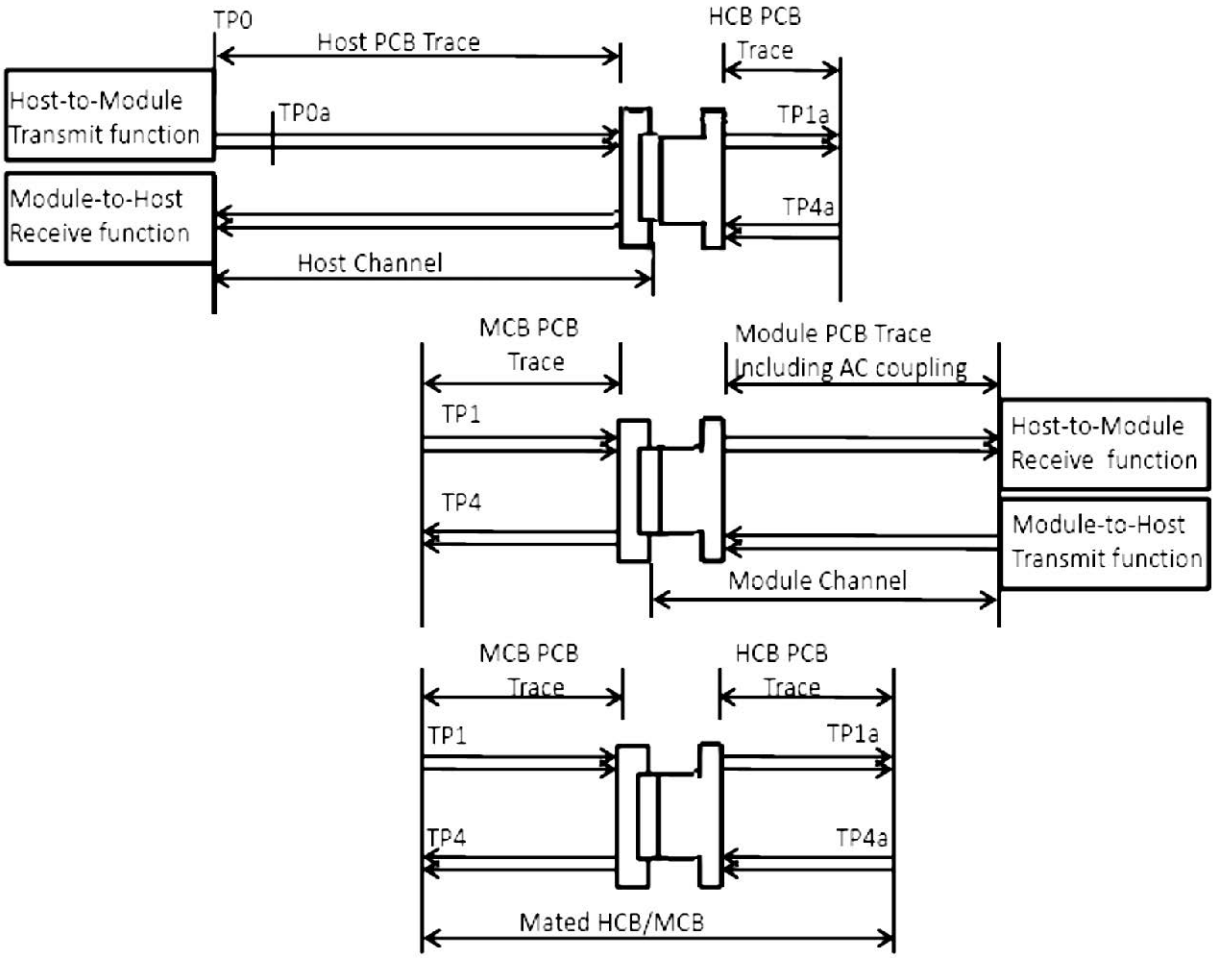
13.3.1 Compliance Point Specifications

Figure 13-1 below gives the reference model and test points associated with host-to-module and module-to-host lanes.

Reference test fixtures, called compliance boards, are used to access the electrical specification parameters. The output of the Host Compliance Board (HCB) provides access to the host-to-module electrical signal (host electrical output) defined at TP1a. Additional module electrical input specifications, for host-to-module communication, are defined at TP1, the input of the Module Compliance Board (MCB). The output of the Module Compliance Board (MCB) provides access to the module to host electrical signal (module electrical output) defined at TP4. Additional host electrical input

specifications, for module-to-host communication, are defined at TP4a, the input of the Host Compliance Board (HCB). Informative specifications for the host transmit function (TP0a) are given in Appendix 13.B.

Figure 13-1. Measurement points using compliance boards



13.3.2 Host-to-Module Electrical Specifications

Each host-to-module lane shall meet the specifications of Table 13-1 and Table 13-2. Definitions and methodologies can be found in Sections 13.3.4 to 13.3.11. The host shall provide a recommended CTLE peaking value selected from Table 13-8 such that the requirements defined in Section 13.3.11.1 are met. The method of providing this is outside the scope of this document.

Table 13-1. Host-to-Module Electrical Specifications at TP1a (host output)

Parameter		Min.	Max.	Units	Conditions
Differential Voltage pk-pk		-	900	mV	
Common Mode Noise RMS		-	17.5	mV	See Section 13.3.5
Differential Termination Resistance Mismatch		-	10	%	At 1 MHz See Section 13.3.6
Differential Return Loss (SDD22)		-	See Equation (13-2)	dB	
Common Mode to Differential Conversion (SDC22)		-	See Equation (13-4)	dB	
Common Mode Return Loss (SCC22)		-	-2	dB	From 250 MHz to 30 GHz
Transition Time, 20 to 80%		10	-	ps	See Section 13.3.10
Common Mode Voltage		-0.3	2.8	V	Referred to host ground
Eye Width at 10^{-15} probability (EW15) Note 1		0.46	-	UI	See Section 13.3.11
Eye Height at 10^{-15} probability (EH15) Note 1	Limit 1	95	-	mV	See Section 13.3.11
	Limit 2	80	-	mV	

NOTES:
1. Open eye is generated through the use of a reference Continuous Time Linear Equalizer (CTLE)

Table 13-2. Host-to-Module Electrical Specifications (module input)

Parameter	Test Point	Min.	Max.	Units	Conditions
Overload Differential Voltage pk-pk	TP1a	900	-	mV	See Section 13.3.12
Common Mode Voltage (Vcm) Note 1	TP1	-350	2850	mV	
Differential Termination Resistance Mismatch	TP1	-	10	%	At 1 MHz See Section 13.3.6
Differential Return Loss (SDD11)	TP1	-	See Equation (13-2)	dB	
Differential to Common Mode Conversion (SCD11)	TP1	-	See Equation (13-3)	dB	
Stressed Input Test	TP1a	See Section 13.3.11.2.1	-		See Section 13.3.12

NOTES:
1. Vcm is generated by the host. Specification includes effects of ground offset voltage.

Table 13-3. Crosstalk parameters for host output test and module stressed input test calibration at TP4

Parameter	Target value	Units
Crosstalk Amplitude Differential Voltage pk-pk	900	mV
Crosstalk Transition Time, 20 to 80%	9.5	ps

13.3.3 Module-to-Host Electrical Specifications

Table 13-4. Module-to-Host Electrical Specifications at TP4 (module output)

Parameter	Min.	Max.	Units	Conditions
Differential Voltage, pk-pk	-	900	mV	
Common Mode Voltage (Vcm) Note 1	-350	2850	mV	
Common Mode Noise, RMS	-	17.5	mV	See Section 13.3.5
Differential Termination Resistance Mismatch	-	10	%	At 1 MHz
Differential Return Loss (SDD22)	-	See Equation (13-2)	dB	
Common Mode to Differential Conversion (SDC22)	-	See Equation (13-4)	dB	
Common Mode Return Loss (SCC22)	-	-2	dB	From 250 MHz to 30 GHz
Transition Time, 20 to 80%	9.5	-	ps	See Section 13.3.10
Vertical Eye Closure (VEC)	-	5.5	dB	See Section 13.3.11.1.1
Eye Width at 10^{-15} probability (EW15)	0.57	-	UI	See Section 13.3.11
Eye Height at 10^{-15} probability (EH15)	228	-	mV	See Section 13.3.11

NOTES:
1. Vcm is generated by the host. Specification includes effects of ground offset voltage.

Table 13-5. Module-to-Host Electrical Specifications (host input)

Parameter	Test Point	Min.	Max.	Units	Conditions
Overload Differential Voltage pk-pk	TP4	900	-	mV	See Section 13.3.12
Differential Termination Resistance Mismatch	TP4a	-	10	%	
Differential Return Loss (SDD11)	TP4a	-	See Equation (13-2)	dB	
Differential to Common Mode Conversion (SCD11)	TP4a	-	See Equation (13-3)	dB	
Stressed Input Test	TP4	See Section 13.3.11.2.1	-		See Section 13.3.12
Common Mode Voltage Note 1	TP4a	-0.3	2.8	V	

NOTES:
1. Referred to host ground. Common mode voltage is generated by host

Table 13-6. Crosstalk parameters for module output test and host stressed input test calibration at TP1a

Parameter	Target value	Units
Crosstalk Amplitude differential voltage pk-pk	900	mV
Crosstalk transition time 20% to 80%	10	ps

13.3.4 Output Differential Voltage, pk-pk

The differential voltage, pk-pk, (see Section 1.6.1 for definition of differential voltage pk-pk), including any transmit de-emphasis, shall meet the specifications given in Table 13-1 or Table 13-4 for the respective communication direction. DC referenced values are not defined for the module because AC coupling is required in the module for both Tx and Rx. The waveform is observed through a fourth-order Bessel-Thomson response with a bandwidth of 40 GHz using a PRBS31 pattern.

13.3.5 Common Mode Noise

See Section 12.3 with the exception that the minimum oscilloscope BW shall be 40 GHz.

13.3.6 Differential Termination Resistance Mismatch

Differential Termination Resistance Mismatch is the percentage difference in low frequency termination resistance with respect to ground of any two signals forming a differential pair. This parameter is used to specify the difference between the two resistances more tightly than each individual resistance for the purpose of minimizing common mode to differential mode conversion.

Differential Termination Resistance Mismatch may be measured by applying a low-frequency test signal (high enough to overcome the high-pass effects of the AC coupling capacitors) to both the positive, I_p, and negative, I_n, terminals. The measured differential impedance, Z_{diff}, and currents going into both (the positive, I_p, and negative, I_n) terminals of the input are used to calculate the Differential Termination Resistance Mismatch using Equation (13-1) below.

Figure 13-2. Host Differential Termination Resistance Mismatch measurement setup

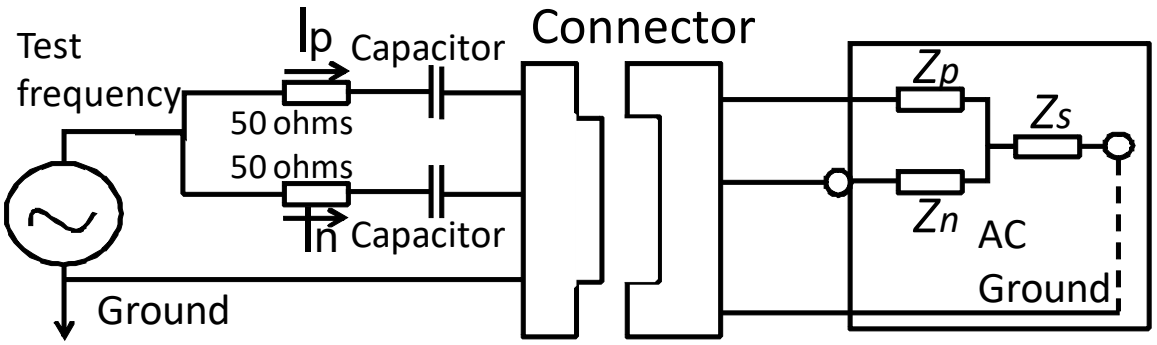
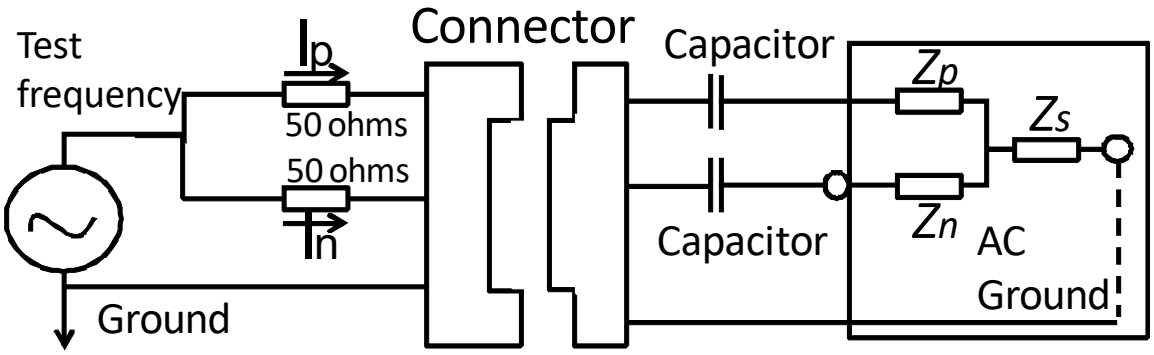


Figure 13-3. Module Differential Termination Resistance Mismatch measurement setup



$$\Delta Z_{mismatch} = 2 \times \frac{|(I_p - I_n)|}{|(I_p + I_n)|} \times \frac{Z_{diff} + 100}{Z_{diff}} \times 100\% \quad (13\text{-}1)$$

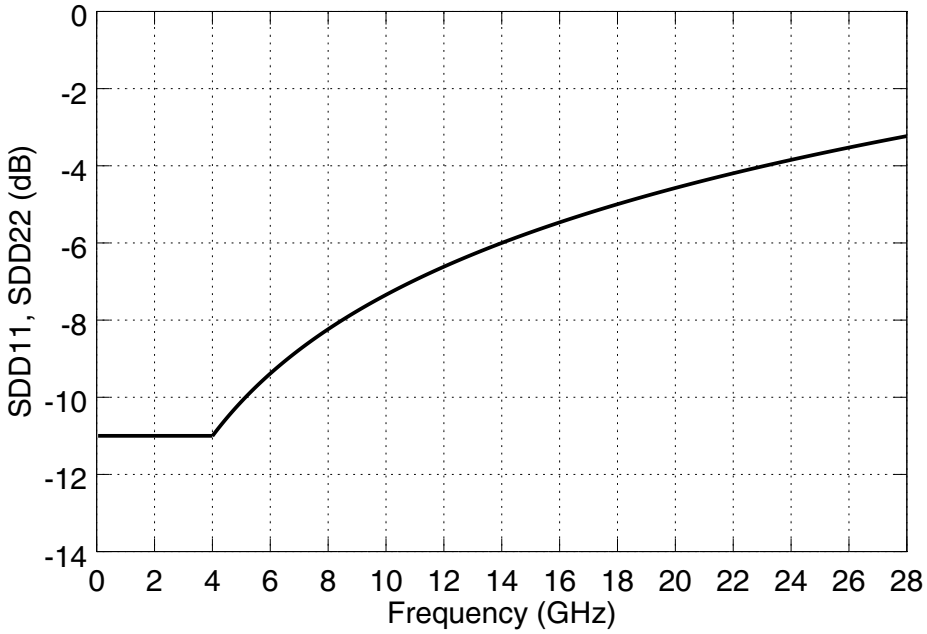
13.3.7 Differential Return Loss

When measured at the respective test point the differential return loss shall not exceed the limits given in Equation (13-2) (illustrated in Figure 13-4 for f_b=28 GHz).

The test points are TP1a for host output, TP4a for host input, TP1 for module input and TP4 for module output.

$$\begin{aligned} &SDD11, SDD22 < -11dB \quad \text{for } 0.05 \le f < f_b/7 \\ &SDD11, SDD22 < -6.0+9.2*\log_{10}\left(2\frac{f}{f_b}\right) dB \quad \text{for } f_b/7 \le f \le f_b \end{aligned} \quad (13\text{-}2)$$

Figure 13-4. SDD11, SDD22 for host output (TP1a), host input (TP4a), module input (TP1) and module output (TP4) (for f_b = 28 GHz)



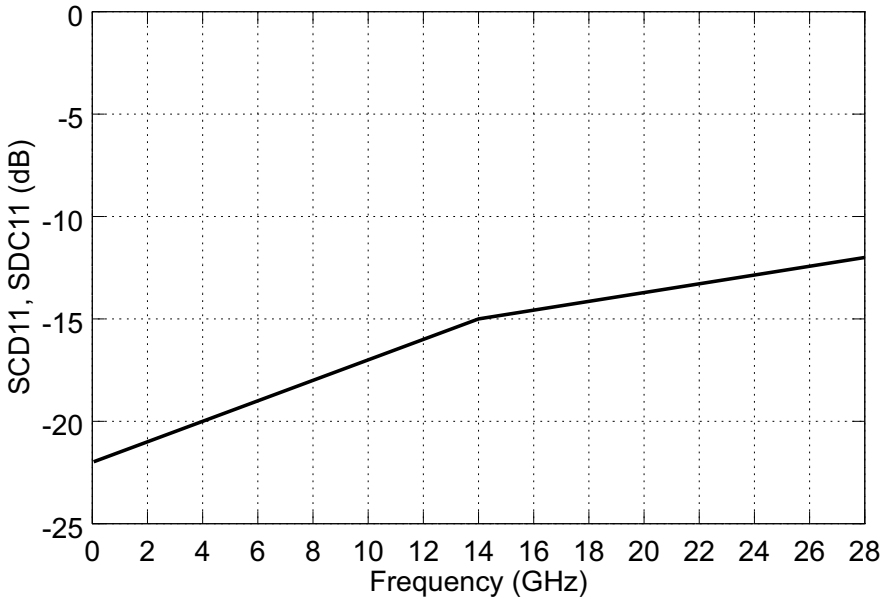
13.3.8 Common to differential mode and differential to common mode conversion

The common to differential mode and differential to common mode conversion specifications are intended to limit the amount of unwanted signal energy that is allowed to be generated due to conversion of common mode voltage to differential mode voltage or vice versa.

When measured at the respective input test point, common to differential mode or differential to common mode conversion shall not exceed the limits given in Equation (13-3) (illustrated in Figure 13-5 for f_b=28 GHz).

.

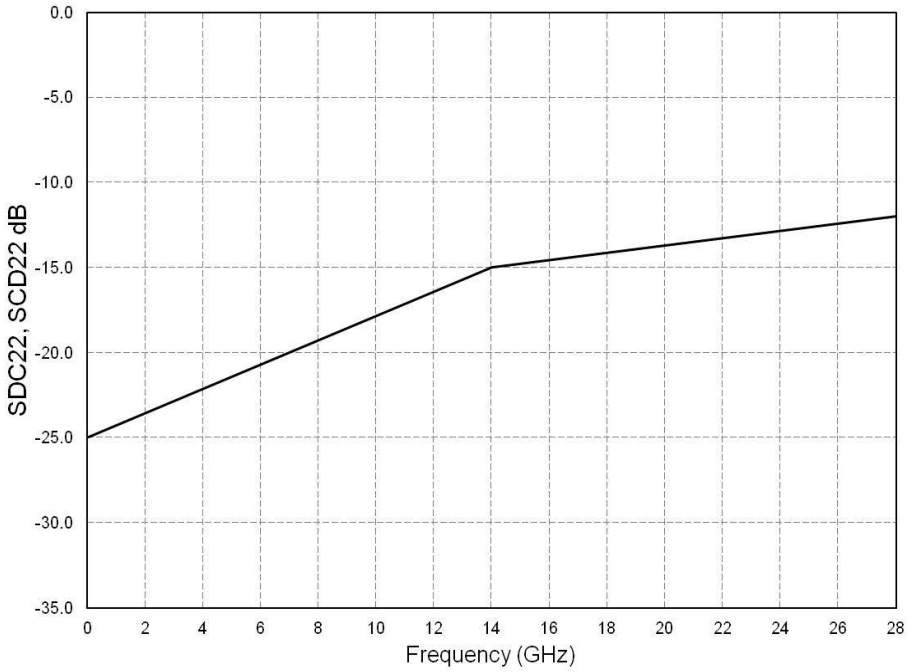
Figure 13-5. SDC11 and SCD11 for module input (TP1) and host input (TP4a) (for f_b = 28 GHz)



$$\text{SDC11, SCD11} < -22+14*(f/f_b)\text{dB} \quad \text{for} \quad 0.05 \le f < f_b/2$$
$$\text{SDC11, SCD11} < -18+6*(f/f_b)\text{dB} \quad \text{for} \quad f_b/2 \le f \le f_b \qquad (13\text{-}3)$$

When measured at the respective output test point, common to differential mode or differential to common mode conversion shall not exceed the limits given in Equation (13-4) (illustrated in Figure 13-6 for f_b=28 GHz).

Figure 13-6. SDC22 and SCD22 for module output (TP4) and host output (TP1a) (for f_b = 28 GHz)



$$\begin{aligned} &\text{SDC22, SCD22} < -25+20*(f/f_b)\text{dB} \quad \text{for} \quad 0.05 \le f < f_b/2 \\ &\text{SDC22, SCD22} < -18+6*(f/f_b)\text{dB} \quad \text{for} \quad f_b/2 \le f \le f_b \end{aligned} \tag{13-4}$$

13.3.9 Common Mode Return Loss

The common mode output return loss specification is intended to limit the amount of common mode energy that can be reflected by the host and module outputs. This has an effect on EMI radiation and differential mode signals generated via common mode to differential mode conversion. The common mode to differential mode conversion specification for the host and module outputs is more stringent than for the inputs to take into account the lack of a common mode input return loss specification.

13.3.10 Transition Time

Rise and fall time define the limits on the Transition Time. These limits are intended to bound crosstalk as well as near-end reflections due to channel return loss.

Transition times (rise and fall times) are defined as the time between the 20% and 80% times, or 80% and 20% times, respectively, of isolated edges.

If the test pattern is the square wave with eight ones and eight zeros, the 0% level and the 100% level are the average values of the center 20% of the two time intervals of the square wave.

If the test pattern is PRBS9 the pattern is generated by the polynomial $x^9 + x^5 + 1$ as specified in ITU-T O.150. The binary (0,1) data sequence d(n) is given by:
d(n) = d(n - 9) + d(n – 5), modulo 2.
The transitions within sequences of five zeros and four ones, and nine ones and five zeros, respectively, are measured. These are bits 10 to 18 and 1 to 14, respectively, where bits 1 to 9 are the run of nine ones. In this case, the 0% level and the 100% level may be estimated by the average signal within windows from –3 UI to –2 UI and from 2 UI to 3 UI relative to the edge.

The waveform is observed through a fourth-order Bessel-Thomson response with a bandwidth of 40 GHz.

NOTE—This definition is not the same as the rise and fall times typically reported by an oscilloscope from an eye diagram, which take all the edges into account.

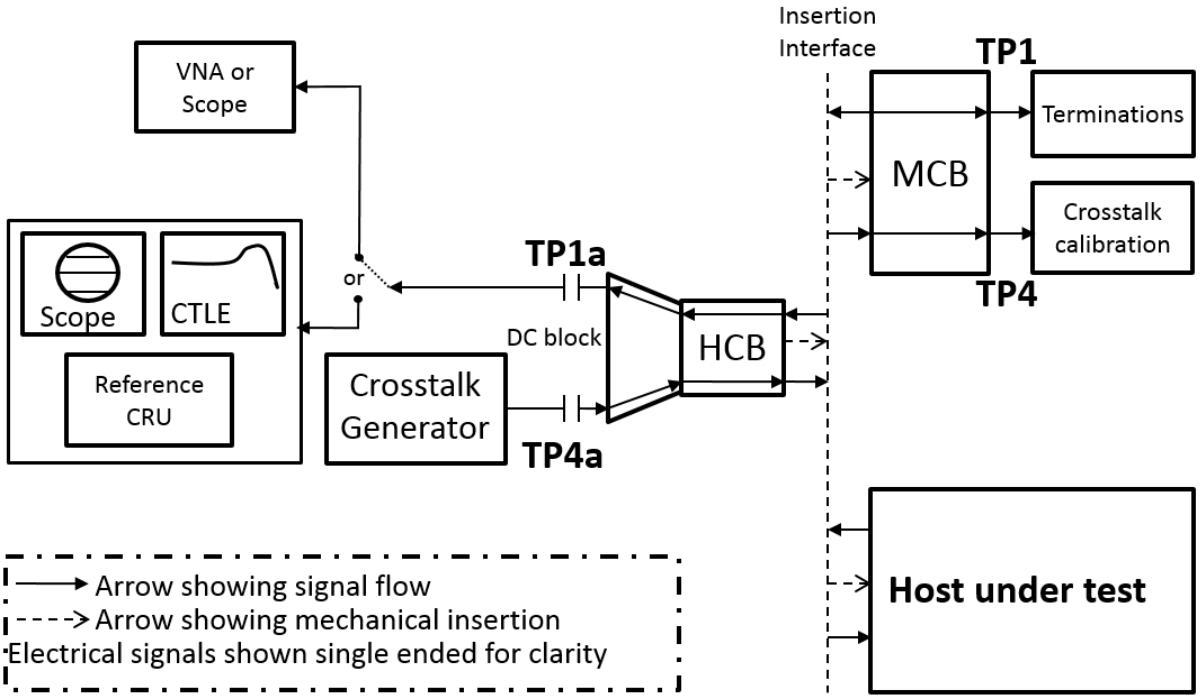
13.3.11 Eye Width, Eye Height and Stressed Input tests

Eye Width and Eye Height are specified in Table 13-1 (host output) and Table 13-4 (module output). Compliance is verified using the test setup shown in Figure 13-7 (host) and Figure 13-8 (module). The Eye Width and Eye Height correspond to eye contours at a probability of 10^{-15} to be consistent with those generated by simulator and oscilloscopes based on CDF/histogram data. Compliance to the input specifications defined in Table 13-2 and Table 13-5 is verified using the test setup shown in Figure 13-10 (host) and Figure 13-11 (module).

13.3.11.1 Host and Module output Eye Width and Eye Height test

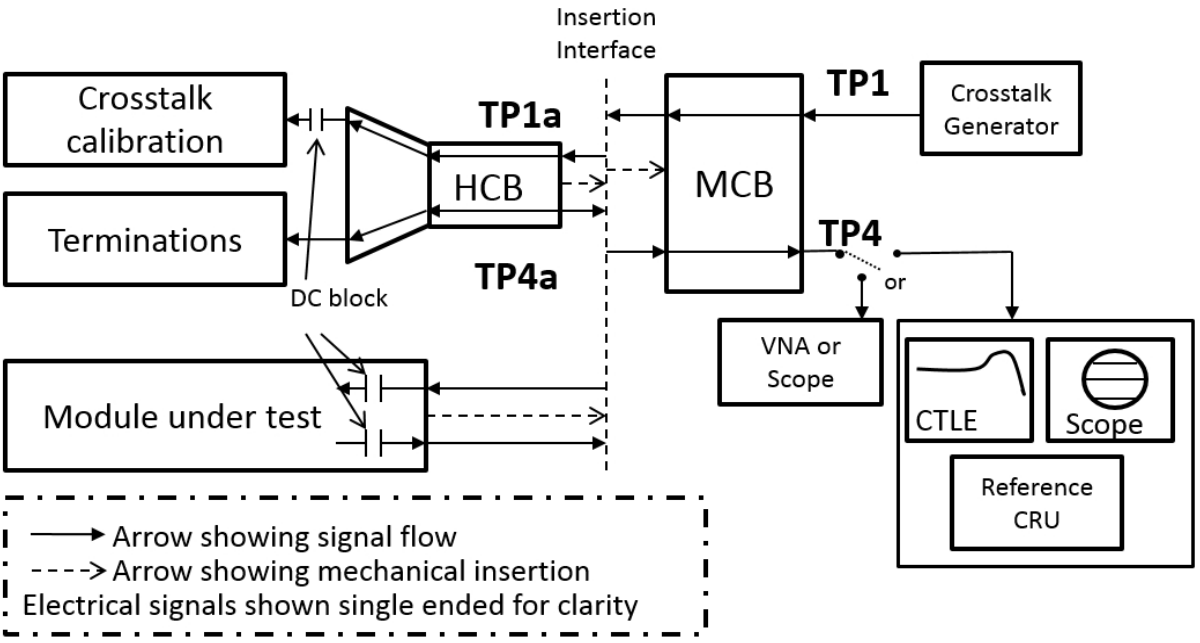
The host output Eye Width and Eye Height are measured at TP1a of Figure 13-1 using a Host Compliance Board as defined in Section 13.4.1. The test setup is shown in Figure 13-7.

Figure 13-7. Host output test setup



The module output Eye Width and Eye Height is tested at TP4 of Figure 13-1 using a Module Compliance Board as defined in Section 13.4.1. The test setup is shown in Figure 13-8.

Figure 13-8. Module output test setup



13.3.11.1.1 Host and Module output test method

The signal at TP1a may be a closed eye. Therefore, a reference receiver with a continuous time linear equalizer (CTLE) (see Section 13.3.11.3) is used to measure Eye Width and Eye Height. Although the signal at TP4 is an open eye, the reference receiver is also used to equalize the module output signal without the use of transmit equalization. The measured signal after the reference receiver shall meet the specifications listed in Section 13.3.2 for host to module and Section 13.3.3 for module to host. All co-propagating and counter-propagating lanes are active as crosstalk sources, using a PRBS31 test pattern or a valid CEI signal. Amplitude and Transition Times for counter-propagating lanes are defined in Table 13-3 and Table 13-6. The lanes under test are asynchronous to the lanes in the opposing direction within the PPM offset defined by the protocol in use.

The test method for measuring either host or module output Eye Width and Eye Height as illustrated in Figure 13-9 is as follows:

1) Set the host or module to PRBS9 pattern (see Section 13.3.10).

-This allows the use of a sampling oscilloscope with a pattern lock.

2) Capture the input signal at TP1a or TP4 with a scope triggered with a clock from a reference clock recovery unit (CRU) with a first order transfer function with a 3 dB tracking bandwidth of $f_b/2578$.

-For TP1a, the scope shall be AC coupled.

-The reference CRU can be a software CRU in case of a real time scope.

-Sample the signal with a minimum sampling rate of 3 (equally spaced) samples per bit. Collect sufficient samples equivalent to 4 million bits in order to construct normalized cumulative distribution functions (normalized CDFs) (see Figure 13-9) of the post-processed captured signals to a probability of 10^{-6} (without extrapolation) as described below. Depending on the sampling rate, careful interpolation using a method such as sin(x)/x or cubic spline may be needed for good accuracy.

3) Apply the reference receiver as defined in Section 13.3.11.3 to equalize the captured signal in step 2.

-For TP4 compliance test, the CTLE peaking in the reference receiver shall be set at either 1 dB or 2 dB. Any CTLE setting that meets both the EH15 and EW15 settings defined for TP4 in Table 13-4 is acceptable.

-For TP1a compliance test, the CTLE peaking in the reference receiver shall be set at two or three values. These are: a) the recommended CTLE peaking value provided by the host, b) the value 1 dB higher if present in Table 13-8 and c) the value 1 dB lower if present in Table 13-8. The two or three results are used in step 9 to determine compliance.

4) Use the differential equalized signal from step 3 to construct CDFs of the jitter at zero crossing, for both the left edge (CDFL) and the right edge (CDFR) of the eye, as a distance in time from the middle of the eye.

-The middle of the eye is defined to be UI/2 away from the mean zero crossing points of the equalized signal from step 3.

Calculate the Eye Width (EW6, see Figure 13-9) as the difference in time between CDFR and CDFL with a value of 10^{-6}. CDFL and CDFR are calculated as the cumulative sum of histograms of the zero crossing samples at the left and right edges of the eye normalized by the total number of sampled bits (e.g., the number of sampled bits is 4 million as specified in step 2). For a pattern with 50% transition density the maximum value for the CDFL and CDFR will be 0.5. CDFL and CDFR are equivalent to bathtub curves where the bit error ratio (BER) is plotted versus sampling time.

5) Apply Dual-Dirac and tail fitting technique (See Agilent white paper: 5989-3206EN) separately to CDFL and CDFR to estimate random jitter. Calculate the best linear fit in Q-scale over the range of probabilities of 10^{-4} to 10^{-6} of the CDFL and CDFR to yield RJL and RJR respectively.

-RJL is the RMS value of the jitter estimated from CDFL.

-RJR is the RMS value of the jitter estimated from CDFR.

-Eye Width (EW15) at 10^{-15} probability is equal to (EW6-3.19*(RJL+RJR)).

6) Use the differential equalized signal from step 3 to construct the CDFs of the signal voltage in the central 5% of the horizontal eye, for both logic one (CDF1) and logic zero (CDF0), as a distance in voltage from the zero crossing.

Calculate the Eye Height (EH6, see Figure 13-9) as the difference in voltage between CDF1 and CDF0 with a value of 10^{-6}. CDF0 and CDF1 are calculated as the cumulative sum of histograms of the voltage samples at the top and bottom of the eye normalized by the total number of sampled bits (e.g., the number of sampled bits is 4 million as specified in step 2). For a pattern with a well balanced number of ones and zeros the maximum value for CDF0 and CDF1 will be 0.5.

7) Apply dual-Dirac and tail fitting techniques to CDF1 and CDF0 to estimate noise in the central 5% of the eye. Calculate the best linear fit in Q-scale over the range of probabilities of 10^{-4} to 10^{-6} of the CDF1 and CDF0 to yield RN1 and RN0 respectively.

-RN1 is the RMS value of the noise estimated above from CDF1.

-RN0 is the RMS value of the noise estimated above from CDF0.

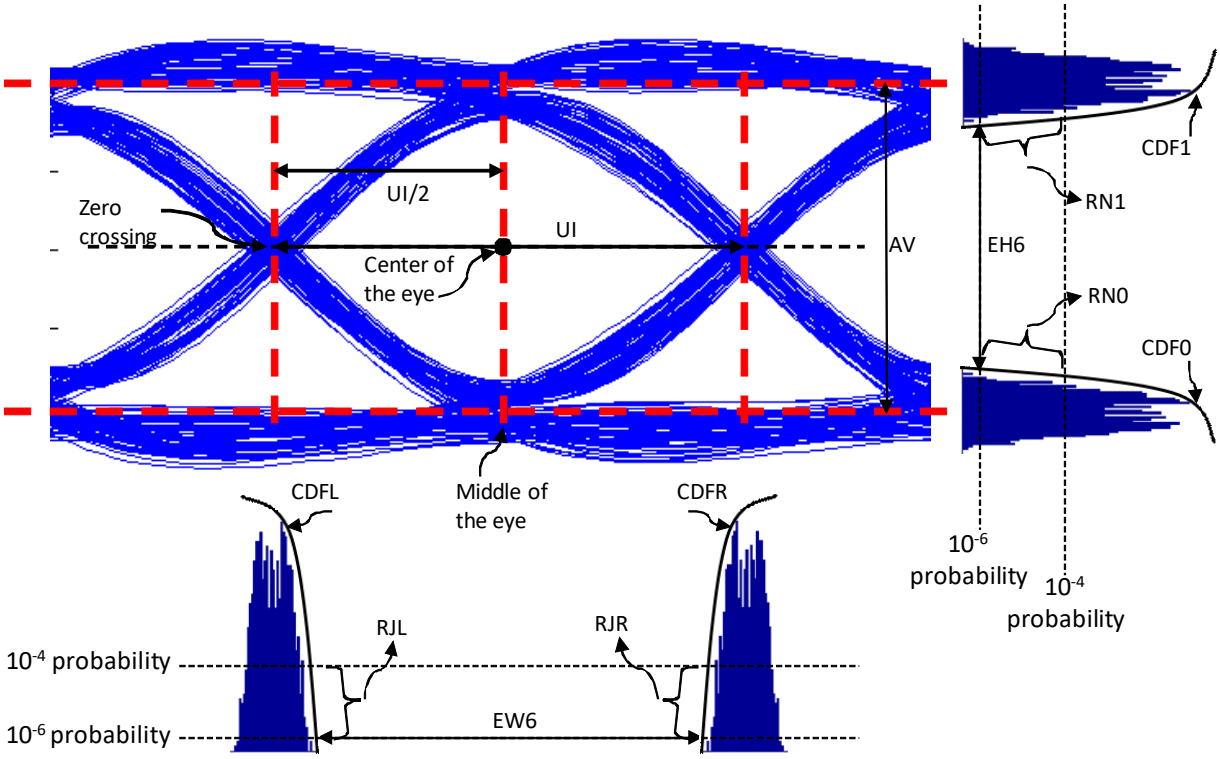
-Eye Height (EH15) at 10^{-15} probability equals (EH6-3.19*(RN0+RN1)).

8) At TP4 calculate vertical eye closure (VEC) as $20*\log_{10}$ (AV/EH15):

- AV is the Eye Amplitude of the equalized waveform. Eye Amplitude is defined as the mean value of logic one minus the mean value of logic zero in the central 5% of the eye.

9) At TP1a, passing is defined as passing both the EW15 and EH15 Limit 1 specified in Table 13-1 for at least one of the equalizer settings, and passing EH15 Limit 2 specified in Table 13-1 at all of the two or three settings. At TP4, passing is defined as a single equalizer setting that meets the EH15, EW15 and VEC specifications given in Table 13-4.

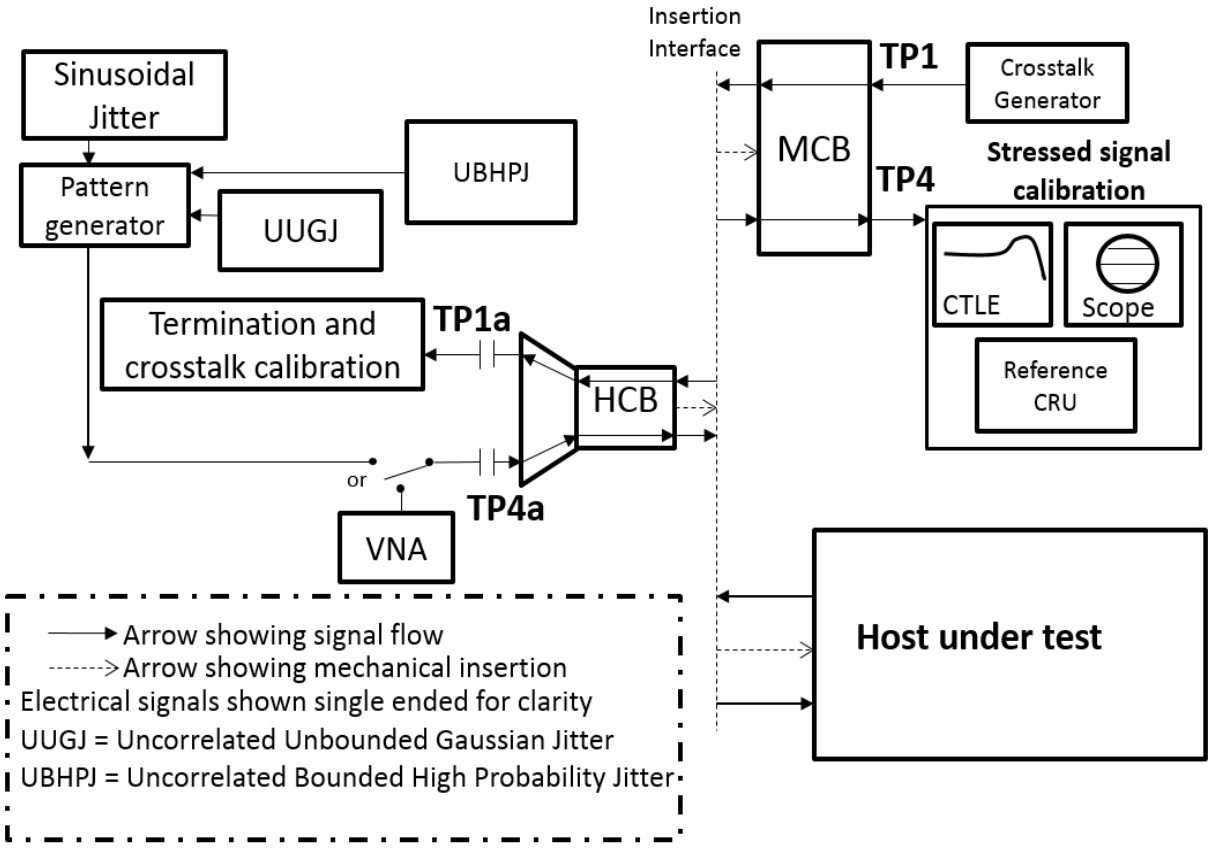
Figure 13-9. TP1a and TP4 jitter and Eye Height parameters



13.3.11.2 Host and Module stressed input test

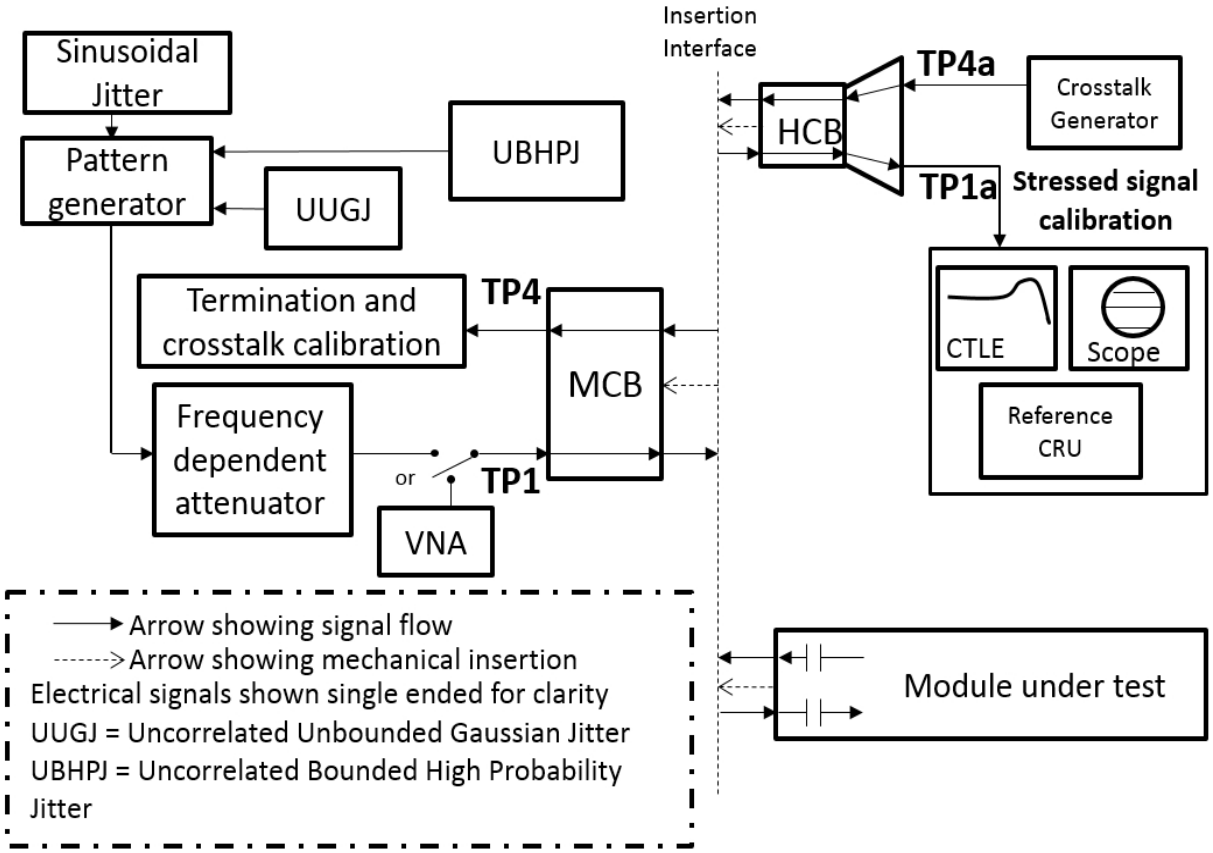
The ability of the host input to tolerate the Eye Width and Eye Height specified in Table 13-4 and the sinusoidal jitter specified in Table 13-7 is tested using a stressed input test. The test signal is applied at TP4a of Figure 13-1, and calibrated at TP4, using a Host Compliance Board and Module Compliance Board specified in Section 13.4.1 The test setup is shown in Figure 13-10. The UBHPJ block is used to create non-compensable DJ in addition to sinusoidal jitter.

Figure 13-10. Host input test setup



The ability of the module input to tolerate the Eye Width and Eye Height specified in Table 13-1 and the sinusoidal jitter specified in Table 13-7 is tested using a stressed input test. The test signal is applied at TP1 of Figure 13-1, and calibrated at TP1a using a Host Compliance Board and Module Compliance Board specified in Section 13.4.1. The test setup is shown in Figure 13-11. The module stressed input test represents the worst case high loss VSR channel. It should be noted that modules are also expected to operate at the BER specified in Section 3.2.3 when presented with lower loss channels that require different CTLE settings as long as the signal complies with the specifications in Table 13-1 and the recommended CTLE peaking value supplied by the host is within 1 dB of the optimal value for the signal (see Section 13.3.11.2.1).

Figure 13-11. Module stressed input test setup



13.3.11.2.1 Host (TP4a) and Module (TP1) stressed input test method

The host and module input shall tolerate a peak-to-peak sinusoidal jitter with the frequency and amplitude defined by the mask of Figure 13-12 and Table 13-7. This sinusoidal jitter shall be part of the jitter applied in the stressed input test.

The reference CRU and reference receiver as defined in Section 13.3.11.3 are used to calibrate the stressed input test signal at TP4 (per Table 13-4) or TP1a (per Table 13-1) using a PRBS9 pattern. The pattern is changed to PRBS31 for the stressed input test.

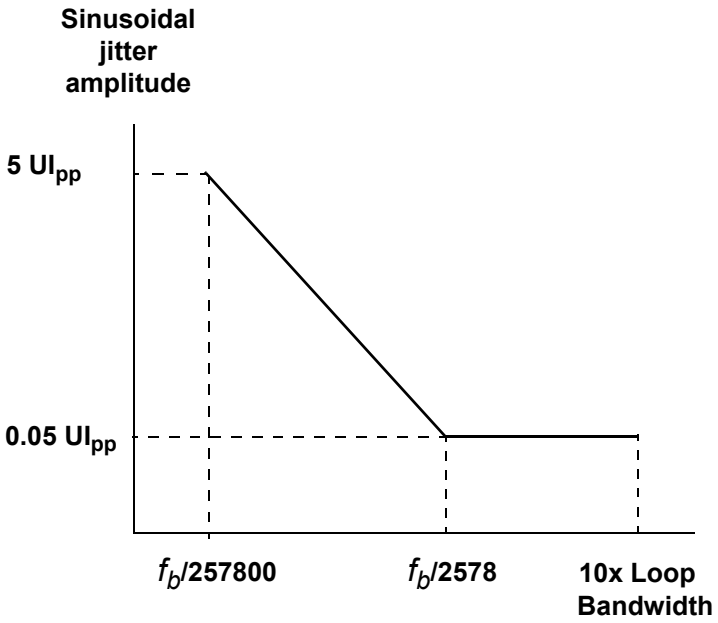
The crosstalk source is asynchronous to the main pattern generator. The amplitude and rise/fall time of the crosstalk source are given in Table 13-3 and Table 13-6. The crosstalk signal is to be calibrated at TP4 or TP1a using a PRBS9 pattern, then changing the pattern to PRBS31 for the test. For multi-lane implementations additional lanes shall be active with an asynchronous PRBS31 pattern using the above calibration methods.

The host under test shall meet the BER specified in Section 3.2.3. The module under test shall meet the BER specified in Section 3.2.3 when provided with each of three recommended CTLE values. These are: a) the optimal value found in Section 13.3.11.2.1.2, b) the value 1 dB higher if present in Table 13-8 and c) the value 1 dB lower if present in Table 13-8. (e.g. If the optimal value found in Section 13.3.11.2.1.2 is 9 dB then the module must meet the specified BER in Section 3.2.3 when provided with recommended CTLE values of 8,9 and 10 dB).

Table 13-7. Sinusoidal jitter frequency for TP4 and TP1 testing

Frequency Range (Hz)	Sinusoidal jitter, Peak to peak (UI)
f<f_b/257800	*Not Specified*
f_b/257800 < f ≤ f_b/2578	*5*f_b/(257800*f)*
f_b/2578 < f ≤ 10xLB (Note 1)	*0.05*
NOTES: 1. LB = Receiver Loop Bandwidth	

Figure 13-12. Host input and Module input Sinusoidal Jitter



13.3.11.2.1.1 Host input test signal calibration

The host input is tested at TP4a of Figure 13-1 using a Host Compliance Board as defined in Section 13.4.1. The host input test setup is shown in Figure 13-10.

UBHPJ, UUGJ and sinusoidal jitter are added to a clean test pattern until the jitter (except for DCD) at the output of the pattern generator approximates the informative transmit specification (as defined in Appendix 13.B).

With the crosstalk generator calibrated to meet the specifications in Table 13-3, the Eye Height and Eye Width at TP4 are measured using the reference receiver defined in Section 13.3.11.3 with the optimal peaking value from Figure 13-14 and the methodology defined in Section 13.3.11.1. The optimal peaking value is defined as the setting that results in the maximum value of EW15*EH15.

The UUGJ and pattern generator amplitude are adjusted to give the minimum Eye Height and Eye Width specified for the module output in Table 13-4.

A host input test signal should have a VEC in the range of 4.5 to 5.5 dB with a target value of 5.0 dB.

13.3.11.2.1.2Module input test signal calibration

The module input is tested at TP1 of Figure 13-1 using a Module Compliance Board as defined in Section 13.4.1. The module input test setup is shown in Figure 13-11.

UBHPJ, UUGJ and sinusoidal jitter are added to a clean test pattern until the jitter (except for DCD) at the output of the pattern generator approximates the informative transmit specification (as defined in Appendix 13.B).

The frequency-dependent attenuator is intended to represent the host channel, and may be implemented with PCB traces. It should be adjusted to result in a loss of 10.25 dB at Nyquist from the output of the pattern generator to TP1a. The crosstalk generator is calibrated to meet the specifications in Table 13-3. The Eye Height and Eye Width at TP1a are measured using the reference receiver (defined in Section 13.3.11.3) with the optimal peaking value and the methodology defined in Section 13.3.11.1. The optimal peaking value is defined as the setting that results in the maximum value of EW15*EH15.

The UUGJ and pattern generator amplitude are adjusted to give the minimum Eye Height and Eye Width specified in Table 13-1.

13.3.11.3 Reference receiver

The waveform is observed through a fourth-order Bessel-Thomson response with a bandwidth of 40 GHz concatenated with a Continuous Time Linear Equalizer (CTLE). The filters may be implemented in software; however, the signal is not averaged. The CTLE shall be implemented based on Equation (13-5) where G is the gain and Z1, P1 and P2 are the CTLE zero and poles coefficients. Figure 13-13 shows the frequency response of the reference equalizer used for host output testing for baud rates between 25 and 28.1 Gsym/s with values for Z1, P1 and P2 listed in Table 13-8. Figure 13-14 shows the frequency response of the reference equalizer used for module output testing for baud rates between 25 and 28.1 Gsym/s with values for Z1, P1 and P2 listed in Table 13-8. Note that the peaking is centered at 14 GHz for all baud rates between

25 and 28.1 Gsym/s. For baud rates below 25 Gsym/s the values of Z1, P1 and P2 should be multiplied by f_b/28. Note that this results in peaking at f_b/2. Note that the peaking value approximates the difference between the low frequency gain (1 MHz) and the high frequency gain at Nyquist in dB.

$$H(s) = \frac{(G)(P1)(P2)}{Z1}\frac{(S+Z1)}{(S+P1)(S+P2)} \quad (13\text{-}5)$$

$$S = j2\pi f$$

Figure 13-13. Host output Reference receiver equalizer (CTLE) transfer function for gains of 1 dB to 9 dB

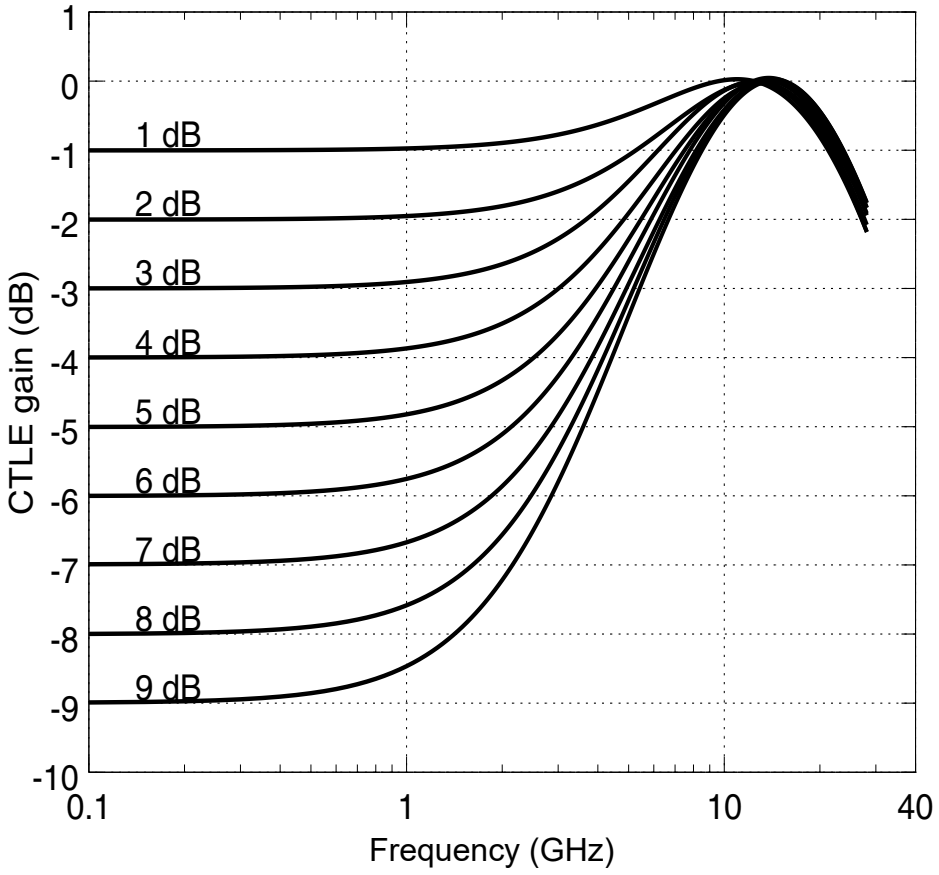


Figure 13-14. Module output Reference receiver equalizer (CTLE) transfer function for gains of 1 and 2 dB

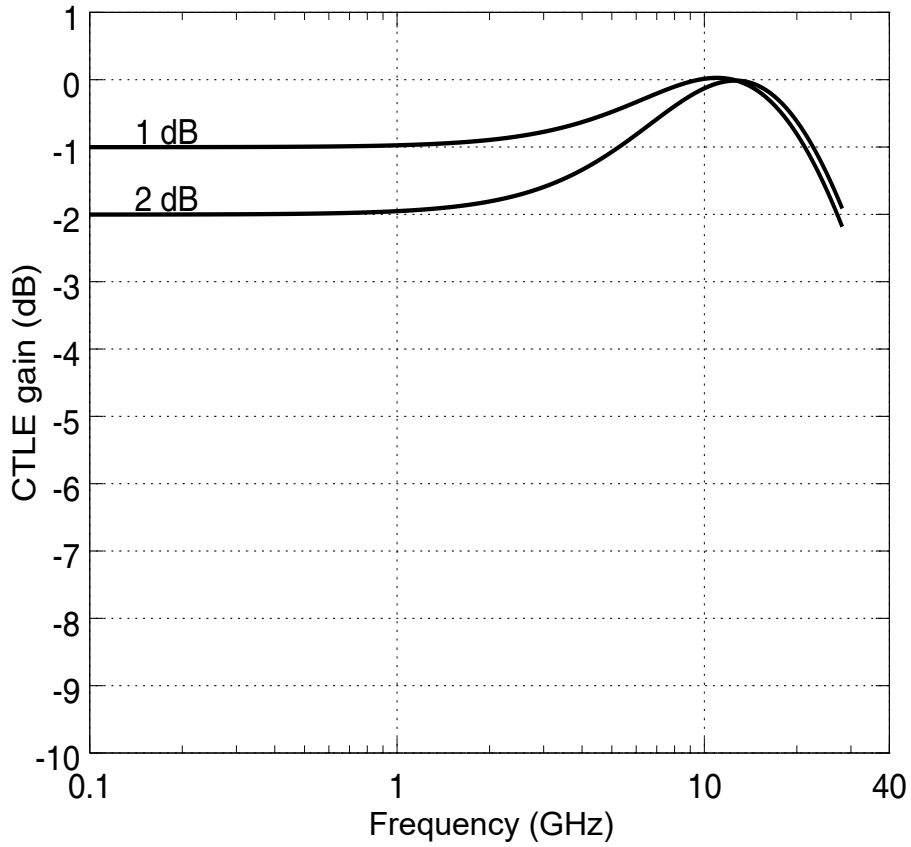


Table 13-8. Reference equalizer coefficients for rate of 28 Gsym/s.

Peaking (dB)	G	P1/2π (GHz)	P2/2π (GHz)	Z1/2π (GHz)
1	0.891	18.6	14.1	8.31
2	0.794	18.6	14.1	7.10
3	0.708	15.6	14.1	5.68
4	0.631	15.6	14.1	4.98
5	0.562	15.6	14.1	4.35
6	0.501	15.6	14.1	3.82
7	0.447	15.6	14.1	3.43
8	0.398	15.6	14.1	3.00
9	0.355	15.6	14.1	2.67

13.3.12 Input Differential Voltage Tolerance

The input voltage tolerance tests the acceptance of differential input pk-pk amplitudes produced by the extremes of operation from the transmitter (e.g. host output for host-to-module communication or module output for module-to-host communication).

The input voltage tolerance maximum value is produced by a compliant transmitter (per Table 13-1) connected with the minimum attenuation to the receiver. This may be larger than the maximum of the driver due to output/input impedances and reflections.

The input voltage tolerance value is defined by the minimum driver amplitude, the actual receiver input impedance, and the loss of the actual PCB. Note that the minimum driver amplitude is defined using a well controlled load impedance; however the real receiver is not, which can leave the receiver input signal smaller than expected. Additionally it will be determined by the environmental noise inside and outside the receiver.

13.4 Measurement methods

13.4.1 Compliance Boards

Use of compliance boards for testing is assumed for the parameters defined in Table 13-1 through Table 13-6. Figure 13-1 shows the test setup for making S-parameter measurements of the mated compliance boards. If compliance boards do not meet the specified S-parameters test results should be corrected for the difference. The requirements in this section are not connector specifications for an implemented design.

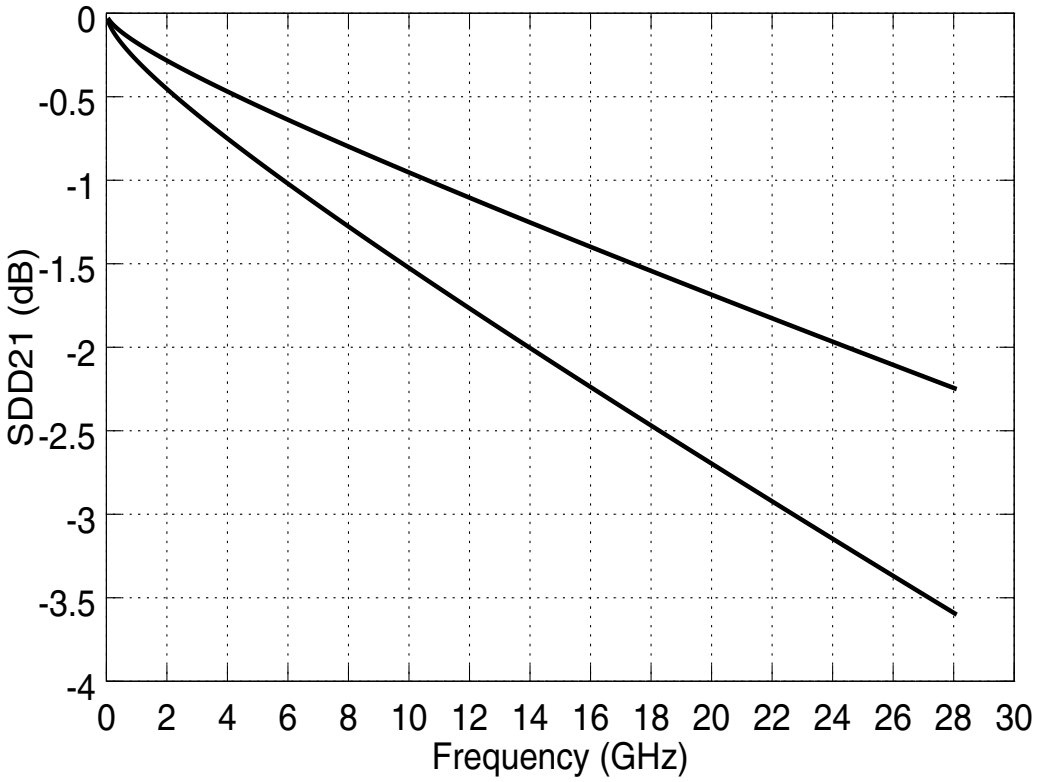
13.4.1.1 HCB and MCB insertion loss

The reference differential insertion loss of the HCB printed circuit board trace follows Equation (13-6) for 0.05 GHz ≤ f ≤ 28.1 GHz. The reference differential insertion loss of the MCB printed circuit board trace follows Equation (13-7) for 0.05 GHz ≤ f ≤ 28.1 GHz. (f is measured in GHz) Both the HCB and MCB equations are illustrated in Figure 13-15, below.

$$\text{HCB SDD21} = 2.00(0.001 - 0.096(\sqrt{f}) - 0.046(f)) \text{ dB} \quad (13\text{-}6)$$

$$\text{MCB SDD21} = (1.25)(0.001 - 0.096\sqrt{f} - 0.046(f))\text{dB} \quad (13\text{-}7)$$

Figure 13-15. Reference SDD21 of HCB and MCB printed circuit board traces



13.4.1.2 Mated HCB and MCB S-parameters

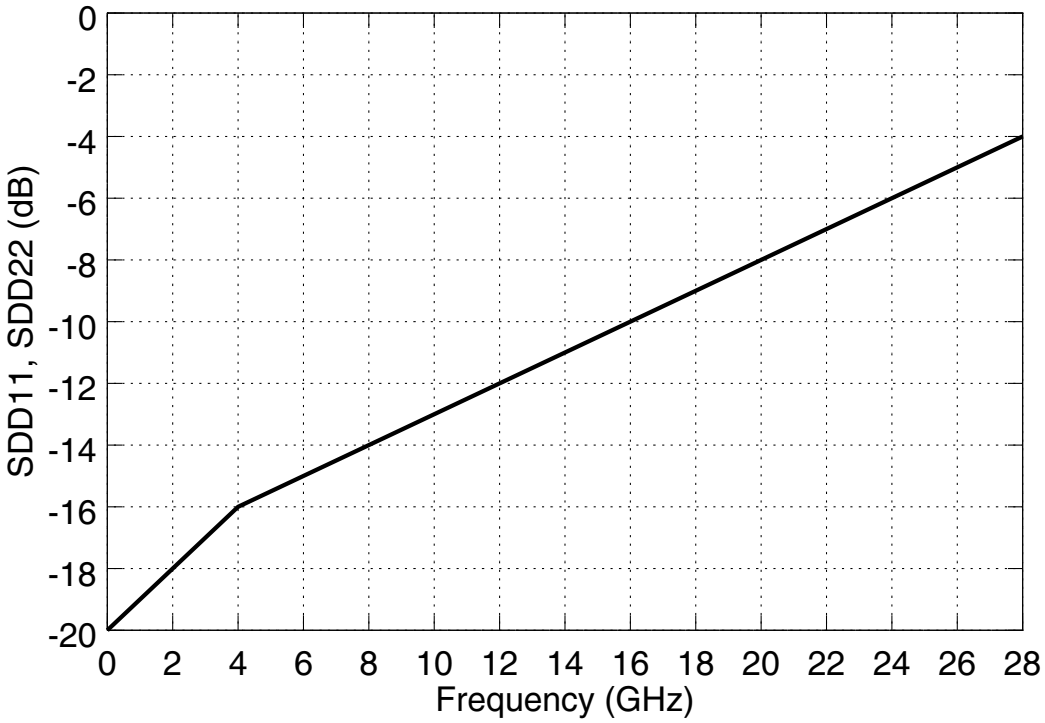
The specifications given for the mated HCB and MCB shall be verified in both directions (exception being differential insertion loss can be in either direction).

The differential return loss of the mated HCB and MCB pair shall follow Equation (13-8), illustrated in Figure 13-16.

Mated HCB-MCB SDD11, SDD22 ≤ -20 + f dB for f < 4 GHz (13-8)

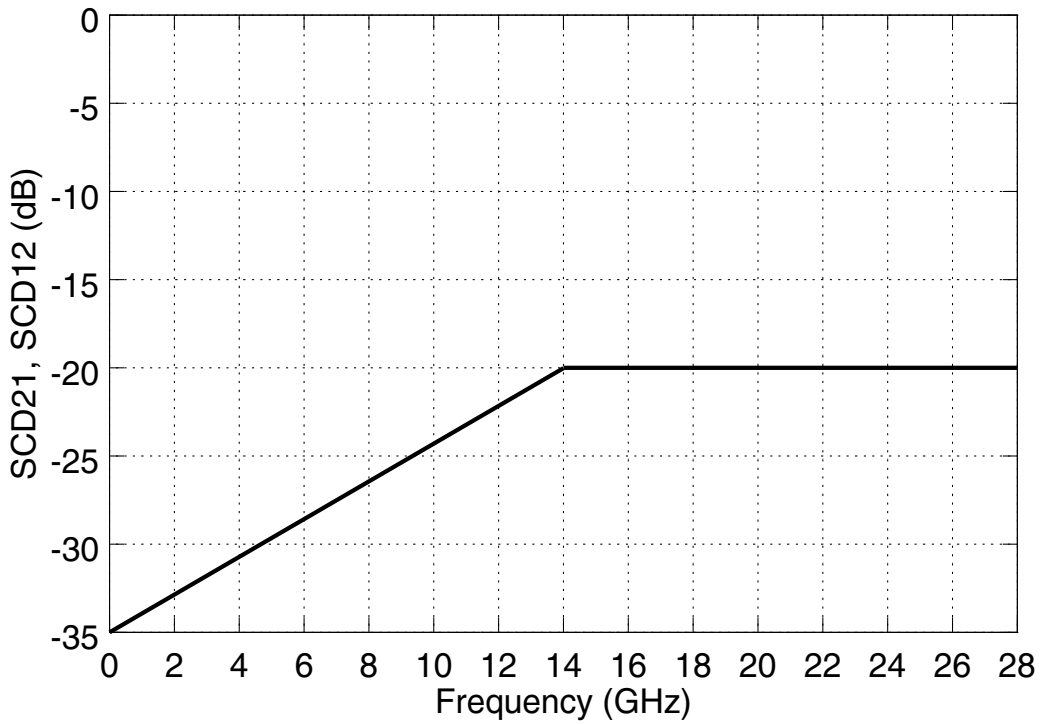
Mated HCB-MCB SDD11, SDD22 = -18 + f/2 dB for 4 GHz ≤ f ≤ 28.1 GHz

Figure 13-16. Mated HCB-MCB SDD11, SDD22



The differential to common mode conversion for a mated HCB and MCB pair is given in Equation (13-9) and shown in Figure 13-17, below.

Figure 13-17. Mated HCB-MCB SCD21, SCD12



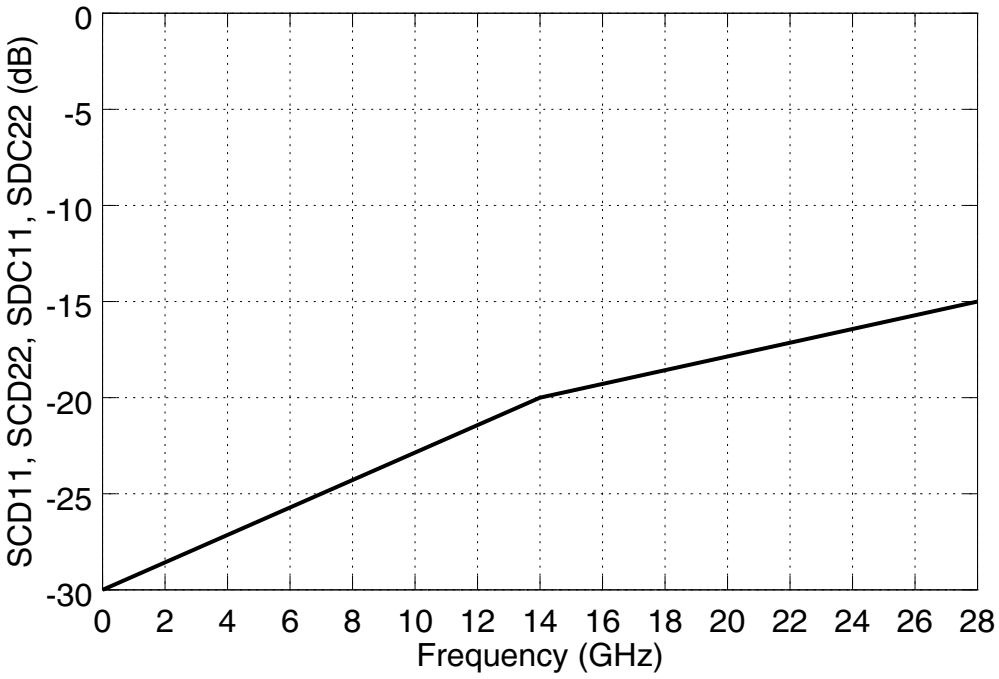
$$\text{Mated HCB-MCB SCD21, SCD12} \le -35 + 1.07\,f \text{ dB} \quad \text{for } f < 14 \text{ GHz}$$

$$\text{Mated HCB-MCB SCD21, SCD12} \le -20 \text{dB} \quad \text{for } 14\text{GHz} \le f \le 28.1 \text{ GHz}$$

(13-9)

The differential to common mode return loss for a mated HCB and MCB pair is given in Equation (13-10) and shown in Figure 13-18, below.

Figure 13-18. Mated HCB-MCB SCD11, SCD22, SDC11, SDC22



$$\text{HCB-MCB SCD11, SCD22 and SDC11, SDC22} \le -30+(5/7)f \text{ dB} \quad \text{for } f < 14 \text{ GHz} \qquad (13\text{-}10)$$

$$\text{HCB-MCB SCD11, SCD22 and SDC11, SDC22} \le -25 + \frac{5}{14} f \text{ dB} \quad \text{for } 14\text{GHz} \le f \le 28.1 \text{ GHz}$$

The maximum common mode return loss for a mated HCB and MCB pair shall be 3dB.

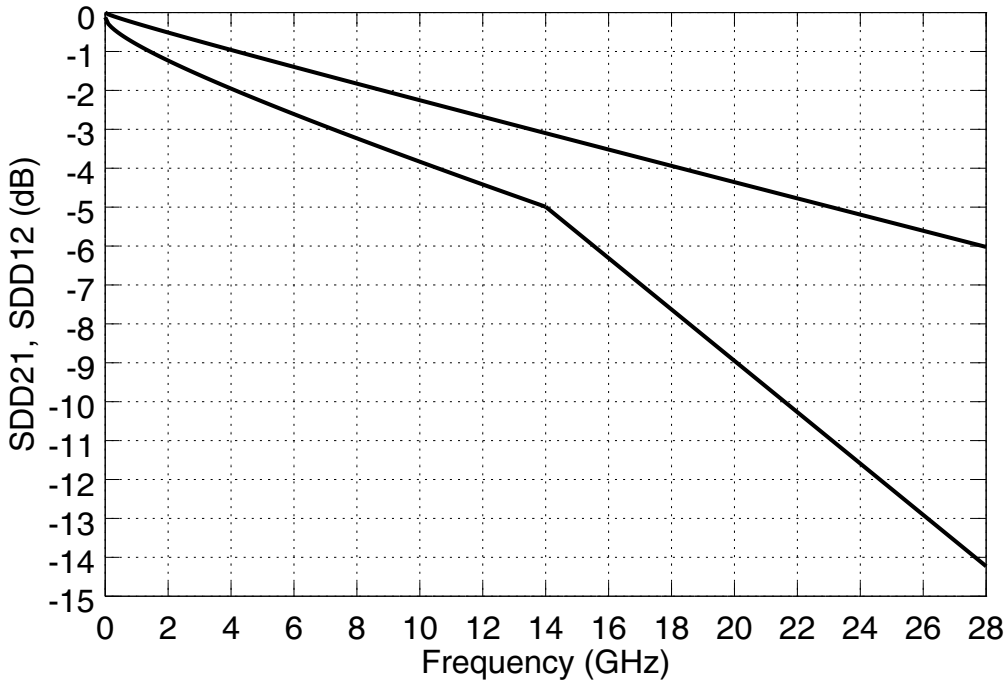
The maximum differential insertion loss for a mated HCB and MCB pair is given in Equation (13-11). The minimum differential insertion loss for a mated HCB and MCB is given in Equation (13-12). Both equations are shown in Figure 13-19, below.

Mated HCB-MCB SDD21, SDD12 > -0.12 - 0.475 $\sqrt{f}$ - 0.221 * f dB for f < 14 GHz (13-11)

Mated HCB-MCB SDD21, SDD12 > 4.25 - 0.66 * f dB for 14 GHz ≤ f ≤ 28.1 GHz

Mated HCB-MCB SDD21, SDD12 < -0.08 $\sqrt{f}$ - 0.2 * f dB for f ≤ 28.1 GHz (13-12)

Figure 13-19. Mated HCB-MCB SDD21, SDD12



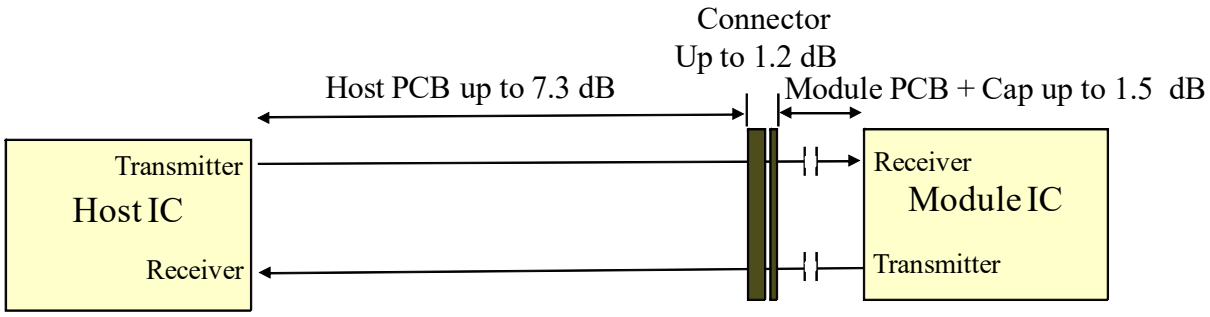
The FOM_{ILD} (as calculated using the method defined in Section 10.2.6.4 and the curve fit method defined in Chapter 12 with f_{ILmax} of 21 GHz and f_{ILmin} of 50 MHz) for the mated HCB and MCB pair is $\leq$ 0.1 dB.

The Integrated Crosstalk Noise (ICN) as calculated using the method defined in Chapter 12 with the aggressor amplitudes and rise/fall times as listed in Table 13-3 shall be less than 3.9 mV. MDNEXT shall be less than 1.35 mV RMS. MDFEXT shall be less than 3.6 mV RMS.

13.A Appendix - Recommended Electrical Channel

The channel consists of Host PCB trace, Module PCB trace, vias, AC coupling capacitor and one connector, not in this order. The recommended PCB trace differential impedance is 100 ± 10 Ω. This full channel model is shown in Figure 13-20 below. Note that in practice the channel is not measurable as appropriate test points are not accessible.

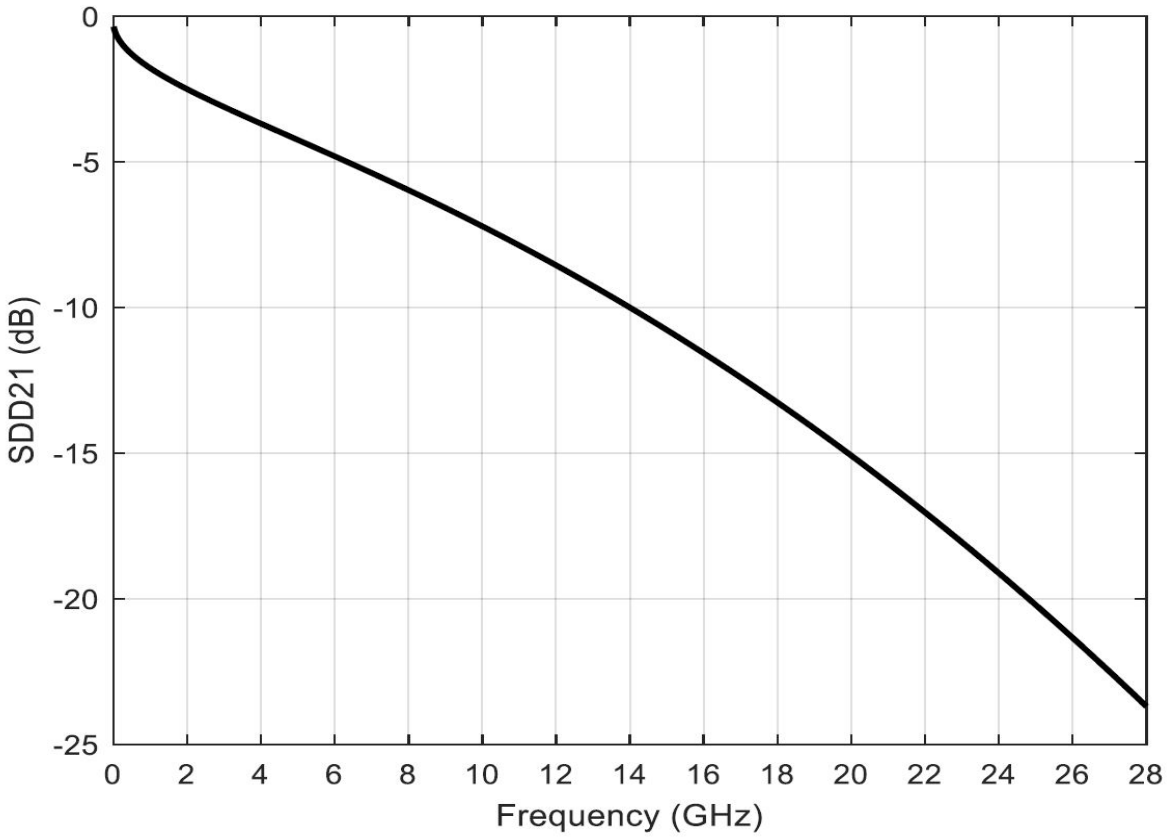
Figure 13-20. CEI-28G-VSR full Channel Reference Model



13.A.1 Insertion Loss

Host insertion loss and module insertion loss are recommended limits only. Achieving these recommended limits does not signify compliance nor guarantee successful communication between two devices. Equation (13-13) (illustrated in Figure 13-21) represents the highest recommended insertion loss of the full channel.

Figure 13-21. Recommended minimum SDD21 of the VSR channel (for f_b = 28 GHz)



$$H(f) = -0.2 - 8.1\sqrt{\frac{f}{f_b}} - 0.895\frac{f}{f_b} - 14.5\left(\frac{f}{f_b}\right)^2 \quad (13\text{-}13)$$

13.B Appendix - Informative Host Transmitter output Electrical Characteristics

Informative host Tx output recommendations are defined in Table 13-9.

13.B.1 Host Transmitter output specification point

Figure 13-1 gives the reference model and test points associated with host-to-module and module-to-host CEI-28G-VSR lanes. The informative host transmitter output electrical characteristics are defined to be measured at TP0a. TP0a is defined to be separated from TP0, the ball of the package performing the host-to-module transmit function, by 1 dB of attenuation at 14 GHz.

13.B.1.1 Host-to-Module transmitter output Electrical Specifications

It is recommended that each host-to-module lane meet the limits of Table 13-9.

Note: A 2 tap FIR filter may be advantageous in meeting the TP1a requirements.

Table 13-9. Host-to-Module Electrical Specifications at TP0a

Parameter	Symbol	Min.	Max.	Units	Conditions
Differential Voltage, pk-pk	T_Vdiff	600	-	mV	PRBS31 pattern. Emphasis off. Note 1
Common Mode Voltage	T_Vcm	-300	2800	mV	Note 2
Differential resistance	T_Rd	80	120	ohms	
Differential Termination Resistance Mismatch	T_Rdm	-	10	%	at 1 MHz
Differential Return Loss	T_SDD22	-	See 10.3.1.3 (CEI-28G-SR)	dB	
Transition Time: 20 to 80%	T_tr, T_tf	8	-	ps	Emphasis off.
Common Mode Noise, RMS	T_Ncm	-	12	mV	See 12.3
Uncorrelated Unbounded Gaussian jitter	T_UUGJ	-	0.15	UI	
Uncorrelated Bounded high probability jitter including DCD	T_UBHPJ	-	0.15	UI	Note 4
Duty Cycle Distortion	T_DCD	-	0.035	UI	
Total Jitter	T_TJ	-	0.28	UI	Note 3

NOTES:
1. Max voltage is limited by specifications at TP1a. Minimum voltage can be lower for low loss channels.
2. Load type 0 with min. T_Vdiff, AC-Coupling or floating load.
3. T_TJ includes all of the jitter components measured without any transmit equalization. A 1 dB CTLE can be used to achieve this specification. (See Section 13.3.11.3). For jitter test parameters see 12.1 except use a CRU tracking BW = f_b/2578.
4. Measured with any value of transmitter equalization See Section 12.1.

14 CEI-28G-MR Medium Reach Interface

This clause details the requirements for the CEI-28G-MR medium reach high speed electrical interface between nominal baud rates of 19.90 Gsym/s and 28.1 Gsym/s using NRZ coding. A compliant device shall meet all of the requirements listed below. The electrical interface is based on high speed, low voltage logic. Connections are point-to-point balanced differential pairs and signaling is unidirectional.

The electrical IA is based on loss and jitter budgets and defines the characteristics required to communicate between a CEI-28G-MR transmitter and a CEI-28G-MR receiver using copper signal traces on a printed circuit board. The characteristic impedance of the signal traces is nominally 100 Ω differential. A 'length' is effectively defined in terms of its attenuation and phase response rather than its physical length. Refer to Section 14.2.6 for transmission line guidelines to meet the channel requirements.

Medium reach CEI-28G-MR devices from different manufacturers shall be interoperable.

14.1 Requirements

1. Support serial baud rates within the range from 19.90 Gsym/s to 28.1 Gsym/s.
2. Capable of low bit error ratio (10^{-15}, with a test requirement to verify 10^{-12}).
3. Capable of driving up to 500 mm of PCB and up to 1 connector.
4. Shall support AC-coupled operation.
5. Shall allow multi-lanes (1 to n).
6. Shall support hot plug.

14.2 General Requirements

14.2.1 Data Patterns

Please refer to Section 3.2.1

14.2.2 Signal levels

Please refer to Section 3.2.2. All transmitter and receiver devices shall support "Load Type 0". Other load types are not supported by this clause.

14.2.3 Signal Definitions

Please refer to Section 1.A

14.2.4 Bit Error Ratio

Please refer to Section 3.2.3

14.2.5 Ground Differences

Please refer to Section 3.2.4

14.2.6 Channel Compliance

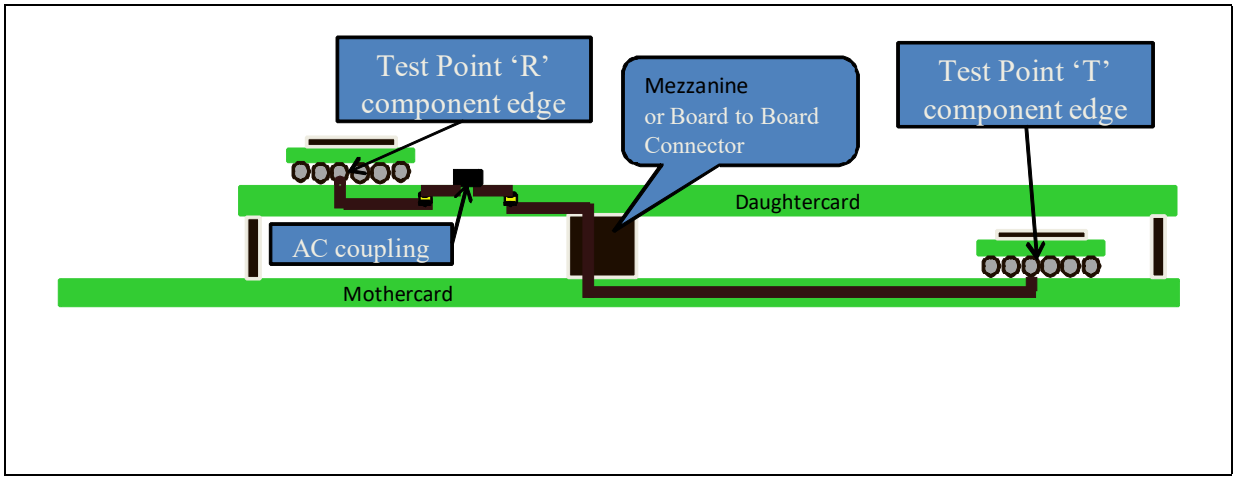
A forward channel and associated dominant crosstalk channels are deemed compliant if the channel characteristics conform to the requirements in this section.

14.2.6.1 Reference Model

The channel consists of PCB traces, vias, and 1 connector. The reference PCB trace differential impedance is 100Ω.

Figure 14-1 shows a diagram of test points on an example board.

Figure 14-1. CEI-28G-MR Reference Model



Note: Test points differ from definitions in Section 1.8, as DC blocking capacitor, if physically located outside of the package, is part of the channel.

Measured at these test points, several channel characteristics are parametrized. Port definitions as noted in Figure 14-1 allow proper measurement of the parameters in Table 14-1 used for calculation of the channel parameters found in Table 14-2.

Table 14-1. Measured Channel Parameters

Symbol	Description
$IL(f)$	Differential insertion loss, -SDD21 magnitude (dB)
$RL_1(f)$	Differential input return loss, -SDD11 magnitude (dB)
$RL_2(f)$	Differential output return loss, -SDD22 magnitude (dB)
$NEXT_m(f)$	Differential near-end crosstalk loss (m^{th} aggressor), -SDD21 magnitude (dB)
$FEXT_n(f)$	Differential far-end crosstalk loss (n^{th} aggressor), -SDD21 magnitude (dB)

Table 14-2. Calculated Channel Parameters

Symbol	Description
$IL_{fitted}(f)$	Fitted insertion loss (dB)
$ILD(f)$	Insertion loss deviation (dB)
$ICN(f)$	Integrated crosstalk noise (mV_{RMS})
FOM_{ILD}	A figure of merit of the insertion loss deviation (dB)

14.2.6.2 Insertion Loss

Channel insertion losses, including PCB traces and connectors, shall comply with the limits specified by equations (14-1), (14-2) and plotted in Figure 14-2. Note that the variable f_b is the maximum baud rate to be supported by the channel under test (19.90 GHz $\le f_b \le$ 28.1 GHz).

Table 14-3. Channel Insertion Loss Frequency Range

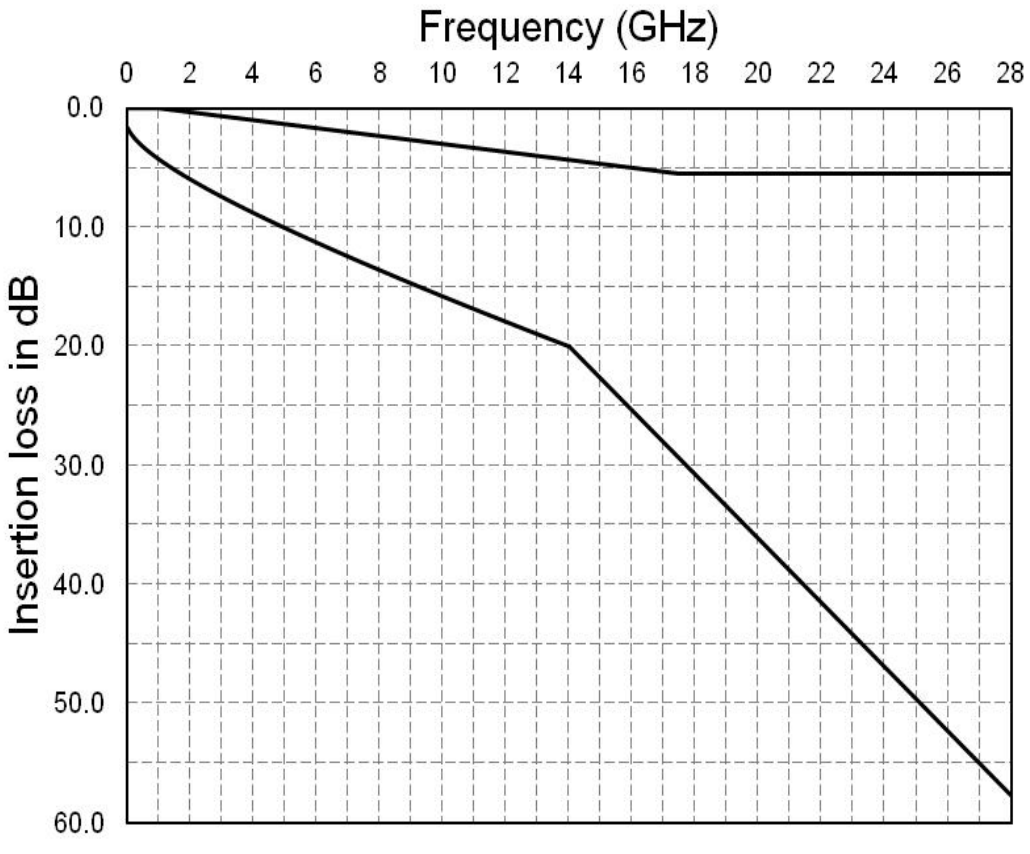
Parameter	Value	Units
fmin	50	MHz
fmax	**f_b**	GHz

$$IL_{max} = \begin{cases} (1.083) + 2.436\sqrt{\frac{f \times 28.1}{f_b}} + 0.698\frac{f \times 28.1}{f_b}, & f_{min} \le f < \frac{f_b}{2} \\ -17.851 + 2.694\frac{f \times 28.1}{f_b}, & \frac{f_b}{2} \le f \le f_b \end{cases} \quad (14\text{-}1)$$

$$IL_{min} = \begin{pmatrix} 0, & f_{min} \le f \le 1\,GHz \\ \frac{1}{3}(f-1), & 1\,GHz < f \le 17.5\,GHz \\ 5.5, & 17.5\,GHz < f \le f_b \end{pmatrix} \quad (14\text{-}2)$$

Note: f in equations (14-1) and (14-2) is in GHz.

Figure 14-2. CEI-28G-MR normative channel insertion loss at 28.1 Gsym/s



14.2.6.3 Fitted insertion loss

For fitted insertion loss definitions, please refer to Section 12.2.1.1

The channel shall meet the insertion loss requirements defined in Table 14-4. Note that the variable f_b is the maximum baud rate to be supported by the channel under test.

Table 14-4. Channel fitted insertion loss characteristics

Parameter	Units	Value	
		Min.	Max.
Minimum frequency, f_{ILmin}	GHz	0.05	-
Maximum frequency, f_{ILmax}	GHz	-	f_b
Fitted Insertion loss at Nyquist	dB	-	20
Fitted insertion loss, a_0	dB	-1	2
Fitted insertion loss, a_1	dB	0	14.914
Fitted insertion loss, a_2	dB	0	41.228
Fitted insertion loss, a_4	dB	0	19.728

14.2.6.4 Insertion loss deviation (ILD)

The insertion loss deviation *ILD* is the difference between the measured insertion *IL* and the fitted insertion loss IL_{fitted} as defined in equation (14-3).

$$ILD = IL - IL_{fitted} \tag{14-3}$$

The insertion loss deviation ILD shall be within the region defined by equations (14-4) and (14-5) where f_b is the maximum baud rate to be supported by the channel under test and f_{ILmin} and f_{ILmax} are given in Table 14-4.

$$ILD \geq ILD_{min} = \begin{cases} -1.0 - 12.0(f/f_b) & f_{ILmin} \leq f < f_b/4 \\ -4.0 & f_b/4 \leq f \leq (3/4)f_{ILmax} \end{cases} \tag{14-4}$$

$$ILD \leq ILD_{max} = \begin{cases} 1.0 + 12.0(f/f_b) & f_{ILmin} \leq f < f_b/4 \\ 4.0 & f_b/4 \leq f \leq (3/4)f_{ILmax} \end{cases} \tag{14-5}$$

FOM_{ILD} is a figure of merit of the channel's insertion loss deviation (dB) from f_{ILmin} to $(3/4)*f_{ILmax}$. In OIF-CEI-0.30 and OIF-CEI-03.1, this was called ILD_{RMS}. FOM_{ILD} is calculated as indicated below.

Define the weight at each frequency *f* using equation (14-6) below.

$$W(f) = \mathrm{sinc}^2(f/f_b)\left[\frac{1}{1+(f/f_t)^4}\right]\left[\frac{1}{1+(f/f_r)^8}\right] \quad (14\text{-}6)$$

Note that -3 dB transmit filter bandwidth f_t is inversely proportional to the minimum 20 to 80% rise and fall times *T_tr and T_tf*. The constant of proportionality is 0.2365 (i.e. T_tr x f_t = 0.2365, T_tr is in ns when f_t is in GHz). In addition, f_r is the -3 dB reference receiver bandwidth, which should be set at (3/4)f_b, where f_b is the maximum baud rate to be supported by the channel.

$$FOM_{ILD} = \sqrt{\frac{\sum W(f) \times ILD(f)^2}{N}} \quad (14\text{-}7)$$

FOM_{ILD} is calculated using equation (14-7) where N is the number of frequency points. The summation is done over the frequency range of ILD with *f* in GHz. FOM_{ILD} shall be less than 0.3 dB for valid channels.

14.2.6.5 Channel Return Loss

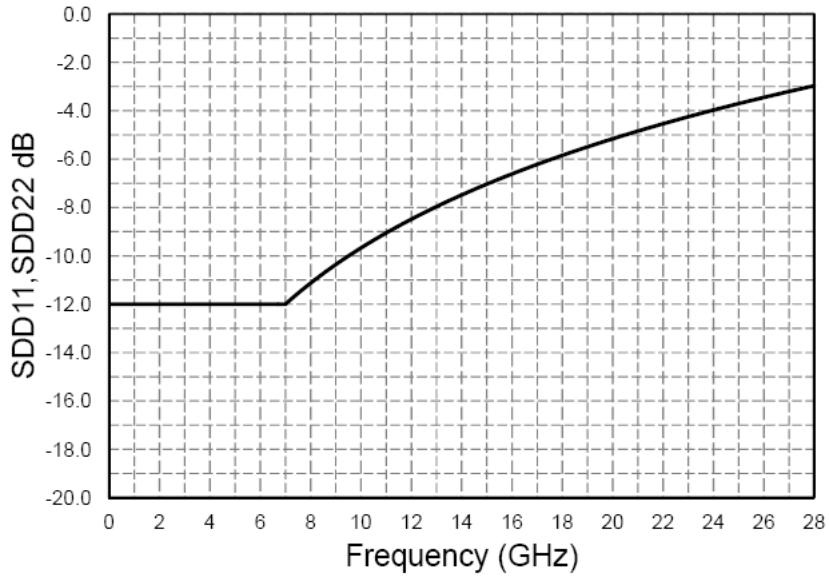
Channel Return Loss shall be bounded by equation (14-8) as shown in Figure 14-3.

- RL(f) >= 12 dB for $f_{min} < f \leq f_b/4$
- RL(f) >= 12 dB - 15 $\mathrm{Log}_{10}(4f/f_b)$ for $f_b/4 < f < f_b$

(14-8)

Note: f_{min} is as defined in Table 14-3

Figure 14-3. CEI-28G-MR normative channel return loss at 28.1 Gsym/s



14.2.6.6 Channel integrated crosstalk noise

Using the Integrated crosstalk noise method of Section 12.2.1.2 and the parameters of Table 14-5, the total integrated crosstalk noise for the channel shall be less than the value specified by equation (14-9) and illustrated in Figure 14-4.

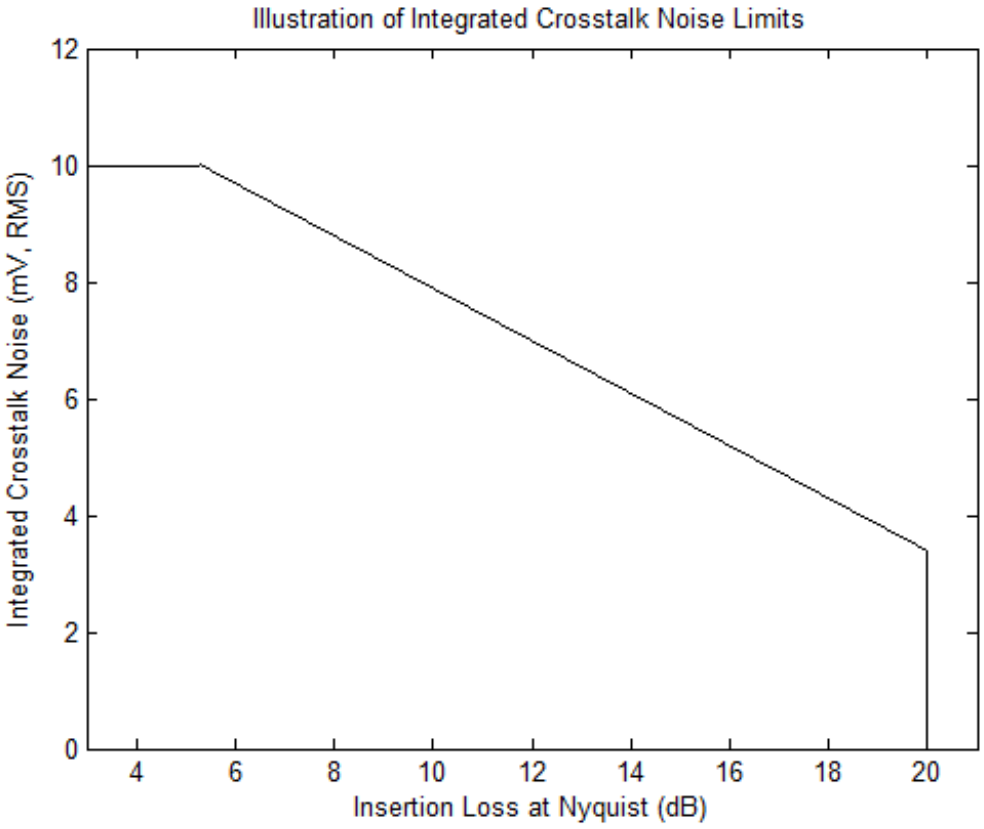
Table 14-5. Channel integrated crosstalk aggressor parameters

Parameter	Symbol	Value	Units
Baud rate	f_b	max. Baud Rate sup. by Channel	Gsym/s
Near-end aggressor peak to peak differential output amplitude	A_{nt}	1200	mVppd
Far-end aggressor peak to peak differential output amplitude	A_{ft}	1200	mVppd
Near-end aggressor 20 to 80% rise and fall times	T_{nt}	8	ps
Far-end aggressor 20 to 80% rise and fall times	T_{ft}	8	ps

$$\begin{aligned} \sigma_x \le \sigma_{x,\,max} &= 10\ (mV, RMS) && for && 3\,dB < IL \le 5.3\ dB \\ &= 12.4 - 0.45\,IL\ (mV, RMS) && for && 5.3\,dB < IL \le 20dB \end{aligned} \quad (14\text{-}9)$$

In equation (14-9), the *IL* denotes the value of the channel insertion loss in dB at 1/2 · baud rate (NRZ).

Figure 14-4. Illustration of integrated crosstalk noise limits



14.3 Electrical Characteristics

The electrical signaling is based on high speed low voltage logic with a nominal differential impedance of 100 Ω.

All devices shall work within the range from 19.90 Gsym/s to 28.1 Gsym/s as specified for the device, with the baud rate tolerance as per Section 3.2.11. Note that implementation of specific protocols will define the operating baud rate without affecting CEI compliance.

14.3.1 Transmitter Characteristics

The transmitter electrical specifications at compliance point T (see Figure 14-1) are given in Table 14-6. The transmitter shall satisfy jitter requirements specified in Table 14-7. Jitter is measured as specified in Section 2.3.3, for a BER as specified in Section 14.2.4. It is assumed that the UBHPJ component of the transmitter jitter is not data-dependent jitter (DDJ) from the receiver view point, hence it cannot be equalized in the receiver. To attenuate noise and absorb even/odd mode reflections, the transmitter shall satisfy the Common Mode Output Return Loss requirement of Table 14-6.

Link budgets in this document assume optimized TX FIR equalization that is part of the system management function. The specific implementation is outside the scope of this document.

Table 14-6. Transmitter Electrical Output Specification.

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	T_Baud		19.90		28.1	Gsym/s
Output Differential Voltage	T_Vdiff	Emphasis off. See Note 4.	800		1200	mVppd
Single Ended Transmitter Output Voltage	T_Vse		-0.3		1.9	V
Differential Resistance	T_Rd		80	100	120	Ω
Differential Termination Resistance Mismatch (see Table 1-2)	T_Rdm				10	%
Output Rise and Fall Time (20% to 80%)	T_tr, T_tf	Emphasis off. See Note 2.	8			ps
Common Mode Noise	T_Ncm	See Note 3.			12	mV_{RMS}
Differential Output Return Loss	T_SDD22	See Section 14.3.1.3				dB
Common Mode Output Return Loss	T_SCC22	Below 10 GHz			-6	dB
		10 GHz to baud rate			-4	
Output Common Mode Voltage	T_Vcm	Load Type 0 See Note 1	-100		1700	mV

NOTES:
1. Load Type 0 with min. T_Vdiff, AC-Coupling or floating load.
2. The transmitter under test is preset such that C0 is its maximum value (C0_max) and all other coefficients are zero. The 20% and 80% values are of the steady state one and zero. The max value is limited by the linear fit pulse peak value in Table 14-11.
3. Measurement procedure is defined in Section 12.3.
4. T_Vdiff is two times the steady-state value V_f as defined in Section 14.3.1.6.2. The value is given as differential p-p voltage.

Table 14-7. Transmitter Output Jitter Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Uncorrelated Unbounded Gaussian Jitter	T_UUGJ	Note 4			0.15	UI_{PP}
Uncorrelated Bounded High Probability Jitter	T_UBHPJ	Note 2			0.15	UI_{PP}
Even-Odd Jitter (component of UBHPJ)	T_EOJ	Note 3			0.035	UI_{PP}
Total Jitter	T_TJ	Note 1			0.28	UI_{PP}

NOTES:
1. T_TJ includes all of the jitter components measured without any transmit equalization.
2. Measured with all possible values of transmitter equalization, excluding DDJ as defined in Section 12.1.
3. Included in T_UBHPJ
4. Measured with all possible values of transmitter equalization

14.3.1.1 Transmitter Baud Rate

All devices shall work within the range from 19.90 Gsym/s to 28.1 Gsym/s as specified for the device, with the baud rate tolerance as per Section 3.2.11. Note that implementation of specific protocols will define the operating baud rate without affecting CEI compliance.

14.3.1.2 Transmitter Amplitude and Swing

Transmitter differential output amplitude shall be able to drive between 800 to 1200 mVppd with transmit emphasis disabled. The single-ended transmitter output voltage shall be between -0.3V and 1.9 V with respect to local ground. Transmitter differential output amplitude shall additionally adhere to the requirements in Section 14.3.1.6.

14.3.1.3 Transmitter Return Loss

Please refer to Section 3.2.10 with the following parameters.

Table 14-8. Transmitter Differential Return Loss Parameters

Parameter	Value	Units
A0	-12	dB
f0	50	MHz
f1	0.1714 x T_Baud	Hz
f2	T_Baud	Hz
Slope	12.0	dB/dec

14.3.1.4 Transmitter Lane-to-Lane Skew

Please refer to Section 3.2.7

14.3.1.5 Transmitter Short Circuit Current

Please refer to Section 3.2.9

14.3.1.6 Transmitter output waveform requirements

The transmitter shall include an equalizer defined as:

$$H(Z) = C_{-1} + C_0 z^{-1} + C_1 z^{-2} \quad (14\text{-}10)$$

14.3.1.6.1 Summary of requirements

The normalized amplitudes of the coefficients of the transmitter equalizer (computed per 14.3.1.6.2) shall meet the requirements in Table 14-9.

Table 14-9. Coefficient range and step size

Coefficient	Normalized Amplitude		Normalized Step Size (%)
	Min (%)	Max (%)	
C_{-1}	-20	0	1.25 to 5
C_1	-25	0	1.25 to 5
C_0	40	100	1.25 to 5

The amplitude of a coefficient can be computed by multiplying its normalized amplitude by v_f, which is defined in equation (14-11). "min" is defined as the minimum normalized amplitude of the coefficient that must be supplied by the transmitter to be compliant. "max" is defined as the maximum normalized amplitude of the coefficient that must be supplied by the transmitter to be compliant.

In addition:

a) $|C_{-1}|+|C_0|+|C_1|$, the peak to peak output voltage shall not exceed 1200 mVppd.

b) $C_{-1} + C_0 + C_1$, the steady-state output voltage shall be greater than or equal to 80 mVppd.

14.3.1.6.2 Process to compute coefficients

The coefficients of the transmitter equalizer are defined by a calculation based on the transmitter output waveform as described below.

1. The transmitter under test is preset such that C_0 is its maximum value (C_{0_max}) and all other coefficients are zero.

2. Capture at least one complete cycle of the test pattern PRBS9 at T [T is defined as the test point at the output of transmitter package] per Section 14.3.1.6.3.

3. Compute the linear fit to the captured waveform per Section 14.3.1.6.4.

4. Define t_x to be the time where the rising edge of the linear fit pulse, p, from step 3 crosses 50% of its peak amplitude.

5. Sample the linear fit pulse, p, at symbol-spaced intervals relative to the time $t_0 = t_x + 0.5$ UI, interpolating as necessary to yield the sampled pulse p_i.

6. Use p_i to compute the vector of coefficients, w, of a T_N_w-tap symbol-spaced transversal filter that equalizes for the transfer function from the transmit function to T per Section 14.3.1.6.5.

The parameters of the pulse fit and the equalizing filter are given in Table 14-10.

Table 14-10. Linear fit pulse and equalizing filter parameters

Parameter	Value (UI)
Linear fit pulse length T_N_p	8
Linear fit pulse delay T_D_p	2
Equalizer length T_N_w	8
Equalizer delay T_D_w	2

The differential zero to peak output voltage at T in the steady state, v_f, is estimated by equation (14-11).

$$v_f = \frac{1}{M} \cdot \sum_{k=1}^{M \cdot T_Np} p(k) \qquad (14\text{-}11)$$

In (14-11), p is the linear fit pulse from step 3 and M is the number of samples per symbol as defined in 14.3.1.6.3. The peak value of the linear fit pulse from step 3, p_{max}, shall satisfy the requirements of Table 14-11.The RMS value of the error between the linear fit and measured waveform from step 3, σ_e, shall satisfy the requirements of Table 14-11.

Table 14-11. Transmitter output waveform requirements

Parameter	Condition	Units	
Steady state output voltage, 2 x v_f	max	mVppd	1200
Steady state output voltage, 2 x v_f	min	mVppd	800
Linear fit pulse peak, p_{max}	min	-	0.80 x v_f
RMS error, σ_e	max	-	0.027 x v_f

For each configuration of the transmit equalizer:

7. Configure the transmitter under test as required.

8. Capture at least one complete cycle of the test pattern PRBS9 at T.

9. Compute the linear fit to the captured waveform per Section 14.3.1.6.4.

10. Define t_x to be the time where the rising edge of the linear fit pulse, *p*, from step 3 crosses 50% of its peak amplitude.

11. Sample the linear fit pulse, *p*, at symbol-spaced intervals relative to the time $t_0 = t_x + 0.5$ UI, interpolating as necessary to yield the sampled pulse p_i.

12. Equalize the sampled pulse, p_i, using the coefficient vector, *w*, computed in step 6 per Section 14.3.1.6.5 to yield the equalized pulse q_i.

The RMS value of the error between the linear fit and measured waveform from step 9, σ_e, shall satisfy the requirements of Table 14-11.

The normalized amplitude of coefficient C_{-1} is the value of q_i at time $t_0 + (T_D_w - 1)$ UI.
The normalized amplitude of coefficient C_0 is the value of q_i at time $t_0 + T_D_w$ UI.
The normalized amplitude of coefficient C_1 is the value of q_i at time $t_0 + (T_D_w + 1)$ UI.

14.3.1.6.3 Waveform acquisition

The transmitter under test repetitively transmits the specified test pattern. The waveform shall be captured with an effective sample rate that is *M* times the signaling rate of the transmitter under test. The value of *M* shall be an integer not less than 7. Averaging multiple waveform captures is recommended.

The captured waveform shall represent an integer number of repetitions of the test pattern totaling *N* bits. Hence the length of the captured waveform should be $M \cdot N$ samples. The waveform should be aligned such that the first *M* samples of waveform correspond to the first bit of the test pattern, the second *M* samples to the second bit, and so on.

14.3.1.6.4 Linear fit to the waveform measured at T

Given the captured waveform *y(k)* and corresponding aligned symbols *x(n)* derived from the procedure defined in Section 14.3.1.6.2, define the *M*-by-*N* waveform matrix *Y* as shown in equation (14-12).

$$Y = \begin{bmatrix} y(1) & y(M+1) & \cdots & y(M(N-1)+1) \\ y(2) & y(M+2) & \cdots & y(M(N-1)+2) \\ \vdots & \vdots & \cdots & \vdots \\ y(M) & y(2M) & \cdots & y(MN) \end{bmatrix} \quad (14\text{-}12)$$

Rotate the symbols vector *x* by the specified pulse delay D_p to yield x_r.

$$x_r = \left[x(T_D_p + 1) \quad x(T_D_p + 2) \quad \cdots \quad x(N) \quad x(1) \quad \cdots \quad x(T_D_p)\right] \tag{14-13}$$

Define the matrix *X* to be an *N*-by-*N* matrix derived from x_r as shown in equation (14-14).

$$X = \begin{bmatrix} x_r(1) & x_r(2) & \cdots & x_r(N) \\ x_r(N) & x_r(1) & \cdots & x_r(N-1) \\ \vdots & \vdots & \cdots & \vdots \\ x_r(2) & x_r(3) & \cdots & x_r(1) \end{bmatrix} \tag{14-14}$$

Define the matrix X_1 to be the first T_N_p rows of *X* concatenated with a row vector of 1's of length *N*. The *M*-by-(T_N_p + 1) coefficient matrix, *P*, corresponding to the linear fit is then defined by equation (14-15).

$$P = YX_1^{\mathrm{T}}(X_1X_1^{\mathrm{T}})^{-1} \tag{14-15}$$

In equation (14-15) the superscript "T" denotes the matrix transpose operator.

$$E = PX_1 - Y = \begin{bmatrix} e(1) & e(M+1) & \cdots & e(M(N-1)+1) \\ e(2) & e(M+2) & \cdots & e(M(N-1)+2) \\ \vdots & \vdots & \cdots & \vdots \\ e(M) & e(2M) & \cdots & e(MN) \end{bmatrix} \tag{14-16}$$

The error waveform, *e(k)*, is then read column-wise from the elements of *E*.

Define P_1 to be a matrix consisting of the first T_N_p columns of the matrix *P* as shown in equation (14-17).

$$P_1 = \begin{bmatrix} p(1) & p(M+1) & \cdots & p(M(T_N_p - 1)+1) \\ p(2) & p(M+2) & \cdots & p(M(T_N_p - 1)+2) \\ \vdots & \vdots & \cdots & \vdots \\ p(M) & p(2M) & \cdots & p(MT_N_p) \end{bmatrix} \quad (14\text{-}17)$$

The linear fit pulse response, *p(k)*, is then read column-wise from the elements of P_1.

14.3.1.6.5 Removal of the transfer function between the transmit function and T

Rotate sampled pulse response p_i by the specified equalizer delay T_D_w to yield p_r as shown in equation (14-18).

$$p_r = \left[p_i(T_D_w + 1) \quad p_i(T_D_w + 2) \quad \cdots \quad p_i(T_N_p) \quad p_i(1) \quad \cdots \quad p_i(T_D_w) \right] \quad (14\text{-}18)$$

Define the matrix P_2 to be a T_N_p-by-T_N_p matrix derived from pr as shown in equation (14-19).

$$P_2 = \begin{bmatrix} p_r(1) & p_r(T_N_p) & \cdots & p_r(2) \\ p_r(2) & p_r(1) & \cdots & p_r(3) \\ \vdots & \vdots & \cdots & \vdots \\ p_r(T_N_p) & p_r(T_N_p - 1) & \cdots & p_r(1) \end{bmatrix} \quad (14\text{-}19)$$

Define the matrix P_3 to be the first T_N_w rows of P_2. Define a unit pulse column vector x_p of length T_N_p. The value of element $x_p(T_D_p + 1)$ is 1 and all other elements have a value of 0. The vector of filter coefficients w that equalizes p_i is then defined by (14-20).

$$w = (P_3^{\mathrm{T}} P_3)^{-1} P_3^{\mathrm{T}} x_p \quad (14\text{-}20)$$

Given the column vector of equalizer coefficients, w, the equalized pulse response q_i is determined by equation (14-21).

$$q_i = P_3 w \quad (14\text{-}21)$$

14.3.2 Receiver Characteristics

A compliant receiver shall operate at the specified BER with the worst case combination of a compliant transmitter and a compliant channel.

Receiver electrical specifications are given in Table 14-12 and measured at compliance point R. To dampen noise sources and absorption of both even and odd mode reflections, the receiver shall satisfy the Common Mode Input Return Loss requirement of Table 14-12. Jitter specifications at reference R (see Figure 14-1) are listed in Table 14-13.

Table 14-12. Receiver Electrical Input Specifications

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud rate	R_Baud		19.90		28.1	GSym/s
Input Differential Voltage	R_Vdiff	Note 1			1200	mVppd
Single Ended Input Voltage	Vse	See 14.3.2.5 See Note 2	-300		2000	mV
Differential Input Impedance	R_Rdin		80	100	120	Ω
Input Impedance Mismatch	R_Rm				10	%
Differential Input Return Loss	R_SDD11	See 14.3.2.3				
Common Mode Input Return Loss	R_SCC11	Below 10 GHz			-6	dB
		10GHz to baud rate			-4	
Input Common Mode Voltage	R_Vcm	Load Type 0 See Note 2	-150		1750	mV

NOTES:
1. The receiver shall have a differential input voltage range sufficient to accept a signal produced at point R by the combined transmitter and channel. The channel response shall include the worst case effects of the return losses at the transmitter and receiver.
2. Load Type 0 with min. T_Vdiff, AC-Coupling or floating load. For floating load, input resistance shall be ≥ 1kΩ. Only applies if AC-coupling capacitor is integrated in receiver

Table 14-13. Receiver Input Jitter Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Sinusoidal Jitter, Maximum	R_SJ-max	See Section 2.3.4, Note 1			5	UIpp
Sinusoidal Jitter, High Frequency	R_SJ-hf	See Section 2.3.4, Note 1			0.05	UIpp

NOTES:
1. The Receiver shall tolerate the sum of these jitter contributions: Total transmitter jitter from Table 14-7;Sinusoidal jitter as defined in Table 14-13;The effects of a channel compliant to the Channel Characteristics (Section 14.2.6).

14.3.2.1 Input Baud Rate

All devices shall work within the range from 19.90 Gsym/s to 28.1 Gsym/s as specified for the device, with the baud rate tolerance as per Section 3.2.11.

14.3.2.2 Reference Input Signals

The receiver shall accept differential input signal amplitudes produced by a compliant transmitter connected with the minimum attenuation specified in Figure 14-2 to the receiver. This may be larger than the 1200 mVppd maximum of the transmitter due to output/input impedances and reflections.

The minimum input amplitude is defined by the minimum transmitter amplitude, the actual receiver input impedance and the loss of the actual PCB. Note that the minimum transmitter amplitude is defined using a well controlled load impedance, however the real receiver is not, which can leave the receiver input signal smaller than expected. Additionally it will be determined by the environmental noise inside and outside the receiver.

14.3.2.3 Input Resistance and Return Loss

Please refer to Section 3.2.10 with the following parameters.

Table 14-14. Receiver Differential Return Loss Parameters

Parameter	Value	Units
A0	-12	dB
f0	50	MHz
f1	0.1714 x R_Baud	Hz
f2	R_Baud	Hz
Slope	12.0	dB/dec

14.3.2.4 Input Lane-to-Lane Skew

Please refer to Section 3.2.8.

14.3.2.5 Single Ended Input Voltage

The single ended voltage levels with respect to the receiver ground at the input of the receiver are dependent on the transmitter implementation and the inter-ground difference. The voltage levels at the input of an AC coupled receiver (if the effective AC coupling is done within the receiver) or at the TX side of the external AC coupling cap (if AC coupling is done externally) will be between -0.3 to 2.0V with respect to local ground.

15 Reserved to add future Clause

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16 CEI-56G-VSR-PAM4 Very Short Reach Interface

This clause details the requirements for the CEI-56G-VSR-PAM4 very short reach high speed chip-to-module electrical interface of nominal baud rates of 18.0 Gsym/s to 29.0 Gsym/s. A compliant host or module shall meet all of the relevant requirements listed below. The electrical interface is based on high speed, low voltage logic, and connections are point-to-point balanced differential pairs.

This clause defines the characteristics required to communicate between CEI-56G-VSR-PAM4 drivers and CEI-56G-VSR-PAM4 receivers using copper signal traces on a printed circuit board, a mated connector pair and copper signal traces inside an optical module. These specifications are normative at the test points shown in Figure 16-1. A 'length' is effectively defined in terms of its attenuation and phase response rather than its physical length.

Hosts and modules compliant to CEI-56G-VSR-PAM4 from different manufacturers shall be interoperable.

16.1 Requirements

The objectives and requirements for the CEI-56G-VSR-PAM4 implementation agreement are given by the project definition as follows:

- Support serial baud rates (f_b) within the range from **18.0** Gsym/s to **29.0** Gsym/s as specified for the device using ***PAM4 coding***. A CEI implementation complies to the specifications of this clause over the range of baud rates stated for the implementation within this range.
- Capable of driving up to a minimum of ***125 mm*** of host PCB trace plus one connector and a minimum of **25 mm** of module PCB trace.
- Capable of achieving a raw Bit Error Ratio (BER) of 10^{-6} or better per lane. FEC is assumed to be used to achieve a corrected BER of 10^{-15} or better per lane. The baud rate includes the overhead required for FEC. The definition of FEC is outside the scope of this IA (see Appendix 16.D).
- Module electrical input to be self-adaptive and autonomous.
- Shall support AC-coupled operation.
- Shall allow multi-lanes (1 to n).
- Shall support hot plug.

16.2 General CEI Requirements

16.2.1 Data Patterns

See Appendix 16.C.5.

16.2.2 Transmitter equalizer function

Both host and module Tx FIRs are likely to be required to meet TP1a and far-end TP4 eye requirements respectively for high loss channels (see Figure 16-1).

16.2.3 Bit Error Ratio

A raw Bit Error Ratio (BER) better than or equal to 10^{-6} is required on each lane. A compliant host or module, when receiving from a compliant module or host, shall deliver the specified raw BER to the subsequent FEC decoder. Error bursts with length more than 15 PAM4 symbols delivered to the PAM4 decoder shall occur with a probability of less than 1 in 10^{20} PAM4 symbols. See also Appendix 16.D.

16.2.4 Ground Differences

The maximum ground difference between the host and module shall be ±50 mV. The common mode voltage limits are set taking this difference into account.

16.3 Electrical Characteristics

Hosts and modules shall meet the applicable specifications defined in Table 16-1, Table 16-2, Table 16-3, Table 16-4, Table 16-5 and Table 16-6 as applicable. The direction of a signal (host-to-module or module-to-host) determines which table is applicable.

AC coupling is required in the module for both Tx and Rx.

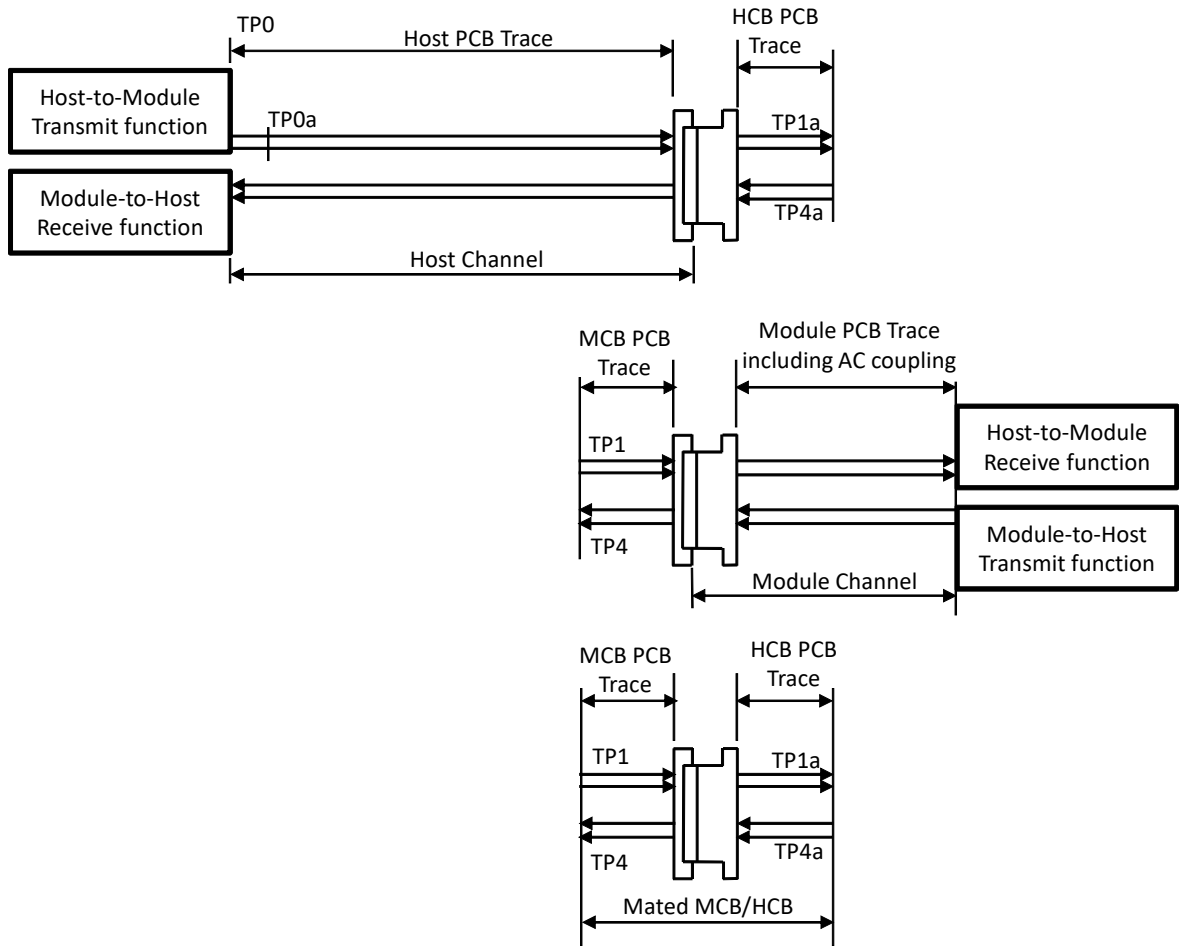
16.3.1 Compliance Point Specifications

Figure 16-1 below gives the reference model and test points associated with host-to-module and module-to-host lanes.

Reference test fixtures, called compliance boards, are used to access the electrical specification parameters. The output of the Host Compliance Board (HCB) provides access to the host-to-module electrical signal (host electrical output) defined at TP1a. Additional module electrical input specifications, for host-to-module communication, are defined at TP1, the input of the Module Compliance Board (MCB). The output of the Module Compliance Board (MCB) provides access to the module to host electrical signal (module electrical output) defined at TP4. Additional host electrical input

specifications, for module-to-host communication, are defined at TP4a, the input of the Host Compliance Board (HCB). Informative specifications for the host transmit function (TP0a) are given in Appendix 16.B.

Figure 16-1. Measurement points using compliance boards.



16.3.2 Host-to-Module Electrical Specifications

Each host-to-module lane shall meet the specifications of Table 16-1 and Table 16-2. Definitions and methodologies can be found in Sections 16.3.4 to 16.3.11.

Table 16-1. Host-to-Module Electrical Specifications at TP1a (host output)

Parameter	Min.	Max.	Units	Conditions
Differential Voltage pk-pk	-	880	mV	See Note 1
Common Mode Voltage (Vcm)	-0.3	2.8	V	Referred to host ground See Note 2
Common Mode Noise RMS	-	17.5	mV	See 16.3.5
Differential Termination Resistance Mismatch	-	10.0	%	At 1 MHz. See 16.3.6
Differential Return Loss (SDD22)	-	Equation (16-1)	dB	See Note 3
Common Mode to Differential Mode Conversion (SDC22)	-	Equation (16-3)	dB	See Note 3
Common Mode Return Loss (SCC22)	-	-2	dB	250 MHz to f_b GHz See Note 3
Transition Time	12.0		ps	See 16.C.4.1
Vertical Eye Closure (VEC)	-	12.5	dB	See 16.C.4.2
Eye Width at 10^{-6} probability (EW6)	0.20	-	UI	See 16.3.10 See Note 4
Eye Height at 10^{-6} probability (EH6)	32	-	mV	See 16.3.10 See Note 4
Eye Linearity	0.85	-	-	See Equation (16-14) See Note 4

NOTES:
1. The differential voltage measured using a QPRBS13-CEI pattern will be less than the in-service differential voltage due to host loss and length of the QPRB13-CEI pattern.
2. Vcm is defined in Table 1-2 of Section 1.6
3. S-parameter specifications based on a differential reference impedance of 100 Ω and a common mode reference impedance of 25 Ω
4. Open eye is generated through the use of a reference Continuous Time Linear Equalizer (CTLE) applicable to all three PAM4 eyes (See Section 16.3.10.4)

Table 16-2. Host-to-Module Electrical Specifications (module input)

Parameter	Test Point	Min.	Max.	Units	Conditions
Overload Differential Voltage pk-pk	TP1a	900	-	mV	See 16.3.11
Common Mode Voltage (Vcm)	TP1	-350	2850	mV	See Note 1, 2
Differential Termination Resistance Mismatch	TP1	-	10	%	At 1 MHz. See 16.3.6
Differential Return Loss (SDD11)	TP1	-	Equation (16-1)	dB	See Note 3
Differential Mode to Common Mode Conversion (SCD11)	TP1	-	Equation (16-2)	dB	See Note 3
Stressed Input Test	TP1a	See Section 16.3.10.3			

NOTES:
1. Vcm is defined in Table 1-2 of Section 1.6
2. Vcm is generated by the host. Specification includes effects of ground offset voltage
3. S-parameter specifications based on a differential reference impedance of 100 Ω and a common mode reference impedance of 25 Ω

Table 16-3. Crosstalk parameters for host output test and module stressed input test calibration at TP4

Parameter	Target value	Units	Conditions
Crosstalk Amplitude Differential Voltage pk-pk	900	mV	
Crosstalk Slew Time (between -270 mV and +270 mV)	9.5	ps	See Note 1

NOTES:
1. See Section 16.C.4.1 Transition Time and Slew Time

16.3.3 Module-to-Host Electrical Specifications

Each module-to-host lane shall meet the specifications of Table 16-4 and Table 16-5. Definitions and methodologies can be found in Sections 16.3.4 to 16.3.11.

Table 16-4. Module-to-Host Electrical Specifications at TP4 (module output)

Parameter	Min.	Max.	Units	Conditions
Differential Voltage, pk-pk	-	900	mV	
Common Mode Voltage (Vcm)	-350	2850	mV	See Note 1, 2
Common Mode Noise, RMS	-	17.5	mV	See 16.3.5
Differential Termination Resistance Mismatch	-	10	%	At 1 MHz. See 16.3.6
Differential Return Loss (SDD22)	-	Equation (16-1)	dB	See Note 3
Common Mode to Differential Mode Conversion (SDC22)	-	Equation (16-3)	dB	See Note 3
Common Mode Return Loss (SCC22)	-	-2	dB	From 250 MHz to f_b GHz See Note 3
Transition Time	9.5		ps	See 16.C.4.1
Near-end Eye Width at 10^{-6} probability (EW6)	0.265	-	UI	See 16.3.10 See Note 4
Near-end Eye Height at 10^{-6} probability (EH6)	70	-	mV	See 16.3.10 See Note 4
Far-end Eye Width at 10^{-6} probability (EW6)	0.20	-	UI	See 16.3.10 See Note 4
Far-end Eye Height at 10^{-6} probability (EH6)	30	-	mV	See 16.3.10 See Note 4
Near-end Eye Linearity	0.85	-	-	See Equation (16-14) See Note 4

NOTES:
1. Vcm is defined in Table 1-2 of Section 1.6
2. Vcm is generated by the host. Specification includes effects of ground offset voltage.
3. S-parameter specifications based on a differential reference impedance of 100 Ω and a common mode reference impedance of 25 Ω
4. Open eye is generated through the use of a reference Continuous Time Linear Equalizer (CTLE) applicable to all three PAM4 eyes (See Section 16.3.10.4)

Table 16-5. Module-to-Host Electrical Specifications (host input)

Parameter	Test Point	Min.	Max.	Units	Conditions
Overload Differential Voltage pk-pk	TP4	900	-	mV	See 16.3.11
Differential Termination Resistance Mismatch	TP4a	-	10	%	At 1 MHz. See 16.3.6
Differential Return Loss (SDD11)	TP4a	-	Equation (16-1)	dB	See Note 1
Differential Mode to Common Mode Conversion (SCD11)	TP4a	-	Equation (16-2)	dB	See Note 1
Stressed Input Test	TP4	See 16.3.10.3			
Common Mode Voltage (Vcm)	TP4a	-0.3	2.8	V	See Note 2, 3

NOTES:
1. S-parameter specifications based on a differential reference impedance of 100 Ω and a common mode reference impedance of 25 Ω
2. Vcm is defined in Table 1-2 of Section 1.6
3. Referred to host ground. Common mode voltage is generated by host

Table 16-6. Crosstalk parameters for module output test and host stressed input test calibration at TP1a

Parameter	Target value	Units	Conditions
Crosstalk Amplitude differential voltage pk-pk	900	mV	
Crosstalk Slew Time (between -270 mV and +270 mV)	19	ps	See Note 1

NOTES:
1. See Section 16.C.4.1 Transition Time and Slew Time

16.3.4 Output Differential Voltage, pk-pk

The differential voltage, pk-pk, (see Section 1.6.1 for definition of differential voltage pk-pk) shall meet the specifications given in Table 16-1 or Table 16-4 for the respective communication direction. Host and module Tx FIRs are likely to be required to meet TP1a and far-end TP4 eye requirements respectively for high loss channels. AC coupling is required in the module for both Tx and Rx. The waveform is observed through a fourth-order Bessel-Thomson response with a 3-dB bandwidth of 40 GHz using a QPRBS13-CEI pattern (see Appendix 16.C.3.1).

16.3.5 Common Mode Noise

See Section 12.3. The oscilloscope bandwidth shall be 40 GHz.

16.3.6 Differential Termination Resistance Mismatch

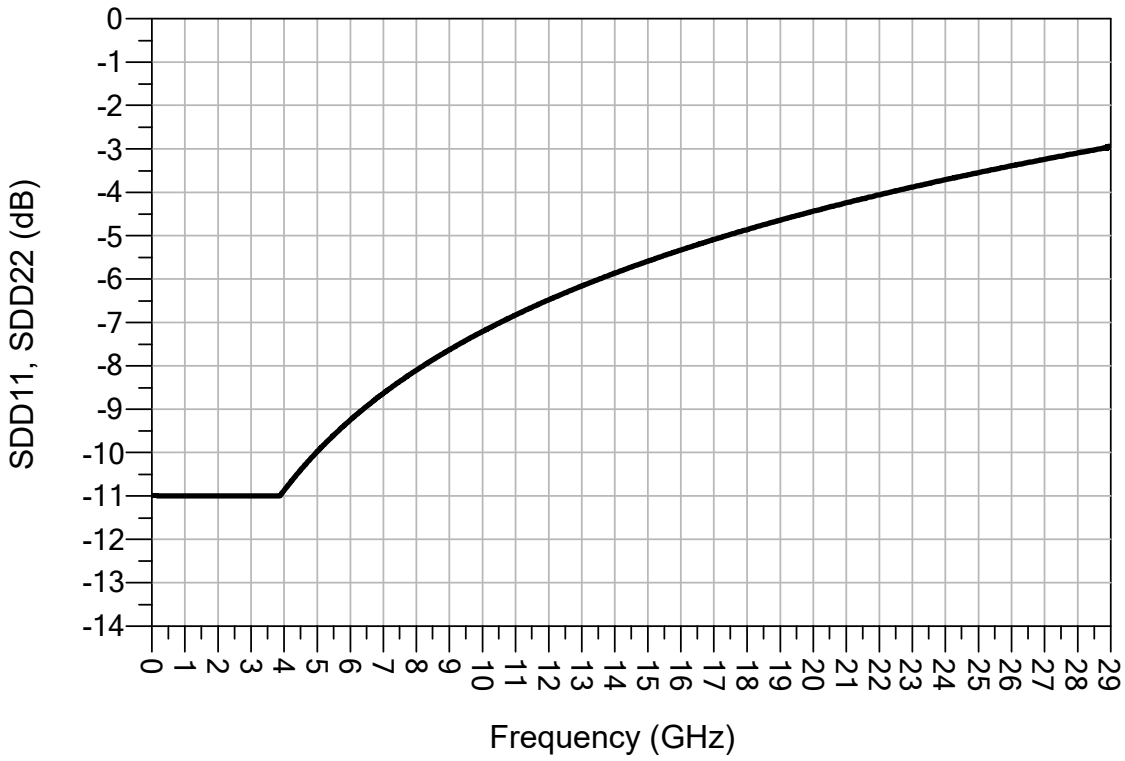
See Section 13.3.6.

16.3.7 Differential Return Loss

When measured at the respective test point the differential return loss shall not exceed the limits given in Equation (16-1) (illustrated in Figure 16-2 for f_b=29.0 GHz).

All return loss measurements require that the relevant input or output be active. For transmitter return loss measurements a QPRBS13-CEI pattern shall be used.

Figure 16-2. SDD11, SDD22 for host output (TP1a), host input (TP4a), module input (TP1) and module output (TP4) (for f_b = 29 GHz)



The test points are TP1a for host output, TP4a for host input, TP1 for module input and TP4 for module output.

$$\text{SDD11, SDD22} < -11\text{dB} \quad \text{for } 0.05 < f < f_b/7.5$$

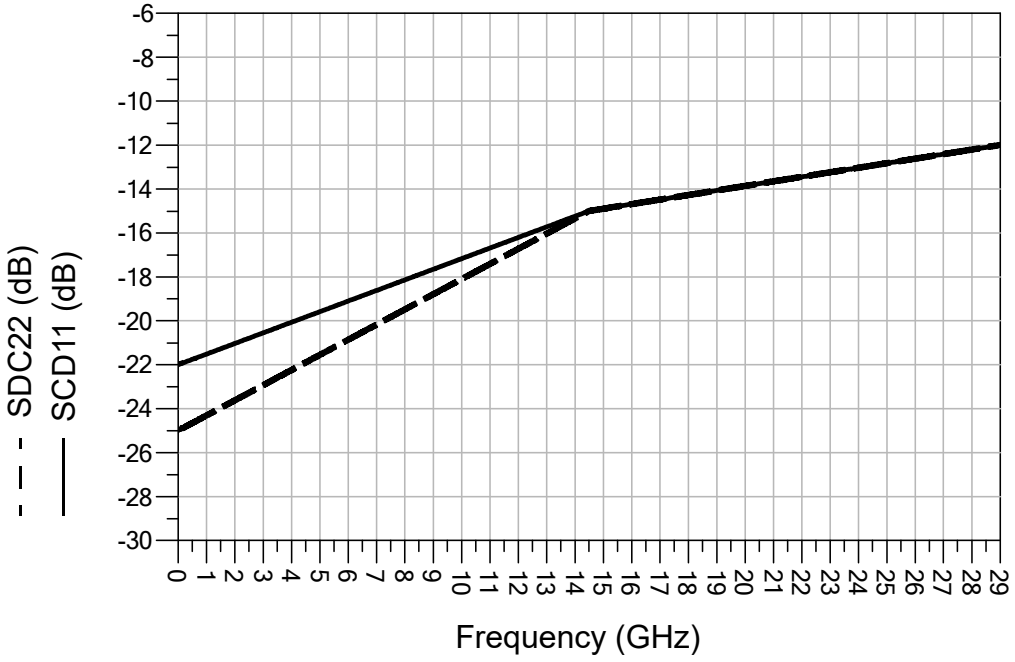
$$\text{SDD11, SDD22} < -6.0+9.2*\log_{10}\left(\frac{15}{7}\frac{f}{f_b}\right)\text{dB} \quad \text{for } f_b/7.5 < f < f_b \qquad (16\text{-}1)$$

16.3.8 Common to differential mode and differential to common mode conversion

The common to differential mode and differential to common mode conversion specifications are intended to limit the amount of unwanted signal energy that is allowed to be generated due to conversion of common mode voltage to differential mode voltage or vice versa.

When measured at the respective input test point, differential to common mode conversion shall not exceed the limits given in Equation (16-2) (illustrated in Figure 16-3 for f_b=29 GHz).

Figure 16-3. SCD11 for module input (TP1) and host input (TP4a), and SDC22 for module output (TP4) and host output (TP1a) (for f_b=29 GHz)



$$\begin{aligned} SCD11 &< -22+14*(f/f_b)dB \quad \text{for } 0.05 < f < f_b/2 \\ SCD11 &< -18+6*(f/f_b)dB \quad \text{for } f_b/2 < f < f_b \end{aligned} \tag{16-2}$$

When measured at the respective output test point, common to differential mode conversion shall not exceed the limits given in Equation (16-3) (illustrated in Figure 16-3 for f_b=29 GHz).

$$\begin{aligned} SDC22 &< -25+20*(f/f_b)dB \quad \text{for } 0.05 < f < f_b/2 \\ SDC22 &< -18+6*(f/f_b)dB \quad \text{for } f_b/2 < f < f_b \end{aligned} \tag{16-3}$$

16.3.9 Common Mode Return Loss

The common mode output return loss specification is intended to limit the amount of common mode energy that can be reflected by the host and module outputs. This has an effect on EMI radiation and differential mode signals generated via common mode to differential mode conversion. The common mode to differential mode conversion specification for the host and module outputs is more stringent than for the inputs to take into account the lack of a common mode input return loss specification.

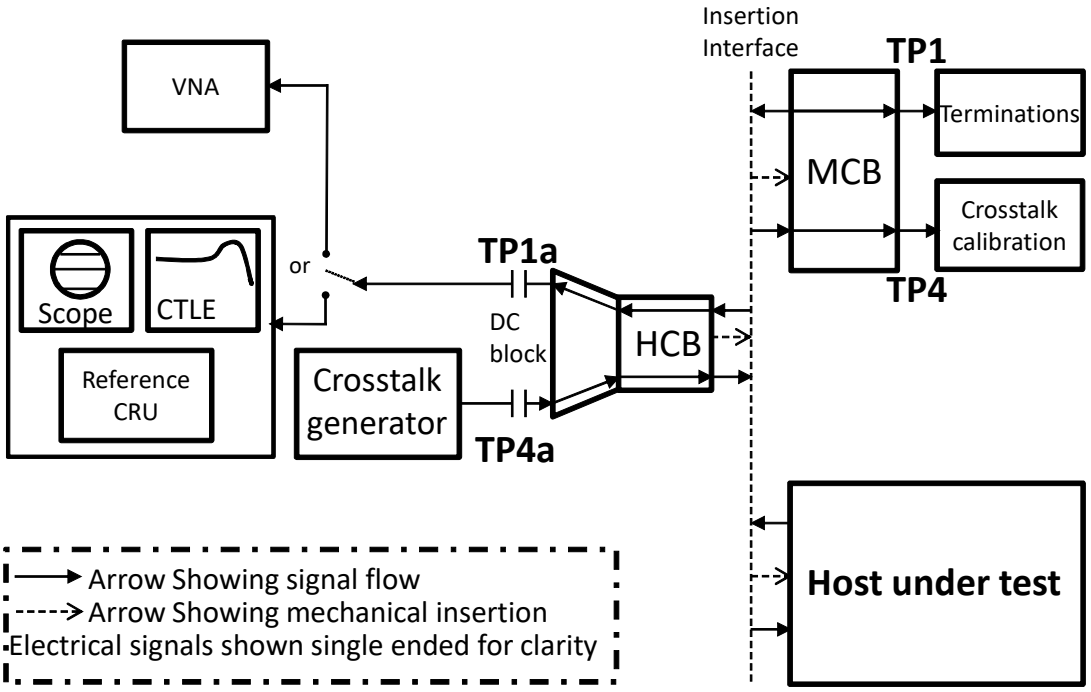
16.3.10 Eye Width, Eye Height and Stressed Input tests

Eye Width and Eye Height are specified in Table 16-1 (host output) and Table 16-4 (module output). Compliance is verified using the test setup shown in Figure 16-4 (host) and Figure 16-5 (module). The Eye Width and Eye Height correspond to eye contours at a probability of 10^{-6} to be consistent with those generated by simulator and oscilloscopes based on CDF/histogram data. The 10^{-6} eye contours are constructed from each individual eye's contributing symbols. For example, the EH6/EW6 measurement could include a total of 32 million captured PAM4 symbols, at a rate of one sample per symbol, with 16 million samples per individual eye (with the two middle levels (i.e. +1/3 and -1/3) used for the outer eyes and the middle eye). The 10^{-6} vertical eye points would have 8 samples at the top of each of the sub-eyes and 8 samples at the bottom of each of the sub-eyes. The EW6 calculations would be based on 16 million edges for the middle eye and 12 million edges for the upper and lower eyes. The 10^{-6} horizontal eye points would have 8 samples at the left edge of the middle eye and 8 samples at the right edge for the middle eye, and 6 samples at the left edge and 6 samples at the right edge for the upper and lower eyes. Compliance to the input specifications defined in Table 16-2 and Table 16-5 is verified using the test setup shown in Figure 16-9 (host) and Figure 16-10 (module).

16.3.10.1 Host and Module output Eye Width and Eye Height test

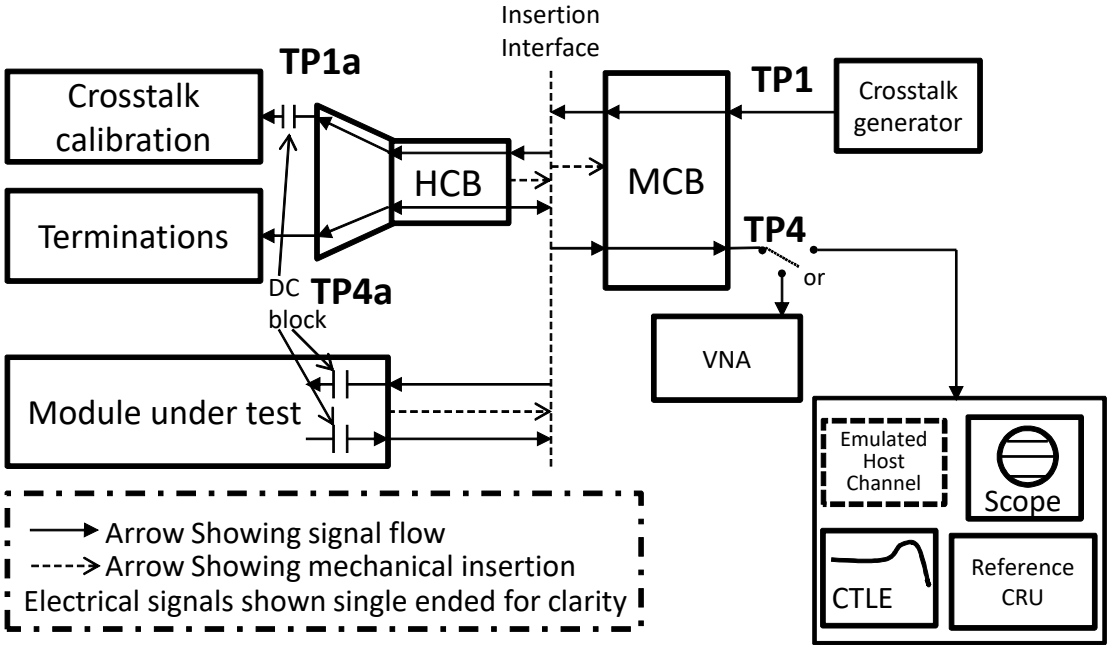
The host output Eye Width and Eye Height are measured at TP1a of Figure 16-1 using a Host Compliance Board as defined in Section 16.4.1. The test setup is shown in Figure 16-4.

Figure 16-4. Host output test setup



The module output Eye Width and Eye Height is tested at TP4 of Figure 16-1 using a Module Compliance Board as defined in Section 16.4.1. The test setup is shown in Figure 16-5.

Figure 16-5. Module output test setup



16.3.10.1.1 Host and Module output test method

The signal at TP1a may be a closed eye. Therefore, a reference receiver with a continuous time linear equalizer (CTLE) (see Section 16.3.10.4) is used to measure Eye Width and Eye Height. The reference receiver is also used to equalize the module output signal. The measured signal after the reference receiver shall meet the specifications listed in Section 16.3.2 for host to module and Section 16.3.3 for module to host. All co-propagating and counter-propagating lanes are active as crosstalk sources, using a QPRBS13-CEI test pattern as defined in Appendix 16.C.3.1, or a QPRBS31-CEI test pattern as defined in Appendix 16.C.3.2, or a valid CEI signal. The QPRBS13-CEI or QPRBS31-CEI patterns on all pairs of aggressor lanes should be asynchronous to each other or sufficiently delayed relative to each other to remove correlation between all pairs of aggressor lanes and between the lane under test and all aggressor lanes. Amplitude and Slew Times for counter-propagating lanes are defined in Table 16-3 and Table 16-6. It is recognized that practical implementations may have longer slew times than the target in Table 16-3.The lanes under test are asynchronous to the lanes in the opposing direction within the PPM offset defined by the protocol in use.

Note: Co- and counter-propagating crosstalk generators based on valid NRZ CEI signals could be used but may over-stress the system as crosstalk from such generators may be greater than from PAM4 generators.

The test method for measuring either host or module output Eye Width and Eye Height as illustrated in Figure 16-6 is as follows:

1) Set the host or module to QPRBS13-CEI pattern (see Appendix 16.C.3.1).

-This allows the use of a sampling oscilloscope with a pattern lock.

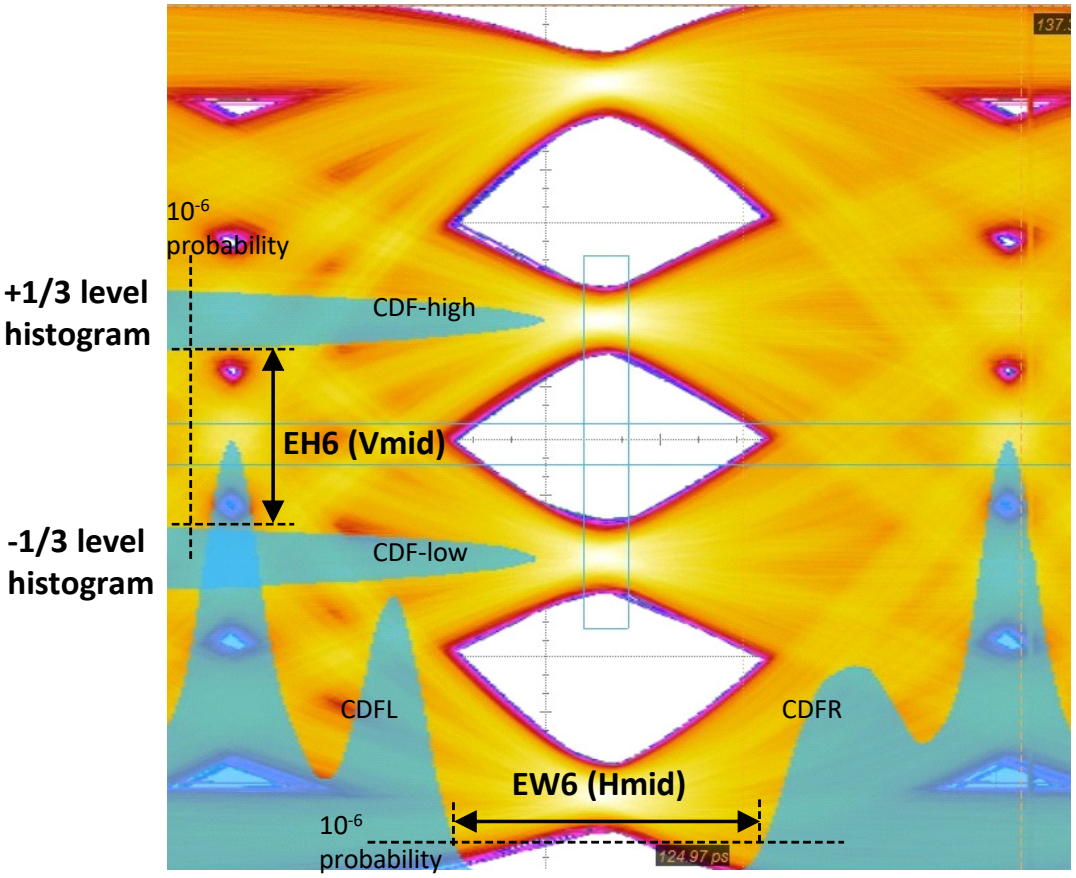
2) Capture the differential signal at TP1a or TP4 with a scope triggered with a clock from a reference clock recovery unit (CRU) with a first order transfer function with a 3 dB tracking bandwidth of $f_b/6640$.

-For TP1a, the scope shall be AC coupled.

-The reference CRU can be a software CRU in case of a real time scope.

-Sample the signal with a minimum of 3 samples per symbol or equivalent. Collect sufficient samples in order to construct normalized cumulative distribution functions (normalized CDFs) (see Figure 16-6) of the post-processed captured signals to a probability of 10^{-6} (without extrapolation) as described below. Depending on the sampling rate, careful interpolation using a method such as sin(x)/x or cubic spline may be needed for good accuracy.

Figure 16-6. TP1a and TP4 Eye Width and Eye Height parameters



3) Apply the reference receiver as defined in Section 16.3.10.4 to equalize the captured signal in step 2.

-For TP4 near-end compliance test, the CTLE peaking in the reference receiver shall be set at 1 dB, 1.5 dB or 2 dB. Any CTLE setting that meets both the EH6 and EW6 defined for TP4 in Table 16-4 is acceptable. EW6 is the minimum value from the set of Hlow, Hmid and Hupp measurements and likewise EH6 is the minimum value from the set of Vlow, Vmid and Vupp measurements (see Section 16.3.10.2 for these eye parameter definitions).

-For TP4 far-end compliance test, the signal measured at TP4 is first convolved with an emulated loss channel (~7 dB loss at $f_b/2$) that represents the worst case channel loss. The loss channel is a host trace having Z_p = (151 x 29.0/f_b) mm as defined below using Equation (16-4) to Equation (16-9) with the transmission line parameters listed in Table 16-7. The response of this channel is illustrated in Figure 16-14. The CTLE peaking in the reference receiver is then set to one of the seventeen CTLE values in Table 16-9. Any CTLE setting that meets both the EH6 and EW6 requirements defined for far-end TP4 in Table 16-4 is acceptable.

$$S_{11}(f) = S_{22}(f) = \frac{\rho(1 - \exp(-\gamma(f)2Z_p))}{1 - \rho^2 \exp(-\gamma(f)2Z_p)} \quad (16\text{-}4)$$

$$S_{21}(f) = S_{12}(f) = \frac{(1 - \rho^2)\exp(-\gamma(f)Z_p)}{1 - \rho^2 \exp(-\gamma(f)2Z_p)} \quad (16\text{-}5)$$

where,

$$\gamma(f) = \gamma_0 + \gamma_1\sqrt{f} + \gamma_2(f)f \quad (16\text{-}6)$$

$$\gamma_1 = a_1(1 + j) \quad (16\text{-}7)$$

$$\gamma_2(f) = a_2(1 - j(2/\pi)\ln f) + j2\pi\tau \quad (16\text{-}8)$$

$$\rho = \frac{Z_c - 2R_0}{Z_c + 2R_0} \quad (16\text{-}9)$$

with f in units of GHz in equations (16-4), (16-7), (16-7) and (16-8).

Table 16-7. Transmission Line Model Parameters and Values

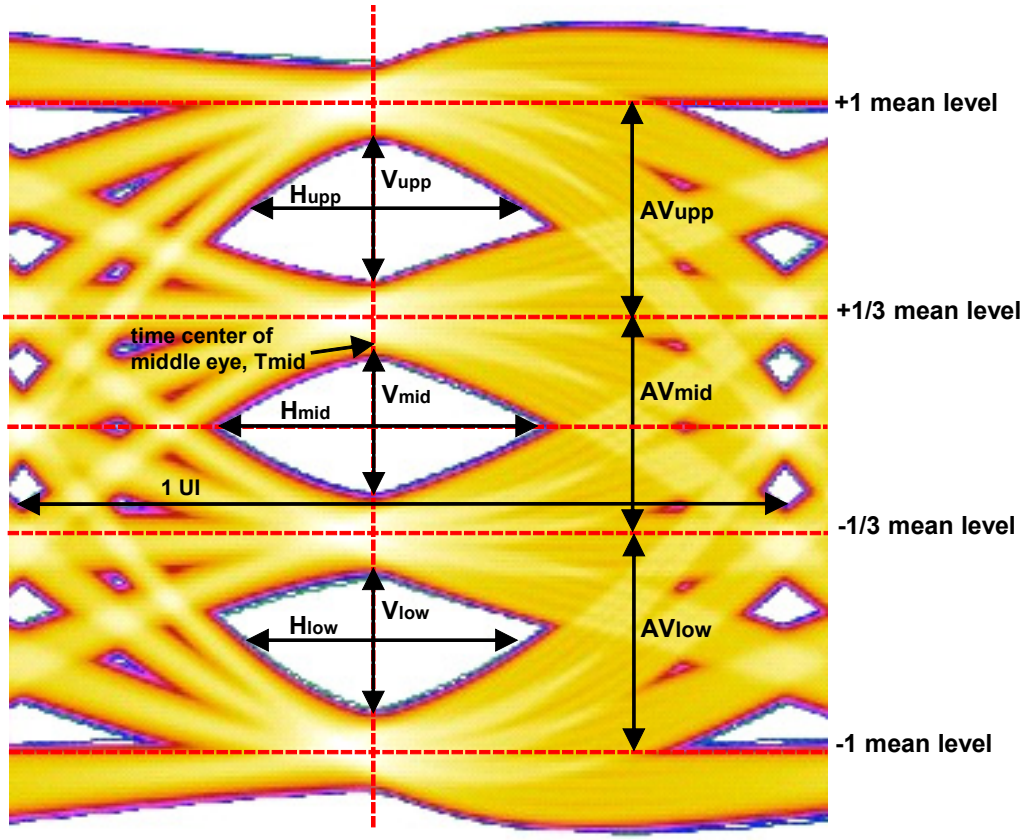
Parameter	Value	Units
Z_p	151 x 29.0/f_b	mm
γ_0	0	1/mm
a_1	4.114 x 10^{-4}	$ns^{1/2}$/mm
a_2	2.547 x 10^{-4}	ns/mm
τ	6.191 x 10^{-3}	ns/mm
Z_c	109.8	Ω
R_0	50.0	Ω

-For TP1a compliance test the CTLE peaking in the reference receiver shall be set to one of the seventeen CTLE values in Table 16-9. Any CTLE setting that meets both the EH6 and EW6 requirements defined for TP1a in Table 16-1 is acceptable. EH6 and EW6 have the same meaning as in the previous paragraph.

4) At TP1a, passing is defined as at least one equalizer setting that meets the EH6, EW6 and linearity specifications defined in Table 16-1 for the lower, upper and middle eyes. At TP4, passing is defined as at least one equalizer setting that meets the near-end EH6, EW6 and linearity specifications given in Table 16-4 and at least one potentially different equalizer setting that meets the far-end EH6 and EW6 specifications given in Table 16-4.

16.3.10.2 Measured PAM4 Eye Parameter Definitions

Figure 16-7. TP1a and TP4 Eye Width, Eye Height and Eye Amplitude



All relevant PAM4 eye parameters are determined from 10^{-6} contours generated from oscilloscope CDF/histogram data except for Tmid which is determined from a 10^{-3} contour of the middle eye.

The approach described in this clause is based upon first locating the midpoint (Tmid) of the middle eye's maximum horizontal eye opening and using that information to determine its vertical eye opening (Vmid) and the vertical eye opening of the upper and lower eyes, Vupp and Vlow, respectively based on the same time window. The midpoints of Vmid, Vupp and Vlow are used to determine Hmid, Hupp and Hlow respectively.

1. Tmid - the midpoint of the maximum horizontal eye opening of the 10^{-3} inner eye contour of the middle eye

2. Vmid - the 10^{-6} inner Eye Height of the middle eye determined from voltage CDFs in a +/- 0.025 UI time window centered on Tmid

3. Vupp - the 10^{-6} inner Eye Height of the upper eye determined from voltage CDFs in a +/- 0.025 UI time window centered on Tmid

4. Vlow - the 10^{-6} inner Eye Height of the lower eye determined from voltage CDFs in a +/- 0.025 UI time window centered on Tmid

5. AVmid, the Eye Amplitude of the middle eye, is the difference of the mean levels of the +1/3 level and -1/3 level voltage histograms in a +/- 0.025 UI time window centered on Tmid

6. AVupp, the Eye Amplitude of the upper eye, is the difference of the mean levels of the +1 level and +1/3 level voltage histograms in a +/- 0.025 UI time window centered on Tmid

7. AVlow, the Eye Amplitude of the lower eye, is the difference of the mean levels of the -1/3 level and -1 level voltage histograms in a +/- 0.025 UI time window centered on Tmid

8. Hmid - the 10^{-6} inner Eye Width determined from CDFs of eye edges half way between the 10^{-6} points of the voltage CDFs of the middle eye (Vmid/2)

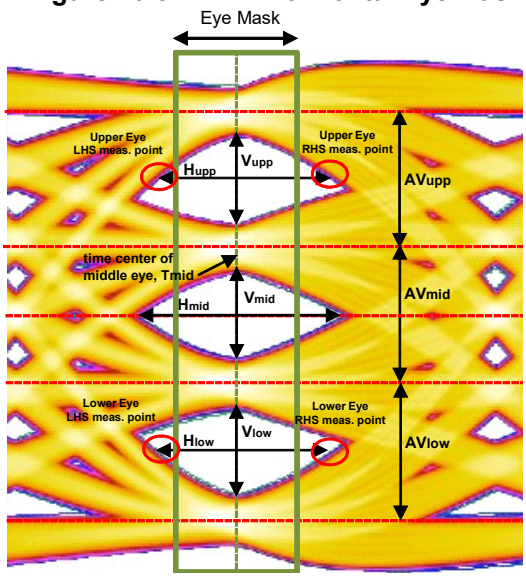
9. Hupp - the 10^{-6} inner Eye Width determined from CDFs of eye edges half way between the 10^{-6} points of the voltage CDFs of the upper eye (Vupp/2)

10. Hlow - the 10^{-6} inner Eye Width determined from CDFs of eye edges half way between the 10^{-6} points of the voltage CDFs of the lower eye (Vlow/2)

11. Create an Eye Width mask centered on Tmid having a width of EW6 from the relevant table (Table 16-1 or Table 16-4, as the case may be) which extends above and below the waveform for the upper and lower PAM4 eyes as shown in Figure 16-8.

12. The Hmid, Hupp and Hlow eye edges shall be outside this Eye Width mask

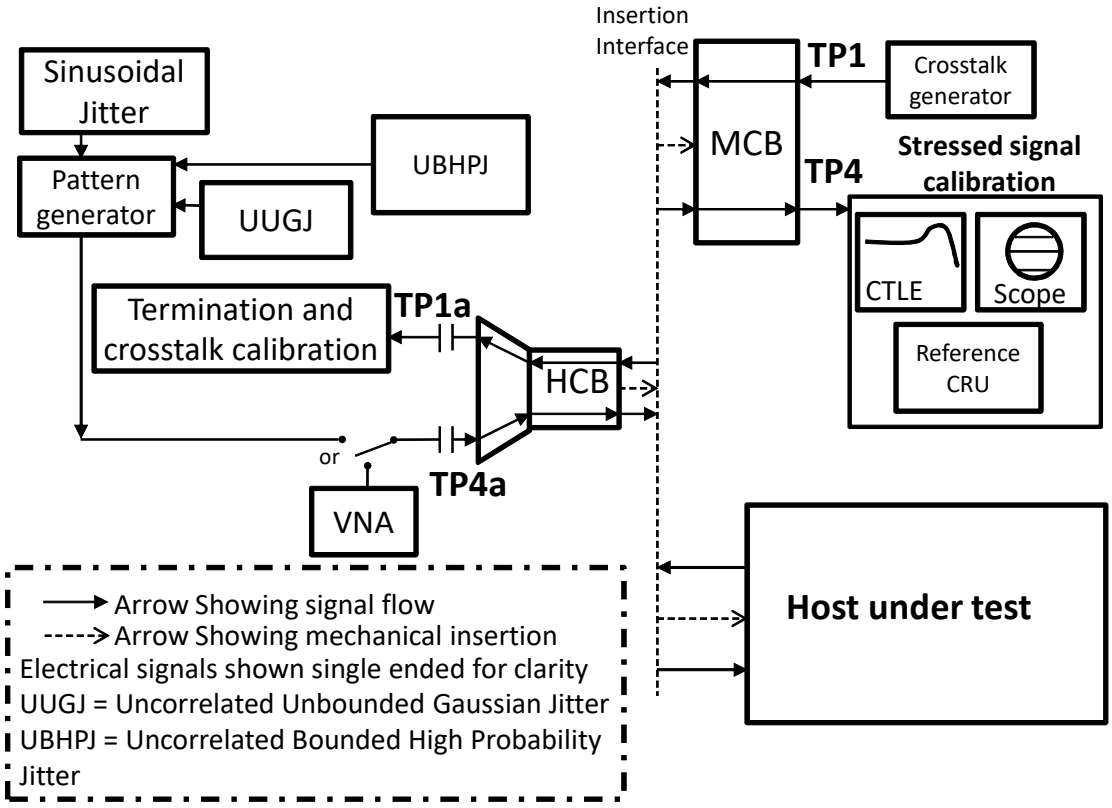
Figure 16-8. PAM4 Horizontal Eye Mask



16.3.10.3 Host and Module stressed input test

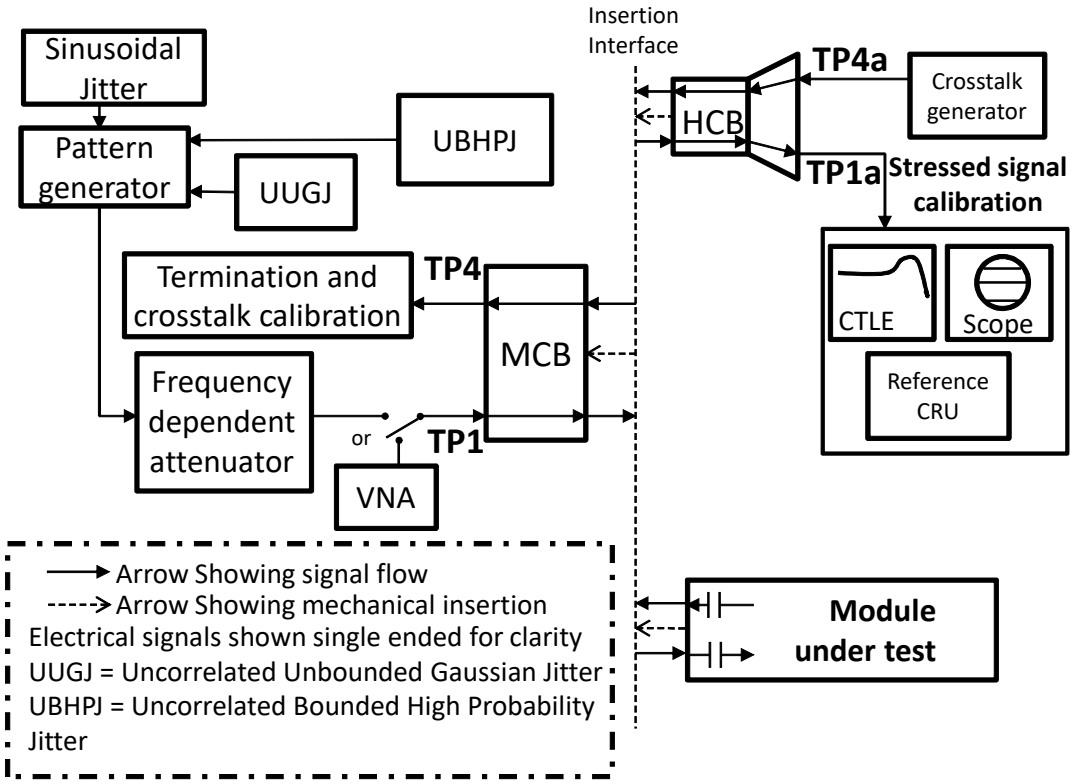
The ability of the host input to tolerate the Eye Width, Eye Height and Eye Linearity specified in Table 16-4 and the sinusoidal jitter specified in Table 16-8 is tested using a stressed input test. The test signal is applied at TP4a of Figure 16-1, and calibrated at TP4, using a Host Compliance Board and Module Compliance Board specified in Section 16.4.1 The test setup is shown in Figure 16-9. The UBHPJ block is used to create non-compensable DJ in addition to sinusoidal jitter.

Figure 16-9. Host input test setup



The ability of the module input to tolerate the Eye Width, Eye Height and Eye Linearity specified in Table 16-1 and the sinusoidal jitter specified in Table 16-8 is tested using a stressed input test. The test signal is applied at TP1 of Figure 16-1, and calibrated at TP1a using a Host Compliance Board and Module Compliance Board specified in Section 16.4.1. The test setup is shown in Figure 16-10. The module stressed input test represents the worst case high loss host. Modules are also expected to operate at the BER specified in Section 16.1 when presented with lower loss channels that require different CTLE settings as long as the signal complies with the specifications in Table 16-1. In contrast with CEI-28G-VSR the module input shall tolerate these various channels in an autonomous manner with no recommended equalization settings being provided by the host.

Figure 16-10. Module input test setup



16.3.10.3.1 Host (TP4a) and Module (TP1) stressed input test method

The host and module input shall tolerate sinusoidal jitter with the frequency and amplitude defined by the mask of Figure 16-11 and Table 16-8. This sinusoidal jitter is part of the jitter applied in the stressed input test. The sinusoidal jitter is calibrated at 10x the reference CRU's bandwidth. The stressed input test frequencies are $f_{CRU}/100$, $f_{CRU}/3$, f_{CRU}, $3f_{CRU}$, and $10f_{CRU}$, where f_{CRU} is the jitter corner frequency given by $f_b/6640$, with sinusoidal jitter of 5 UI, 0.15 UI, 0.05 UI, 0.05 UI and 0.05 UI respectively.

The reference CRU and reference receiver as defined in Section 16.3.10.4 are used to calibrate the stressed input test signal at TP4 (per Table 16-4) or TP1a (per Table 16-1) using a QPRBS13-CEI pattern. The pattern is changed to QPRBS31-CEI for the stressed input test.

The crosstalk source is asynchronous to the main pattern generator. The amplitude and slew time of the crosstalk source are given in Table 16-3 and Table 16-6. The crosstalk signal is calibrated at TP4 or TP1a using a QPRBS13-CEI pattern, then the pattern is changed to QPRBS31-CEI for the test. For multi-lane implementations additional lanes shall be active with either uncorrelated QPRBS31-CEI or QPRBS13-CEI patterns or valid CEI signals, using the above calibration methods.

Figure 16-11. Host input and Module input Sinusoidal Jitter

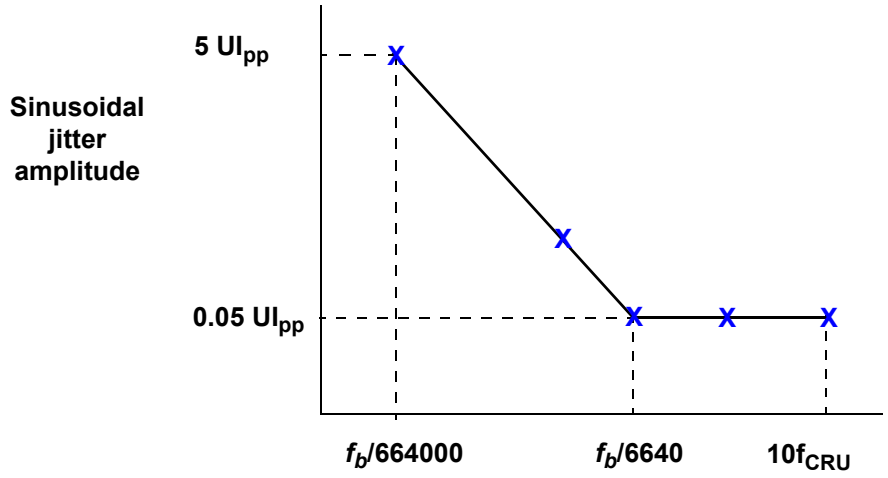


Table 16-8. Sinusoidal jitter frequency for TP4 and TP1a testing

Frequency Range	Sinusoidal jitter, peak-to-peak (UI)
f<f_b/664000	Not specified
f_b/664000 < f ≤ f_b/6640	5·f_b/(664000·f)
f_b/6640 < f ≤ 10f_{CRU}	0.05

16.3.10.3.1.1 Host input test signal calibration

The host input is tested at TP4a of Figure 16-1 using a Host Compliance Board as defined in Section 16.4.1. The host input test setup is shown in Figure 16-9.

UBHPJ, UUGJ and sinusoidal jitter are added to a clean test pattern until the jitter (except for EOJ) at the output of the pattern generator approximates the informative transmit recommendations given in Appendix 16.B.

With the crosstalk generator calibrated to meet the specifications in Table 16-6, the Far-end Eye Height and Far-end Eye Width at TP4 are measured using the reference receiver defined in Section 16.3.10.4 with the optimal CTLE peaking value from Figure 16-12 and the methodology defined in Section 16.3.10.1. The optimal CTLE peaking value is defined as the setting that results in the maximum value of EW6*EH6.

The UUGJ and pattern generator amplitude are adjusted to give the minimum far-end Eye Height and far-end Eye Width and minimum Eye Linearity specified for the module output in Table 16-4. The upper and lower PAM4 eyes are adjusted to be smaller than the middle eye and set to the minimum Eye Height and Eye Width requirement. This

calibrated signal must also equal or exceed the Near-end Eye Height and Near-end Eye Width in Table 16-4 measured using the reference receiver defined in Section 16.3.10.4 with one of the CTLE peaking values from Figure 16-13.

16.3.10.3.1.2 Module input test signal calibration

The module input is tested at TP1 of Figure 16-1 using a Module Compliance Board as defined in Section 16.4.1. The module input test setup is shown in Figure 16-10.

Sinusoidal jitter compliant to Table 16-8 and UUGJ are added to a clean test pattern until the jitter (except for EOJ) at the output of the pattern generator approximates the informative transmit recommendations given in Appendix 16.B. Note that the sinusoidal jitter provides the UBHPJ component including the effects of host transmitter crosstalk.

The frequency-dependent attenuator is intended to represent the host channel, and may be implemented with PCB traces. It should be chosen to result in a loss of 12.2 dB at Nyquist to TP1a from the output of a pattern generator having a nominal rise/fall time of 10.5 ps. (Cable or PCB loss may be added between the pattern generator and the test channel to produce the 10.5 ps rise/fall time, in which case the output of the cable or PCB is counted as the output of the pattern generator).The complete path from the output of the pattern generator to TP1a should also meet the return loss specifications given for the mated HCB and MCB (see sections 16.4.1 and 13.4.1.2). The crosstalk generator is calibrated to meet the specifications in Table 16-3. The Eye Height and Eye Width at TP1a are measured using the reference receiver (defined in Section 16.3.10.4) with the optimal CTLE peaking value and the methodology defined in Section 16.3.10.1. The optimal CTLE peaking value is defined as the setting that results in the maximum value of EW6*EH6. The pattern generator output is adjusted so that this optimal CTLE peaking value is greater than or equal to 7 dB.

The UUGJ and pattern generator amplitude are adjusted to give the minimum Eye Height and Eye Width and minimum Eye Linearity specified in Table 16-1.

The upper and lower PAM4 eyes are adjusted to be smaller than the middle eye and set to the minimum Eye Height and Eye Width requirement.

16.3.10.4 Reference receiver

The waveform is observed through a fourth-order Bessel-Thomson response with a bandwidth of 40 GHz concatenated with a Continuous Time Linear Equalizer (CTLE). The filters may be implemented in software; however, the signal is not averaged. The CTLE shall be implemented based on Equation (16-10) where G is the low-frequency gain and ZLF, Z1, PLF, P1 and P2 are the CTLE zero and poles coefficients. Figure 16-12 shows the frequency response of the reference equalizer used for module far-end and host output testing for baud rates between 25 and 29.0 Gsym/s with values for ZLF, Z1, PLF, P1 and P2 listed in Table 16-9. Figure 16-13 shows the frequency response of the reference equalizer used for module near-end output testing for baud rates between 25 and 29.0 Gsym/s with values for ZLF, Z1, PLF, P1 and P2 listed in Table 16-9. The CTLE is the same for baud rates between 25 and 29.0 Gsym/s. For

baud rates below 25 Gsym/s the values of ZLF, Z1, PLF, P1 and P2 should be multiplied by $f_b/28$. The CTLE peaking value is the approximate difference between the low-frequency response (1 MHz) and the maximum high-frequency response in dB.

$$H(f) = \frac{(G)(P1)(P2)(PLF)}{(Z1)(ZLF)} \frac{(jf + Z1)}{(jf + P1)(jf + P2)} \frac{(jf + ZLF)}{(jf + PLF)} \quad (16\text{-}10)$$

Figure 16-12. Host output reference equalizer (CTLE) transfer function for 1 dB to 9 dB of peaking at 25 Gsym/s

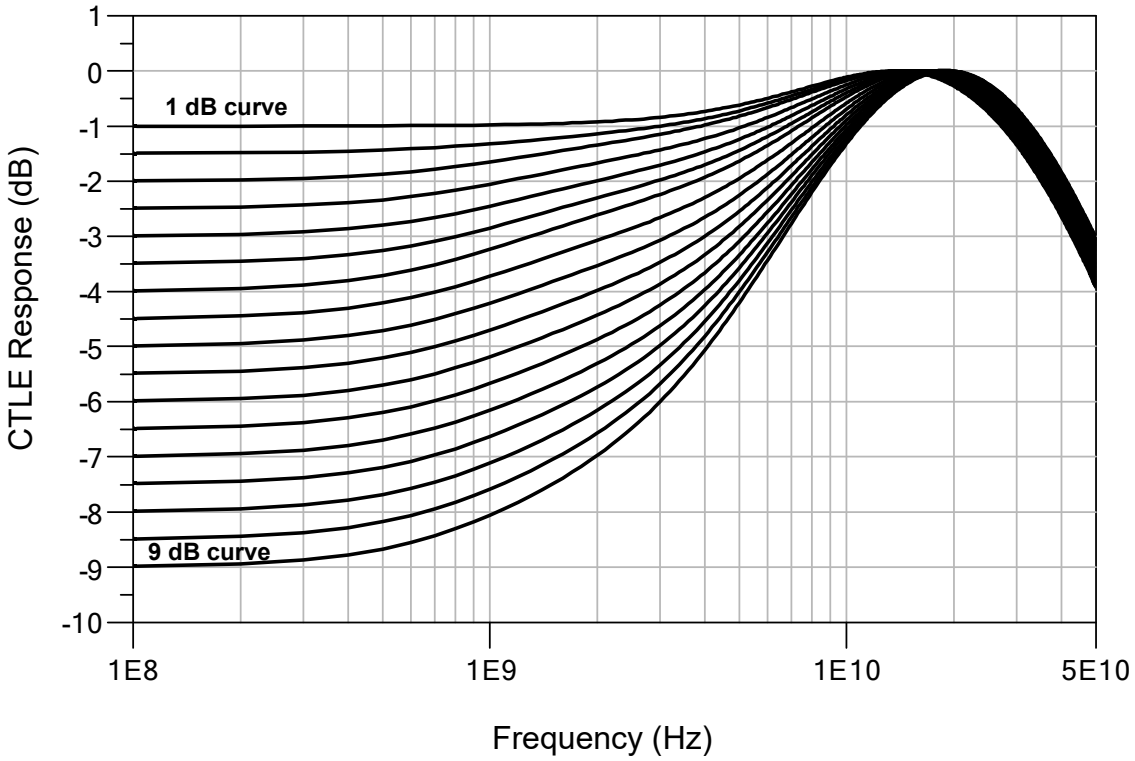


Figure 16-13. Module near-end output reference equalizer (CTLE) transfer function for 1 dB to 2 dB of peaking at 25 Gsym/s

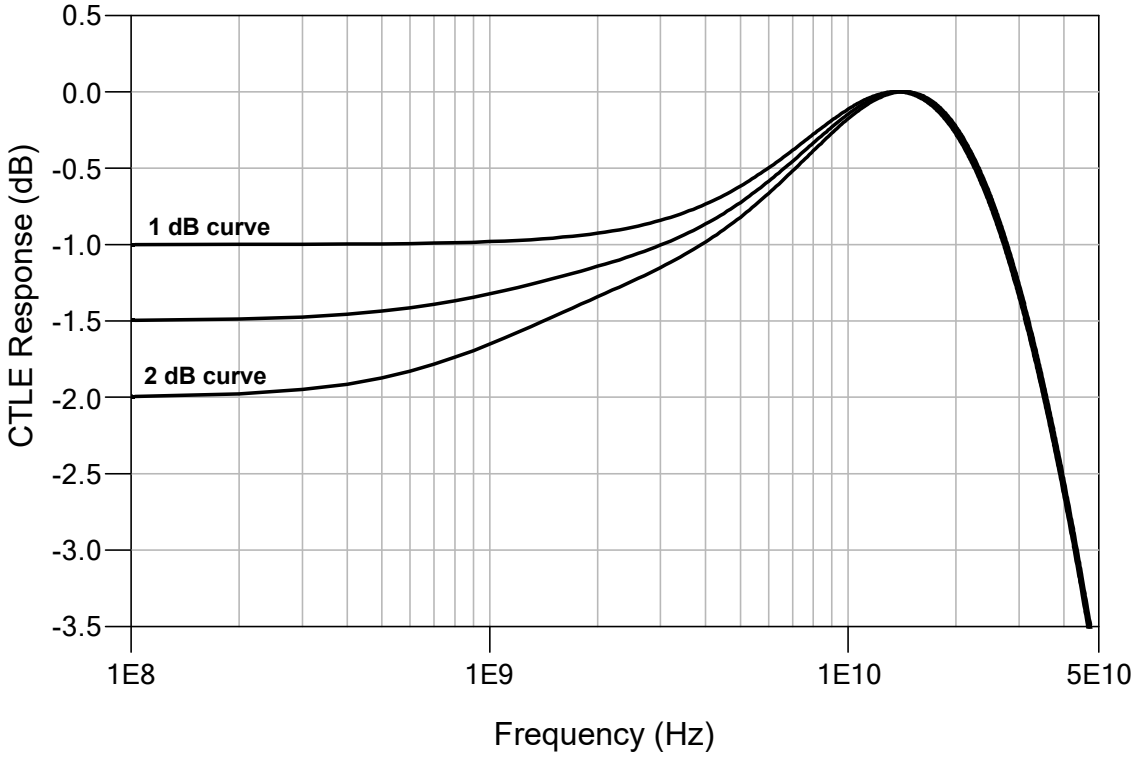


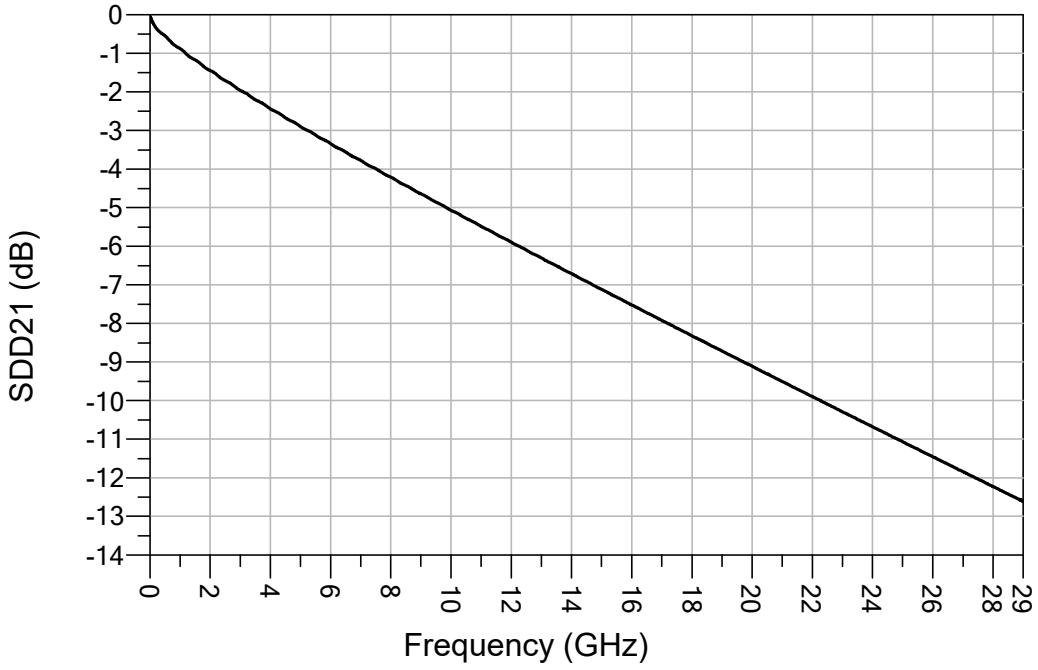
Table 16-9. Reference equalizer coefficients for rates of 25 Gsym/s and above

Peaking (dB)	G	P1 (GHz)	P2 (GHz)	Z1 (GHz)	PLF (GHz)	ZLF (GHz)
1	0.891251	26.5625	14.1	9.463748	1.2	1.2
1.5	0.841395	26.5625	14.1	9.248465	1.2	1.15
2	0.794328	26.5625	14.1	9.069645	1.2	1.1
2.5	0.749894	26.5625	14.1	8.640319	1.2	1.075
3	0.707946	26.5625	14.1	8.255665	1.2	1.05
3.5	0.668344	26.5625	14.1	7.906766	1.2	1.025
4	0.630957	26.5625	14.1	7.587650	1.2	1
4.5	0.595662	26.5625	14.1	7.076858	1.2	1
5	0.562341	26.5625	14.1	6.614781	1.2	1
5.5	0.530884	26.5625	14.1	6.193091	1.2	1
6	0.501187	26.5625	14.1	5.805801	1.2	1
6.5	0.473151	26.5625	14.1	5.448395	1.2	1
7	0.446684	26.5625	14.1	5.117337	1.2	1

Peaking (dB)	G	P1 (GHz)	P2 (GHz)	Z1 (GHz)	PLF (GHz)	ZLF (GHz)
7.5	0.421697	26.5625	14.1	4.809777	1.2	1
8	0.398107	26.5625	14.1	4.523367	1.2	1
8.5	0.375837	26.5625	14.1	4.256129	1.2	1
9	0.354813	26.5625	14.1	4.006377	1.2	1

The TP4 far-end module output test uses the emulated host channel specified in Section 16.3.10.1.1 with insertion loss represented by SDD21 as shown in Figure 16-14.

Figure 16-14. TP4 Far-end Host Channel SDD21 for f_b = 29 GHz



16.3.11 Input Overload Voltage Tolerance

The input voltage tolerance tests the acceptance of differential input pk-pk amplitudes produced by the extremes of operation from the host output (for host-to-module communication) or module output (for module-to-host communication).

The maximum voltage at an IC input can be larger than the maximum at the compliance point due to output/input impedances and reflections.

The input overload voltage tolerance specification is to be met for any valid CEI pattern. The differential voltage specified in Table 16-1 is somewhat smaller than the module input voltage tolerance due to host loss and the QPRBS13-CEI's pattern length.

16.4 Measurement methods

16.4.1 Compliance Boards

Use of compliance boards for testing is assumed for the parameters defined in Table 16-1 through Table 16-6. The test results for test and calibration at TP1a should be corrected for any deviations between the Host Compliance Board's loss and the Host Compliance Board's reference loss given in Section 13.4.1.1. The test results for test and calibration at TP4 should be corrected for any deviations between the mated compliance board loss minus the Host Compliance Board's loss and the mated compliance board reference loss (given in Section 16.4.1.1) minus the Host Compliance Board's reference loss given in Section 13.4.1.1.

Figure 16-1 shows the test setup for making S-parameter measurements of the mated compliance boards.The requirements in this section are not connector specifications for an implemented design. The compliance boards are as defined in Section 13.4 with the exceptions that their specifications are extended from 28.1 GHz to 29.0 GHz, and other exceptions in Section 16.4.1.1.

16.4.1.1 Mated HCB and MCB S-parameters

The reference mated MCB-HCB loss is given in Equation (16-11).

$$\mathrm{SDD21,SDD12} = (-0.475)\sqrt{f} - 0.1204f - 0.002f^2 \quad \text{(16-11)}$$

for 0.05 GHz < f < 29.0 GHz, where f is frequency in GHz, loss in dB.

The FOM_{ILD} (as calculated using the method defined in Section 10.2.6.4 and the curve fit method defined in Clause 12 with f_{ILmax} of 21.75 GHz and f_{ILmin} of 50 MHz) for the mated HCB and MCB pair is ≤ 0.1 dB.

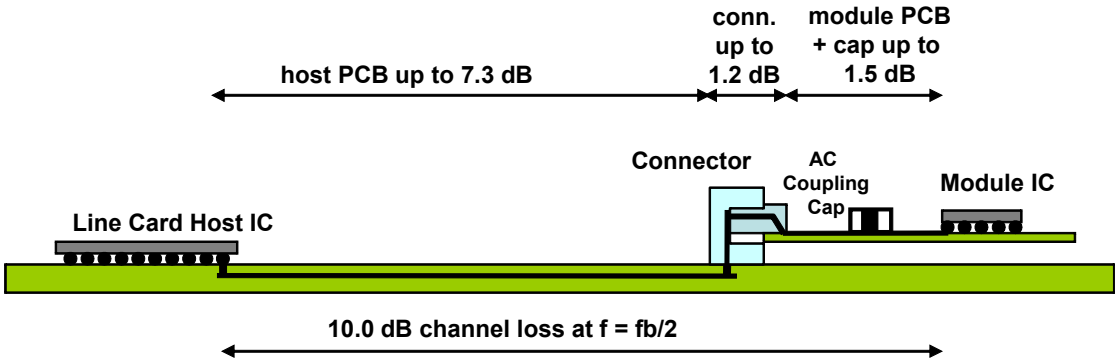
Note: FOM_{ILD} is called ILD_{rms} in OIF-CEI-03.0 clauses 10 & 11 and OIF-CEI-03.1 clauses 10, 11, 13 & 14.

The Integrated Crosstalk Noise (ICN) as calculated using the method defined in Clause 12 with the aggressor amplitudes and rise/fall times as listed in Table 16-3 shall be less than 3.9 mV RMS. MDNEXT shall be less than 1.35 mV RMS. MDFEXT shall be less than 3.6 mV RMS.

16.A Appendix - Recommended Electrical Channel

The channel consists of Host PCB trace, Module PCB trace, vias, AC coupling capacitor and one connector, not in this order. The recommended PCB trace differential impedance is 100 ± 10 Ω. This full channel model is shown in Figure 16-15 below. Note that in practice the channel is not measurable as appropriate test points are not accessible.

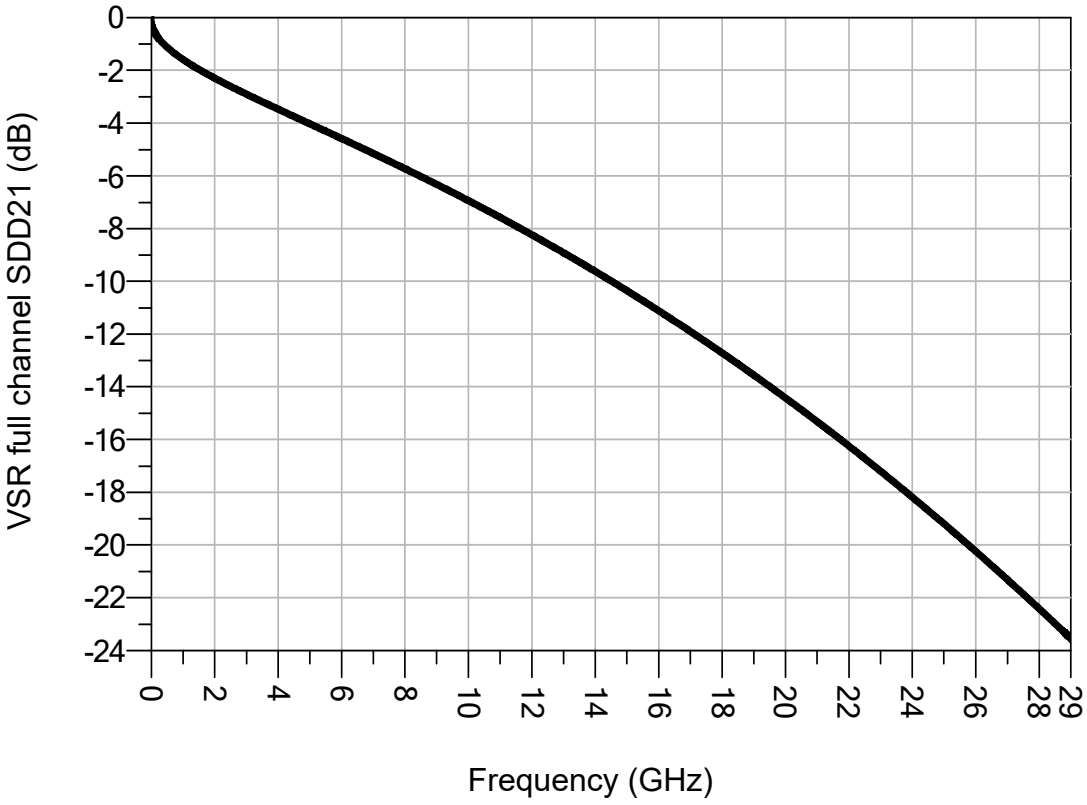
Figure 16-15. CEI-56G-VSR-PAM4 Channel Reference Model



16.A.1 Insertion Loss

Host insertion loss and module insertion loss are recommended limits only. Achieving these recommended limits does not signify compliance nor guarantee successful communication between two devices. Equation (16-12) (illustrated in Figure 16-16) represents the highest recommended insertion loss (see SDD21) of the end-to-end channel.

Figure 16-16. Recommended minimum SDD21 of the end-to-end channel (for f_b = 29 GHz)



$$H(f) = a_0 + a_1\sqrt{\frac{f}{f_b}} + a_2\frac{f}{f_b} + a_4\left(\frac{f}{f_b}\right)^2 \quad (16\text{-}12)$$

where a_0 = -0.1, a_1 = -7.51, a_2 = -2.38, a_4 = -13.56

In addition it is recommended that the VSR channel have an FOM_{ILD} less than or equal to 0.3 dB.

Note: FOM_{ILD} is called ILD_{rms} in OIF-CEI-03.0 clauses 10 & 11 and OIF-CEI-03.1 clauses 10, 11, 13 & 14.

16.B Appendix - Informative Host Transmitter output Electrical Recommendations

Informative host Tx output recommendations are defined in Table 16-10.

16.B.1 Host Transmitter output test point

Figure 16-1 gives the reference model and test points associated with host-to-module and module-to-host CEI-56G-VSR-PAM4 lanes. The informative host transmitter output electrical recommendations are defined to be measured at TP0a. TP0a is defined to be separated from TP0, the ball of the package performing the host-to-module transmit function, by 1 dB of PCB attenuation at 14 GHz.

16.B.1.1 Host-to-Module transmitter output Electrical Recommendations

It is recommended that each host-to-module lane meet the limits of Table 16-10.

Table 16-10. Host-to-Module Electrical Recommendations at TP0a

Parameter	Symbol	Min.	Max.	Units	Conditions
Baud Rate		18.0	29.0	Gsym/s	
Differential Voltage, pk-pk	T_Vdiff	750	-	mV	See Note 1
DC Common Mode Voltage	T_Vcm	-0.3	2.8	V	See Note 2
Differential Termination Resistance Mismatch	T_Rdm	-	10	%	at 1 MHz
Differential Return Loss	T_SDD22	-	Equation (17-4)	dB	at TP0
Transition Time: 20% to 80%	T_tr, T_tf	7.5	-	ps	With emphasis off
Common-mode return loss	T_SCC22	-6 + 3*f/f_b	-	dB	
Common Mode Noise, RMS	T_Ncm	-	12	mV	
Uncorrelated Jitter RMS (standard deviation of the probability distribution)	T_J_{RMS}		0.023	UI_{RMS}	See Note 3
Uncorrelated Jitter (time interval from 0.005% to 99.995% of the probability distribution)	T_J_{4u}		0.118	UI	See Note 3
Even-Odd Jitter	T_EOJ		0.019	UI	See Note 3
Signal-to-noise-and-distortion ratio		31	-	dB	See Section 17.3.1.6.4 for definition

NOTES:
1. Max voltage is limited by specifications at TP1a. Minimum voltage can be lower for low loss channels.
2. Load type 0 with min. T_Vdiff, AC-Coupling or floating load.
3. Measured as described in Section 17.3.1.7.

It is unlikely that all TP1a requirements of Table 16-1 can be met simultaneously with maximum channel insertion loss and the worst-case limits of Table 16-10.

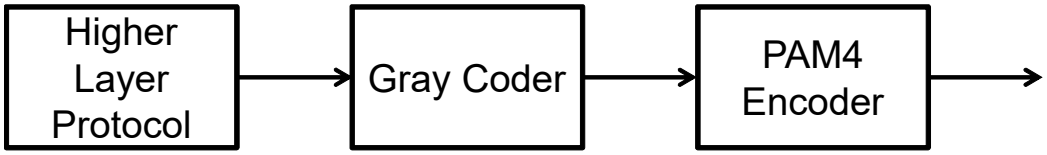
16.C Appendix - General PAM4 Requirement

This annex contains normative requirements for PAM4 signaling and includes information relevant to all of the CEI-56G PAM4 clauses.

16.C.1 Transmit Functional Requirements

In the transmit direction, the role of the TX is to map the signal from the higher layer protocol to a PAM4 encoded signal to be passed to the physical channel for transfer. The mapping process shown in Figure 16-17 includes application of Gray coding followed by PAM4 encoding.

Figure 16-17. Transmit signaling and mapping diagram



16.C.1.1 Gray Coding

The TX signaling process shall map consecutive pairs of bits to one of four Gray-coded symbols as specified in this subclause. Each pair of bits, (A, B) of digital input bits are converted to a Gray-coded symbol with one of the four Gray-coded levels as follows: (0, 0) maps to 0, (0, 1) maps to 1, (1, 1) maps to 2, and (1, 0) maps to 3. The “A” bit is the first bit received.

16.C.1.2 PAM4 Encoding

The TX transmit process shall encode each Gray coded output symbol to one of four PAM4 levels as specified in this subclause.

Mapping from the Gray coder output to a PAM4 encoded symbol is as follows:

0 maps to –1,

1 maps to –1/3,

2 maps to +1/3, and

3 maps to +1.

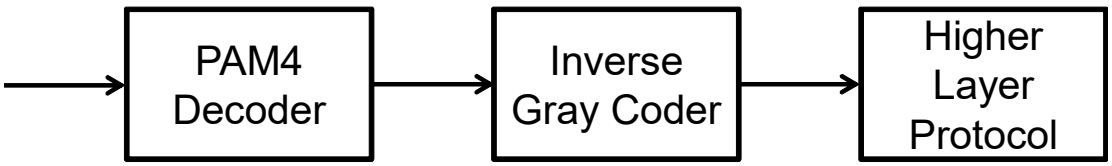
16.C.1.3 Optional Precoding

Certain systems susceptible to DFE burst errors, such as those based on MR and LR PAM4 interfaces, may take advantage of a simple per lane precoding block implementing a 1/(1+D) modulo 4 function following the Gray coder, where D is defined as 1 UI of delay at the baud rate.

16.C.2 Receive Functional Requirements

The receive process shall recover the data generated by the transmit process. In the receive direction, the role of the RX is to unmap the PAM4 encoded signal to the higher layer protocol. The mapping processes shown in Figure 16-18 includes application of PAM4 decoding followed by inverse Gray coding.

Figure 16-18. Receive signaling and mapping diagram



16.C.2.1 Optional Precoding Decoder

Systems that have the optional precoding block are required to have a precoding decoder block located before the inverse Gray coder which implements a (1+D) modulo 4 function, where D is defined as 1 UI of delay at the baud rate. Such systems should be able to bypass this decoder function in order to be compatible with non-precoder based systems.

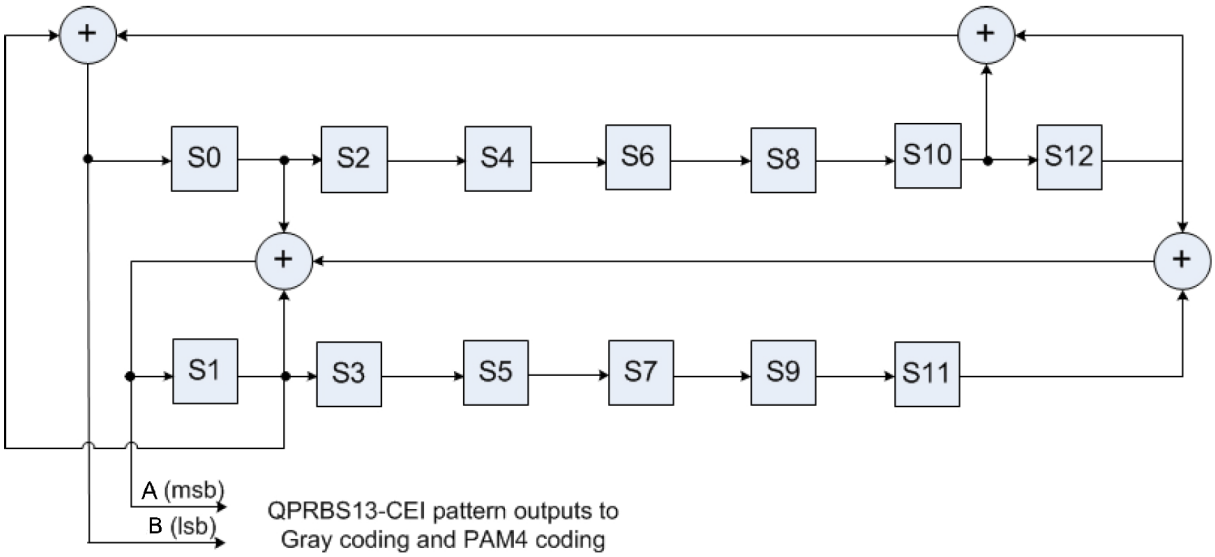
16.C.3 Test Patterns

16.C.3.1 Quaternary PRBS13 test pattern - QPRBS13-CEI

The QPRBS13-CEI test pattern is the 4-level pattern created by encoding a repeating PRBS13 pattern as defined in this paragraph using the Gray coding and PAM4 encoding described in this Annex. Each cycle of QPRBS13-CEI is 8191 symbols long. The QPRBS13-CEI pattern generator produces the same result as the implementation shown in Figure 16-19, which implements the generator polynomial shown in Equation (16-13). If multiple test patterns are required at one time, they shall not be aligned (for example, by use of different seeds or delays).

$$G(x) = 1 + x + x^2 + x^{12} + x^{13} \quad (16\text{-}13)$$

Figure 16-19. QPRBS13-CEI pattern generator



16.C.3.2 Quaternary PRBS31 test pattern - QPRBS31-CEI

The QPRBS31-CEI test pattern is the 4-level pattern created by encoding the PRBS31 test pattern defined in [21] using the Gray Coding and PAM4 encoding described in this Annex.

16.C.4 PAM4 Signal Parameters

16.C.4.1 Transition Time and Slew Time Based on the QPRBS13-CEI Test Pattern

Transition times (rise and fall times) are defined as the time between the 20% and 80% times, or 80% and 20% times, respectively, of isolated -1 to +1 or +1 to -1 PAM4 edges. Slew times are defined as the time interval between the times at defined voltages. Using the QPRBS13-CEI test pattern the transitions within sequences of three -1s followed by three +1s, and three +1s followed by three -1s, respectively, are measured. These are PAM4 symbols 1820 to 1825 and 2086 to 2091, respectively, where symbols 1 to 7 are the run of seven +1s. In this case, the 0% level and 100% level may be estimated as the average signal within windows from -1.5 UI to -1 UI and from 1.5 UI to 2 UI relative to the edge.

The waveform is observed through a fourth-order, low-pass Bessel-Thomson filter response having a 3-dB bandwidth of 40 GHz.

16.C.4.2 Eye Linearity and Vertical Eye Closure (VEC)

Eye Linearity is a metric based upon PAM4 eye parameters as determined from contours generated from oscilloscope CDF/histogram data as described in Section 16.3.10. Eye Linearity is calculated according to Equation (16-14).

$$\text{Eye Linearity} = \frac{\min(AVupp, AVmid, AVlow)}{\max(AVupp, AVmid, AVlow)} \quad (16\text{-}14)$$

Vertical Eye Closure (VEC) is calculated according to Equation (16-15). This is used for host output only.

$$VEC = 20\log_{10}(\max[AVupp/Vupp, AVmid/Vmid, AVlow/Vlow]) \quad (16\text{-}15)$$

16.C.4.3 Transmitter Linearity

Transmitter linearity is defined as a function of the mean signal level transmitted for each PAM4 symbol. Given the PAM4 symbols -1, -1/3, +1/3, and +1, the mean signal level for each symbol are V_{-1}, $V_{-1/3}$, $V_{+1/3}$, and V_{+1} respectively. The calculation of the mean signal levels is defined below. The mid-range level Vmid is defined by Equation (16-16). The mean signal levels are then normalized and the signal offset is adjusted so that V_{-1} corresponds to -1, $V_{-1/3}$ to $-ES_1$, $V_{+1/3}$ to ES2, and V_{+1} to +1. ES_1 is defined by Equation (16-17) and ES_2 is defined by Equation (16-18). The level separation mismatch ratio R_{LM} is defined by Equation (16-19).

$$V_{mid} = (V_{-1} + V_{+1}) / 2 \quad (16\text{-}16)$$

$$ES_1 = (V_{-1/3} - V_{mid}) / (V_{-1} - Vmid) \quad (16\text{-}17)$$

$$ES_2 = (V_{+1/3} - V_{mid}) / (V_{+1} - Vmid) \quad (16\text{-}18)$$

$$R_{LM} = \min((3 \cdot ES_1), (3 \cdot ES_2), (2 - 3 \cdot ES_1), (2 - 3 \cdot ES_2)) \quad (16\text{-}19)$$

The mean signal levels described above are measured from a waveform captured while the transmitter is transmitting the QPRBS13-CEI test pattern. The waveform consists of M samples per unit interval and is aligned such that the first M samples of the waveform correspond to the first PAM4 symbol of the test pattern, the second M samples to the second PAM4 symbol, and so on. This allows each sample of the waveform to be associated with a specific PAM4 symbol in the test pattern.

Denote the number of PAM4 symbols in the test pattern as N. Reduce the captured waveform to N samples by choosing the central sample from each unit interval. The central sample is defined as the m^{th} sample in each unit interval where m is the integer closest to M / 2.

For each PAM4 symbol x, Vx is the mean value of the waveform samples that correspond to that symbol.

Note. Transmitter Linearity is not used in this clause but is used by other PAM4 clauses.

16.C.5 PAM4 Data Patterns

The PAM4 Implementation Agreements do not have any requirements for specific data patterns, data coding, or scrambling. However the following requirements are necessary to insure proper operation of a CEI PAM4 interface. If all of these conditions are not met, then the link may not work to the full distance, or meet the specified BER, or in fact work at all.

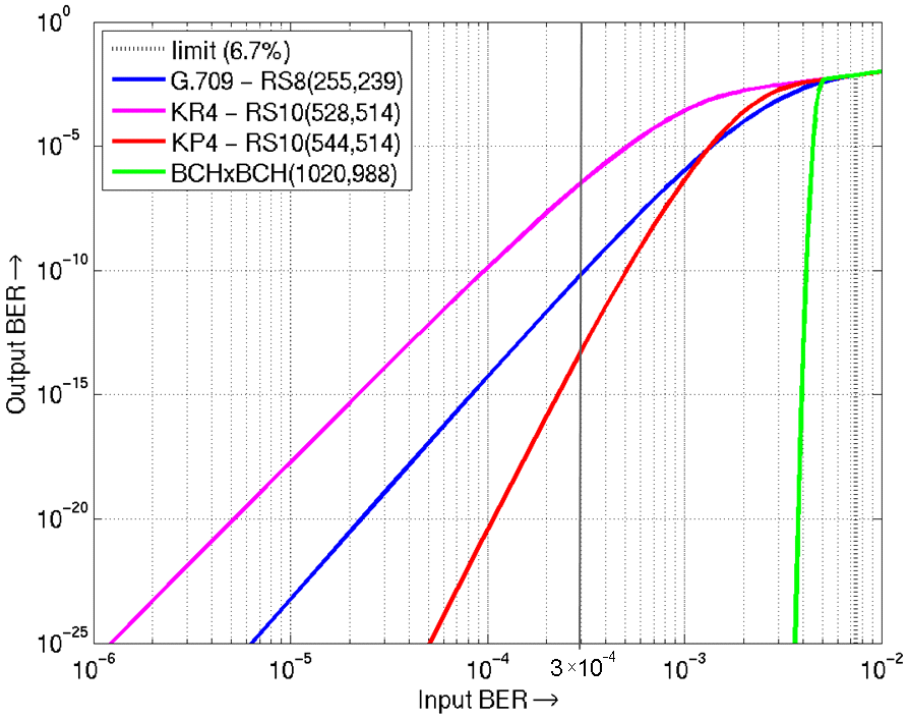
- A transition occurs for the middle PAM4 eye if the signal level changes from either -1 or -1/3 to either +1/3 or +1, or vice versa. The average transition density of middle eye transitions needs to converge to 0.5 over a long period (> 10^9 symbols), but can in the extreme be between 0.45 and 0.55 over a 30,000 symbol period with a probability of at least one minus the BER ratio (1 - 10^{-6}).
- A transition occurs for the upper PAM4 eye if the signal level changes from +1 to any other signal level, or from any other signal level to +1. A transition occurs for the lower PAM4 eye if the signal level changes from -1 to any other signal level, or from any other signal level to -1. The average transition density of the upper or lower eye transitions needs to converge to 0.375 over a long period (> 10^9 symbols), but can in the extreme be between 0.3375 and 0.4125 over a 30,000 symbol period with a probability of at least one minus the BER ratio (1 - 10^{-6}).
- The weighted average DC balance is calculated by assigning a weights of { +1, +2/3, +1/3, 0 } to the PAM4 signal levels { +1, +1/3, -1/3, and -1 } respectively. The weighted average DC balance needs to converge to 0.5 over a long period (> 10^9 symbols), but can in the extreme be between 0.45 and 0.55 over a 30,000 symbol period with a probability of at least one minus the BER ratio (1 - 10^{-6}).
- The probability of symbol run lengths over 10 is to be proportional to 4^{-N} for N-like symbols in a row (N>10). Hence, a run length of 40 symbols would occur with a maximum probability of 4^{-40}.
- If a fixed block coding scheme is used, the raw data must be scrambled before coding or the coded data must be scrambled prior to transmission to prevent the occurrence of worst case patterns (e.g. CJPAT-like patterns).

16.D Appendix - FEC Guidance and Background Material

This annex provides general guidance with regards to system FEC coding schemes and receiver error propagation behavior in order to ensure that end-to-end system performance may be sufficient to enable corrected BER less than 10^{-15} for the CEI-56G PAM4 interfaces.

In cases where the raw BER of the electrical link is expected to be greater than the targeted BER, it is necessary to ensure that a suitable FEC algorithm be chosen which is able to provide the necessary coding gain to achieve the targeted end-to-end corrected BER. Figure 16-20 shows a graph of the input to output BER for some common FEC code examples in the form of Additive White Gaussian Noise (AWGN).

Figure 16-20. Input to Output BER of common FEC codes



A different way of quantifying the correction capabilities of above FEC codes is shown in Table 16-11 below. The expected performance of each FEC code in the presence of AWGN is quantified by the random error coding gain. However, depending upon various system behaviors a receiver may not only experience random errors but may be required to mitigate a combination of random and burst errors. Therefore it is important that the specified pre-FEC BER of each CEI-56G-PAM4 clause include the potential bursts that are forwarded to the FEC correction block. In addition a maximum PAM4 symbol burst error length that a CEI-56G-PAM4 receiver shall expect with a probability less than 10^{-20} is defined for each clause to allow tailoring of the FEC solution with respect to randomization of bursts by means of symbol interleaving or similar methods.

Random error distribution for a FEC code can only be assumed, if the burst size does not exceed the code symbol size, “m”. One significant source of burst errors are the presence of DFE blocks in any system which can multiply a single error into a burst of errors and is highly dependent on DFE tap weights. As an example a 10-bit burst would not exceed the symbol size of either the RS(528,514) or RS(544,514) codes and therefore it could not affect more than two symbols but could affect three FEC symbols of the RS(255,239) whose symbol is made up of 8-bits. The BCHxBCH(1020,988) is unable to address any significant burst errors.

Table 16-11. Common FEC Codes

Code Name	Symbol size, m (bits)	Correctable symbols per block, t	Rate Overhead (%)	Random Error Coding Gain (dB)	Input BER for 10^{-15} corrected BER	Conditions
G.709 RS8(255,239) [8]	8	8	6.7	5.4	$8 \cdot 10^{-5}$	
IEEE 100GBASE-KR4 RS(528,514) [25]	10	7	2.7	4.9	$2 \cdot 10^{-5}$	
IEEE 100GBASE-KP4 RS(544,514) [25]	10	15	5.8	6.1	$2 \cdot 10^{-4}$	See Note 1
ITU G.975.1 (I.9) [26] BCHxBCH(1020,988)	1	N/A due to concate-nated code	3.2	9	$4 \cdot 10^{-3}$	

NOTES:
1. IEEE KP4 is presently under consideration by several standards bodies for electrical PAM4 interfaces.

One technique to mitigate burst errors is the use of code word interleaving in order to randomize received errors. For example, a system based on RS (255,239) coding and 2x interleaving would be able to successfully decode a 10-bit burst over two code blocks. However interleaving multiplies the FEC latency proportional to the depth of interleaving and also increases the implementation complexity.

Another technique to mitigate burst errors due to Decision Feedback Equalizers is to use the pre-coding described in Section 16.C.1.3. This converts typical error bursts caused by DFEs into one symbol error at the beginning of the burst and one symbol error at the end. However, pre-coding converts single symbol errors into two symbol errors, doubling the error rate for random errors.

A selected FEC implementation is considered sufficient for the application, if it can correct the raw BER of a dedicated CEI-56G-PAM4 clause to the desired system target BER, assuming a normal, uniform random error distribution (according Figure 16-20), plus implements the required burst handling to effectively randomize the maximum error bursts specified in the relevant clause.

Another important consideration is the worst-case error statistics for end-to-end systems, specifically where all of the error correction is performed at a far-end termination point and the system is made up of several errored links. In such cases the performance of each of the links must be understood in order to determine the overall

expected raw BER and the maximum possible burst error length. Raw BERs and bursts lengths of the individual concatenated links may add up over the complete end-to-end path and the required FEC implementation has to be selected accordingly.

17 CEI-56G-MR-PAM4 Medium Reach Interface

This clause details the requirements for the CEI-56G-MR-PAM4 medium reach high speed electrical interface between nominal baud rates of 18.0 Gsym/s and 29.0 Gsym/s using PAM4 coding. A compliant device shall meet all of the requirements listed below. The electrical interface is based on high speed, low voltage logic. Connections are point-to-point balanced differential pairs and signaling is unidirectional.

The electrical IA is based on loss and jitter budgets and defines the characteristics required to communicate between a CEI-56G-MR-PAM4 transmitter and a CEI-56G-MR-PAM4 receiver using copper signal traces on a printed circuit board. The characteristic impedance of the signal traces is nominally 100 Ω differential. The signal trace or channel between a transmitter and a receiver shall meet the channel operating margin (COM), a method and a threshold quantity used for channel compliance.

CEI-56G-MR-PAM4 assumes using forward error correction (FEC) to achieve the bit error ratio (BER) target. The FEC guidances are described in Appendix 16.D.

Medium reach CEI-56G-MR-PAM4 devices from different manufacturers shall be interoperable.

17.1 Requirements

1. Support serial baud rates (f_b) within the range from 18.0 Gsym/s to 29.0 Gsym/s as specified for the device using PAM4 coding. A CEI implementation complies to the specifications of this clause over the range of baud rates stated for the implementation within this range.
2. Capable of achieving a raw Bit Error Ratio (BER) of 10^{-6} or better per lane. FEC is assumed to be used in the system to achieve corrected BER of 10^{-15}or better per lane. The baud rate includes the overhead required for FEC. The definition of FEC is outside the scope of this IA (see Appendix 16.D).
3. Capable of driving up to 500 mm of PCB and up to 1 connector.
4. Shall support AC-coupled operation.
5. Shall allow multi-lanes (1 to n).
6. Shall support hot plug.

17.2 General Requirements

17.2.1 Data Patterns

See Appendix 16.C.5.

17.2.2 Bit Error Ratio

A raw Bit Error Ratio (BER) better than or equal to 10^{-6} is required on each lane. A compliant receiver, when receiving from a compliant transmitter over a compliant channel, shall deliver the specified raw BER to the subsequent FEC decoder. Error bursts with length more than 94 PAM4 symbols delivered to the PAM4 decoder shall occur with a probability of less than 1 in 10^{20} PAM4 symbols. See Appendix 16.D.

17.2.3 Ground Differences

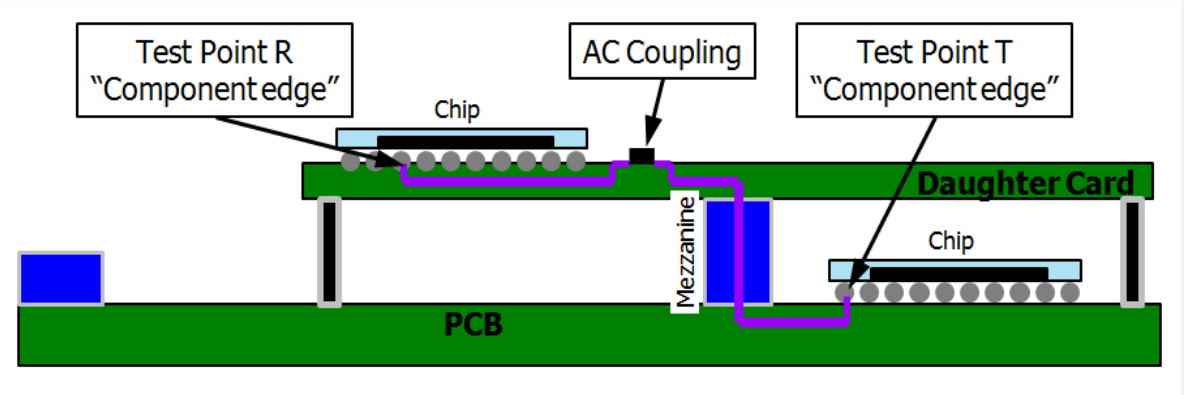
Please refer to Section 3.2.4.

17.2.4 Channel Compliance

A forward channel and associated dominant crosstalk channels are deemed compliant if the channel characteristics conform to the requirements defined in this section.

17.2.4.1 Reference Model

Figure 17-1. CEI-56G-MR Reference Model



Note: Test points differ from definitions in Section 1.8, as a DC blocking capacitor, if physically located outside of the package, is part of the channel. The mezzanine connector represents any board to board connector.

The channel is defined between test point T and test point R.

17.2.4.2 Channel Operating Margin

The Channel Operating Margin (COM) of the channel is computed using the procedure in Annex 93A of IEEE Std 802.3 [27], with the Test 1 and Test 2 values in Table 17-1. Test 1 and Test 2 differ in the value of the device package model transmission line length *zp*. Moreover, using *Tr* = 0.345 UI, *and* β=2 for *Ht*(*f*) in Equation (93A–19), COM

shall be greater than or equal to 3.0 dB for each test. This minimum value allocates margin for practical limitations on the receiver implementation and the largest step size allowed for transmitter equalizer coefficients.

Table 17-1. COM Parameter Values

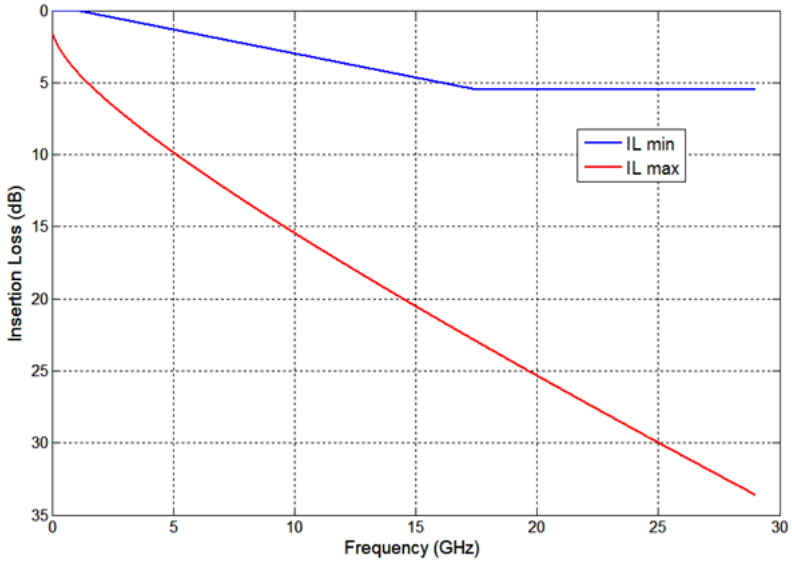
Parameter	Symbol	Value	Units
Signaling rate	f_b	18.0 - 29.0	Gsym/s
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length, Test 1 Transmission line length, Test 2 Transmission line characteristic impedance Single-ended package capacitance at package-to-board interface	 C_d z_p z_p Z_c C_p	 160 12 30 95 110	 fF mm mm Ω fF
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	50	Ω
Receiver 3 dB bandwidth	f_r	0.75 × f_b	GHz
Transmitter equalizer, minimum cursor	$c(0)$	0.60	—
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.15 0 0.05	 — — —
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.25 0 0.05	 — — —
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –15 0 1	 dB dB dB
Continuous time filter, DC gain2 Minimum value Maximum value Step size	g_{DC2}	 –4 0 1	 dB dB dB
Continuous time filter, scaled zero frequency	f_z	f_b /2.5	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	f_b /2.5 f_b	GHz GHz
Continuous time filter, low frequency pole/scaled zero	f_{LF}	f_b /40	GHz

Table 17-1. COM Parameter Values

Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.41 0.41 0.60	 V V V
Number of signal levels	L	4	—
Level separation mismatch ratio	R_{LM}	0.95	—
Transmitter signal-to-noise ratio	SNR_{TX}	32.5	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	10	UI
Normalized DFE coefficient magnitude limit for n = 2 to N_b	$b_{max}(1)$ $b_{max}(2\text{-}Nb)$	0.5 0.2	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.02	UI
One-sided noise spectral density	η_0	2.6×10^{-8}	V^2/GHz
Target detector error ratio	DER_0	10^{-6}	—
Channel operating margin, min	COM	3.0	dB

17.2.4.3 Informative Channel Insertion Loss

Figure 17-2. Channel Insertion Loss Limit for 29.0 Gsym/s



$$IL_{max} = \left[1.083 + 2.398 \sqrt{\frac{f \times 29}{f_b}} + 0.676 \frac{f \times 29}{f_b}, \quad f_{min} \le f \le f_b \right] \tag{17-1}$$

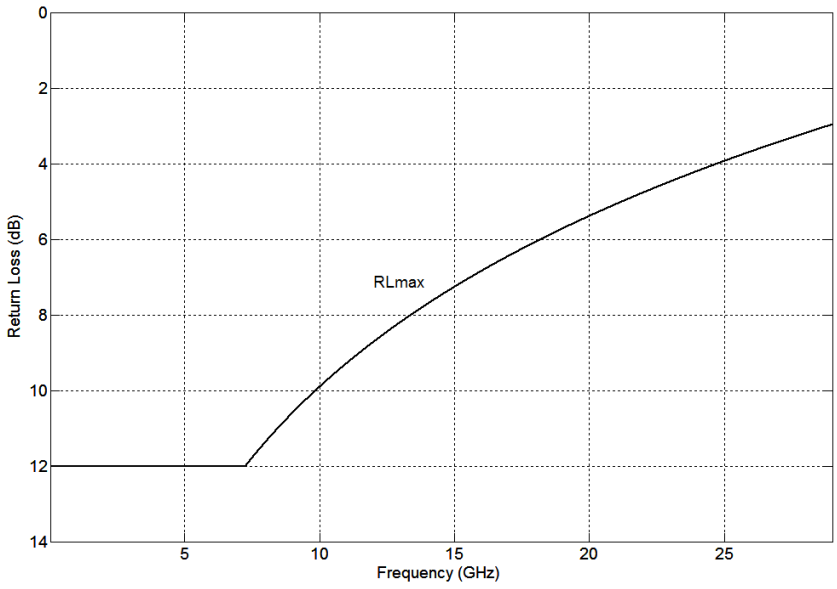
$$IL_{min} = \begin{bmatrix} 0, & f_{min} \le f \le 1\,GHz \\ \frac{1}{3}(f-1), & 1\,GHz < f \le 17.5\,GHz \\ 5.5, & 17.5\,GHz < f \le f_b \end{bmatrix} \tag{17-2}$$

Channel insertion loss is an informative recommendation.

The channel must comply with the normative specification in Section 17.2.4.2.

17.2.4.4 Channel Return Loss

Figure 17-3. Channel Return Loss Limit for 29.0 Gsym/s



Channel Return Loss shall be bounded by Equation (17-3) as shown in Figure 17-3.

$$RL_{max} = \begin{bmatrix} 12, & f_{min} \le f < \frac{f_b}{4} \\ 12 - 15\log_{10}\left(\frac{4f}{f_b}\right), & \frac{f_b}{4} \le f \le f_b \end{bmatrix} \quad \text{(17-3)}$$

17.2.4.5 Channel AC-coupling

The transmitter shall be AC-coupled to the receiver. The impact of a DC-blocking capacitor implemented in the channel between the package balls of the transmitter and receiver (i.e., between compliance points T and R) is accounted for within the channel specifications. Common-mode specifications are defined as if the DC-blocking capacitor is implemented in the channel between compliance points T and R. Should the capacitor not be implemented between compliance point T and compliance point R, it is the responsibility of implementers to consider any necessary modifications to common-mode and channel specifications required for interoperability as well as any impact on the verification of transmitter and receiver compliance. In particular the common-mode specifications for the transmitter in Table 17-2 may not be appropriate.

The low-frequency 3 dB cutoff of the AC-coupling shall be less than 100 kHz.

17.3 Electrical Characteristics

The electrical signaling is based on high speed low voltage logic with a nominal differential impedance of 100 Ω.

17.3.1 Transmitter Characteristics

The transmitter electrical requirements at compliance point T (see Figure 17-1) are specified in Table 17-2, and the jitter requirements are specified in Table 17-3.

Table 17-2. Transmitter Electrical Output Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	T_Baud		18.0		29.0	Gsym/s
Output Differential Voltage	T_Vdiff	See Note 1, 2.			1200	mVppd
DC Common mode Voltage	T_Vcm	See Note 2.	0		1.9	V
Output AC Common Mode Voltage	T_VcmAC	See Note 1, 2.			30	mVrms
Single-ended Transmitter Output Voltage	T_Vse	See Note 1, 2.	-0.3		1.9	V
Differential Output Return Loss	T_SDD22	Equation (17-4)				dB
Common Mode Output Return Loss	T_SCC22	Equation (17-5)				dB
Level Separation Mismatch Ratio	T_RLM	See Note 1, 2, 3, 4	0.95			-
Steady-state Voltage	T_Vf		0.4		0.6	V
Linear Fit Pulse Peak	T_Pk		0.83 × T_Vf			V
Signal-to-Noise-and-Distortion-Ratio	T_SNDR		31			dB

NOTES:
1. Signals are specified as measured through a fourth-order Bessel-Thomson low-pass response with 40 GHz 3 dB bandwidth.
2. Measured as described in Section 17.3.1.2. T_Vdiff min is set by the steady-state voltage T_Vf min.
3. Measured as described in Section 17.3.1.6.
4. T_RLM is defined in Appendix 16.C.4.3.

Table 17-3. Transmitter Output Jitter Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Uncorrelated Jitter (time interval from 0.005% to 99.995% of the probability distribution)	T_J_{4u}	See Note 1			0.118	UI
Uncorrelated jitter RMS (standard deviation of the probability distribution)	T_J_{RMS}				0.023	UIrms
Even-Odd Jitter	T_EOJ				0.019	UIpp

NOTES:
1. Measured as described in Section 17.3.1.7.

17.3.1.1 Transmitter Baud Rate

All devices shall work within the range from 18.0 Gsym/s to 29.0 Gsym/s as specified for the device, with the baud rate tolerance as per Section 3.2.11. A CEI implementation complies to the specifications of this clause over the range of baud rates stated for the implementation within this range.

17.3.1.2 Transmitter Amplitude and Swing

The differential output voltage T_Vdiff is defined to be True minus Complement. The common-mode output voltage T_Vcm is defined to be one half of the sum of True and Complement. These definitions are illustrated in Section 1.6.1.

For a QPRBS13-CEI test pattern (Appendix 16.C.3.1), the peak-to-peak value of the differential output voltage (T_Vdiff) shall be less than or equal to the limit given in Table 17-2 regardless of the transmit equalizer setting.

The DC common-mode output voltage (T_Vcm) shall be within the limits in Table 17-2 with respect to local ground.

The AC common-mode output voltage (T_VcmAC) shall be less than or equal to the limit given in Table 17-2 with respect to local ground. Common-mode output voltage requirements shall be met regardless of the transmit equalizer setting.

The single-ended transmitter output voltage (T_Vse) shall be within the limits in Table 17-2 with respect to local ground.

The transmitter shall be capable of providing a differential steady state output amplitude (2xT_V_f) between 800 and 1200 mVppd with transmit emphasis disabled.

Transmitter differential output amplitude shall additionally adhere to the requirements in Section 17.3.1.6.

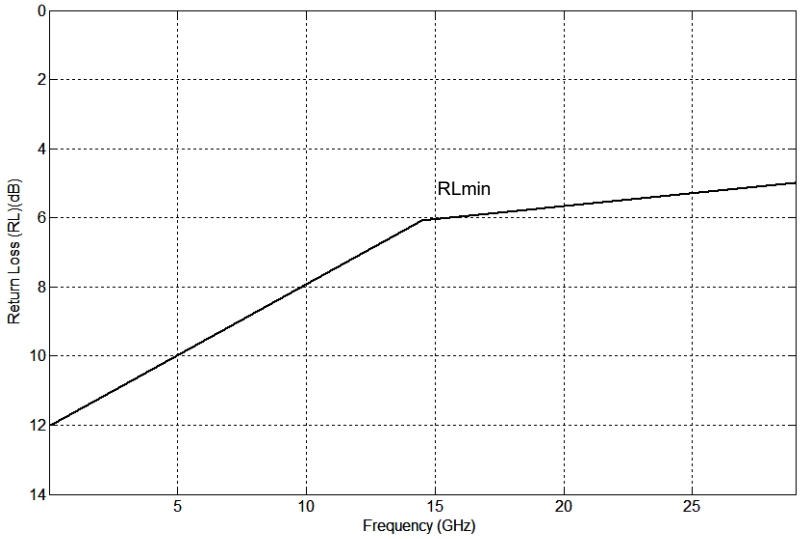
Power-down behavior is beyond the scope of CEI IA.

17.3.1.3 Transmitter Return Loss

The differential output return loss, in dB, of the transmitter shall meet Equation (17-4), where f is the frequency in GHz. The differential return loss limit $RL_d(f)$ is shown in Figure 17-4. This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements shall be 100 Ω.

$$RL_d(f) \geq RLmin(f) = \begin{pmatrix} 12.05 - 0.4112\left(\frac{f \times 29}{f_b}\right) & (0.05 \leq f \leq 0.5\, f_b) \\ 7.175 - 0.075\left(\frac{f \times 29}{f_b}\right) & (0.5\, f_b < f \leq f_b) \end{pmatrix} \quad (dB) \qquad (17\text{-}4)$$

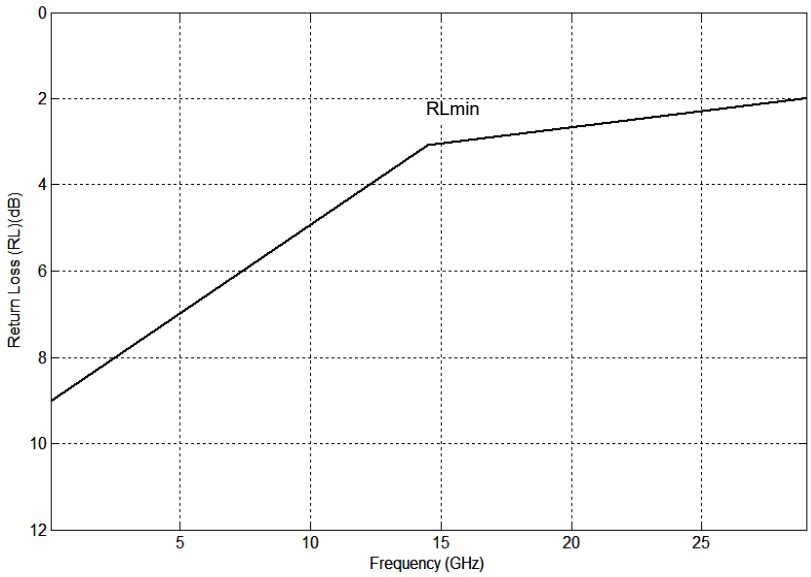
Figure 17-4. Transmitter differential return loss limit for 29.0 Gsym/s



The common-mode output return loss, in dB, of the transmitter shall meet Equation (17-5), where f is the frequency in GHz. The common-mode return loss limit $RL_C(f)$ is shown in Figure 17-5. This output impedance requirement applies to all valid output levels. The reference impedance for common-mode return loss measurements shall be 25 Ω.

$$RL_c(f) \geq RLmin(f)) = \begin{pmatrix} 9.05 - 0.4112\left(\frac{f \times 29}{f_b}\right) & (0.05 \leq f \leq 0.5 f_b) \\ 4.175 - 0.075\left(\frac{f \times 29}{f_b}\right) & (0.5 f_b < f \leq f_b) \end{pmatrix} \quad (dB) \qquad (17\text{-}5)$$

Figure 17-5. Transmitter common mode return loss limit for 29.0 Gsym/s.



17.3.1.4 Transmitter Lane-to-Lane Skew

Please refer to Section 3.2.7.

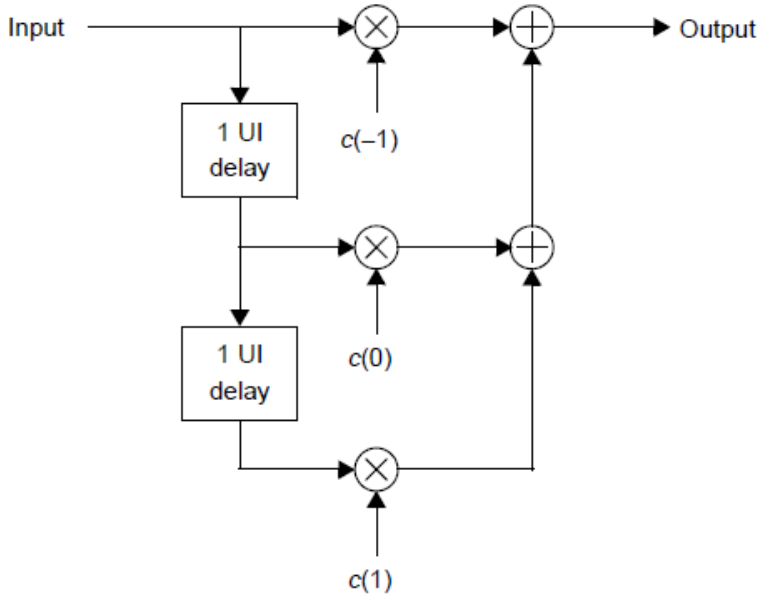
17.3.1.5 Transmitter Short Circuit Current

Please refer to Section 3.2.9.

17.3.1.6 Transmitter output waveform requirements

The transmitter function includes programmable equalization to compensate for the frequency-dependent loss of the channel and facilitate data recovery at the receiver. The functional model for the transmit equalizer is the three tap transversal filter shown in Figure 17-6.

Figure 17-6. Transmit equalizer functional model



Link budgets in this document assume optimized TX FIR equalization that is part of the system management function. The specific implementation is outside the scope of this document.

17.3.1.6.1 Linear fit to the measured waveform

The following test procedure defines linear fit pulse response, linear fit error (e(k), see Section 11.3.1.6.4), and normalized transmitter coefficient values.

For each configuration of the transmit equalizer, capture at least one complete cycle of the QPRBS13-CEI test pattern (Appendix 16.C.3.1) at the TX package ball (see Figure 17-1).

Compute the linear fit pulse response p(k) from the captured waveform per Section 11.3.1.6.2 using Np = 12 and Dp = 2. For aligned symbol values x(n) use -1, -ES1, ES2, and 1 to represent symbol values of -1, -1/3, 1/3, and 1, respectively, and where ES1 and ES2 are the effective symbol levels determined in Appendix 16.C.4.3.

Define r(k) to be the linear fit pulse response when transmit equalizer coefficients have been set to the “preset” values (see Section 11.3.1.6.1).

For each configuration of the transmit equalizer, compute the normalized transmit equalizer coefficients, c(i), according to Section 11.3.1.6.2 - Section 11.3.1.6.5.

17.3.1.6.2 Steady-state voltage and linear fit pulse peak

The linear fit pulse, p(k), is determined according to the linear fit procedure in Section 11.3.1.6.2 - Section 11.3.1.6.5, as modified by Section 17.3.1.6.1. The steady-state voltage T_Vf is defined to be the sum of the linear fit pulse p(k) divided by M, as shown in Equation (11-2).

The steady-state voltage, T_Vf, shall satisfy the requirements in Table 17-2.

The linear fit pulse peak, T_Pk, is the highest value of p(k). It shall satisfy the requirement in Table 17-2.

17.3.1.6.3 Transmitter equalizer coefficients

Table 17-4. Coefficient Range and Step Size

Coefficients	Normalized Amplitude		Normalized Step Size (%)
	Min (%)	Max (%)	
c(-1)	-15	0	0.5 to 5
c(1)	-25	0	0.5 to 5
c(0)	60	100	0.5 to 5

The normalized amplitudes of the coefficients of the transmitter equalizer (computed per Section 17.3.1.6.1) shall meet the requirements in Table 17-4. "min" is defined as the minimum normalized amplitude of the coefficient that must be supplied by the transmitter to be compliant. "max" is defined as the maximum normalized amplitude of the coefficient that must be supplied by the transmitter to be compliant.

The amplitude of a coefficient can be computed by multiplying its normalized amplitude by T_Vf, which is defined in Section 17.3.1.6.2.

The peak-to-peak output voltage is approximated by

$$(|c(-1)| + |c(0)| + |c(1)|) * 2 * T_Vf \quad (17\text{-}6)$$

and should not exceed the limit for T_Vdiff given in Table 17-2.

17.3.1.6.4 Transmitter Output Noise and Distortion

Signal-to-noise-and-distortion ratio (SNDR) is measured at the transmitter output using the following method, with the transmitter on the lane under test transmitting QPRBS13-CEI and transmitters on lanes not under test enabled and transmitting QPRBS31-CEI test pattern as defined in Appendix 16.C.3.2, or a valid CEI signal, or transmitting the same pattern with a slightly different Baud rate on each lane so that lane to lane signals are asynchronous. These transmitters shall have identical transmit equalizer settings to the transmitter under test.

Compute the linear fit to the captured waveform and the linear fit pulse response, p(k), and error, e(k), according to Section 17.3.1.6.1. Denote the standard deviation of e(k) as σ_e.

With the QPRBS13-CEI pattern and the same configuration of the transmit equalizer, measure the RMS deviation from the mean voltage at a fixed point in a run of at least 6 consecutive identical PAM4 symbols. The RMS deviation is measured for a run of each of the four PAM4 symbol levels.The average of the four measurements is denoted as σ_n.

SNDR is defined by Equation (17-7) where p_{max} is the maximum value of p(k).

$$SNDR = 10\log_{10}\left(\frac{p_{max}^2}{\sigma_e^2 + \sigma_n^2}\right)(dB) \quad (17\text{-}7)$$

SNDR shall be greater than 31 dB for any allowable transmit equalizer setting.

17.3.1.7 Transmitter output jitter

Jitter measurements in this sub-clause are performed with transmitters on physical lanes not under test enabled and transmitting QPRBS31-CEI test pattern as defined in Appendix 16.C.3.2, or a valid CEI signal, or transmitting the same pattern with a slightly different Baud rate on each lane so that lane to lane signals are asynchronous. These transmitters shall have identical transmit equalizer settings to the transmitter under test.

J_{4u}, J_{RMS}, and EOJ are defined by measurements of 12 specific transitions in a QPRBS13-CEI pattern in order to exclude correlated jitter. The 12 transitions represent all possible combinations of four identical symbols followed by two different identical symbols as shown in Table 17-5. The sequences are located by the symbol indices given in the table where symbols 1 to 7 are the run of seven +1s.

The threshold used to define each transition is given in Table 17-5 where V_{-1}, $V_{-1/3}$, $V_{1/3}$, and V_1 are as defined in Appendix 16.C.4.3.

The jitter is measured with a clock from a clock recovery unit (CRU) (i.e., a first order golden PLL, with corner frequency at f_b/6640, and a 20 dB/decade slope, see Section 1.6) as the trigger or reference clock.

J_{4u}, J_{RMS}, and EOJ specifications shall be met regardless of the transmit equalization setting.

Table 17-5. QPRBS13-CEI Pattern Symbols Used for Jitter Measurement

Label	Description	Gray Coded PAM4 Symbols	Index of First Symbol	Index Transition Begins	Index Transition Ends	Index of Last Symbol	Threshold Level
REF	Reference for symbol index	3333333	1	--	--	7	--
R03	0 to 3 rise	10000 330	1830	1834	1835	1837	$(V_{-1}+V_1)/2$
F30	3 to 0 fall	23333 001	1269	1273	1274	1276	
R12	1 to 2 rise	0111111 2222221	3638	3644	3645	3651	$(V_{-1/3}+V_{1/3})/2$
F21	2 to 1 fall	022222 113	1198	1203	1204	1206	
R01	0 to 1 rise	100000 113	6835	6840	6841	6843	$(V_{-1}+V_{-1/3})/2$
F10	1 to 0 fall	21111 003	2992	2996	2997	2999	
R23	2 to 3 rise	32222 330	6824	6828	6829	6831	$(V_{1/3}+V_1)/2$
F32	3 to 2 fall	033333 2222223	7734	7739	7740	7746	
R02	0 to 2 rise	10000 223	3266	3270	3271	3273	$(V_{-1}+V_{1/3})/2$
F20	2 to 0 fall	122222 0000002	7282	7287	7288	7294	
R13	1 to 3 rise	011111 331	133	138	139	141	$(V_{-1/3}+V_1)/2$
F31	3 to 1 fall	23333 112	7905	7909	7910	7912	

17.3.1.7.1 J_{4u} and J_{RMS} Jitter

For each transition i, 1 ..i ..12, of the transitions specified in Table 17-5, obtain a set S_i = {$t_i(1)$, $t_i(2)$, ...} of transition times modulo the period of the pattern. The 12 sets should be of equal size and the size of all sets should be chosen to enable calculation of J_{4u} (as defined below) with sufficient accuracy.

Calculate the average of each set Si, Tavgi, and subtract it from all elements of that set, to create a set $S0_i$ = {$t_i(1)$ - $Tavg_i$, $t_i(2)$ - $Tavg_i$, ...}.

Combine the sets $S0_i$, i=1 to 12, to create an estimated probability distribution $f_J(t)$.

J_{4u} is defined as the time interval that includes all but 10^{-4} of $f_J(t)$, from the 0.005th to the 99.995th percentile of $f_J(t)$.

J_{RMS} is defined as the standard deviation of $f_J(t)$.

17.3.1.7.2 Even-Odd Jitter (EOJ)

For one of the 12 specific transitions in QPRBS13-CEI in Table 17-5:

a) Trigger once in 3 repeats of the QPRBS13-CEI test pattern.

Obtain the mean time (T3) for this transition in the first QPRBS13-CEI.

Obtain the mean time (T4) for the same transition in the second QPRBS13-CEI.

b) The difference between the two means (T4 – T3), is the estimated period of the repeating pattern.

For each of the 12 specific transitions in QPRBS13-CEI in Table 17-5:

1) Trigger once in 2 repeats of the QPRBS13-CEI test pattern.

Obtain the mean time (T1) for the specific transition in the first QPRBS13-CEI.

Obtain the mean time (T2) for the same transition in the second QPRBS13-CEI.

2) Calculate EOJ for this transition as |(T2 – T1) – (T4 – T3)|.

EOJ is the maximum of the 12 measurements.

NOTE 1—Both of (T2 - T1) and (T4 - T3) are about 8191 UI, which is much larger than the EOJ value. Hence, each of T1 through T4 should have high precision.

17.3.2 Receiver Characteristics

A compliant receiver shall autonomously operate at the specified BER with the worst case combination of a compliant transmitter and a compliant channel. The receiver also shall not cause error propagation that violates the error burst length requirement as defined in Section 17.2.1. Further receiver electrical requirements at compliance point R (see Figure 17-1) are specified in Table 17-6, with the receiver interference tolerance parameters specified in Table 17-7. Lanes not under test should be enabled and transmitting or receiving asynchronous or uncorrelated signals.

Table 17-6. Receiver Electrical Input Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	R_Baud		18.0		29.0	Gsym/s
Differential Input Return Loss	R_SDD11	Equation (17-4)				dB
Differential to Common Mode Input Conversion	R_SCD11	Equation (17-8)				dB
Interference Tolerance		Table 17-7				
Jitter Tolerance		Table 17-8				

Table 17-7. Receiver interference tolerance parameters (Note 3)

Parameter	Test 1 values		Test 2 values		Units
	Min	Max	Min	Max	
Pre-FEC Bit Error Ratio (BER)		10^{-6}		10^{-6}	
COM, including effects of broadband noise		3		3	dB
Insertion loss at Nyquist, Note 1		10		20	dB
RSS_DFE4, Note 2	0.025	-	0.05	-	

NOTES:
1. Measured between TX and RX package balls (see Figure 17-1).
2. Definition can be found in Annex 93A of IEEE Std 802.3 [27].
3. See Section 17.3.2.4

17.3.2.1 Input Baud Rate

All devices shall work within the range from 18.0 Gsym/s to 29.0 Gsym/s as specified for the device, with the baud rate tolerance as per Section 3.2.11. A CEI implementation complies to the specifications of this clause over the range of baud rates stated for the implementation within this range.

17.3.2.2 Reference Input Signals

The receiver shall accept differential input signal amplitudes produced by a compliant transmitter connected with the minimum attenuation specified in Figure 17-2 to the receiver. This may be larger than the 1200 mVppd maximum of the transmitter due to output/input impedances and reflections.

The minimum input amplitude is defined by the minimum transmitter amplitude, the actual receiver input impedance and the loss of the actual PCB. Note that the minimum transmitter amplitude is defined using a well controlled load impedance, however the real receiver is not, which can leave the receiver input signal smaller than expected.

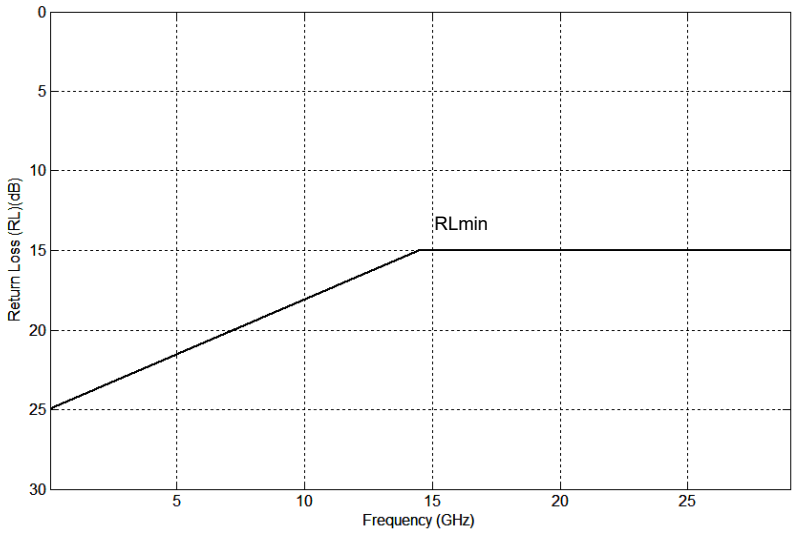
17.3.2.3 Receiver Input Return Loss

The differential input return loss, in dB, of the receiver shall meet Equation (17-4). The reference impedance for differential return loss measurements shall be 100 Ω.

The differential to common-mode return loss, in dB, of the receiver shall meet Equation (17-8). The differential to common-mode return loss limit $RL_{dc}(f)$ is shown in Figure 17-7.

$$RL_{dc}(f) \geq RLmin(f) = \begin{pmatrix} 25 - 0.6897\left(\frac{f \times 29}{f_b}\right) & (0.05 \leq f \leq 0.5f_b) \\ 15 & (0.5f_b < f \leq f_b) \end{pmatrix} (dB) \quad (17\text{-}8)$$

Figure 17-7. Receiver differential to common-mode return loss limit for 29.0 Gsym/s.



17.3.2.4 Receiver Interference Tolerance

The receiver interference tolerance test is based on the test defined in Annex 120D.3.2.1 of IEEE P802.3 [27].

The receiver on each lane shall meet the pre-FEC BER requirement with channels matching the Channel Operating Margin (COM) and loss parameters for Test 1 and Test 2 in Table 17-7.

The test channel should be created using printed circuit boards with short interconnecting cables.

The following considerations apply to the interference tolerance test. The transmitter package is omitted in the COM calculation. The test transmitter's measured SNDR should be used for SNR_{TX} in the COM calculation. The transmitter output levels are set such that R_{LM} is equal to 0.95. The test transmitter meets the specifications in Section 17.3.1. The test transmitter is constrained such that for any transmitter equalizer setting the differential peak-to-peak voltage is less than 800 mV, and the normalized amplitudes of the coefficients of the transmitter equalizer c(-1), c(0) and c(1) are between the minimum and maximum limits given in Table 17-4.

The lower frequency bound for the noise spectral density constraints, fNSD1, is 1 GHz. The differential return-loss of the test channel at TP5 (as defined in Annex 93A of Std. IEEE802.3 [25]) shall meet the requirements of Equation (17-4), and be 3.0 dB better than the requirements of Equation (17-4) for all frequencies less than $f_b/2$. The test transmitter's jitter parameters J_{4u} and J_{RMS} are measured. A_{DD} and σ_{RJ} are calculated from the measured values of J_{4u} and J_{RMS} using Equation (17-9), and Equation (17-10), respectively and used for COM parameters. Other COM parameters are set according to the values in Table 17-1. The broadband noise is added and adjusted to

achieve the COM value in Table 17-7. The test pattern to be used is QPRBS31-CEI defined in Appendix 16.C.3.2. A test system with a fourth-order Bessel-Thomson low-pass response with 40 GHz 3 dB bandwidth is to be used for measurement of the signal applied by the pattern generator and for measurements of the broadband noise.

$$A_{DD} = \left(\left(\frac{J_{4u}}{2}\right) + Q4\sqrt{\left((Q4^2+1)\times J_{RMS}{}^2 - \left(\frac{J_{4u}}{2}\right)^2\right)}\right)/(Q4^2+1) \quad (17\text{-}9)$$

Q4 = 3.8906

$$\sigma_{RJ} = \left(\frac{J_{4u}}{2} - A_{DD}\right)/(Q4) \quad (17\text{-}10)$$

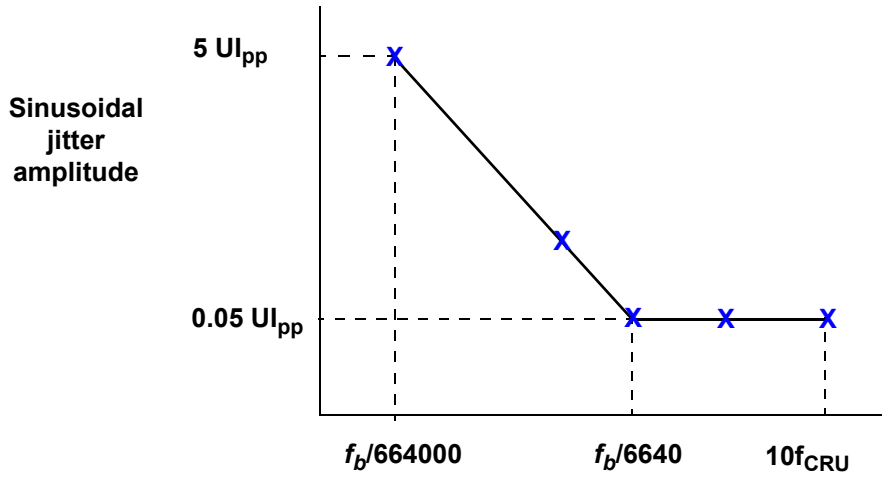
17.3.2.5 Receiver Jitter Tolerance

Receiver jitter tolerance shall meet the conditions and parameters defined in Table 17-8. This sinusoidal jitter is part of the jitter applied in the stressed input test. The sinusoidal jitter is calibrated at 10x the reference CRU's bandwidth and must be tested at $f_{CRU}/100$, $f_{CRU}/3$, f_{CRU}, $3f_{CRU}$, and $10f_{CRU}$, where f_{CRU} is the jitter corner frequency given by $f_b/6640$, with sinusoidal jitter of 5 UI, 0.15 UI, 0.05 UI, 0.05 UI and 0.05 UI respectively. For this test the channel used is as for the receiver interference tolerance described in Section 17.3.2.4. Note that the values measured for J_{4u} and J_{RMS} include the effects of this added sinusoidal jitter and noise is added to obtain a COM of 3 dB with these measured jitter values as for the interference tolerance test. The receiver bit error ratio (BER) shall meet the requirements of Section 17.2.2 for each pair of jitter frequency and peak-to-peak amplitude values listed above and shown in Figure 17-8.

Table 17-8. Receiver Jitter Tolerance Parameters

Frequency Range	Sinusoidal jitter, peak-to-peak (UI)
$f < f_b/664000$	Not Specified
$f_b/664000 < f \leq f_b/6640$	$5*f_b/(664000*f)$
$f_b/6640 < f \leq 10f_{CRU}$	0.05

Figure 17-8. Receiver Jitter Tolerance Mask



17.3.2.6 Single Ended Input Voltage

The single ended voltage levels with respect to the receiver ground at the input of the receiver are dependent on the transmitter implementation and the inter-ground difference. The voltage levels at the input of an AC coupled receiver (if the effective AC coupling is done within the receiver) or at the TX side of the external AC coupling cap (if AC coupling is done externally) will be between -0.35V and 1.95V with respect to local ground.

17.3.2.7 Input Lane-to-Lane Skew

Refer to Section 3.2.8.

18 CEI-56G-USR-NRZ Ultra Short Reach Interface

This clause details the requirements for the CEI-56G-USR-NRZ ultra short-reach high speed electrical interface between nominal baud rates of 19.6 Gsym/s to 58.0 Gsym/s using NRZ coding. A compliant device must meet all of the requirements listed below. The electrical interface is based on high speed, low voltage DC-coupled logic with nominal differential impedance of 100 Ω and a channel with a nominal differential impedance of 92.5 Ω. Connections are point-to-point balanced differential pair and signaling is unidirectional.

The electrical IA is based on loss & jitter budgets and defines the characteristics required to communicate between a CEI-56G-USR-NRZ driver and a CEI-56G-USR-NRZ receiver using signal traces on a package substrate. The characteristic impedance of the signal traces is nominally 92.5 Ω differential. A 'length' is effectively defined in terms of its attenuation rather than physical length.

Ultra short reach CEI-56G-USR-NRZ devices from different manufacturers shall be interoperable.

18.1 Requirements

1. Support serial data rate from 19.6 Gsym/s to 58.0 Gsym/s. A CEI implementation complies to the specifications of this clause over the range of baud rates stated by the implementer within this range.
2. Capable of low bit error rate (10^{-15}, with a test requirement to verify 10^{-12}).
3. Capable of driving 0 – 10 mm of package substrate
4. Shall support DC-coupled operation.
5. Shall allow multi-lanes (1 to n).

18.2 General Requirements

18.2.1 Data Patterns

Please refer to Section 3.2.1.

18.2.2 Signal levels

The signal is a low swing DC coupled differential interface.

18.2.3 Signal Definitions

Please refer to Appendix 1.A.

A single clock signal is shared between the transmitting and receiving devices in the ingress direction and another single clock signal is shared between the transmitting and receiving devices in the egress direction, avoiding the need for a clock recovery circuit at the receiver.

18.2.4 Bit Error Ratio

Please refer to Section 3.2.3.

18.2.5 Ground Differences

As the driver and receiver are on the package substrate (with no intervening connectors), the ground difference is approximately 0 mV.

18.2.6 Cross Talk

Please refer to Section 3.2.5.

18.2.7 Channel Compliance

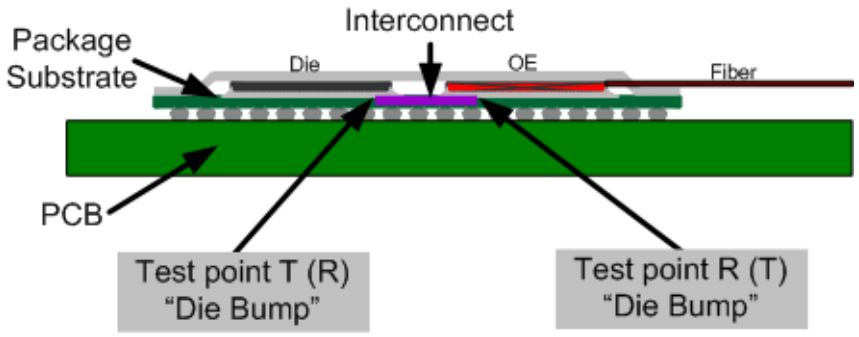
A forward channel and associated dominant crosstalk channels are deemed compliant if the channel characteristics conform to the requirements in this section.

18.2.7.1 Reference Model

The channel consists of a package substrate trace and any required vias. The reference package substrate trace differential impedance is 92.5 Ω and all channel specifications are referenced to this impedance.

Figure 18-1 shows a diagram of the intended application.

Figure 18-1. CEI-56G-USR-NRZ Reference Model



Several channel characteristics are parametrized according to Table 18-1 at these test points and are used for calculation of the channel parameters found in Table 18-2.

Table 18-1. Measured Channel Parameters

Symbol	Description
IL(*f*)	Differential insertion loss, -SDD21 magnitude (dB)
$RL_1(f)$	Differential input return loss, -SDD11 magnitude (dB)
$RL_2(f)$	Differential output return loss, -SDD22 magnitude (dB)
$NEXT_m(f)$	Differential near-end crosstalk loss (m^{th} aggressor), -SDD21 magnitude (dB)
$FEXT_n(f)$	Differential far-end crosstalk loss (n^{th} aggressor), -SDD21 magnitude (dB)

Table 18-2. Calculated Channel Parameters

Symbol	Description
$IL_{fitted}(f)$	Fitted insertion loss (dB)
ILD(*f*)	Insertion loss deviation (dB)
ICN(*f*)	Integrated crosstalk noise (mVRMS)
FOM_{ILD}	Channel Figure of merit - Weighted insertion loss deviation (dB)

18.2.7.2 Insertion Loss

Channel insertion losses, including package substrate traces and vias, shall comply with the limits specified by Equation (18-1) and plotted in Figure 18-2. Note that the variable f_b is the maximum baud rate to be supported by the channel under test (19.6 GHz < f_b < 58.0 GHz) and the measurement is to be made relative to the nominal impedance of 92.5 Ω.

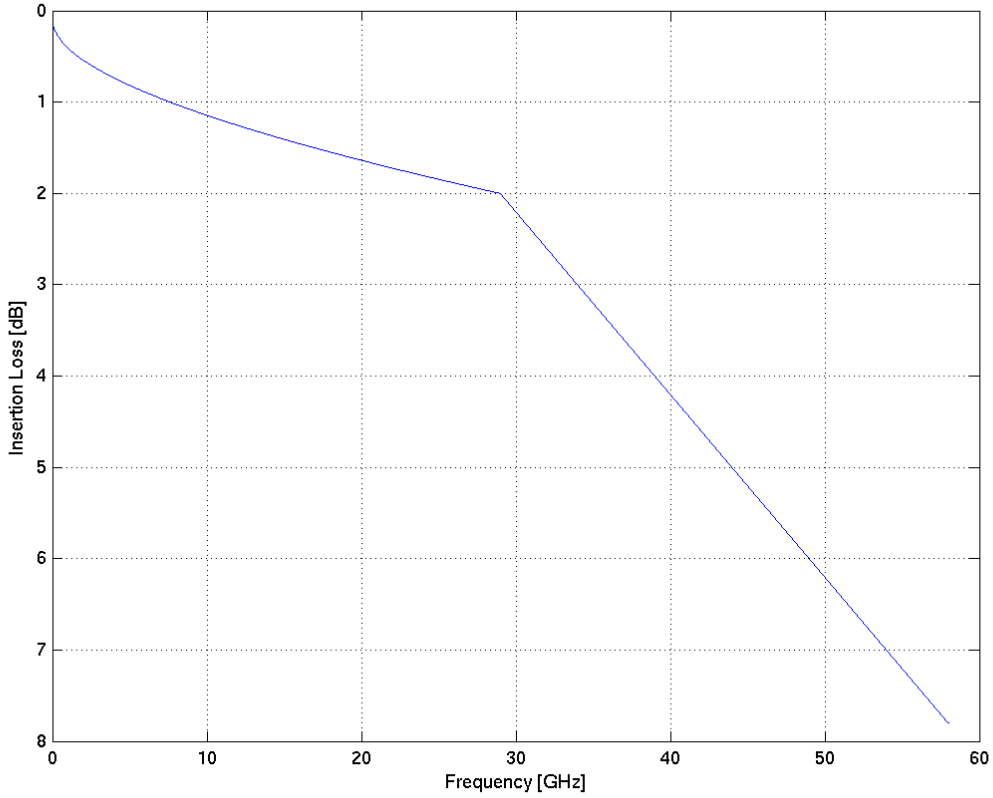
Table 18-3. Channel Insertion Loss Frequency Range

Parameter	Value	Units
f_{min}	50	MHz
f_{max}	f_b	GHz

$$IL_{max} = \begin{cases} 0.095 + 0.3\sqrt{\frac{f \times 58.0}{f_b}} + 0.01\frac{f \times 58.0}{f_b} & f_{min} \le f < \frac{f_b}{2} \\ -3.798 + 0.2\frac{f \times 58.0}{f_b} & \frac{f_b}{2} \le f \le f_b \end{cases} \quad \text{(18-1)}$$

Note: *f* in Equation (18-1) is in GHz.

Figure 18-2. CEI-56G-USR-NRZ normative channel insertion loss at 58.0 Gsym/s



18.2.7.3 Fitted Insertion Loss

For fitted insertion loss definitions, please refer to Section 12.2.1.1.

The channel shall meet the insertion loss requirements defined in Table 18-4 and also meet the IL mask in Equation (18-1). Note that the variable f_b is the maximum baud rate to be supported by the channel under test.

Table 18-4. Channel fitted insertion loss characteristics

Parameter	Units	Min Value	Max Value
Min frequency, f_{ILmin}	GHz	0.05	-
Max frequency, f_{ILmax}	GHz	-	fb
Fitted insertion loss at Nyquist	dB	-	2
Fitted insertion loss, a_0	dB	-1	2
Fitted insertion loss, a_1	dB	0	-
Fitted insertion loss, a_2	dB	0	-
Fitted insertion loss, a_4	dB	0	-

18.2.7.4 Insertion Loss Deviation (ILD)

The insertion loss deviation ILD is the difference between the measured insertion loss IL and the fitted insertion loss IL_{fitted} as defined in Equation (18-2) where f_{ILmin} and f_{ILmax} are given in Table 18-4.

$$ILD = IL - IL_{fitted} \qquad f_{ILmin} \le f \le (3/4) \times f_{ILmax} \tag{18-2}$$

The insertion loss deviation ILD shall be within the region defined by Equation (18-3).

$$-1.0 \le ILD \le 1.0 \tag{18-3}$$

A Figure Of Merit (FOM_{ILD}) for the channel is the weighted insertion loss deviation from f_{ILmin} to (3/4)*f_{ILmax}. FOM_{ILD} is calculated as indicated below. Note FOM_{ILD} is called ILD_{RMS} in OIF-CEI-03.0 clauses 10 & 11 and OIF-CEI-03.1 clauses 10, 11, 13 & 14.

Define the weight at each frequency *f* using Equation (18-4) below.

$$W(f) = \sin c^2(f/f_b)\left[\frac{1}{1+(f/f_t)^4}\right]\left[\frac{1}{1+(f/f_r)^8}\right] \tag{18-4}$$

Note that -3 dB transmit filter bandwidth f_t is inversely proportional to the minimum 20% to 80% rise and fall times T_*tr* and T_*tf*. The constant of proportionality is 0.2365 (i.e. min(T_*tr*, T_*tf*) x f_t = 0.2365, T_*tr* is in ns when f_t is in GHz). In addition, f_r is the -3 dB reference receiver bandwidth, which should be set at (3/4)f_b, where f_b is the maximum baud rate to be supported by the channel.

FOM_{ILD} is calculated using Equation (18-5) where N is the number of frequency points. The summation is done over the frequency range of ILD with *f* in GHz. FOM_{ILD} shall be less than 0.2 dB for compliant channels.

$$FOM_{ILD} = \sqrt{\frac{\sum W(f) \times ILD\langle f \rangle^2}{N}} \tag{18-5}$$

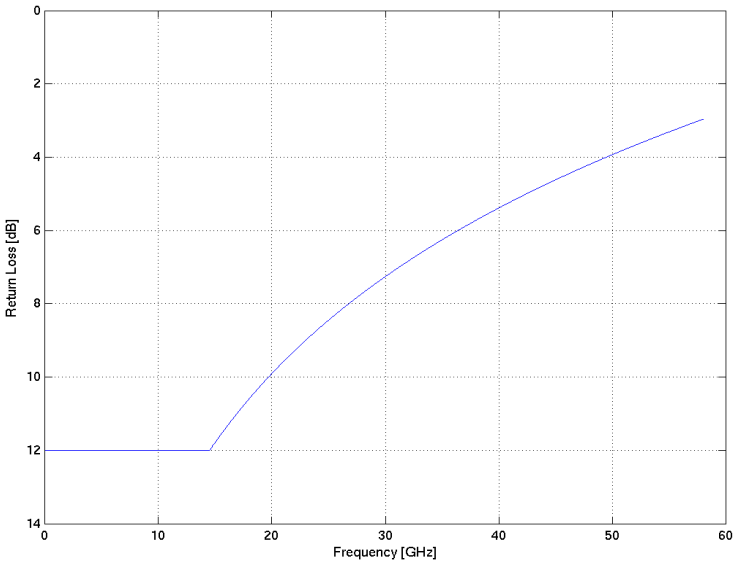
18.2.7.5 Channel Return Loss

Channel Return Loss shall be bounded by Equation (18-6) as shown in Figure 18-3 relative to the nominal impedance of 92.5 Ω.

$$\begin{aligned} RL(f) &> 12\ dB & f_{min} \le f \le \frac{f_b}{4} \\ RL(f) &> 12\ dB - 15\log_{10}\left(\frac{4f}{f_b}\right) & \frac{f_b}{4} < f \le f_b \end{aligned} \tag{18-6}$$

Note: f_{min} is as defined in Table 18-3

Figure 18-3. CEI-56G-USR-NRZ normative channel return loss at 58.0 Gsym/s



18.2.7.6 Channel integrated crosstalk noise

Using the Integrated crosstalk noise method of Section 12.2.1.2 and the parameters of Table 18-5, the total integrated crosstalk noise for the channel shall be less than 1 mV_{RMS}.

Table 18-5. Channel integrated crosstalk aggressor parameters

Parameter	Symbol	Value	Units
Baud rate	f_b	max. Baud Rate supported by channel	Gsym/s
Near-end aggressor peak to peak differential output amplitude	A_{nt}	250	mVppd
Far-end aggressor peak to peak differential output amplitude	A_{ft}	250	mVppd
Near-end aggressor 20% to 80% rise and fall times	T_{nt}	4	ps
Far-end aggressor 20% to 80% rise and fall times	T_{ft}	4	ps

18.3 Electrical Characteristics

The electrical interface is based on high speed, low voltage DC-coupled logic with nominal differential impedance of 100 Ω and a channel with a nominal differential impedance of 92.5 Ω.

All devices shall work within the range 19.6 Gsym/s to 58.0 Gsym/s as specified for the device, with all ingress lanes synchronous to a common reference frequency having a stability of ± 100ppm from nominal and all egress lanes synchronous to a common reference frequency having a stability of ± 100ppm from nominal. The reference clocks of the ingress and egress directions are not necessarily synchronous to each other. Note that implementation of specific protocols will define the operating baud rate without affecting CEI compliance.

18.3.1 Reference Clock

Both ends of the link are to have a common clock frequency, which is set to be 1/64th of the baud rate. This clock could come from the same source or could be “forwarded” from the driver side to the receiver side. For details of applicable clock architecture options please refer to Annex 18.A. In a forwarded clock architecture the clock path needs to meet the same requirements as the data path. The electrical specifications at R_C are given in Table 18-6.

Table 18-6. Reference Clock Electrical Specification.

Characteristic	Symbol	Condition	MIN.	NOM.	MAX.	UNIT
Reference Clock Rate	Ref_Freq			f_b/64		GHz
Input Differential Voltage	Ref_Vdiff		240		900	mVppd
Input Single Ended Voltage	Ref_Vse		0.1		1.2	V
Differential Termination Resistance Mismatch	Ref_Rdm				5	%
Input Clock Rise and Fall Time (20% to 80%)	Ref_tr, Ref_tf		4		200	ps
Differential Input Return Loss	Ref_SDD11	at f_b/128 ≤ f < f_b/4 Note 1			-6	dB
Input Clock Duty Cycle	Ref_DC		40		60	%
High Frequency Uncorrelated Unbounded Gaussian Jitter	Ref_UUGJ_hf	Note 2			0.009	UI rms
Reference Clock Single Side Band Phase Noise	Ref_PN	@ 1kHz offset			-70	dBc/Hz
		@10kHz offset			-93	
		@100kHz offset			-113	
		@1MHz offset			-133	
		≥10MHz offset			-143	

NOTES:
1. Return loss is referenced to 100 Ohm
2. UUGJ measured using the methodology defined in Appendix 2.E.1 with a golden PLL cut-off frequency of fb/500, observing with a bandwidth of 43GHz

18.3.2 Transmitter Characteristics

The transmitter electrical specifications at compliance point T (see Figure 18-1) are given in Table 18-7. The transmitter shall satisfy jitter requirements specified in Table 18-8. Jitter is measured relative to the reference clock as timing source, using a golden clock multiplier as detailed in Annex 18.A.4, for a BER as specified in Section 3.2.3. To attenuate noise and absorb even/odd mode reflections, the transmitter shall satisfy the Common Mode Output Return Loss requirement of Table 18-7. The waveform is observed through a fourth-order Bessel-Thomson response with a bandwidth of 43 GHz using a PRBS31 pattern.

The link budget in this document assumes no Tx emphasis.

Table 18-7. Transmitter Electrical Output Specification.

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	T_Baud		19.6		58.0	Gsym/s
Output Differential Voltage	T_Vdiff		100		250	mVppd
Single Ended Transmitter Output Voltage Note 1	T_Vse		0.1		1.2	V
Differential Termination Resistance Mismatch	T_Rdm				5	%
Output Rise and Fall Time (20% to 80%)	T_tr, T_tf		4			ps
Differential Output Return Loss	T_SDD22	See 18.3.2.2 Note 2				dB
Common mode Output Return Loss	T_SCC22	500MHz to f_b			-6	dB
Transmitter Common Mode Noise	T_Ncm				15	mVrms

NOTES:
1. DC Coupling compliance is mandatory.
2. Return loss is referenced to 100 Ohm

Table 18-8. Transmitter Output Jitter Specification

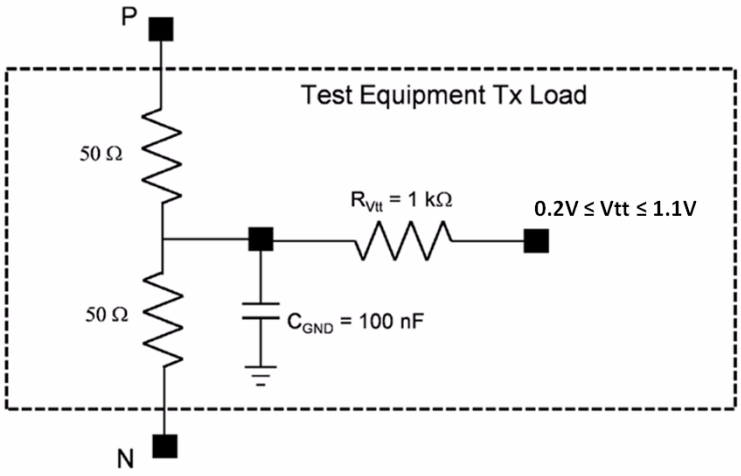
Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Uncorrelated Unbounded Gaussian Jitter	T_UUGJ				0.24	UIpp
Uncorrelated Bounded High Probability Jitter	T_UBHPJ				0.25	UIpp
Even Odd jitter (component of UBHPJ)	T_EOJ	Note 2			0.035	UIpp
Total Jitter	T_TJ	Note 1			0.44	UI
Eye Mask	T_X1	See 18.3.2.4			0.22	UI
Eye Mask	T_X2	See 18.3.2.4			0.4	UI
Eye Mask	T_Y1	See 18.3.2.4	50			mV
Eye Mask	T_Y2	See 18.3.2.4			125	mV

NOTES:
1. T_TJ includes all of the jitter components measured without any transmit equalization.
2. Included in T_UBHPJ. Even-odd jitter is defined in Table 1-3.

18.3.2.1 Transmitter Amplitude and Swing

Transmitter differential output amplitude shall be able to drive between 100 and 250 mVppd. Further the single-ended voltage must be between 0.1 and 1.2 V. Figure 18-4 shows the transmitter test load configuration.

Figure 18-4. Transmitter Amplitude Test Load



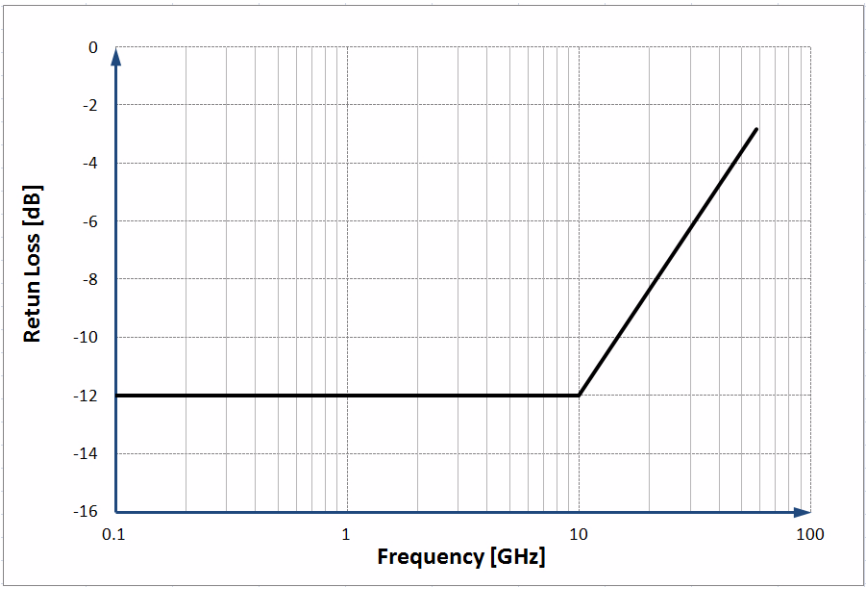
18.3.2.2 Transmitter Resistance and Return Loss

Please refer to Section 3.2.10 with the following parameters in Table 18-9 and as illustrated in Figure 18-5.

Table 18-9. Driver Return Loss Parameters

Parameter	Value	Units
A0	-12	dB
f0	100	MHz
f1	0.1714 x T_Baud	Hz
f2	T_Baud	Hz
Slope	12.0	dB/dec

Figure 18-5. Illustration of Return Loss for T_Baud = 58.0 Gsym/s



18.3.2.3 Transmitter Lane-to-Lane Skew

Please refer to Section 3.2.7.

18.3.2.4 Transmitter Template and Jitter

When provided with the reference clock meeting the specifications in Section 18.3.1 as a timing source, using a golden clock multiplier as detailed in Annex 18.A.4, for a BER as per Section 3.2.3, the transmitter shall satisfy the eye template and jitter requirements as given in Table 18-8 and Figure 1-4. The measurement of jitter and eye diagram is to be relative to the “forwarded” clock if the transmitter provides one. If it does not provide a “forwarded” clock then the measurement is to be relative to the reference clock provided to it.

18.3.3 Receiver Characteristics

A compliant receiver shall operate at the specified BER with the worst case combination of a compliant transmitter and a compliant channel.

Receiver electrical specifications are given in Table 18-10 and measured at compliance point R. To dampen noise sources and absorption of both even and odd mode reflections, the receiver shall satisfy the Common Mode Input Return Loss requirement of Table 18-10.

The link budget in this document assumes no Rx equalization.

Table 18-10. Receiver Electrical Input Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	R_Baud		19.6		58.0	Gsym/s
Input Differential Voltage	R_Vdiff	Note 1			250	mVppd
Receiver Common Mode Noise Tolerance	R_Ncm				25	mVrms
Differential Termination Resistance Mismatch	R_Rm				5	%
Differential Input Return Loss	R_SDD11	See 18.3.3.2 Note 2				dB
Common mode Return Loss	R_SCC11	200 MHz to 10 GHz			-6	dB
		10 GHz to f_b			-4	dB
Rx Input Single Ended Voltage Range	R_V_{inSE}		0.1		1.2	V

NOTES:
1. The receiver shall have a differential input voltage range sufficient to accept a signal produced at point R by the combined transmitter and channel. The channel response shall include the worst case effects of the return losses at the transmitter and receiver
2. Return loss is referenced to 100 Ohm

When provided with the reference clock meeting the specifications in Section 18.3.1 as a timing source, the receiver shall tolerate the sum of these jitter contributions and meet the BER as per Section 3.2.3: the total transmitter jitter from Table 18-8 and the effects of a channel compliant to the Channel Characteristics (Section 18.2.7).

18.3.3.1 Reference Receiver Input Signals

The receiver shall accept differential input signal amplitudes produced by a compliant transmitter connected directly to the receiver. This may be larger than the 250 mVppd maximum of the transmitter due to output/input impedances and reflections.

The minimum input amplitude is defined by the minimum transmitter amplitude, the actual receiver input impedance and the loss of the actual package substrate. Note that the minimum transmitter amplitude is defined using a well controlled load impedance; however the real receiver's impedance may differ, which can leave the receiver input signal smaller than expected. Additionally the real receiver may be affected by environmental noise.

18.3.3.2 Receiver Return Loss

Please refer to Section 3.2.10 with the following parameters in Table 18-11 and as illustrated in Figure 18-5.

Table 18-11. Receiver Input Return Loss Parameters

Parameter	Value	Units
A0	-12	dB
f0	100	MHz
f1	0.1714 x R_Baud	Hz
f2	R_Baud	Hz
Slope	12.0	dB/dec

18.3.3.3 Input Lane-to-Lane Skew

Please refer to Section 3.2.8.

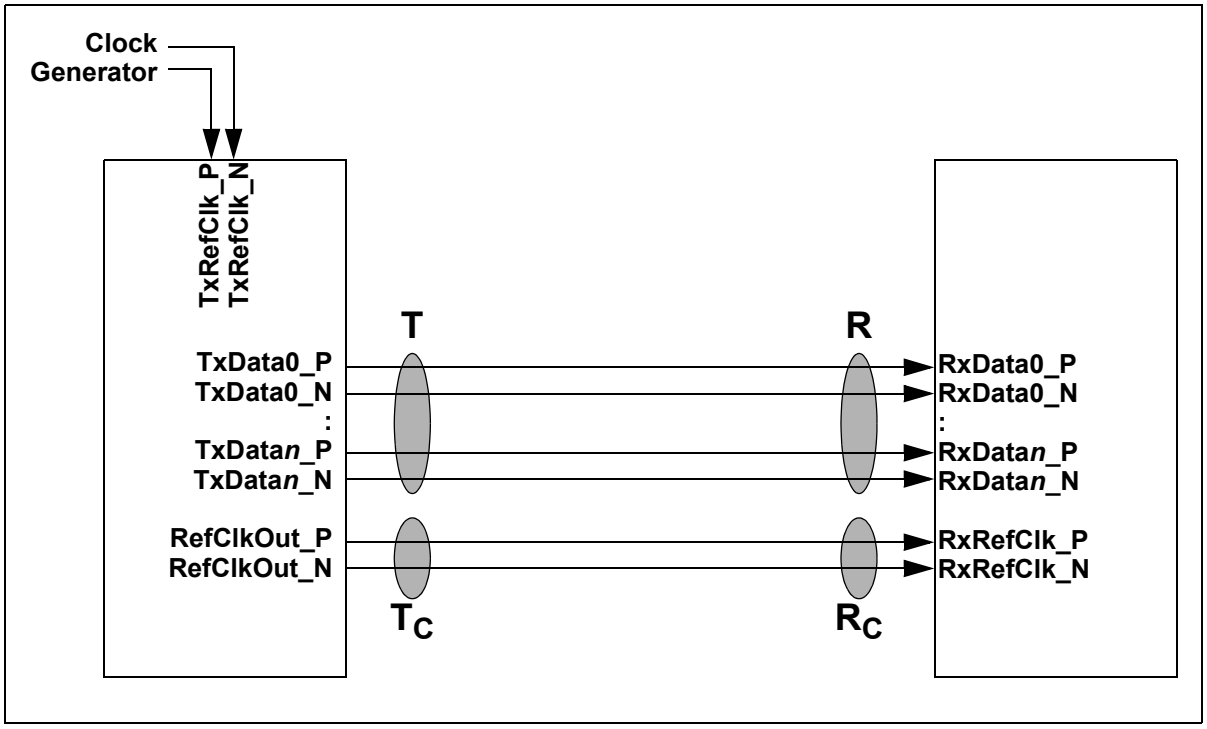
18.A Annex - Clock Architecture Options

This annex clarifies the applicability of reference clock specifications for clauses that allow forwarded clock and common clock architectures. The electrical requirements specified in these clauses support several different architectures for clock distribution and data recovery. Devices shall be interoperable regardless of the clock distribution method used by the system or the data recovery method used by the receiver device. The intent is to allow low power receiver architectures which do not use Clock Data Recovery (CDR) circuits to sample data.

18.A.1 Forwarded Clock Architecture

Receiver devices designed to support forwarded clock architectures use a clock from the transmitter and a clock multiplier circuit to synchronously sample data in the receiver. The device interconnections for a forwarded clock architecture are shown in Figure 18-6.

Figure 18-6. Forwarded Clock Architecture



The signals at reference point R_C that are connected to the RxRefClk input shall meet the requirements defined for the Reference Clock in the applicable clause.

The TxData signals in the figure at reference point T shall meet the requirements in the Transmitter Characteristics section of the applicable clause. The transmitter shall satisfy the jitter requirements defined in the Transmitter Characteristics section of the

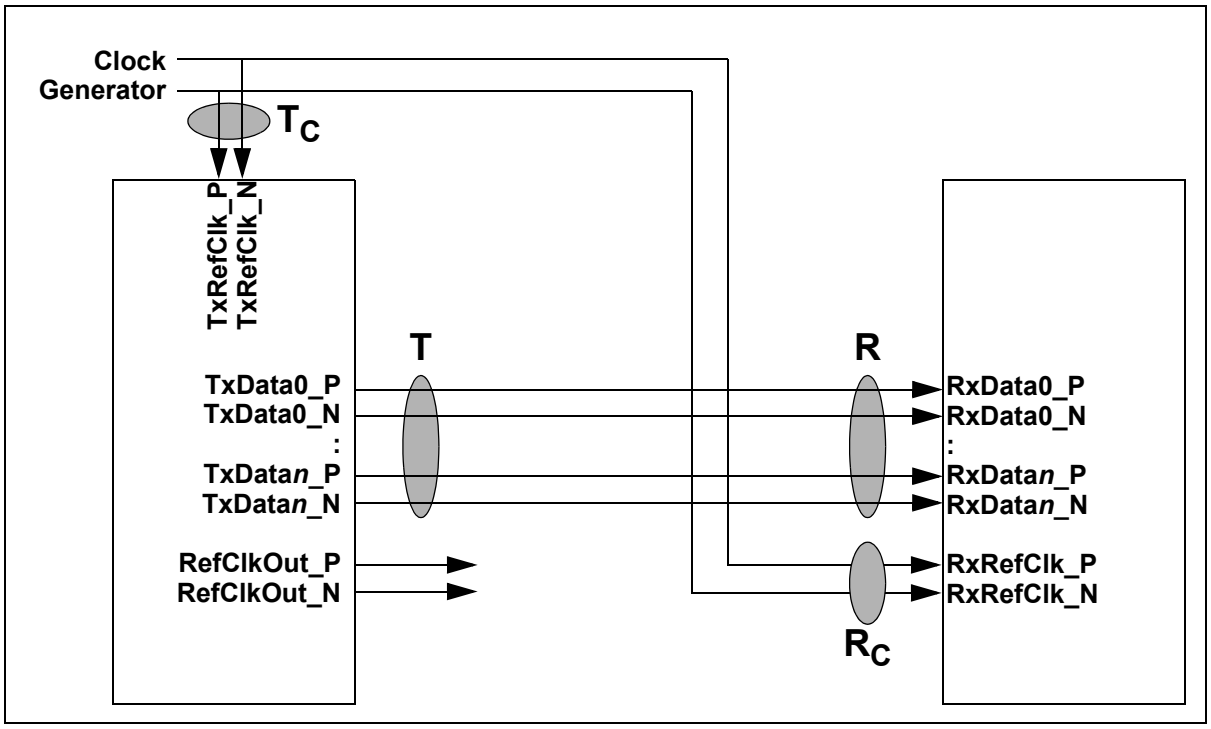
applicable clause when the signals at reference point T are measured using the signal at reference point R_C as a timing source. The signals at R_C are connected through a Golden Clock Multiplier to make these measurements as described in Annex 18.A.4.

Requirements for the TxRefClk input signal from the clock generator are determined by the device manufacturer. Device interoperability does not require the imposition of any specific requirements on this signal.

18.A.2 Common Clock Architecture

Devices connected in a common clock architecture configuration drive the same clock generator signal to both the Transmitter and the Receiver devices. The Receiver uses this clock and a clock multiplier circuit to synchronously sample data in the receiver. The device interconnections for a common clock architecture are shown in Figure 18-7.

Figure 18-7. Common Clock Architecture



The signals at reference point R_C that are connected to the RxRefClk input shall meet the requirements defined for the Reference Clock in the applicable clause. Since transmitter and receiver share a common clock source, it is implied that the signal at T_C meets the similar requirements as the signal at R_C, although this is not required for interoperability.

The TxData signals in the figure at reference point T shall meet the requirements in the Transmitter Characteristics section of the applicable clause. The transmitter shall satisfy the jitter requirements defined in the Transmitter Characteristics section of the

applicable clause when the signals at reference point T are measured using the signal at reference point R_C as a timing source. The signals at R_C are connected through a Golden Clock Multiplier to make these measurements as described in Annex 18.A.4.

18.A.3 Receiver Clock Data Recovery (CDR) Circuits

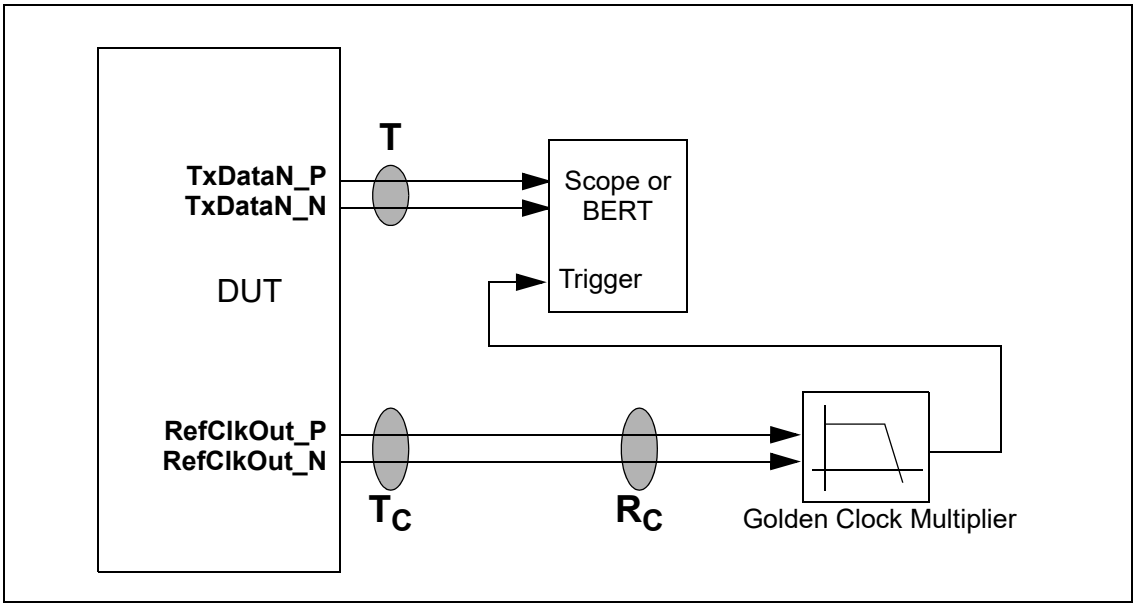
While the intent is to support receiver architectures that do not use CDR circuits, there is no restriction that prevents receiver implementations from using CDR circuits to sample data. Such receivers are connected using the Common Clock Architecture shown in Figure 18-7. To ensure interoperability with receiver devices that do not use CDR circuits, the reference clock, transmitter, and receiver requirements are applied in the same manner as was described in Annex 18.A.2.

18.A.4 Golden Clock Multiplier

Clauses which allow a forwarded clock architecture specify that transmitter jitter is measured relative to the reference clock as a timing source. This section specifies the relevant measurement methodology.

Transmitter jitter for applicable clauses is measured as described in Figure 18-8. The electrical characteristics of the reference clock at R_C are specified by the applicable clause. A Golden Clock Multiplier is used to multiply this clock to produce a full-rate sample clock, and this sample clock is used to sample the transmitter data output at T.

Figure 18-8. Transmitter Measurements Using a Golden Clock Multiplier



The Golden Clock Multiplier shown in the figure is a PLL or DLL that shall have a cutoff frequency equal to the frequency of the reference clock divided by 6, a 20 dB/decade rolloff, and has no peaking around the corner frequency.

19 CEI-56G-XSR-NRZ Extra Short Reach Interface

This clause details the requirements for the CEI-56G-XSR-NRZ extra short reach high speed electrical interface between nominal baud rates of 39.8 Gsym/s to 58.0 Gsym/s using NRZ coding. A compliant device must meet all of the requirements listed below. The electrical interface is based on high speed, low voltage DC-coupled logic with nominal differential impedance of 100 Ω and a channel with a nominal differential impedance of 92.5 Ω. Connections are point-to-point balanced differential pair and signalling is unidirectional.

The electrical IA is based on loss & jitter budgets and defines the characteristics required to communicate between a CEI-56G-XSR-NRZ driver and a CEI-56G-XSR-NRZ receiver using copper signal traces on a printed circuit board. The characteristic impedance of the signal traces is nominally 92.5 Ω differential. A 'length' is effectively defined in terms of its attenuation rather than physical length.

Extra short reach CEI-56G-XSR-NRZ devices from different manufacturers shall be interoperable.

19.1 Requirements

1. Support serial data rate from 39.8 Gsym/s to 58.0 Gsym/s. A CEI implementation complies to the specifications of this clause over the range of baud rates stated by the implementer within this range.
2. Capable of low bit error rate (10^{-15}, with a test requirement to verify 10^{-12}).
3. Capable of driving 0 – 50 mm of PCB trace.
4. Shall support DC-coupled operation.
5. Shall allow multi-lanes (1 to n).

19.2 General Requirements

19.2.1 Data Patterns

Please refer to Section 3.2.1.

19.2.2 Signal levels

The signal is a low swing DC coupled differential interface.

19.2.3 Signal Definitions

Please refer to Appendix 1.A.

A single clock signal is shared between the transmitting and receiving devices in the ingress direction and another single clock signal is shared between the transmitting and receiving devices in the egress direction, avoiding the need for a clock recovery circuit at the receiver.

19.2.4 Bit Error Ratio

Please refer to Section 3.2.3.

19.2.5 Ground Differences

As the driver and receiver are on the same PCB (with no intervening connectors), the ground difference is approximately 0 mV.

19.2.6 Cross Talk

Please refer to Section 3.2.5.

19.2.7 Channel Compliance

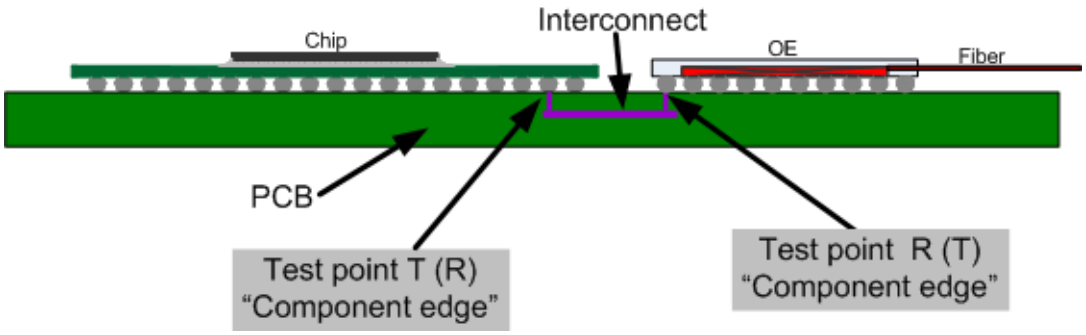
A forward channel and associated dominant crosstalk channels are deemed compliant if the channel characteristics conform to the requirements in this section.

19.2.7.1 Reference Model

The channel consists of PCB traces and any required vias. The reference PCB trace differential impedance is 92.5 Ω and all channel specifications are referenced to this impedance.

Figure 19-1 shows a diagram of the intended application.

Figure 19-1. CEI-56G-XSR-NRZ Reference Model



Several channel characteristics are parametrized according to Table 19-1 at these test points and are used for calculation of the channel parameters found in Table 19-2.

Table 19-1. Measured Channel Parameters

Symbol	Description
IL(f)	Differential insertion loss, -SDD21 magnitude (dB)
$RL_1(f)$	Differential input return loss, -SDD11 magnitude (dB)
$RL_2(f)$	Differential output return loss, -SDD22 magnitude (dB)
$NEXT_m(f)$	Differential near-end crosstalk loss (m^{th} aggressor), -SDD21 magnitude (dB)
$FEXT_n(f)$	Differential far-end crosstalk loss (n^{th} aggressor), -SDD21 magnitude (dB)

Table 19-2. Calculated Channel Parameters

Symbol	Description
$IL_{fitted}(f)$	Fitted insertion loss (dB)
ILD(f)	Insertion loss deviation (dB)
ICN(f)	Integrated crosstalk noise (mVRMS)
FOM_{ILD}	Channel Figure of merit - Weighted insertion loss deviation (dB)

19.2.7.2 Insertion Loss

Channel insertion losses, including PCB traces and connectors, shall comply with the limits specified by Equation (19-1), Equation (19-2) and plotted in Figure 19-2. Note that the variable f_b is the maximum baud rate to be supported by the channel under test (39.8 GHz < f_b < 58.0 GHz) and the measurement is to be made relative to the nominal impedance of 92.5 Ω.

Table 19-3. Channel Insertion Loss Frequency Range

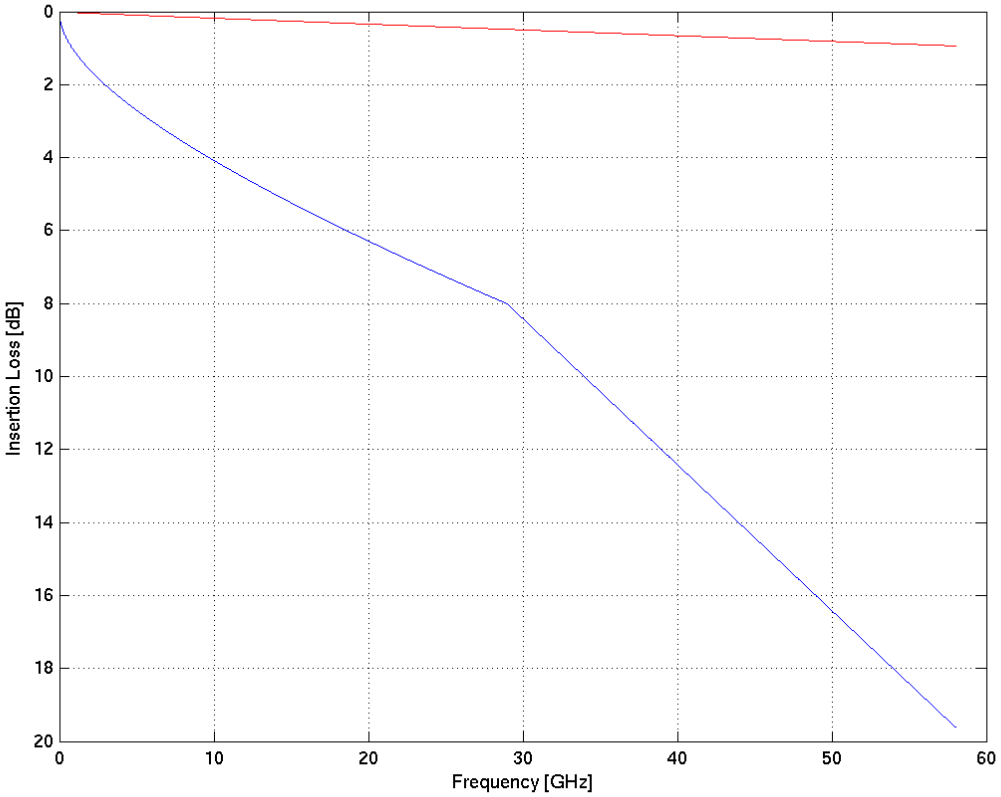
Parameter	Value	Units
f_{min}	50	MHz
f_{max}	f_b	GHz

$$IL_{max} = \begin{cases} 0.01 + 1.0\sqrt{\frac{f \times 58.0}{f_b}} + 0.09\frac{f \times 58.0}{f_b} & f_{min} \le f < \frac{f_b}{2} \\ -3.595 + 0.4\frac{f \times 58.0}{f_b} & \frac{f_b}{2} \le f \le f_b \end{cases} \quad (19\text{-}1)$$

$$IL_{min} = \begin{cases} 0.009\sqrt{f} + 0.015f & f_{min} \le f < f_b \end{cases} \quad (19\text{-}2)$$

Note: f in Equation (19-1) and Equation (19-2) is in GHz.

Figure 19-2. CEI-56G-XSR-NRZ normative channel insertion loss at 58.0 Gsym/s



19.2.7.3 Fitted Insertion Loss

For fitted insertion loss definitions, please refer to Section 12.2.1.1

The channel shall meet the insertion loss requirements defined in Table 19-4 and also meet the IL mask in Equation (19-1) and Equation (19-2). Note that the variable f_b is the maximum baud rate to be supported by the channel under test.

Table 19-4. Channel fitted insertion loss characteristics

Parameter	Units	Min Value	Max Value
Min frequency, f_{ILmin}	GHz	0.05	-
Max frequency, f_{ILmax}	GHz	-	fb
Fitted insertion loss at Nyquist	dB	-	8
Fitted insertion loss, a_0	dB	-1	2
Fitted insertion loss, a_1	dB	0	5
Fitted insertion loss, a_2	dB	0	16
Fitted insertion loss, a_4	dB	0	7.3

19.2.7.4 Insertion Loss Deviation (ILD)

The insertion loss deviation ILD is the difference between the measured insertion loss IL and the fitted insertion loss IL_{fitted} as defined in Equation (19-3) where f_{ILmin} and f_{ILmax} are given in Table 19-4.

$$ILD = IL - IL_{fitted} \qquad f_{ILmin} \le f \le (3/4) \times f_{ILmax} \tag{19-3}$$

The insertion loss deviation ILD shall be within the region defined by Equation (19-4).

$$-1.5 \le ILD \le 1.5 \tag{19-4}$$

A Figure Of Merit (FOM_{ILD}) for the channel is the weighted insertion loss deviation from f_{ILmin} to (3/4)*f_{ILmax}. FOM_{ILD} is calculated as indicated below. Note FOM_{ILD} is called ILD_{RMS} in OIF-CEI-03.0 clauses 10 & 11 and OIF-CEI-03.1 clauses 10, 11, 13 & 14.

Define the weight at each frequency *f* using Equation (19-5) below.

$$W(f) = \sin c^2(f/f_b)\left[\frac{1}{1+(f/f_t)^4}\right]\left[\frac{1}{1+(f/f_r)^8}\right] \tag{19-5}$$

Note that -3 dB transmit filter bandwidth f_t is inversely proportional to the minimum 20% to 80% rise and fall times T_*tr* and T_*tf*. The constant of proportionality is 0.2365 (i.e. min(T_*tr*, T_*tf*) x f_t = 0.2365, T_*tr* is in ns when f_t is in GHz). In addition, f_r is the -3 dB reference receiver bandwidth, which should be set at (3/4)f_b, where f_b is the maximum baud rate to be supported by the channel.

FOM_{ILD} is calculated using Equation (19-6) where N is the number of frequency points. The summation is done over the frequency range of ILD with *f* in GHz. FOM_{ILD} shall be less than 0.2 dB for compliant channels.

$$FOM_{ILD} = \sqrt{\frac{\sum W(f) \times ILD\langle f \rangle^2}{N}} \tag{19-6}$$

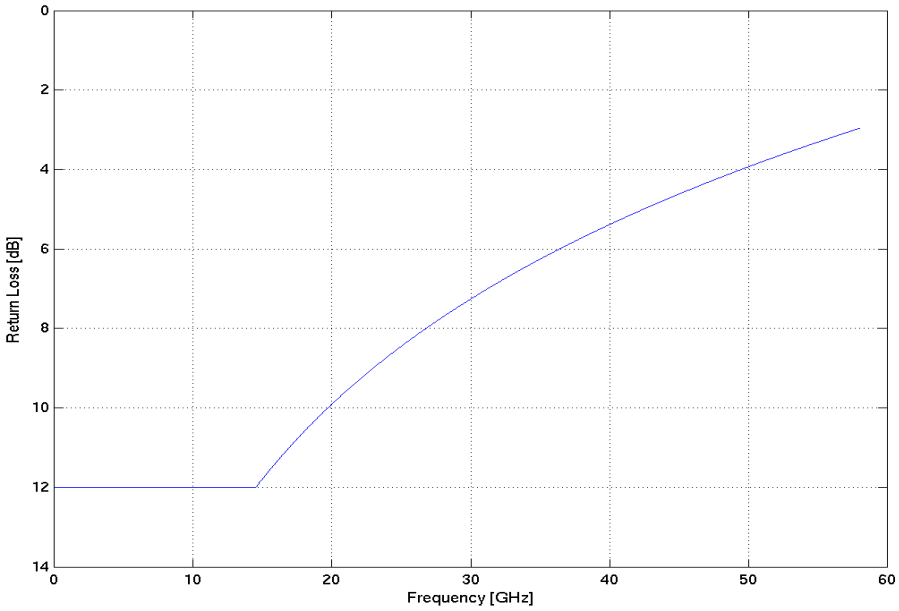
19.2.7.5 Channel Return Loss

Channel Return Loss shall be bounded by Equation (19-7) as shown in Figure 19-3 relative to the nominal impedance of 92.5 Ω.

$$\begin{aligned} RL(f) &> 12\ dB & f_{min} \le f \le \frac{f_b}{4} \\ RL(f) &> 12\ dB - 15\log_{10}\left(\frac{4f}{f_b}\right) & \frac{f_b}{4} < f \le f_b \end{aligned} \tag{19-7}$$

Note: f_{min} is as defined in Table 19-3

Figure 19-3. CEI-56G-XSR-NRZ normative channel return loss at 58.0 Gsym/s



19.2.7.6 Channel integrated crosstalk noise

Using the Integrated crosstalk noise method of Section 12.2.1.2 and the parameters of Table 19-5, the total integrated crosstalk noise for the channel shall be less than 2 mV_{RMS}.

Table 19-5. Channel integrated crosstalk aggressor parameters

Parameter	Symbol	Value	Units
Baud rate	f_b	max. Baud Rate supported by channel	Gsym/s
Near-end aggressor peak to peak differential output amplitude	A_{nt}	400	mVppd
Far-end aggressor peak to peak differential output amplitude	A_{ft}	400	mVppd
Near-end aggressor 20% to 80% rise and fall times	T_{nt}	4	ps
Far-end aggressor 20% to 80% rise and fall times	T_{ft}	4	ps

19.3 Electrical Characteristics

The electrical interface is based on high speed, low voltage DC-coupled logic with nominal differential impedance of 100 Ω and a channel with a nominal differential impedance of 92.5 Ω.

All devices shall work within the range 39.8 Gsym/s to 58.0 Gsym/s as specified for the device, with all ingress lanes synchronous to a common reference frequency having a stability of ± 100ppm from nominal and all egress lanes synchronous to a common reference frequency having a stability of ± 100ppm from nominal. The reference clocks of the ingress and egress directions are not necessarily synchronous to each other. Note that implementation of specific protocols will define the operating baud rate without affecting CEI compliance.

19.3.1 Reference Clock

Both ends of the link are to have a common clock frequency, which is set to be 1/64th of the baud rate. This clock could come from the same source or could be “forwarded” from the driver side to the receiver side. For details of applicable clock architecture options please refer to Annex 18.A.In a forwarded clock architecture the clock path needs to meet the same requirements as the data path. The electrical specifications at R_C are given in Table 19-6.

Table 19-6. Reference Clock Electrical Specification.

Characteristic	Symbol	Condition	MIN.	NOM.	MAX.	UNIT
Reference Clock Rate	Ref_Freq			f_b/64		GHz
Input Differential Voltage	Ref_Vdiff		240		900	mVppd
Input Single Ended Voltage	Ref_Vse		0.1		1.2	V
Differential Termination Resistance Mismatch	Ref_Rdm				5	%
Input Clock Rise and Fall Time (20% to 80%)	Ref_tr, Ref_tf		4		200	ps
Differential Input Return Loss	Ref_SDD11	at f_b/128 ≤ f < f_b/4 Note 1			-6	dB
Input Clock Duty Cycle	Ref_DC		40		60	%
High Frequency Uncorrelated Unbounded Gaussian Jitter	Ref_UUGJ_hf	Note 2			0.009	UI rms
Reference Clock Single Side Band Phase Noise	Ref_PN	@ 1kHz offset			-70	dBc/Hz
		@10kHz offset			-93	
		@100kHz offset			-113	
		@1MHz offset			-133	
		≥10MHz offset			-143	

NOTES:
1. Return loss is referenced to 100 Ohm
2. UUGJ measured using the methodology defined in Appendix 2.E.1 with a golden PLL cut-off frequency of fb/500, observing with a bandwidth of 43GHz

19.3.2 Transmitter Characteristics

The transmitter electrical specifications at compliance point T (see Figure 19-1) are given in Table 19-7. The transmitter shall satisfy jitter requirements specified in Table 19-8. Jitter is measured relative to the reference clock as timing source, using a golden clock multiplier as detailed in Annex 18.A.4, for a BER as specified in Section 3.2.3. It is assumed that the UBHPJ component of the transmitter jitter is not data-dependent jitter (DDJ) from the receiver view point, hence it cannot be equalized in the receiver. To attenuate noise and absorb even/odd mode reflections, the transmitter shall satisfy the Common Mode Output Return Loss requirement of Table 19-7. The waveform is observed through a fourth-order Bessel-Thomson response with a bandwidth of 43 GHz using a PRBS31 pattern.

The link budget in this document assumes no Tx emphasis.

Table 19-7. Transmitter Electrical Output Specification.

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	T_Baud		39.8		58.0	Gsym/s
Output Differential Voltage	T_Vdiff		250		400	mVppd
Single Ended Transmitter Output Voltage Note 1	T_Vse		0.1		1.2	V
Differential Termination Resistance Mismatch	T_Rdm				5	%
Output Rise and Fall Time (20% to 80%)	T_tr, T_tf		4			ps
Differential Output Return Loss	T_SDD22	See 19.3.2.2 Note 2				dB
Common mode Output Return Loss	T_SCC22	200MHz to $f_b/2$			-6	dB
Transmitter Common Mode Noise	T_Ncm				15	mVrms

NOTES:
1. DC Coupling compliance is mandatory.
2. Return loss is referenced to 100 Ohm

Table 19-8. Transmitter Output Jitter Specification

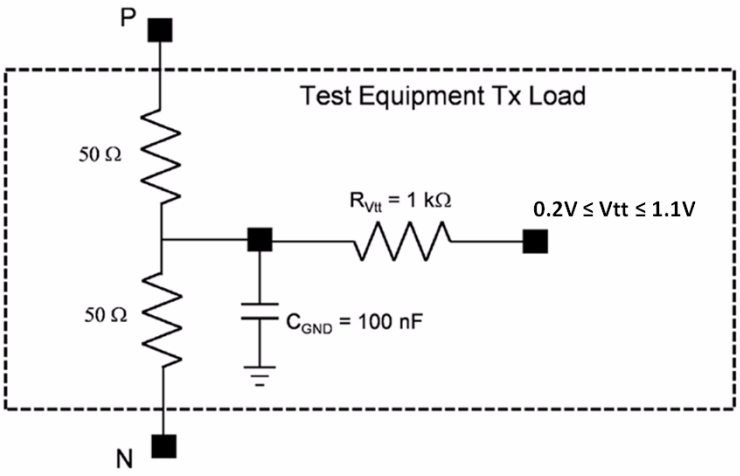
Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Uncorrelated Unbounded Gaussian Jitter	T_UUGJ				0.15	UIpp
Uncorrelated Bounded High Probability Jitter	T_UBHPJ				0.15	UIpp
Even Odd jitter (component of UBHPJ)	T_EOJ	Note 2			0.035	UIpp
Total Jitter	T_TJ	Note 1			0.28	UI
Eye Mask	T_X1	See 19.3.2.4			0.14	UI
Eye Mask	T_X2	See 19.3.2.4			0.4	UI
Eye Mask	T_Y1	See 19.3.2.4	125			mV
Eye Mask	T_Y2	See 19.3.2.4			200	mV

NOTES:
1. T_TJ includes all of the jitter components.
2. Included in T_UBHPJ. Even-odd jitter is defined in Table 1-3.

19.3.2.1 Transmitter Amplitude and Swing

Transmitter differential output amplitude shall be able to drive between 250 and 400 mVppd. Further the single-ended voltage must be between 0.1 and 1.2 V. Figure 19-4 shows the transmitter test load configuration.

Figure 19-4. Transmitter Amplitude Test Load



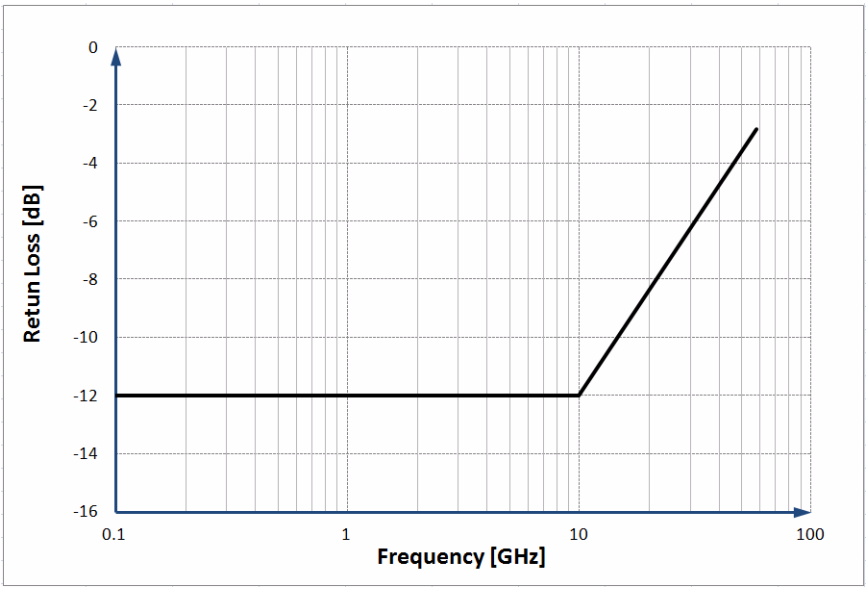
19.3.2.2 Transmitter Resistance and Return Loss

Please refer to Section 3.2.10 with the following parameters in Table 19-9 and as illustrated in Figure 19-5.

Table 19-9. Driver Return Loss Parameters

Parameter	Value	Units
A0	-12	dB
f0	100	MHz
f1	0.1714 x T_Baud	Hz
f2	T_Baud	Hz
Slope	12.0	dB/dec

Figure 19-5. Illustration of Return Loss for T_Baud = 58.0 Gsym/s



19.3.2.3 Transmitter Lane-to-Lane Skew

Please refer to Section 3.2.7.

19.3.2.4 Transmitter Template and Jitter

When provided with the reference clock meeting the specifications in Section 19.3.1 as a timing source, using a golden clock multiplier as detailed in Annex 18.A.4, for a BER as per Section 3.2.3, the transmitter shall satisfy the eye template and jitter requirements as given in Table 19-8 and Figure 1-4. The measurement of jitter and eye diagram is to be relative to the “forwarded” clock if the transmitter provides one. If it does not provide a “forwarded” clock then the measurement is to be relative to the reference clock provided to it.

19.3.3 Receiver Characteristics

A compliant receiver shall operate at the specified BER with the worst case combination of a compliant transmitter and a compliant channel.

Receiver electrical specifications are given in Table 19-10 and measured at compliance point R. To dampen noise sources and absorption of both even and odd mode reflections, the receiver shall satisfy the Common Mode Input Return Loss requirement of Table 19-10.

Table 19-10. Receiver Electrical Input Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	R_Baud		39.8		58.0	Gsym/s
Input Differential Voltage	R_Vdiff	Note 1			400	mVppd
Receiver Common Mode Noise Tolerance	R_Ncm				25	mVrms
Differential Termination Resistance Mismatch	R_Rm				5	%
Differential Input Return Loss	R_SDD11	See 19.3.3.2 Note 2				dB
Common mode Return Loss	R_SCC11	200 MHz to10 GHz			-6	dB
		10 GHz to f_b			-4	dB
Rx Input Single Ended Voltage Range	R_V_{inSE}		0.1		1.2	V

NOTES:
1. The receiver shall have a differential input voltage range sufficient to accept a signal produced at point R by the combined transmitter and channel. The channel response shall include the worst case effects of the return losses at the transmitter and receiver
2. Return loss is referenced to 100 Ohm

When provided with the reference clock meeting the specifications in Section 19.3.1 as a timing source, the receiver shall tolerate the sum of these jitter contributions and meet the BER as per Section 3.2.3: the total transmitter jitter from Table 19-8 and the effects of a channel compliant to the Channel Characteristics (Section 19.2.7).

19.3.3.1 Reference Receiver Input Signals

The receiver shall accept differential input signal amplitudes produced by a compliant transmitter connected with the minimum attenuation specified in Equation (19-2) to the receiver. This may be larger than the 400 mVppd maximum of the transmitter due to output/input impedances and reflections.

The minimum input amplitude is defined by the minimum transmitter amplitude, the actual receiver input impedance and the loss of the actual PCB. Note that the minimum transmitter amplitude is defined using a well controlled load impedance; however the real receiver's impedance may differ, which can leave the receiver input signal smaller than expected. Additionally the real receiver may be affected by environmental noise.

19.3.3.2 Receiver Return Loss

Please refer to Section 3.2.10 with the following parameters in Table 19-11 and as illustrated in Figure 19-5.

Table 19-11. Receiver Input Return Loss Parameters

Parameter	Value	Units
A0	-12	dB
f0	100	MHz
f1	0.1714 x R_Baud	Hz
f2	R_Baud	Hz
Slope	12.0	dB/dec

19.3.3.3 Input Lane-to-Lane Skew

Please refer to Section 3.2.8.

20 CEI-56G-XSR-PAM4 Extra Short Reach Interface

This clause details the requirements for the CEI-56G-XSR-PAM4 extra short reach high speed electrical interface between nominal baud rates of 18.0 Gsym/s and 29.0 Gsym/s using PAM-4 coding. A compliant device shall meet all of the requirements listed below. The electrical interface is based on high speed, low voltage DC-coupled logic with nominal differential impedance of 100 Ω and a channel with nominal differential impedance of 92.5 Ω. Connections are point-to-point balanced differential pairs and signaling is unidirectional.

The electrical IA is based on loss and jitter budgets and defines the characteristics required to communicate between a CEI-56G-XSR-PAM4 transmitter and a CEI-56G-XSR-PAM4 receiver using copper signal traces on a printed circuit board. Refer to Section 20.2.7 for channel requirements.

Extra short reach CEI-56G-XSR-PAM4 devices from different manufacturers shall be interoperable.

20.1 Requirements

1. Support serial baud rates within the range from 18.0 Gsym/s to 29.0 Gsym/s. A CEI implementation complies to the specifications of this clause over the range of baud rates stated for the implementation within this range.
2. Capable of achieving a raw Bit Error Ratio performance of 10^{-9} or better per lane. FEC is assumed to be used in the system to achieve corrected BER of 10^{-15} or better per lane. The baud rate includes the overhead required for FEC. The definition of FEC is outside the scope of this IA (see Appendix 16.D).
3. Capable of driving 0 - 50 mm of PCB trace.
4. Shall support DC-coupled operation.
5. Shall allow multi-lanes (1 to n).

20.2 General Requirements

20.2.1 Data Patterns

See 16.C.5.

20.2.2 Signal levels

The signal is a low swing DC-coupled differential interface.

20.2.3 Signal Definitions

Please refer to Section 1.A

20.2.4 Bit Error Ratio

A raw Bit Error Ratio (BER) better than or equal to 10^{-9} is required on each lane. A compliant receiver, when receiving from a compliant transmitter, shall deliver the specified raw BER to the subsequent FEC decoder. Error bursts with length more than 15 PAM4 symbols delivered to the PAM4 decoder shall occur with a probability of less than 1 in 10^{20} PAM4 symbols. See Appendix 16.D.

Specifications for the Tx, Rx, and channel are included in this clause all of which must be met to ensure that the required BER performance is met.

20.2.5 Ground Differences

As the transmitter and receiver are on the same PCB (with no intervening connectors), the ground difference is approximately 0 mV.

20.2.6 Crosstalk

Please refer to Section 3.2.5.

20.2.7 Channel Compliance

A forward channel and associated dominant crosstalk channels are deemed compliant if the channel characteristics conform to the requirements in this section.

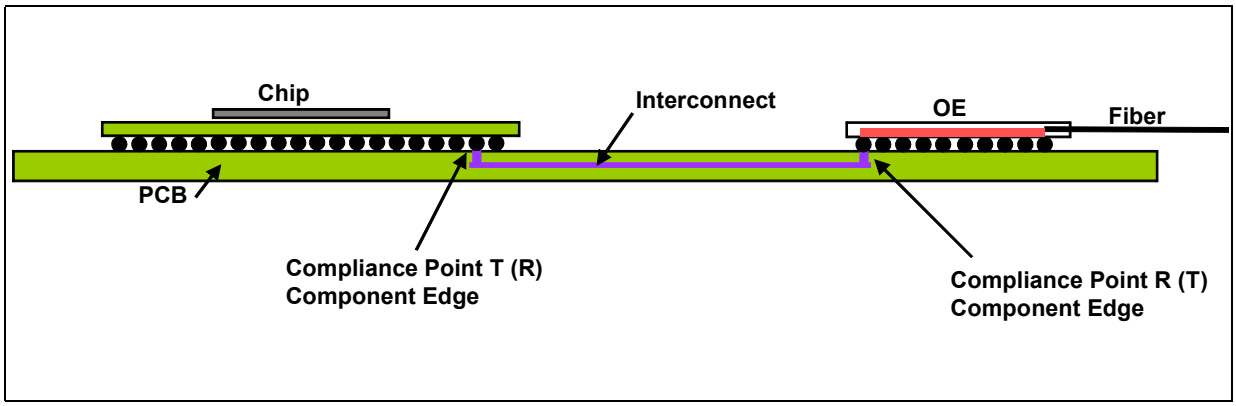
20.2.7.1 Reference Model

A single clock signal is shared between the transmitters and receivers in one direction and a single clock signal is shared between the transmitters and receivers in the opposite direction, avoiding the need for a clock recovery circuit at the receivers.

The channel consists of PCB traces and any required vias. The reference differential impedance for the channel is 92.5 Ω.

Figure 20-1 shows a diagram of compliance points on an example board.

Figure 20-1. CEI-56G-XSR-PAM4 Reference Model



Several channel characteristics are parametrized according to Table 20-1 at these compliance points and are used for calculation of the channel parameters found in Table 20-2.

Table 20-1. Measured Channel Parameters

Symbol	Description
$IL(f)$	Differential insertion loss, -SDD21 magnitude (dB)
$RL_1(f)$	Differential input return loss, -SDD11 magnitude (dB)
$RL_2(f)$	Differential output return loss, -SDD22 magnitude (dB)
$NEXT_m(f)$	Differential near-end crosstalk loss (m^{th} aggressor), -SDD21 magnitude (dB)
$FEXT_n(f)$	Differential far-end crosstalk loss (n^{th} aggressor), -SDD21 magnitude (dB)

Table 20-2. Calculated Channel Parameters

Symbol	Description
$IL_{fitted}(f)$	Fitted insertion loss (dB)
$ILD(f)$	Insertion loss deviation (dB)
$ICN(f)$	Integrated crosstalk noise (mV, RMS)
FOM_{ILD}	Channel Figure of Merit - Weighted insertion loss deviation (dB)

20.2.7.2 Insertion Loss

Channel insertion losses, including PCB traces, shall comply with the limits specified by Equation 20-1 and Equation 20-2 and plotted in Figure 20-2 using parameters in Table 20-3. Note that the variable f_b is the baud rate to be supported by the channel under test

(18.0 Gsym/s ≤ f_b ≤ 29.0 Gsym/s).

Table 20-3. Channel Insertion Loss Frequency Range

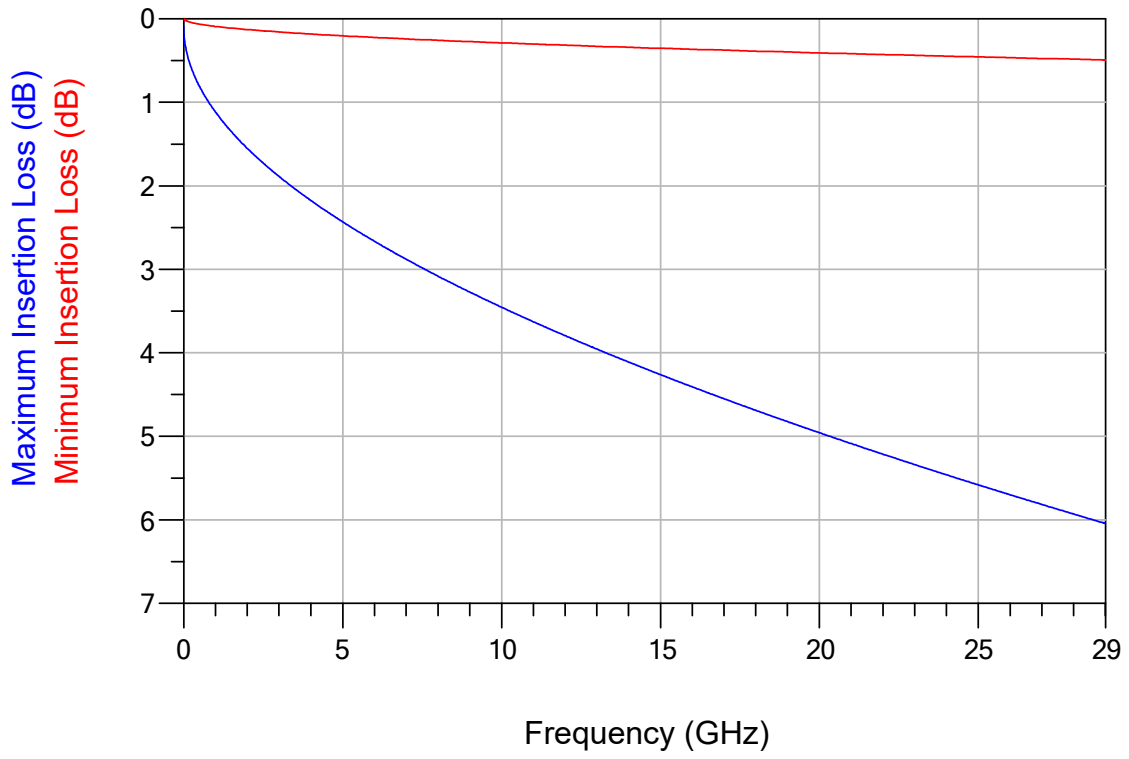
Parameter	Value	Units
fmin	50	MHz
fmax	f_b	GHz

$$IL_{max} = 0.1 + \sqrt{\frac{f \times 29}{f_b}} + 0.0193 \times \frac{f \times 29}{f_b} \qquad f_{min} \le f \le f_b \tag{20-1}$$

$$IL_{min} = 0.0913 \sqrt{\frac{f \times 29}{f_b}} \qquad f_{min} \le f \le f_b \tag{20-2}$$

Note: f in Equation 20-1 and Equation 20-2 is in GHz. The channel insertion loss is relative to a 92.5 Ω differential impedance.

Figure 20-2. CEI-56G-XSR-PAM4 Normative Channel Insertion Loss at 29.0 Gsym/s



20.2.7.3 Fitted Insertion Loss

For fitted insertion loss definitions, please refer to Section 12.2.1.1

The channel shall meet the insertion loss requirements defined in Table 20-4 and also meet the Insertion Loss mask in Equation 20-1 and Equation 20-2. Note that the variable f_b is the baud rate to be supported by the channel under test.

Table 20-4. Channel fitted insertion loss characteristics

Parameter	Units	Value	
		Min.	Max.
Minimum frequency, f_{ILmin}	GHz	0.05	-
Maximum frequency, f_{ILmax}	GHz	-	f_b
Fitted Insertion loss at Nyquist	dB	0.35	4.25
Fitted insertion loss, a_0	dB	-1	2
Fitted insertion loss, a_1	dB	0	3.7
Fitted insertion loss, a_2	dB	0	8.5
Fitted insertion loss, a_4	dB	0	3.9

20.2.7.4 Insertion Loss Deviation (ILD)

The insertion loss deviation *ILD* is the difference between the measured insertion loss *IL* and the fitted insertion loss IL_{fitted} as defined in Equation 20-3.

$$ILD = IL - IL_{fitted} \qquad f_{ILmin} \le f \le f_{ILmax} \tag{20-3}$$

The insertion loss deviation ILD shall be within the region defined by Equation 20-4.

$$-1.0 \le ILD \le 1.0 \tag{20-4}$$

FOM_{ILD}, a figure of merit for the channel, is derived from the weighted insertion loss deviation (dB) from f_{ILmin} to (3/4)*f_{ILmax} as indicated below.

Define the weight at each frequency f using Equation 20-5 below.

$$W(f) = \mathrm{sinc}^2(f/f_b)\left[\frac{1}{1+(f/f_t)^4}\right]\left[\frac{1}{1+(f/f_r)^8}\right] \tag{20-5}$$

Note that -3 dB transmit filter bandwidth f_t is inversely proportional to the minimum 20% to 80% rise and fall times, *T_tr and T_tf,* respectively. The constant of proportionality is 0.2365 (e.g. min(T_tr,T_tf) *x* f_t = 0.2365), where T_tr is in nano seconds and f_t is in GHz. In addition, f_r is the -3 dB reference receiver bandwidth, which should be set at (3/4)f_b, where f_b is the baud rate to be supported by the channel.

$$FOM_{ILD} = \sqrt{\frac{\sum_{i=1}^{N} W(f_i) \times ILD(f_i)^2}{N}} \quad (20\text{-}6)$$

where N is the number of frequency points, the summation is done over the frequency range of ILD with f in GHz.

FOM_{ILD} shall be less than 0.1 dB for compliant channels.

Note: FOM_{ILD} is called ILD_{RMS} in OIF-CEI-03.0 clauses 10 & 11 and OIF-CEI-03.1 clauses 10, 11, 13 & 14.

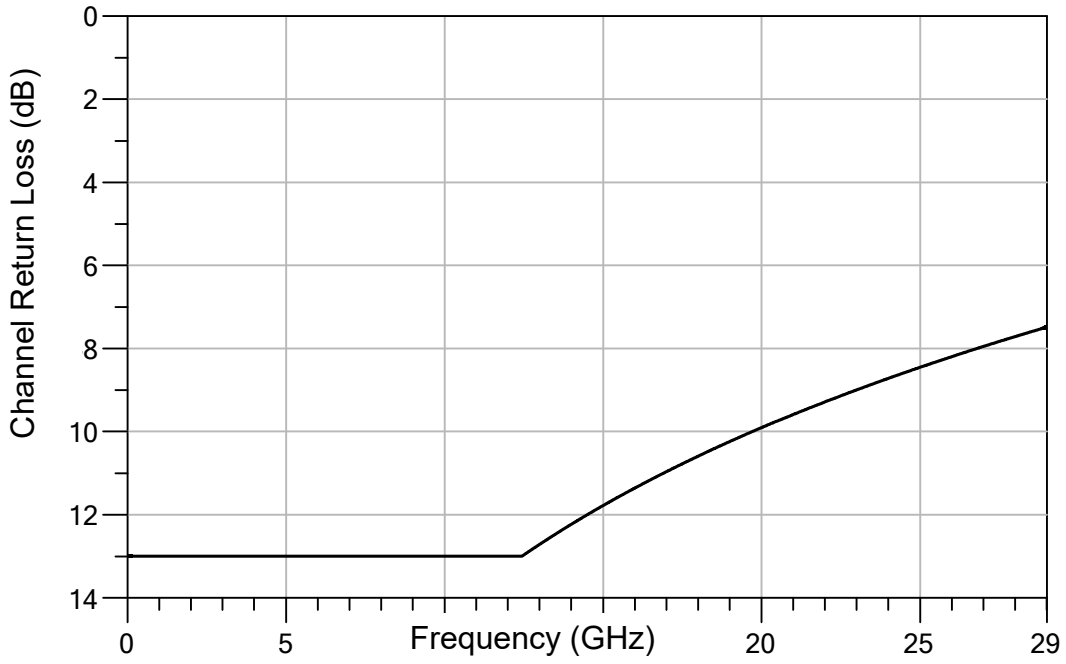
20.2.7.5 Channel differential return loss

Channel differential return loss shall be bounded by:

$$RL(f) \geq 13 \qquad f_{min} \leq f \leq 0.4288 f_b$$
$$RL(f) \geq 12 - 15 \log_{10}(2f/f_b) \qquad 0.4288 f_b < f \leq f_b \quad (20\text{-}7)$$

Where f_{min} is given in Table 20-3. The channel return loss is relative to a 92.5 Ω differential impedance.

Figure 20-3. CEI-56G-XSR-PAM4 Normative Channel Return Loss at 29 Gsym/s



20.2.7.6 Channel integrated crosstalk noise

Using the integrated crosstalk noise method of Section 12.2.1.2 and the parameters of Table 20-5, the total integrated crosstalk noise for the channel shall be less than 1 mV RMS. The ICN calculation method of Section 12.2.1.2, which was originally intended for NRZ interfaces is used here despite this being a PAM4 interface.

Table 20-5. Channel integrated crosstalk aggressor parameters

Parameter	Symbol	Value	Units
Baud rate	f_b	max. Baud Rate sup. by Channel	Gsym/s
Near-end aggressor peak to peak differential output amplitude	A_{nt}	600	mVppd
Far-end aggressor peak to peak differential output amplitude	A_{ft}	600	mVppd
Near-end aggressor 20% to 80% rise and fall times	T_{nt}	7.5	ps
Far-end aggressor 20% to 80% rise and fall times	T_{ft}	7.5	ps

20.3 Electrical Characteristics

A CEI implementation complies to the specifications of this clause over the range of baud rates stated for the implementation, within the range from 18.0 Gsym/s to 29.0 Gsym/s, and with the baud rate tolerance as per Section 3.2.11.

CEI-56G-XSR-PAM4 requires all ingress lanes be synchronous to a common reference clock having a stability of ± 100 ppm from nominal and all egress lanes be synchronous to a common reference clock having a stability of ± 100 ppm from nominal. The reference clocks of the ingress and egress directions are not necessarily synchronous to each other.

20.3.1 Reference Clock

Both ends of the link are to have a common clock frequency, which is set to be 1/64th of the baud rate. The clock either comes from the same source or is “forwarded” from the transmitter side to the receiver side (see Annex 18.A for additional details). The electrical specifications are given in Table 20-6.

Table 20-6. Reference Clock Electrical Specification at R_C

Characteristic	Symbol	Condition	MIN.	NOM.	MAX.	UNIT
Clock Rate	Ref_Freq			fb/64		GHz
Differential Voltage	Ref_Vdiff		240		900	mVppd
Single Ended Voltage	Ref_Vse		0.1		1.2	V
Differential Termination Resistance Mismatch	Ref_Rdm				5	%
Clock Rise and Fall Time (20% to 80%)	Ref_tr, Ref_tf		9		200	ps
Differential Input Return Loss	Ref_SDD11	at fb/128 < f < fb/4 See Note 1			-6	dB
Clock Duty Cycle	Ref_DC		40		60	%
High Frequency Uncorrelated Unbounded Gaussian Jitter (UUGJ-hf)	Ref_UUGJ_hf	See Notes 2, 3			0.009	UIrms
Clock Single Side Band Phase Noise	Ref_PN	@ 1 kHz offset			-70	dBc/Hz
		@ 10 kHz offset			-93	
		@ 100 kHz offset			-113	
		@ 1 MHz offset			-133	
		> 10 MHz offset			-143	

NOTES:
1. Return loss is reference to 100 Ω. differential impedance.
2. UUGJ measured using the methodology defined in Appendix 2.E.1, with a golden PLL cut-off frequency of fb/500, observed with a bandwidth of 43 GHz.
3. 1 UI = 1/fb

20.3.2 Transmitter Characteristics

The transmitter electrical specifications at compliance point T are given in Table 20-7. The transmitter shall satisfy Eye Height and Eye Width requirements specified in Table 20-8. These requirements are measured relative to the reference clock as timing source, using a golden clock multiplier as detailed in Annex 18.A.4, for a BER as specified in Section 3.2.3. To attenuate noise and absorb even/odd mode reflections, the transmitter shall satisfy the Common Mode Output Return Loss requirement of Table 20-7. The waveform is observed with a fourth-order Bessel-Thomson low-pass filter response having a 3-dB bandwidth of 40 GHz using a QPRBS13-CEI pattern defined in Appendix 16.C.3.1. (Note: QPRBS13-CEI is used as the test pattern so an accurate software filter response can be used for the 40 GHz Bessel-Thomson filter response. However this pattern does not exercise the low-frequency response of the system).

Link budgets in this clause assume no Tx emphasis.

Table 20-7. Transmitter Electrical Output Specification

Characteristic	Symbol	Condition	MIN.	NOM.	MAX.	UNIT
Baud Rate	T_Baud		18.0		29.0	Gsym/s
Output Differential Voltage	T_Vdiff	See Notes 1 & 2			600	mVppd
Eye Linearity		See Note 3	0.85			-
Single-ended Transmitter Output Voltage	T_Vse		0.1		1.2	V
Differential Resistance	T_Rd		80	100	120	Ω
Differential Termination Resistance Mismatch (see Table 1-2)	T_Rdm				5	%
Output Transition Time (20% to 80%)	T_tr, T_tf	See Appendix 16.C.4.1	7.5			ps
Differential Output Return Loss	T_SDD22	See Section 20.3.2.2				dB
Common Mode to Differential Mode Conversion	T_SDC22	See Equation 16-3 in Section 16.3.8				dB
Common Mode Output Return Loss	T_SCC22	200 MHz to fb			-6	dB
Transmitter Common Mode Noise	T_Ncm				12	mVrms

NOTES:
1. DC Coupling compliance is mandatory.
2. Output differential voltage is defined as peak-to-peak voltage with QPRBS13-CEI pattern.
3. Eye linearity = min(AVupp, AVmid, AVlow) / max(AVupp, AVmid, AVlow) See 16.C.4.2 for details.

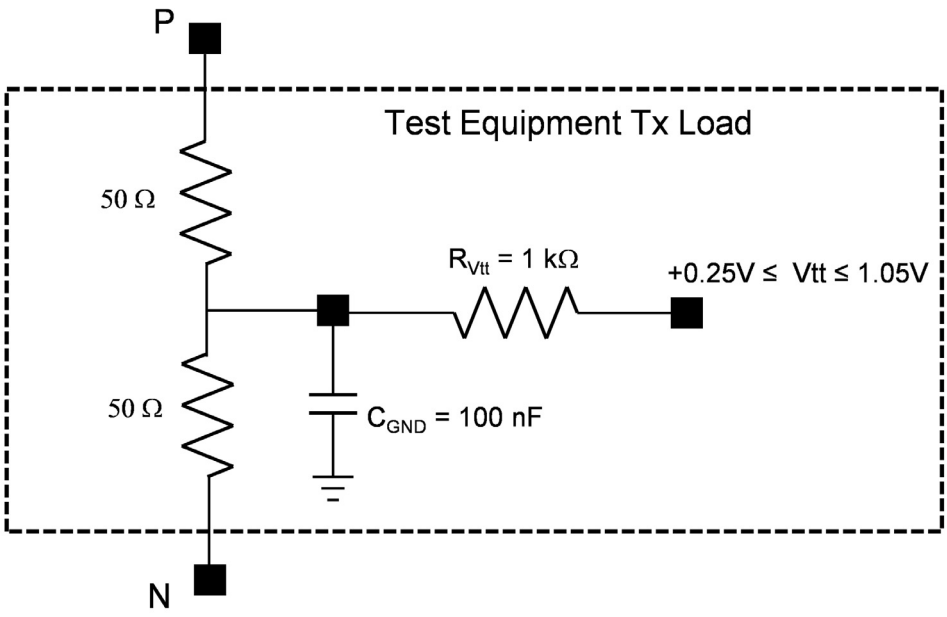
Table 20-8. Transmitter Eye Width and Eye Height

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Eye Width at 10^{-9} Probability	EW9		0.36			UI
Eye Height at 10^{-9} Probability	EH9		40			mV

20.3.2.1 Transmitter Amplitude and Swing

Transmitter differential output amplitude shall be able to drive between 400 to 600 mVppd. Further the single-ended voltage must be between +0.1 and 1.2 V. Figure 20-4 shows a compliant transmitter test load configuration.

Figure 20-4.Transmitter Amplitude Test Load



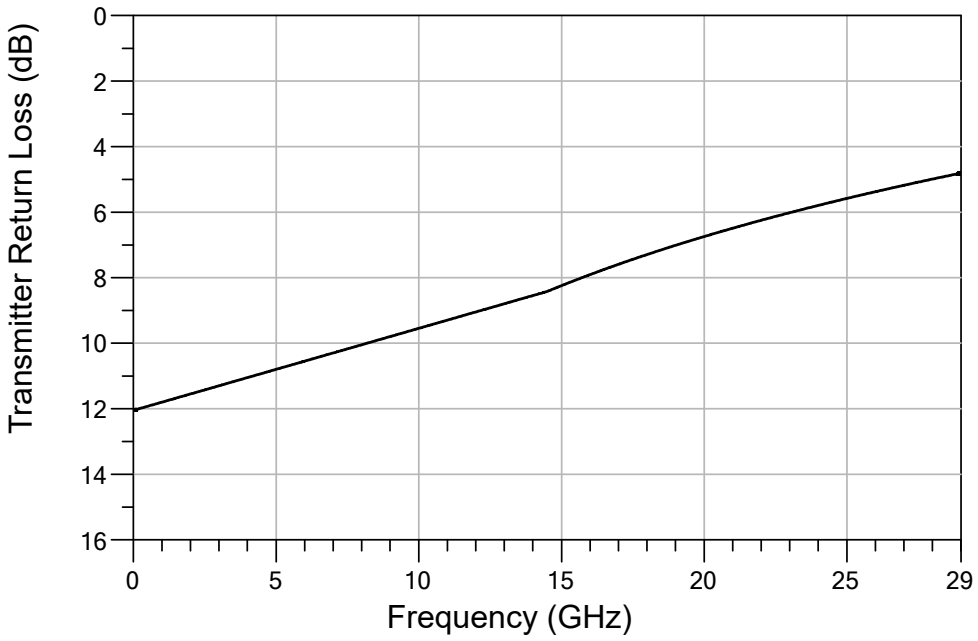
20.3.2.2 Transmitter Return Loss

Transmitter differential return loss shall be bounded by:

$$RL(f) \geq 12.05 - 0.25(29f/f_b) \quad f_{min} \leq f \leq 0.5f_b$$
$$RL(f) \geq 14 - 12\log_{10}(f/(0.1714f_b)) \quad 0.5f_b < f \leq f_b \qquad (20\text{-}8)$$

Where f_{min} is given in Table 20-3.

Figure 20-5. CEI-56G-XSR-PAM4 Transmitter Return Loss at 29 Gsym/s



20.3.2.3 Transmitter Lane-to-Lane Skew

Please refer to Section 3.2.7.

20.3.2.4 Transmitter Compliance at Test Point T

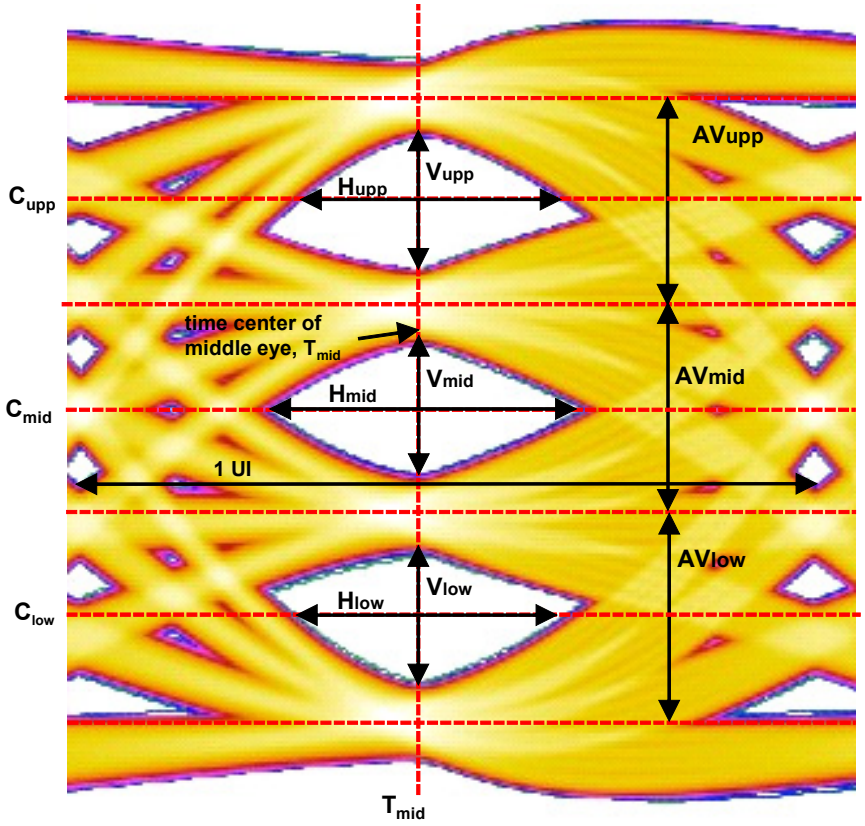
When provided with the reference clock meeting the specifications in Section 20.3.1 as a timing source, using a golden clock multiplier as detailed in Annex 18.A.4, for a BER as per Section 3.2.3, the transmitter shall satisfy the eye parameters as given in Table 20-7 and Table 20-8. All co-propagating and counter-propagating lanes are active as crosstalk sources, using a QPRBS13-CEI test pattern as defined in Appendix 16.C.3.1, or a QPRBS31-CEI test pattern as defined in Appendix 16.C.3.2, or a valid CEI signal. The patterns on all pairs of aggressor lanes or lane under test should be asynchronous to each other or sufficiently delayed relative to each other to remove correlation between all pairs of aggressor lanes and between the lane under test and all aggressor lanes. The measurement of the eye parameters is to be relative to the “forwarded” clock if the transmitter provides one. If it does not provide a “forwarded” clock then the measurement is to be relative to the reference clock provided to it.

20.3.2.4.1 PAM4 Eye Definitions and Parameters

All relevant PAM-4 eye parameters are determined from 10^{-9} contours generated from oscilloscope CDF/histogram data except for Tmid which is determined from a 10^{-3} contour of the middle eye and Cmid, Cupp, and Clow which are derived from 10^{-6} contours. The 10^{-6} eye contours are constructed from each individual eye’s contributing

symbols. For example, the EH6 measurement may be based on a total of 64 million captured PAM4 symbols, at a rate of one sample per symbol, with 32 million samples per individual eye (with the two middle levels (i.e. +1/3 and -1/3) used for the outer eyes and the middle eye). Similarly, the EW6 measurement may be based on 32 million edges for the middle eye and 24 million edges for the upper and lower eyes.

Figure 20-6. PAM4 Eye definitions and parameters



1. Tmid - the midpoint of the maximum horizontal eye opening of the 10^{-3} inner eye contour of the middle eye

2. Vmid - the 10^{-9} inner Eye Height of the middle eye determined from voltage CDFs in a +/- 0.025 UI time window centered on Tmid

3. Vupp - the 10^{-9} inner Eye Height of the upper eye determined from voltage CDFs in a +/- 0.025 UI time window centered on Tmid

4. Vlow - the 10^{-9} inner Eye Height of the lower eye determined from voltage CDFs in a +/- 0.025 UI time window centered on Tmid

5. AVmid, the Eye Amplitude of the middle eye, is the difference of the mean levels of the 1/3 level and -1/3 level voltage histograms in the time window used in Step 2

6. AVupp, the Eye Amplitude of the upper eye, is the difference of the mean levels of the 1 level and 1/3 level voltage histograms in the time window used in Step 3

7. AVlow, the Eye Amplitude of the lower eye, is the difference of the mean levels of the -1/3 level and -1 level voltage histograms in the time window used in Step 4

8. Cmid, the midpoint of the vertical eye opening of the 10^{-6} points determined from the voltage CDFs of Step 2

9. Cupp, the midpoint of the vertical eye opening of the 10^{-6} determined from the voltage CDFs of Step 2

10. Clow, the midpoint of the vertical eye opening of the 10^{-6} eye determined from the voltage CDFs of Step 2

11. Hmid - the 10^{-9} inner eye width determined from CDFs of eye edges at the Cmid threshold

12. Hupp - the 10^{-9} inner eye width determined from CDFs of eye edges at the Cupp threshold

13. Hlow - the 10^{-9} inner eye width determined from CDFs of eye edges at the Clow threshold

14. TL6 - the time of a 10^{-6} eye contour's left edge

15. TR6 - the time of a 10^{-6} eye contour's right edge

20.3.2.4.2 Transmitter Output Eye Test Methodology

The approach described in this clause is based upon first locating the midpoint (Tmid) of the middle eye's maximum horizontal eye opening and using that information to determine its vertical eye opening (Vmid) and the vertical eye opening of the upper and lower eyes, Vupp and Vlow, respectively based on the same time window.

The test method for measuring the Transmitter output Eye Width and Eye Height as illustrated in Figure 20-6 and Figure 20-7 is as follows:

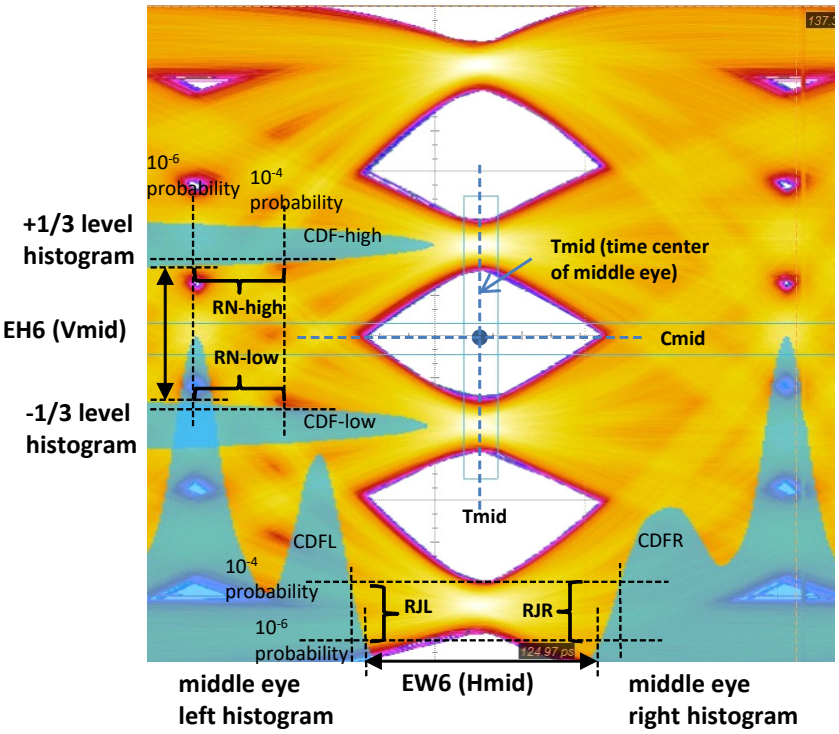
1) Set the Transmitter to QPRBS13-CEI pattern (see Appendix 16.C.3.1).

-This allows the use of a sampling oscilloscope with a pattern lock.

2) Capture the differential signal at Compliance Point T with a scope triggered with the clock generated by a golden PLL from the fb/64 reference clock (see Annex 18.A).

-Sample the signal with a minimum of 3 samples per PAM4 symbol, or equivalent. Collect sufficient samples equivalent to 8 million PAM4 symbols in order to construct normalized cumulative distribution functions (normalized CDFs) (see Figure 20-7) of the captured signals to a probability of 10^{-6} (without extrapolation) as described below. Depending on the sampling rate, careful interpolation using a method such as sin(x)/x or cubic spline may be needed for good accuracy.

Figure 20-7. Test Point Eye Width and Eye Height parameters



3) Use the captured signal from step 2 to construct the CDFs of the signal voltage in the central 5% of the time window centered on Tmid for the middle eye (as defined below and shown in Figure 20-7), for both logic levels, logic high (CDF-high) and logic low (CDF-low).

Calculate the Eye Height, EH6, for the middle eye as the difference in voltage between CDF-high and CDF-low with a value of 10^{-6}. CDF-high and CDF-low are calculated as the cumulative sum of histograms of the voltage samples at the top and bottom of the eye normalized by the total number of sampled symbols (e.g., the number of sampled symbols is 8 million as specified in step 2). For a pattern with a well balanced number of -1s, -1/3s, +1/3s and +1s the maximum value for CDF-high and CDF-low will each be 0.25.

4) Apply dual-Dirac and tail fitting techniques to CDF-high and CDF-low to estimate noise in the central 5% of the eye. Calculate the best linear fit in Q-scale over the range of probabilities of 10^{-4} to 10^{-6} of the CDF-high and CDF-low to yield RN-high and RN-low respectively.

-RN-high is the RMS value of the noise estimated above from CDF-high.

-RN-low is the RMS value of the noise estimated above from CDF-low.

-Eye Height (EH9) at 10^{-9} probability equals (EH6 - 1.2444*(RN-low+RN-high)).

5) Use the captured signal from step 2 to construct CDFs of eye edges at Cmid for both the left edge (CDFL) and the right edge (CDFR), as a distance in time from the middle of the eye (Tmid).

CDFL and CDFR are calculated as the cumulative sum of histograms at the left and right edges of the eye normalized by the total number of sampled symbols. For the QPRBS13-CEI pattern the maximum value for the CDFL and CDFR will be 0.5. CDFL and CDFR are equivalent to bathtub curves where the bit error ratio (BER) is plotted versus sampling time.

Calculate the Eye Width EW6 as the difference in time between CDFR and CDFL with a value of 10^{-6}.

6) Apply Dual-Dirac and tail fitting technique (See Keysight white paper: 5989-3206EN) separately to CDFL and CDFR to estimate random jitter. Calculate the best linear fit in Q-scale over the range of probabilities of 10^{-4} to 10^{-6} of the CDFL and CDFR to yield RJL and RJR respectively.

-RJL is the RMS value of the jitter estimated from CDFL.

-RJR is the RMS value of the jitter estimated from CDFR.

-Eye Width (EW9) at 10^{-9} probability is equal to (EW6 - 1.2444*(RJL+RJR)).

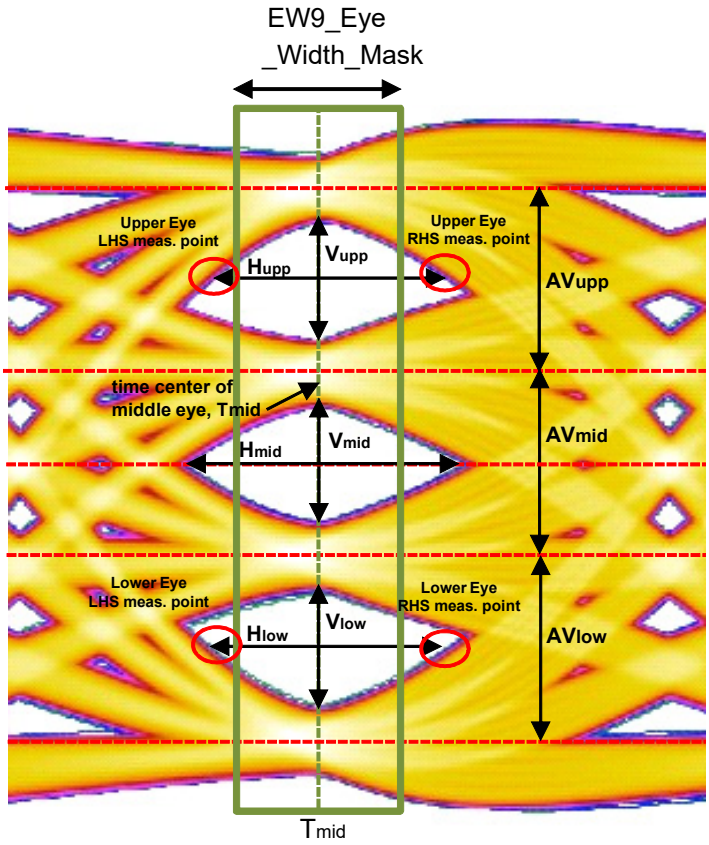
7) Repeat steps 3) and 4) for both the upper and lower eyes based on constructed CDFs of the signal voltages in the central 5% of the time windows centered on the Tmid determined for the middle eye.

8) Repeat steps 5) and 6) for both the upper and lower eyes based on constructed CDFs of eye edges of the upper and lower eyes, at Cupp and Clow respectively. However note that the maximum values for the CDFL and CDFR will be 0.375 rather than 0.5.

9) At Transmitter Compliance Point T, passing is defined as complying to the EH9 and EW9 limits specified in Section 20.3.2 for all three eyes.

10) In addition, Transmitter Compliance requires the EW9_Eye_Width_Mask be met for the upper and lower eye edges, at Cupp and Clow respectively. Create an eye width mask centered on Tmid having a width of EW9 which extends outside the mask for the upper and lower PAM4 eyes as shown in Figure 20-8.

Figure 20-8. PAM4 Eye width mask



11) The requirement is that TL6 + 1.2444·RJL <= Tmid - EW9_Eye_Width_Mask/2 for a left edge and TR6 - 1.2444·RJR >= Tmid + EW9_Eye_Width_Mask/2.

20.3.3 Receiver Characteristics

When provided with a worst case reference clock meeting the specifications of Section 20.3.1 as a timing source, a receiver shall operate at the specified BER with the worst case combination of a compliant transmitter and a compliant channel.

Receiver electrical specifications are given in Table 20-9 and measured at compliance point R. To dampen noise sources and absorption of both even and odd mode reflections, the receiver shall satisfy the Common Mode Input Return Loss requirement of Table 20-9.

Table 20-9. Receiver Electrical Input Specifications

Characteristic	Symbol	Condition	MIN.	NOM.	MAX.	UNIT
Baud rate	R_Baud		18.0		29.0	GSym/s
Input Differential Voltage	R_Vdiff	Note 1, 2			600	mVppd
Differential Input Impedance	R_Rdin		80	100	120	Ω
Receiver Common Mode Noise Tolerance	R_Ncm				25	mVrms
Input Resistance Mismatch	R_Rm				5	%
Differential Input Return Loss	R_SDD11	See Section 20.3.3.3				dB
Common Mode Return Loss	R_SCC11	200 MHz to fb	4			dB
Receiver Input Single-ended Voltage Tolerance	R_VinSE		0.1		1.2	V

NOTES:
1. The receiver shall have a differential input voltage range sufficient to accept a signal produced at point R by any combination of compliant transmitters and channels.
2. The receiver input is DC-coupled.

20.3.3.1 Input Baud Rate

All devices shall work within the range from 18.0 Gsym/s to 29.0 Gsym/s as specified for the device, with the baud rate tolerance as per Section 3.2.11. Note that implementation of specific protocols will define the operating baud rate without affecting CEI compliance.

20.3.3.2 Reference Input Signals

The receiver shall accept differential input signal amplitudes produced by a compliant transmitter connected with the minimum attenuation specified by Equation 20-2 to the receiver. This may be larger than the 600 mVppd maximum of the transmitter due to output/input impedances and reflections.

The minimum input amplitude is defined by the minimum transmitter amplitude, the actual receiver input impedance and the loss of the actual PCB. Note that the minimum transmitter amplitude is defined using a well controlled load impedance; however the real receiver's impedance may differ, which can leave the receiver input signal smaller than expected.

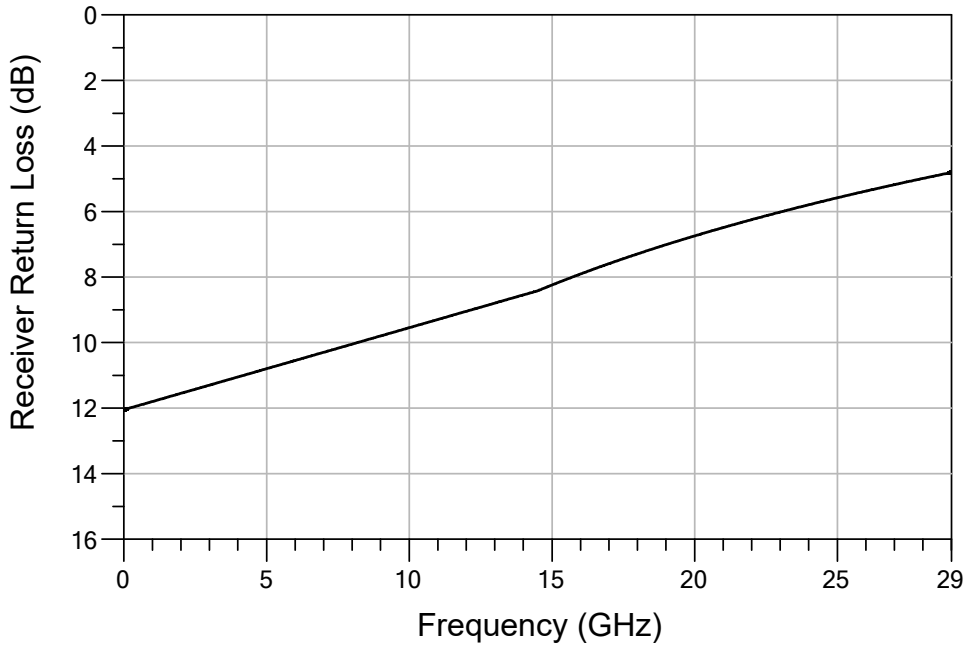
20.3.3.3 Receiver Return Loss

Receiver differential return loss shall be bounded by:

$$RL(f) \geq 12.05 - 0.25(29f/f_b) \quad f_{min} \leq f \leq 0.5f_b$$
$$RL(f) \geq 14 - 12\log_{10}(f/(0.1714f_b)) \quad 0.5f_b < f \leq f_b \qquad (20\text{-}9)$$

Where f_{min} is given in Table 20-3.

Figure 20-9. CEI-56G-XSR-PAM4 Receiver Return Loss at 29 Gsym/s



20.3.3.4 Input Lane-to-Lane Skew

Please refer to Section 3.2.7.

21 CEI-56G-LR-PAM4 Long Reach Interface

This clause details the requirements for the CEI-56G-LR-PAM4 long reach high speed electrical interface between nominal baud rates of 18.0 Gsym/s and 29.0 Gsym/s using PAM4 coding. A compliant device shall meet all of the requirements listed below. The electrical interface is based on high speed, low voltage logic. Connections are point-to-point balanced differential pairs and signaling is unidirectional.

The electrical IA is based on loss and jitter budgets and defines the characteristics required to communicate between a CEI-56G-LR-PAM4 transmitter and a CEI-56G-LR-PAM4 receiver using copper signal traces on a printed circuit board. The characteristic impedance of the signal traces is nominally 100 Ω differential. The signal trace or channel between a transmitter and a receiver shall meet the channel operating margin (COM), a method and a threshold quantity used for channel compliance.

CEI-56G-LR-PAM4 assumes using forward error correction (FEC) to achieve the bit error ratio (BER) target. The FEC guidances are described in Appendix 16.D.

Long reach CEI-56G-LR-PAM4 devices from different manufacturers shall be interoperable.

21.1 Requirements

1. Support serial baud rates (f_b) within the range from 18.0 Gsym/s to 29.0 Gsym/s as specified for the device using PAM4 coding. A CEI implementation complies to the specifications of this clause over the range of baud rates stated for the implementation within this range.
2. Capable of achieving a raw Bit Error Ratio (BER) of 10^{-4} or better per lane. FEC is assumed to be used in the system to achieve corrected BER of 10^{-15} or better per lane. The baud rate includes the overhead required for FEC. The definition of FEC is outside the scope of this IA (see Appendix 16.D).
3. Capable of driving up to 1000 mm of PCB and up to 2 connectors.
4. Shall support AC-coupled operation.
5. Shall allow multi-lanes (1 to n).
6. Shall support hot plug.

21.2 General Requirements

21.2.1 Data Patterns

See Appendix 16.C.5.

21.2.2 Bit Error Ratio

A raw Bit Error Ratio (BER) better than or equal to 10^{-4} is required on each lane. A compliant receiver, when receiving from a compliant transmitter over a compliant channel, shall deliver the specified raw BER to the subsequent FEC decoder. Error bursts with length more than 126 PAM4 symbols delivered to the PAM4 decoder shall occur with a probability of less than 1 in 10^{20} PAM4 symbols. See Appendix 16.D.

21.2.3 Ground Differences

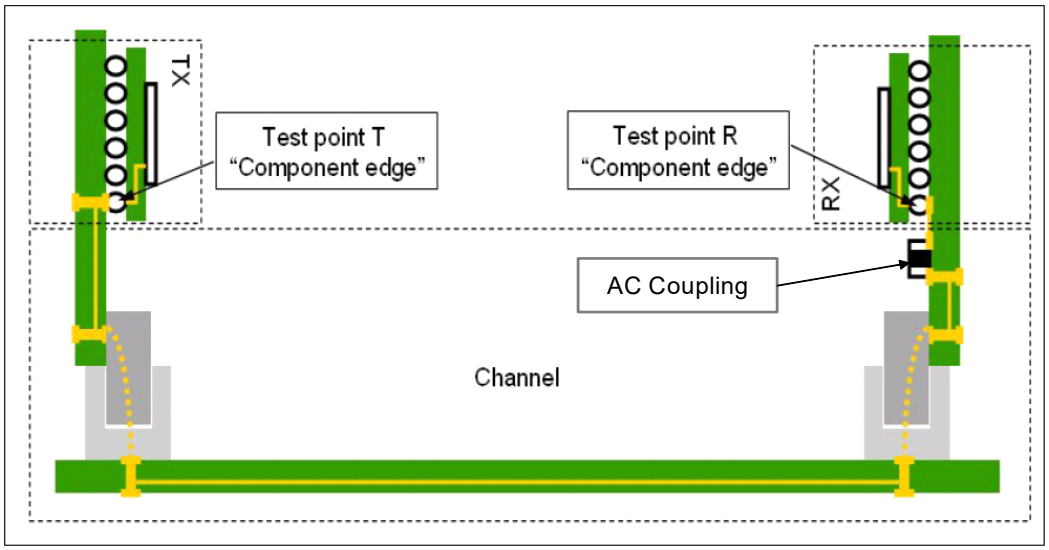
Please refer to Section 3.2.4.

21.2.4 Channel Compliance

A forward channel and associated dominant crosstalk channels are deemed compliant if the channel characteristics conform to the requirements defined in this section.

21.2.4.1 Reference Model

Figure 21-1.CEI-56G-LR Reference Model



Note: Test points differ from definitions in Section 1.8, as a DC blocking capacitor, if physically located outside of the package, is part of the channel.

The channel is defined between test point T and test point R.

21.2.4.2 Channel Operating Margin

The Channel Operating Margin (COM) of the channel is computed using the procedure in Annex 93A of IEEE Std 802.3 [27], with the Test 1 and Test 2 values in Table 21-1. Test 1 and Test 2 differ in the value of the device package model transmission line

length *zp*. Moreover, using *Tr* = 0.345 UI, *and* β=2 for *Ht*(*f*) in Equation (93A–19), COM shall be greater than or equal to 3.0 dB for each test. This minimum value allocates

Table 21-1. COM Parameter Values

Parameter	Symbol	Value	Units
Signaling rate	f_b	18.0 - 29.0	Gsym/s
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length, Test 1 Transmission line length, Test 2 Transmission line characteristic impedance Single-ended package capacitance at package-to-board interface	 C_d z_p z_p z_c C_p	 160 12 30 95 110	 fF mm mm Ω fF
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	50	Ω
Receiver 3 dB bandwidth	f_r	0.75 × f_b	GHz
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.60	—
Transmitter equalizer, 2nd pre-cursor coefficient Minimum value Maximum value Step size	$c(-2)$	 0 0.10 0.025	 — — —
Transmitter equalizer, 1st pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.28 0 0.025	 — — —
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.28 0 0.025	 — — —
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –20 0 1	 dB dB dB
Continuous time filter, DC gain2 Minimum value Maximum value Step size	g_{DC2}	 –6 0 1	 dB dB dB
Continuous time filter, scaled zero frequency	f_z	f_b /2.5	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	f_b /2.5 f_b	GHz GHz

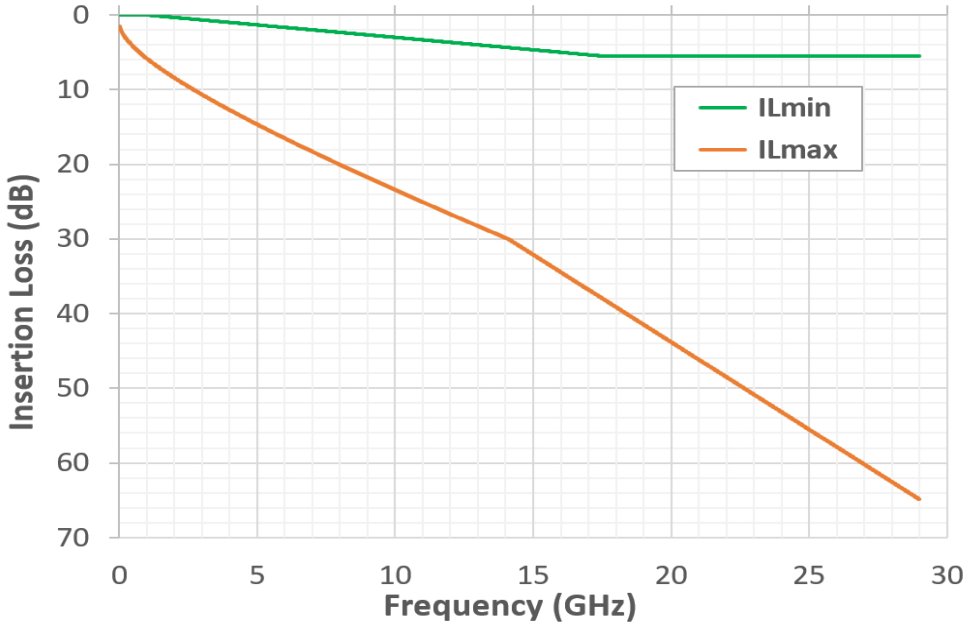
Table 21-1. COM Parameter Values

Continuous time filter, low frequency pole/scaled zero	f_{LF}	$f_b/40$	GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.41 0.41 0.60	 V V V
Number of signal levels	L	4	—
Level separation mismatch ratio	R_{LM}	0.95	—
Transmitter signal-to-noise ratio	SNR_{TX}	32.5	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	12	UI
Normalized DFE coefficient magnitude limit for n = 2 to N_b	$b_{max}(1)$ $b_{max}(2\text{-}Nb)$	0.7 0.2	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.02	UI
One-sided noise spectral density	η_0	1.64×10^{-8}	V^2/GHz
Target detector error ratio	DER_0	10^{-4}	—
Channel operating margin, min	COM	3.0	dB

margin for practical limitations on the receiver implementation and the largest step size allowed for transmitter equalizer coefficients.

21.2.4.3 Informative Channel Insertion Loss

Figure 21-2.Channel Insertion Loss Limit for 29.0 Gsym/s



$$IL_{max} = \begin{bmatrix} 1.083 + 3.631\sqrt{\frac{f \times 29}{f_b}} + 1.041\frac{f \times 29}{f_b}, & f_{min} \le f \le f_b/2 \\ -3 + 2.2759\frac{f \times 29}{f_b}, & f_b/2 \le f \le f_b \end{bmatrix} \quad \text{(21-1)}$$

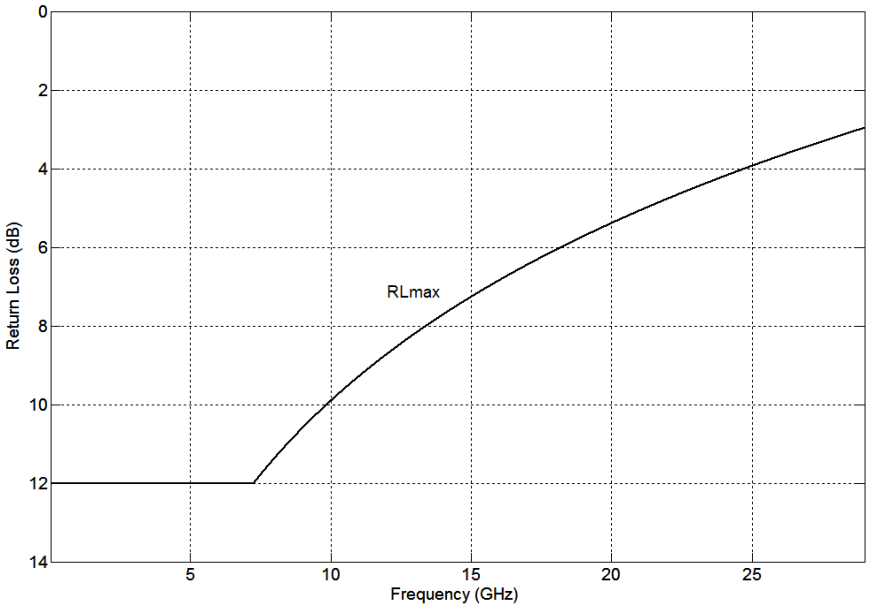
$$IL_{min} = \begin{bmatrix} 0, & f_{min} \le f \le 1GHz \\ \frac{1}{3}(f-1), & 1GHz \le f \le 17.5\ GHz \\ 5.5, & 17.5\ GHz < f \le f_b \end{bmatrix} \quad \text{(21-2)}$$

Channel insertion loss is an informative recommendation.

The channel must comply with the normative specification in Section 21.2.4.2.

21.2.4.4 Channel Return Loss

Figure 21-3.Channel Return Loss Limit for 29.0 Gsym/s



Channel Return Loss shall be bounded by Equation (21-3) as shown in Figure 21-3.

$$RL_{max} = \begin{bmatrix} 12, & f_{min} \le f < \frac{f_b}{4} \\ 12 - 15\log_{10}\left(\frac{4f}{f_b}\right), & \frac{f_b}{4} \le f \le f_b \end{bmatrix} \quad (21\text{-}3)$$

21.2.4.5 Channel AC-coupling

The transmitter shall be AC-coupled to the receiver. The impact of a DC-blocking capacitor implemented in the channel between the package balls of the transmitter and receiver (i.e., between compliance points T and R) is accounted for within the channel specifications. Common-mode specifications are defined as if the DC-blocking capacitor is implemented in the channel between compliance points T and R. Should the capacitor not be implemented between compliance point T and compliance point R, it is the responsibility of implementers to consider any necessary modifications to common-mode and channel specifications required for interoperability as well as any impact on the verification of transmitter and receiver compliance. In particular the common-mode specifications for the transmitter in Table 21-2 may not be appropriate.

The low-frequency 3 dB cutoff of the AC-coupling shall be less than 100 kHz.

21.3 Electrical Characteristics

The electrical signaling is based on high speed low voltage logic with a nominal differential impedance of 100 Ω.

21.3.1 Transmitter Characteristics

The transmitter electrical requirements at compliance point T (see Figure 21-1) are specified in Table 21-2, and the jitter requirements are specified in Table 21-3.

Table 21-2. Transmitter Electrical Output Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	T_Baud		18.0		29.0	Gsym/s
Output Differential Voltage	T_Vdiff	. See Note 1, 2.			1200	mVppd
DC Common mode Voltage	T_Vcm	See Note 2.	0		1.9	V
Output AC Common Mode Voltage	T_VcmAC	See Note 1, 2.			30	mVrms
Single-ended Transmitter Output Voltage	T_Vse	See Note 1, 2.	-0.3		1.9	V
Differential Output Return Loss	T_SDD22	Equation (21-4)				dB
Common Mode Output Return Loss	T_SCC22	Equation (21-5)				dB
Level Separation Mismatch Ratio	T_RLM	See Note 1, 2, 3. 4	0.95			-
Steady-state Voltage	T_Vf		0.4		0.6	V
Linear Fit Pulse Peak	T_Pk		0.83 × T_Vf			V
Signal-to-Noise-and-Distortion-Ratio	T_SNDR		31			dB

NOTES:
1. Signals are specified as measured through a fourth-order Bessel-Thomson low-pass response with 40 GHz 3 dB bandwidth.
2. Measured as described in Section 21.3.1.2. T_Vdiff min is set by the steady-state voltage T_Vf min.
3. Measured as described in Section 21.3.1.6
4. T_RLM is defined in Appendix 16.C.4.3.

Table 21-3. Transmitter Output Jitter Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Uncorrelated Jitter (time interval from 0.005% to 99.9955% of the probability distribution)	T_J_{4u}	See Note 1			0.118	UI
Uncorrelated jitter RMS (standard deviation of the probability distribution)	T_J_{RMS}				0.023	UIrms
Even-Odd Jitter	T_EOJ				0.019	UIpp

NOTES:
1. Measured as described in Section 21.3.1.7.

21.3.1.1 Transmitter Baud Rate

All devices shall work within the range from 18.0 Gsym/s to 29.0 Gsym/s as specified for the device, with the baud rate tolerance as per Section 3.2.11. A CEI implementation complies to the specifications of this clause over the range of baud rates stated for the implementation within this range.

21.3.1.2 Transmitter Amplitude and Swing

The differential output voltage T_Vdiff is defined to be True minus Complement. The common-mode output voltage T_Vcm is defined to be one half of the sum of True and Complement. These definitions are illustrated in Section 1.6.1.

For a QPRBS13-CEI test pattern (Appendix 16.C.3.1), the peak-to-peak value of the differential output voltage (T_Vdiff) shall be less than or equal to the limit given in Table 21-2 regardless of the transmit equalizer setting.

The DC common-mode output voltage (T_Vcm) shall be within the limits in Table 21-2 with respect to local ground.

The AC common-mode output voltage (T_VcmAC) shall be less than or equal to the limit given in Table 21-2 with respect to local ground. Common-mode output voltage requirements shall be met regardless of the transmit equalizer setting.

The single-ended transmitter output voltage (T_Vse) shall be within the limits in Table 21-2 with respect to local ground.

The transmitter shall be capable of providing a differential steady state output amplitude (2xT_V_f) between 800 and 1200 mVppd with transmit emphasis disabled.

Transmitter differential output amplitude shall additionally adhere to the requirements in Section 21.3.1.6.

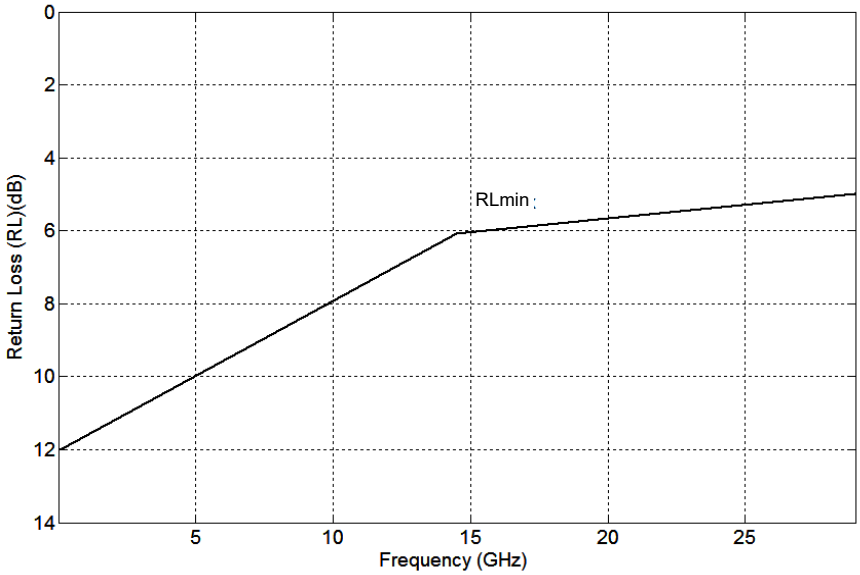
Power-down behavior is beyond the scope of CEI IA.

21.3.1.3 Transmitter Return Loss

The differential output return loss, in dB, of the transmitter shall meet Equation (21-4), where *f* is the frequency in GHz. The differential return loss limit $RL_d(f)$ is shown in Figure 21-4. This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements shall be 100 Ω.

$$RL_d(f) \geq RLmin(f) = \begin{pmatrix} 12.05 - 0.4112\left(\frac{f \times 29}{f_b}\right) & (0.05 \leq f \leq 0.5f_b) \\ 7.175 - 0.075\left(\frac{f \times 29}{f_b}\right) & (0.5f_b \leq f \leq f_b) \end{pmatrix} (dB) \qquad (21\text{-}4)$$

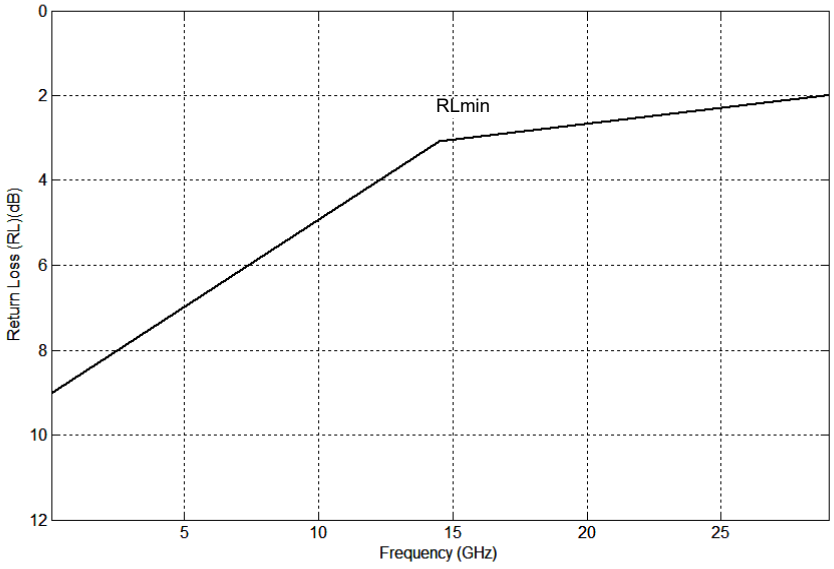
Figure 21-4.Transmitter differential return loss limit for 29.0 Gsym/s



The common-mode output return loss, in dB, of the transmitter shall meet Equation (21-5), where f is the frequency in GHz. The common-mode return loss limit $RL_C(f)$ is shown in Figure 21-5. This output impedance requirement applies to all valid output levels. The reference impedance for common-mode return loss measurements shall be 25 Ω.

$$RL_C(f) \geq RLmin(f)) = \begin{pmatrix} 9.05 - 0.4112\left(\frac{f \times 29}{f_b}\right) & (0.05 \leq f \leq 0.5 f_b) \\ 4.175 - 0.075\left(\frac{f \times 29}{f_b}\right) & (0.5 f_b < f \leq f_b) \end{pmatrix} \quad (dB) \qquad (21\text{-}5)$$

Figure 21-5.Transmitter common mode return loss limit for 29.0 Gsym/s.



21.3.1.4 Transmitter Lane-to-Lane Skew

Please refer to Section 3.2.7.

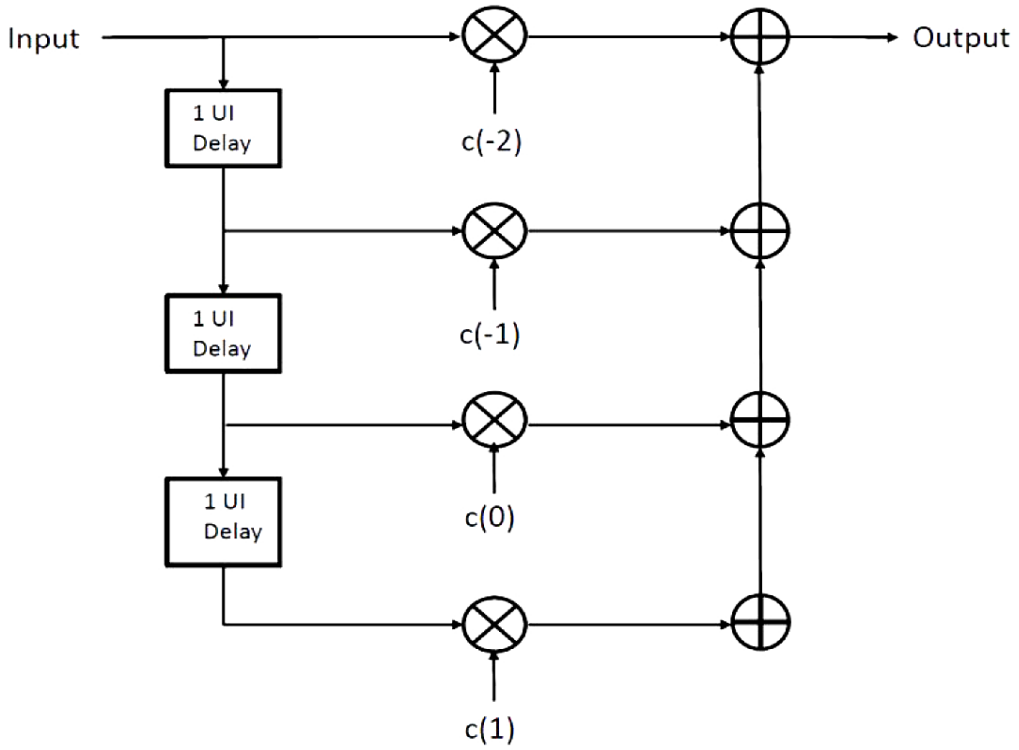
21.3.1.5 Transmitter Short Circuit Current

Please refer to Section 3.2.9.

21.3.1.6 Transmitter output waveform requirements

The transmitter function includes programmable equalization to compensate for the frequency-dependent loss of the channel and facilitate data recovery at the receiver. The functional model for the transmit equalizer is the four tap transversal filter shown in Figure 21-6.

Figure 21-6.Transmit equalizer functional model



Link budgets in this document assume optimized TX FIR equalization that is part of the system management function. The specific implementation is outside the scope of this document.

21.3.1.6.1 Linear fit to the measured waveform

The following test procedure defines linear fit pulse response, linear fit error (e(k), see Section 11.3.1.6.4), and normalized transmitter coefficient values.

For each configuration of the transmit equalizer, capture at least one complete cycle of the QPRBS13-CEI test pattern (Appendix 16.C.3.1) at the TX package ball (see Figure 21-1).

Compute the linear fit pulse response p(k) from the captured waveform per Section 11.3.1.6.2 using Np = 15 and Dp = 3. For aligned symbol values x(n) use -1, -ES1, ES2, and 1 to represent symbol values of -1, -1/3, 1/3, and 1, respectively, and where ES1 and ES2 are the effective symbol levels determined in Appendix 16.C.4.3.

Define r(k) to be the linear fit pulse response when transmit equalizer coefficients have been set to the “preset” values (see Section 11.3.1.6.1).

For each configuration of the transmit equalizer, compute the normalized transmit equalizer coefficients, c(i), according to Section 11.3.1.6.2 - Section 11.3.1.6.5.

21.3.1.6.2 Steady-state voltage and linear fit pulse peak

The linear fit pulse, p(k), is determined according to the linear fit procedure in Section 11.3.1.6.2 - Section 11.3.1.6.5, as modified by Section 21.3.1.6.1. The steady-state voltage T_Vf is defined to be the sum of the linear fit pulse p(k) divided by M, as shown in Equation (11-12).

The steady-state voltage, T_Vf, shall satisfy the requirements in Table 21-2.

The linear fit pulse peak, T_Pk, is the highest value of p(k). It shall satisfy the requirement in Table 21-2.

21.3.1.6.3 Transmitter equalizer coefficients

Table 21-4. Coefficient Range and Step Size

Coefficients	Normalized Amplitude		Normalized Step Size (%)
	Min (%)	Max (%)	
c(-2)	0	10	0.5 to 2.5
c(-1)	-28	0	0.5 to 2.5
c(1)	-28	0	0.5 to 2.5
c(0)	60	100	0.5 to 2.5

The normalized amplitudes of the coefficients of the transmitter equalizer (computed per Section 21.3.1.6.1) shall meet the requirements in Table 21-4. "min" is defined as the minimum normalized amplitude of the coefficient that must be supplied by the transmitter to be compliant. "max" is defined as the maximum normalized amplitude of the coefficient that must be supplied by the transmitter to be compliant.

The amplitude of a coefficient can be computed by multiplying its normalized amplitude by T_Vf, which is defined in Section 21.3.1.6.2.

The peak-to-peak output voltage is approximated by

$$(|c(-2)| + |c(-1)| + |c(0)| + |c(1)|) * 2 * T_Vf \quad (21\text{-}6)$$

and should not exceed the limit for T_Vdiff given in Table 21-2.

21.3.1.6.4 Transmitter Output Noise and Distortion

Signal-to-noise-and-distortion ratio (SNDR) is measured at the transmitter output using the following method, with the transmitter on the lane under test transmitting QPRBS13-CEI and transmitters on lanes not under test enabled and transmitting QPRBS31-CEI test pattern as defined in Appendix 16.C.3.2, or a valid CEI signal, or transmitting the same pattern with a slightly different Baud rate on each lane so that lane to lane signals are asynchronous. These transmitters shall have identical transmit equalizer settings to the transmitter under test.

Compute the linear fit to the captured waveform and the linear fit pulse response, p(k), and error, e(k), according to Section 21.3.1.6.1. Denote the standard deviation of e(k) as σ_e.

With the QPRBS13-CEI pattern and the same configuration of the transmit equalizer, measure the RMS deviation from the mean voltage at a fixed point in a run of at least 6 consecutive identical PAM4 symbols. The RMS deviation is measured for a run of each of the four PAM4 symbol levels.The average of the four measurements is denoted as σ_n.

SNDR is defined by Equation (21-7) where p_{max} is the maximum value of p(k).

$$SNDR = 10\log_{10}\left(\frac{p_{max}^2}{\sigma_e^2 + \sigma_n^2}\right)(dB) \quad (21\text{-}7)$$

SNDR shall be greater than 31 dB for any allowable transmit equalizer setting.

21.3.1.7 Transmitter output jitter

Jitter measurements in this sub-clause are performed with transmitters on physical lanes not under test enabled and transmitting QPRBS31-CEI test pattern as defined in Appendix 16.C.3.2, or a valid CEI signal, or transmitting the same pattern with a slightly different Baud rate on each lane so that lane to lane signals are asynchronous. These transmitters shall have identical transmit equalizer settings to the transmitter under test.

J_{4u}, J_{RMS}, and EOJ are defined by measurements of 12 specific transitions in a QPRBS13-CEI pattern in order to exclude correlated jitter. The 12 transitions represent all possible combinations of four identical symbols followed by two different identical symbols as shown in Table 21-5. The sequences are located by the symbol indices given in the table where symbols 1 to 7 are the run of seven +1s.

The threshold used to define each transition is given in Table 21-5 where V_{-1}, $V_{-1/3}$, $V_{1/3}$, and V_1 are as defined in Appendix 16.C.4.3.

The jitter is measured with a clock from a clock recovery unit (CRU) (i.e., a first order golden PLL, with corner frequency at f_b/6640, and a 20 dB/decade slope, see Section 1.6) as the trigger or reference clock.

J_{4u}, J_{RMS}, and EOJ specifications shall be met regardless of the transmit equalization setting.

Table 21-5. QPRBS13-CEI Pattern Symbols Used for Jitter Measurement

Label	Description	Gray Coded PAM4 Symbols	Index of First Symbol	Index Transition Begins	Index Transition Ends	Index of Last Symbol	Threshold Level
REF	Reference for symbol index	3333333	1	--	--	7	--
R03	0 to 3 rise	10000 330	1830	1834	1835	1837	$(V_{-1}+V_1)/2$
F30	3 to 0 fall	23333 001	1269	1273	1274	1276	
R12	1 to 2 rise	0111111 2222221	3638	3644	3645	3651	$(V_{-1/3}+V_{1/3})/2$
F21	2 to 1 fall	022222 113	1198	1203	1204	1206	
R01	0 to 1 rise	100000 113	6835	6840	6841	6843	$(V_{-1}+V_{-1/3})/2$
F10	1 to 0 fall	21111 003	2992	2996	2997	2999	
R23	2 to 3 rise	32222 330	6824	6828	6829	6831	$(V_{1/3}+V_1)/2$
F32	3 to 2 fall	033333 2222223	7734	7739	7740	7746	
R02	0 to 2 rise	10000 223	3266	3270	3271	3273	$(V_{-1}+V_{1/3})/2$
F20	2 to 0 fall	122222 0000002	7282	7287	7288	7294	
R13	1 to 3 rise	011111 331	133	138	139	141	$(V_{-1/3}+V_1)/2$
F31	3 to 1 fall	23333 112	7905	7909	7910	7912	

21.3.1.7.1 J_{4u} and J_{RMS} Jitter

For each transition i, 1 ..i ..12, of the transitions specified in Table 21-5, obtain a set S_i = {$t_i(1)$, $t_i(2)$, ...} of transition times modulo the period of the pattern. The 12 sets should be of equal size and the size of all sets should be chosen to enable calculation of J_{4u} (as defined below) with sufficient accuracy.

Calculate the average of each set Si, Tavgi, and subtract it from all elements of that set, to create a set $S0_i$ = {$t_i(1)$ - $Tavg_i$, $t_i(2)$ - $Tavg_i$, ...}.

Combine the sets $S0_i$, i=1 to 12, to create an estimated probability distribution $f_J(t)$.

J_{4u} is defined as the time interval that includes all but 10^{-4} of $f_J(t)$, from the 0.005th to the 99.995th percentile of $f_J(t)$.

J_{RMS} is defined as the standard deviation of $f_J(t)$.

21.3.1.7.2 Even-Odd Jitter (EOJ)

For one of the 12 specific transitions in QPRBS13-CEI in Table 21-5:

a) Trigger once in 3 repeats of the QPRBS13-CEI test pattern.

Obtain the mean time (T3) for this transition in the first QPRBS13-CEI.

Obtain the mean time (T4) for the same transition in the second QPRBS13-CEI.

b) The difference between the two means (T4 – T3), is the estimated period of the repeating pattern.

For each of the 12 specific transitions in QPRBS13-CEI in Table 21-5:

1) Trigger once in 2 repeats of the QPRBS13-CEI test pattern.

Obtain the mean time (T1) for the specific transition in the first QPRBS13-CEI.

Obtain the mean time (T2) for the same transition in the second QPRBS13-CEI.

2) Calculate EOJ for this transition as |(T2 – T1) – (T4 – T3)|.

EOJ is the maximum of the 12 measurements.

NOTE: Both of (T2 - T1) and (T4 - T3) are about 8191 UI, which is much larger than the EOJ value. Hence, each of T1 through T4 should have high precision.

21.3.2 Receiver Characteristics

A compliant receiver shall autonomously operate at the specified BER with the worst case combination of a compliant transmitter and a compliant channel. The receiver also shall not cause error propagation that violates the error burst length requirement as defined in Section 21.2.2. Further receiver electrical requirements at compliance point R (see Figure 21-1) are specified in Table 21-6, with the receiver interference tolerance parameters specified in Table 21-7. Lanes not under test should be enabled and transmitting or receiving asynchronous or uncorrelated signals.

Table 21-6. Receiver Electrical Input Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	R_Baud		18.0		29.0	Gsym/s
Differential Input Return Loss	R_SDD11	Equation (21-4)				dB
Differential to Common Mode Input Conversion	R_SCD11	Equation (21-8)				dB
Interference Tolerance		Table 21-7				
Jitter Tolerance		Table 21-8				

Table 21-7. Receiver interference tolerance parameters (Note 3)

Parameter	Test 1 values		Test 2 values		Units
	Min	Max	Min	Max	
Pre-FEC Bit Error Ratio (BER)		10^{-4}		10^{-4}	
COM, including effects of broadband noise		3		3	dB
Insertion loss at Nyquist, Note 1		15		30	dB
RSS_DFE4. Note 2	0.05	-	0.05	-	

NOTES:
1. Measured between TX and RX package balls (see Figure 21-1).
2. Definition can be found in Annex 93A of IEEE Std 802.3 [27].
3. See Section 21.3.2.4.

21.3.2.1 Input Baud Rate

All devices shall work within the range from 18.0 Gsym/s to 29.0 Gsym/s as specified for the device, with the baud rate tolerance as per Section 3.2.11. A CEI implementation complies to the specifications of this clause over the range of baud rates stated for the implementation within this range.

21.3.2.2 Reference Input Signals

The receiver shall accept differential input signal amplitudes produced by a compliant transmitter connected with the minimum attenuation specified in Figure 21-2 to the receiver. This may be larger than the 1200 mVppd maximum of the transmitter due to output/input impedances and reflections.

The minimum input amplitude is defined by the minimum transmitter amplitude, the actual receiver input impedance and the loss of the actual PCB. Note that the minimum transmitter amplitude is defined using a well controlled load impedance, however the real receiver is not, which can leave the receiver input signal smaller than expected.

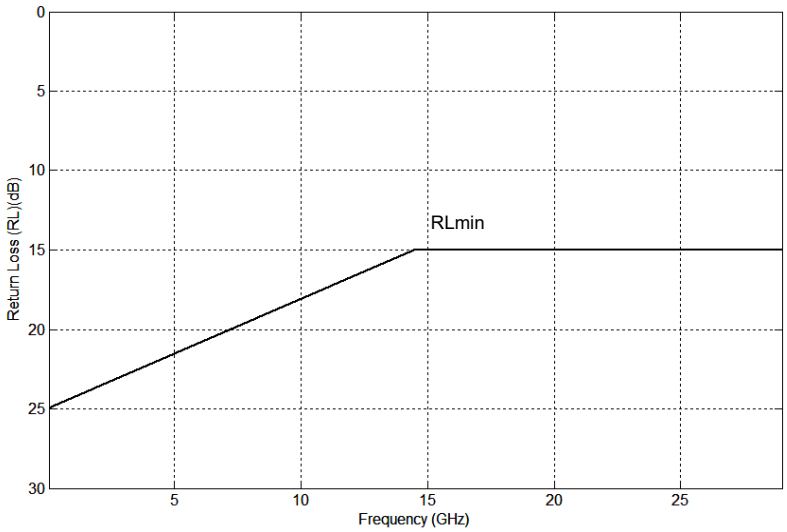
21.3.2.3 Input Resistance and Return Loss

The differential input return loss, in dB, of the receiver shall meet Equation (21-4). The reference impedance for differential return loss measurements shall be 100 Ω.

The differential to common-mode return loss, in dB, of the receiver shall meet Equation (21-8). The differential to common-mode return loss limit $RL_{dc}(f)$ is shown in Figure 21-7.

$$RL_{dc}(f) \geq RLmin(f) = \begin{pmatrix} 25 - 0.6897\left(\frac{f \times 29}{f_b}\right) & (0.05 \leq f \leq 0.5f_b) \\ 15 & (0.5f_b < f \leq f_b) \end{pmatrix} (dB) \quad (21\text{-}8)$$

Figure 21-7.Receiver differential to common-mode return loss limit for 29.0 Gsym/s.



21.3.2.4 Receiver Interference Tolerance

The receiver interference tolerance test is based on the test defined in Annex 120D.3.2.1 of IEEE P802.3 [27].

The receiver on each lane shall meet the pre-FEC BER requirement with channels matching the Channel Operating Margin (COM) and loss parameters for Test 1 and Test 2 in Table 21-7.

The test channel should be created using printed circuit boards with short interconnecting cables.

The following considerations apply to the interference tolerance test. The transmitter package is omitted in the COM calculation. The Test transmitter's measured SNDR should be used for SNR_{TX} in the COM calculation. The transmitter output levels are set such that R_{LM} is equal to 0.95. The test transmitter meets the specifications in Section 21.3.1. The test transmitter is constrained such that for any transmitter equalizer setting the differential peak-to-peak voltage is less than 800 mV, and the normalized amplitudes of the coefficients of the transmitter equalizer c(-2), c(-1), c(0) and c(1) are between the minimum and maximum limits given in Table 21-4.

The lower frequency bound for the noise spectral density constraints, fNSD1, is 1 GHz. The differential return-loss of the test channel at TP5 (as defined in Annex 93A of Std. IEEE802.3 [25]) shall meet the requirements of Equation (21-4), and be 3 dB better than the requirements of Equation (21-4) for all frequencies less than $f_b/2$. The test transmitter's jitter parameters J_{4u} and J_{RMS} are measured. A_{DD} and σ_{RJ} are calculated from the measured values of J_{4u} and J_{RMS} using Equation (21-9), and Equation (21-10), respectively and used for COM parameters. Other COM parameters are set

according to the values in Table 21-1. The broadband noise is added and adjusted to achieve the COM value in Table 21-7. The test pattern to be used is QPRBS31-CEI defined in Appendix 16.C.3.2. A test system with a fourth-order Bessel-Thomson low-pass response with 40 GHz 3 dB bandwidth is to be used for measurement of the signal applied by the pattern generator and for measurements of the broadband noise.

$$A_{DD} = \left(\left(\frac{J_{4u}}{2}\right) + Q4\sqrt{\left((Q4^2+1)\times {J_{RMS}}^2 - \left(\frac{J_{4u}}{2}\right)^2\right)}\right)/(Q4^2+1) \quad (21\text{-}9)$$

$$\sigma_{RJ} = \left(\frac{J_{4u}}{2} - A_{DD}\right)/(Q4) \quad (21\text{-}10)$$

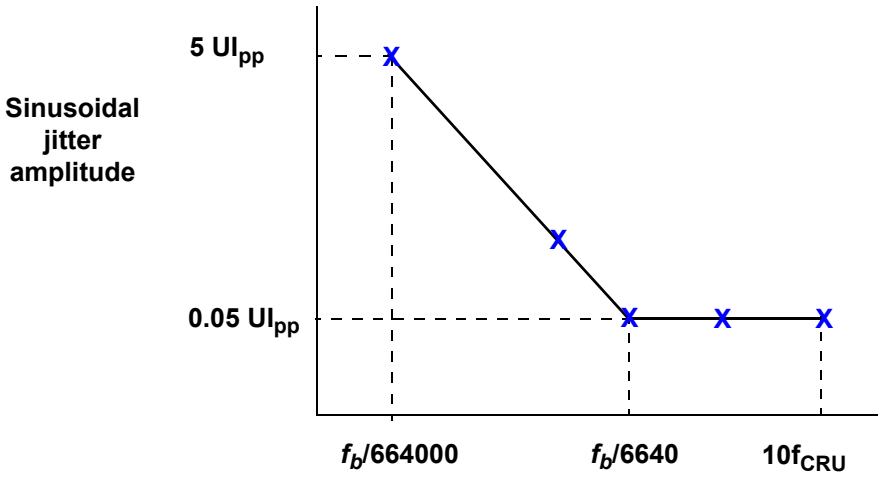
21.3.2.5 Receiver Jitter Tolerance

Receiver jitter tolerance shall meet the conditions and parameters defined in Table 21-8. This sinusoidal jitter is part of the jitter applied in the stressed input test. The sinusoidal jitter is calibrated at 10x the reference CRU's bandwidth and must be tested at $f_{CRU}/100$, $f_{CRU}/3$, f_{CRU}, $3f_{CRU}$, and $10f_{CRU}$, where f_{CRU} is the jitter corner frequency given by $f_b/6640$, with sinusoidal jitter of 5 UI, 0.15 UI, 0.05 UI, 0.05 UI and 0.05 UI respectively. For this test the channel used is as for the receiver interference tolerance described in Section 21.3.2.4. Note that the values measured for J_{4u} and J_{RMS} include the effects of this added sinusoidal jitter and noise is added to obtain a COM of 3 dB with these measured jitter values as for the interference tolerance test.The receiver bit error ratio (BER) shall meet the requirements of Section 21.2.2 for each pair of jitter frequency and peak-to-peak amplitude values listed above and shown in Figure 21-8.

Table 21-8. Receiver Jitter Tolerance Parameters

Frequency Range	Sinusoidal jitter, peak-to-peak (UI)
$f < f_b/664000$	Not Specified
$f_b/664000 < f \leq f_b/6640$	$5*f_b/(664000*f)$
$f_b/6640 < f \leq 10f_{CRU}$	0.05

Figure 21-8. Receiver Jitter Tolerance Mask



21.3.2.6 Single Ended Input Voltage

The single ended voltage levels with respect to the receiver ground at the input of the receiver are dependent on the transmitter implementation and the inter-ground difference. The voltage levels at the input of an AC coupled receiver (if the effective AC coupling is done within the receiver) or at the TX side of the external AC coupling cap (if AC coupling is done externally) will be between -0.35V and 1.95V with respect to local ground.

21.3.2.7 Input Lane-to-Lane Skew

Refer to Section 3.2.8.

22 CEI-56G-LR-ENRZ Long Reach Interface

This clause details the requirements for the CEI-56G-LR-ENRZ long reach high speed electrical interface between nominal data rates of 99.5 Gbit/s and 112.4 Gbit/s using ENRZ coding across four wires. This throughput, normalized per wire, is equivalent to other CEI-56G variants which define signaling over two wires.

A compliant device shall meet all of the requirements listed below. The electrical interface is based on high speed, low voltage logic. Connections are point-to-point balanced quad wire groups and signaling is unidirectional.

The electrical IA is based on loss and jitter budgets and defines the characteristics required to communicate between a CEI-56G-LR-ENRZ transmitter and a CEI-56G-LR-ENRZ receiver using copper signal traces on a printed circuit board. The characteristic impedance of the signal traces is nominally 50 Ω between any wire of the quad channel to AC ground. A 'length' is effectively defined in terms of its attenuation and phase response rather than its physical length. Refer to Section 22.2.6 for the channel requirements.

Long reach CEI-56G-LR-ENRZ devices from different manufacturers shall be interoperable.

22.1 Requirements

1. Support data rates within the range of 99.5 Gbit/s and 112.4 Gbit/s across four wires. Corresponding baud rates are within the range of 33.16 Gsym/s and 37.50 Gsym/s.
2. Capable of low bit error ratio (10^{-15}, with a test requirement to verify 10^{-12}).
3. Capable of driving up to 1000 mm of PCB and up to 2 connectors.
4. Shall support AC-coupled operation.
5. Shall allow multiple CEI lanes (1 to n).
6. Shall support hot plug.

22.2 General Requirements

22.2.1 Data Patterns

Please refer to Section 3.2.1

22.2.2 Signal levels

The signal is a low swing Ensemble NRZ (ENRZ) interface using four wires, designated W3, W2, W1, and W0. Low swing ENRZ signaling provides noise immunity and improved electromagnetic interference (EMI) similar to the characteristics of differential NRZ signaling. See Figure 22-1 for an illustration of absolute driver output voltage limits and voltage levels for driver output states V_{+1}, $V_{+1/3}$, $V_{-1/3}$, and V_{-1}. See Figure 22-2 for a definition of differential peak-to-peak amplitude and differential voltages for bit values of 1 and 0 (V_{diff-1} and V_{diff-0}).

Figure 22-1. Definition of Driver Amplitude and Swing

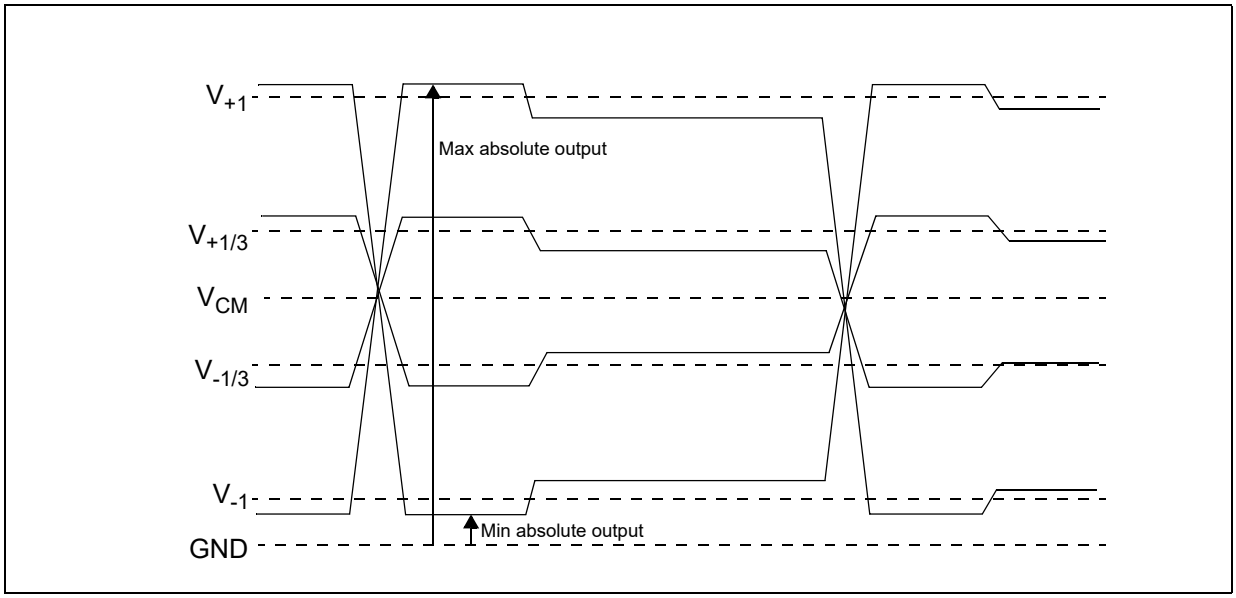
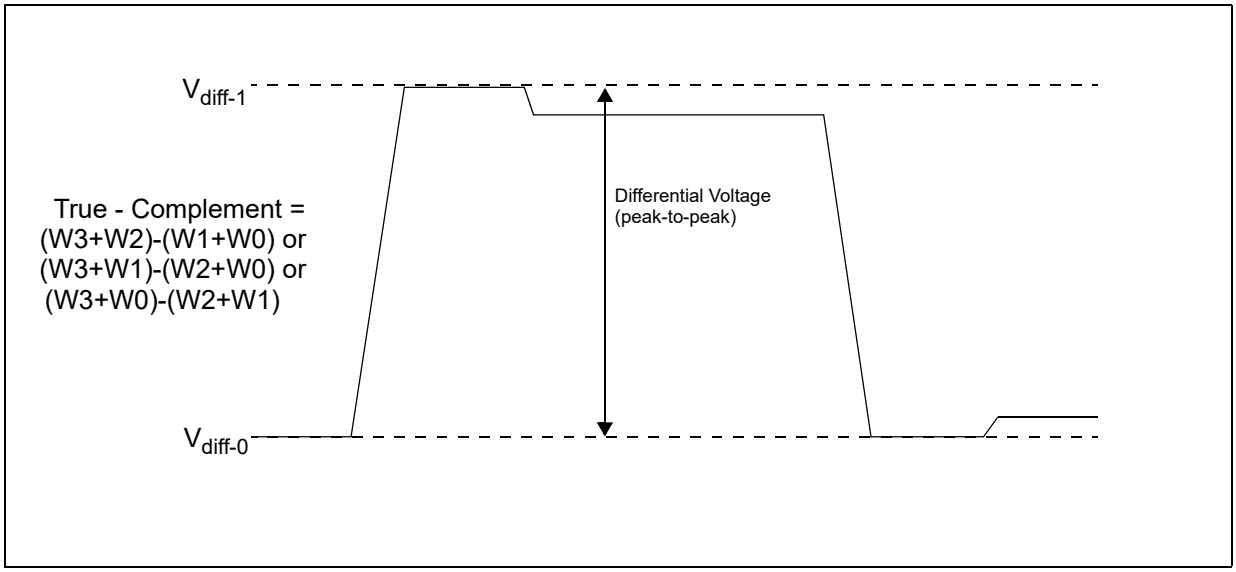


Figure 22-2. Definition of Driver Amplitude and Swing



Given absolute voltages V_{W3}, V_{W2}, V_{W1}, and V_{W0} referenced to ground on the respective wires W3, W2, W1, and W0, the DC common mode voltage of the ENRZ interface is defined as the average on the voltage on the four wires.

The single-ended voltage on wire *i* with respect to V_{CM} is defined as:

$$V_{CM} = \frac{V_{W3} + V_{W2} + V_{W1} + V_{W0}}{4} \quad (22\text{-}1)$$

The single-ended voltage on wire *i* with respect to V_{CM} is defined as:

$$V_{SE(i)} = V_i - V_{CM} \qquad (i = W3, W2, W1, W0) \quad (22\text{-}2)$$

The maximum and minimum single-ended voltages on any of the four wires are:

$$\begin{aligned} V_{SE\text{-}max} &= max(V_{SE(W3)}, V_{SE(W2)}, V_{SE(W1)}, V_{SE(W0)}) \\ V_{SE\text{-}min} &= min(V_{SE(W3)}, V_{SE(W2)}, V_{SE(W1)}, V_{SE(W0)}) \end{aligned} \quad (22\text{-}3)$$

The maximum peak-to-peak swing of V_{SE} is defined as:

$$V_{SEpp} = V_{SE\text{-}max} - V_{SE\text{-}min} \quad (22\text{-}4)$$

As illustrated in Figure 22-1, the output driver may assume any one of four output states, where the nominal drive voltages of these states are defined in Table 22-1. Each of wires W3, W2, W1, and W0 can be driving different states, but only combinations of driver states which maintain a constant V_{CM} are allowed.

Table 22-1. ENRZ Signal Drive States

Nomenclature for Signal State	Nom. V_{SE}	Nom. V_i
+1	+ (V_{SEpp} / 2)	+ (V_{SEpp} / 2) + V_{CM}
+(1/3)	+ (V_{SEpp} / 6)	+ (V_{SEpp} / 6) + V_{CM}
-(1/3)	- (V_{SEpp} / 6)	- (V_{SEpp} / 6) + V_{CM}
-1	- (V_{SEpp} / 2)	- (V_{SEpp} / 2) + V_{CM}

The four wire ENRZ interface carries data over three differential subchannels designated as D2, D1, and D0. Each ENRZ symbol conveys one data bit on each of the three subchannels. The corresponding code map is described in Table 22-2.

Table 22-2. ENRZ Signaling Code Map

Data Value (Subchannels D2, D1, D0)	Wire States (W3, W2, W1, W0)	Data Value (Subchannels D2, D1, D0)	Wire States (W3, W2, W1, W0)
0 0 0	(-1, +1/3, +1/3, +1/3)	1 0 0	(-1/3, -1/3, -1/3, +1)
0 0 1	(-1/3, +1, -1/3, -1/3)	1 0 1	(+1/3, +1/3, -1, +1/3)
0 1 0	(-1/3, -1/3, +1, -1/3)	1 1 0	(+1/3, -1, +1/3, +1/3)
0 1 1	(+1/3, +1/3, +1/3, -1)	1 1 1	(+1, -1/3, -1/3, -1/3)

Each subchannel is decoded by a comparator which implements linear combination Equation (22-5), where the weights of each wire for decoder c_i is defined in Table 22-3.

$$c_i = \sum_{j=0}^{m-1} (\text{weight of wire j})(\text{signal level on wire j}) \quad (22\text{-}5)$$

Table 22-3. ENRZ Linear Combination Table

	Contribution of each wire to comparator decode			
Comparator	w_3	w_2	w_1	w_0
d_0	+1/2	+1/2	-1/2	-1/2
d_1	+1/2	-1/2	+1/2	-1/2
d_2	+1/2	-1/2	-1/2	+1/2

If c_i is greater than 0, then d_i = 1; if c_i is less than 0, then d_i = 0. The differential amplitude at the comparator in the absence of any gain in the receiver is:

$$V_{ppd} = 0.33(V_{SEpp}) \quad (22\text{-}6)$$

22.2.3 Signal Definitions

The signal paths of CEI channels are unidirectional point-to-point connections. Each quad channel for CEI-56G-LR-ENRZ is made up of four balanced electrical connections. Figure 22-3 illustrates two quad channels comprising a full duplex CEI lane. However the CEI specification does not preclude use for unidirectional protocol applications.

Figure 22-3. Signal Diagram

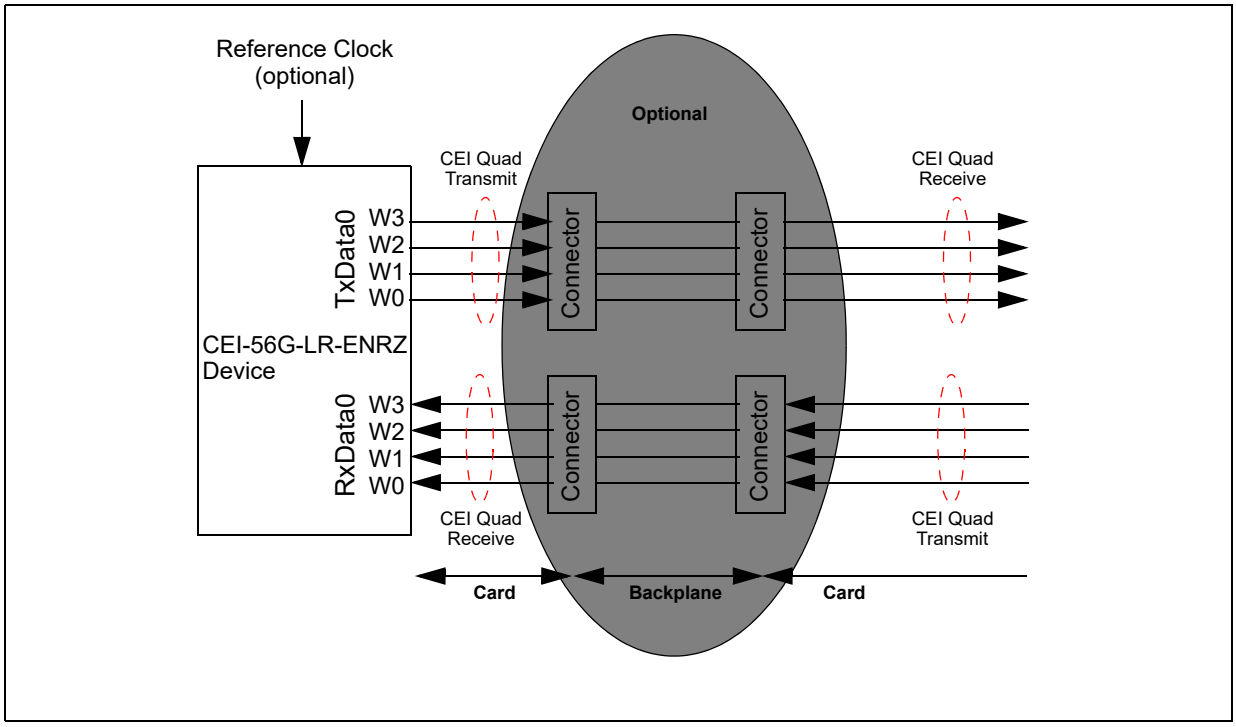


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Table 22-4. Receive Signal Summary

Signal Name	Direction	Function
RXDATA[n..0]	Input to SERDES Component	The Receive Data (RXDATA[n]) signals are the inputs to the SERDES component.

Table 22-5. Transmit Signal Summary

Signal Name	Direction	Function
TXDATA[n..0]	Output of SERDES Component	The Transmit Data (TXDATA[n]) signals are the outputs of the SERDES component.

Please refer to Appendix 1.A for a description of the reference clock in Figure 22-3.

22.2.4 Bit Error Ratio

Please refer to Section 3.2.3. Forward Error Correction (FEC) may be used to extend BER beyond these limits.

22.2.5 Ground Differences

Please refer to the maximum ground difference for LR links in Section 3.2.4.

22.2.6 Channel Compliance

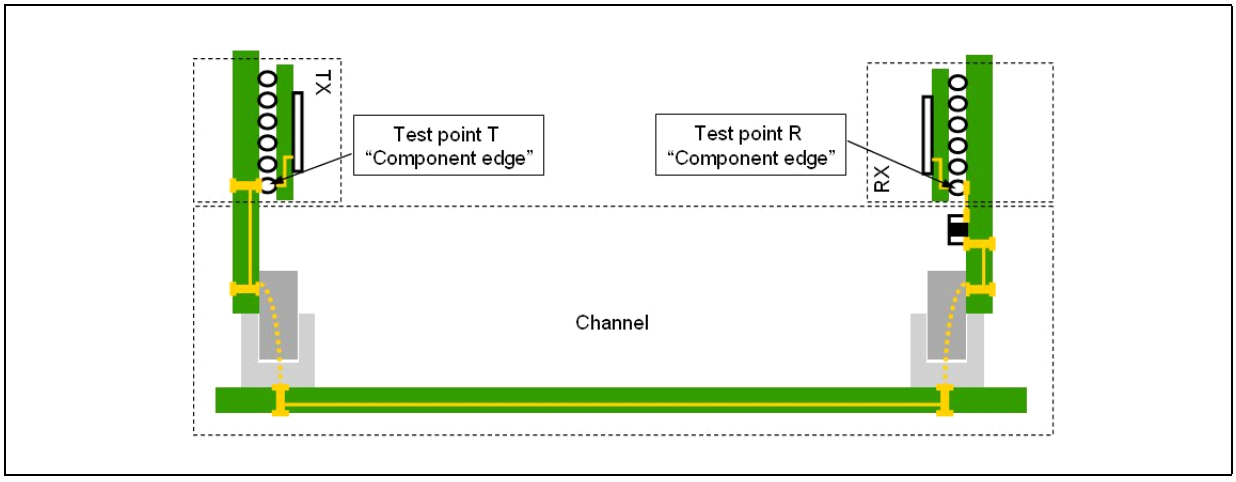
A forward channel and associated dominant crosstalk channels are deemed compliant if the channel characteristics conform to the requirements in this section.

22.2.6.1 Reference Model

The channel consists of PCB traces, vias, and up to 2 connectors. Traces are routed as two differential pairs (stripline). The reference PCB trace impedance is 50 Ω. (single-ended), with loose coupling between the differential pairs. The S-parameters of each ENRZ subchannel must meet the requirements described in Section 22.2.6.2, Section 22.2.6.3, Section 22.2.6.4, Section 22.2.6.5, and Section 22.2.6.6. Appendix 22.D.3 provides guidance for meeting these requirements.

Figure 22-4 shows a diagram of test points on an example board. The DC blocking capacitor, if physically located outside of the package, is part of the channel.

Figure 22-4. CEI-56G-LR-ENRZ Reference Model



Eight port S-parameter measurements of the channel are used to determine channel compliance. These measurements are obtained using one of the methods described in Appendix 22.D. Measured at these test points, several channel characteristics are parameterized for each subchannel D2, D1, and D0. Port definitions as noted in Figure 22-4 allow proper measurement of the parameters in Table 22-6 used for calculation of the channel parameters found in Table 22-7.

Table 22-6. Measured Channel Parameters

Symbol	Description
$IL(f)$	Differential insertion loss, -SDD21 magnitude (dB)
$RL_1(f)$	Differential input return loss, -SDD11 magnitude (dB)
$RL_2(f)$	Differential output return loss, -SDD22 magnitude (dB)
$NEXT_m(f)$	Differential near-end crosstalk loss (m^{th} aggressor), -SDD21 magnitude (dB)
$FEXT_n(f)$	Differential far-end crosstalk loss (n^{th} aggressor), -SDD21 magnitude (dB)

Table 22-7. Calculated Channel Parameters

Symbol	Description
$IL_{fitted}(f)$	Fitted insertion loss (dB)
$ILD(f)$	Insertion loss deviation (dB)
$ICN(f)$	Integrated crosstalk noise (mV_{RMS})
FOM_{ILD}	A figure of merit for the channel that is calculated based on weighted insertion loss deviation.

22.2.6.2 Insertion Loss

Insertion losses for each subchannel of the ENRZ channel, including PCB traces and connectors, shall comply with the limits specified by Equation (22-7), Equation (22-8) and plotted in Figure 22-5. Note that the variable f_b is the maximum baud rate to be supported by the channel under test (33.16 Gsym/s $\le f_b \le$ 37.50 Gsym/s).

Table 22-8. Channel Insertion Loss Frequency Range

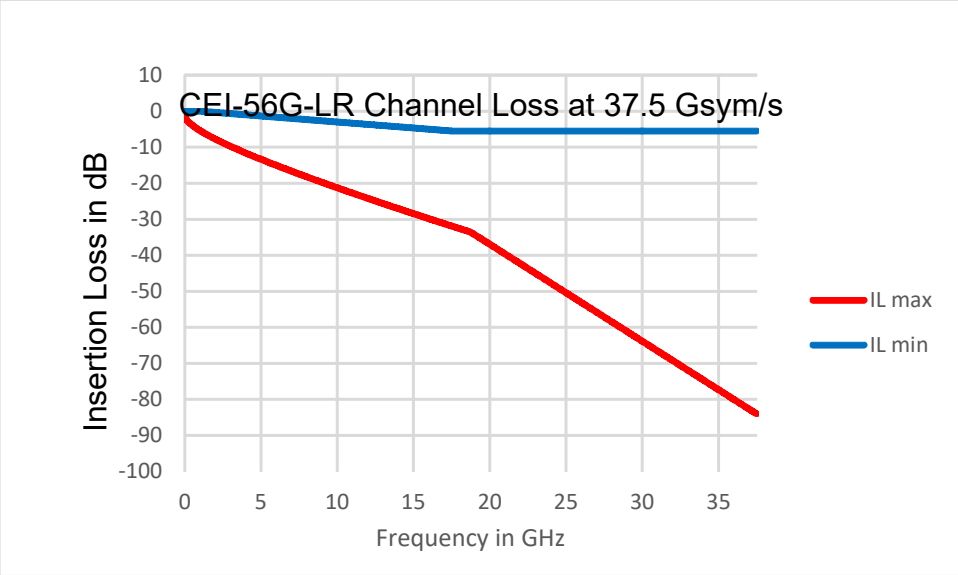
Parameter	Value	Units
fmin	50	MHz
fmax	37.5	GHz

$$IL_{max} = \begin{cases} 1.083 + 3.35\sqrt{\frac{f \times 37.5}{f_b}} + 0.96\frac{f \times 37.5}{f_b}, & f_{min} \le f < \frac{f_b}{2} \\ -16.8673 + 2.691\frac{f \times 37.5}{f_b}, & \frac{f_b}{2} \le f \le f_b \end{cases} \quad (22\text{-}7)$$

$$IL_{min} = \begin{pmatrix} 0, & f_{min} \le f \le 1\,GHz \\ \frac{1}{3}(f-1), & 1\,GHz < f \le 17.5\,GHz \\ 5.5, & 17.5\,GHz < f \le f_b \end{pmatrix} \quad (22\text{-}8)$$

Note: f in Equation (22-7) and Equation (22-8) is in GHz.

Figure 22-5. CEI-56G-LR normative channel insertion loss at 37.5 Gsym/s



22.2.6.3 Fitted insertion loss

For fitted insertion loss definitions, please refer to Section 12.2.1.1.

Each subchannel of the ENRZ channel shall meet the insertion loss requirements defined in Table 22-9. Note that the variable f_b is the maximum baud rate to be supported by the channel under test.

Table 22-9. Channel fitted insertion loss characteristics

Parameter	Units	Value	
		Min.	Max.
Minimum frequency, f_{ILmin}	GHz	0.05	-
Maximum frequency, f_{ILmax}	GHz	-	f_b
Fitted Insertion loss at Nyquist	dB	-	33.59
Fitted insertion loss, a_0	dB	-1	2.0
Fitted insertion loss, a_1	dB	0	24.494
Fitted insertion loss, a_2	dB	0	75.000
Fitted insertion loss, a_4	dB	0	53.437

22.2.6.4 Insertion loss deviation (ILD)

The insertion loss deviation *ILD* is the difference between the measured insertion *IL* and the fitted insertion loss IL_{fitted} as defined in Equation (22-9).

$$ILD = IL - IL_{fitted} \tag{22-9}$$

The insertion loss deviation ILD shall be within the region defined by Equation (22-10) and Equation (22-11) where f_b is the maximum baud rate to be supported by the subchannel under test and f_{ILmin} and f_{ILmax} are given in Table 22-9.

$$ILD \geq ILD_{min} = \begin{cases} -1.0 - 12.0(f/f_b) & f_{ILmin} \leq f < f_b/4 \\ -4.0 & f_b/4 \leq f \leq (3/4)f_{ILmax} \end{cases} \tag{22-10}$$

$$ILD \leq ILD_{max} = \begin{cases} 1.0 + 12.0(f/f_b) & f_{ILmin} \leq f < f_b/4 \\ 4.0 & f_b/4 \leq f \leq (3/4)f_{ILmax} \end{cases} \tag{22-11}$$

FOM_{ILD} is a figure of merit for the subchannel, and is calculated as indicated below.

Define the weight at each frequency *f* using Equation (22-12).

$$W(f) = \mathrm{sinc}^2(f/f_b)\left[\frac{1}{1+(f/f_t)^4}\right]\left[\frac{1}{1+(f/f_r)^8}\right] \tag{22-12}$$

Note that -3 dB transmit filter bandwidth f_t is inversely proportional to the minimum 20% to 80% rise and fall times *T_tr* and *T_tf*. The constant of proportionality is 0.2365 (i.e. T_tr x f_t = 0.2365), where T_tr is in ns when f_t is in GHz). In addition, f_r is the -3 dB reference receiver bandwidth, which should be set at (3/4)f_b, where f_b is the maximum baud rate to be supported by the channel.

$$FOM_{ILD} = \sqrt{\frac{\sum W(f) \times ILD\langle f \rangle^2}{N}} \quad (22\text{-}13)$$

FOM_{ILD} is calculated using Equation (22-13) where N is the number of frequency points. The summation is done over the frequency range of ILD with *f* in GHz. FOM_{ILD} shall be less than 0.3dB for each subchannel of valid ENRZ channels.

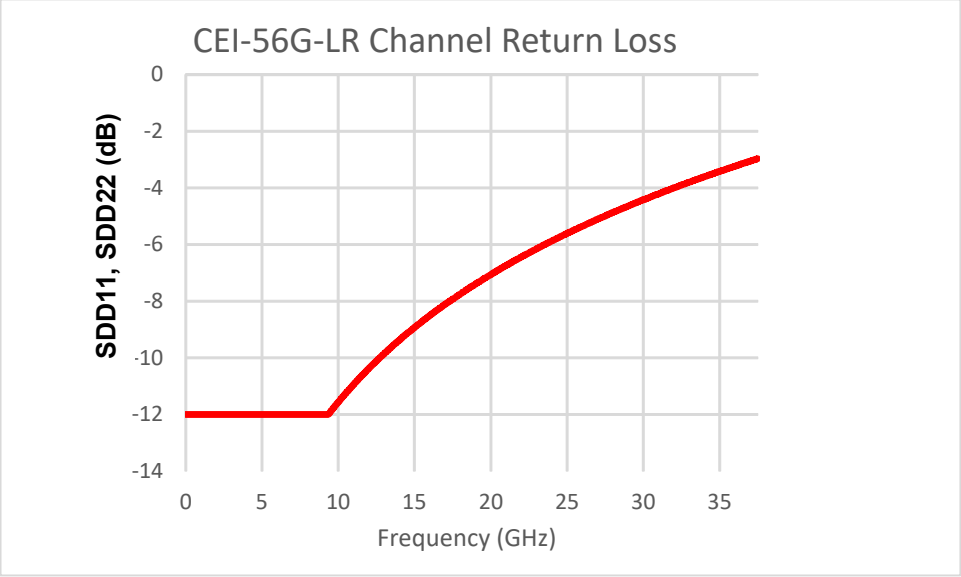
22.2.6.5 Channel Return Loss

The Return Loss for each subchannel of the ENRZ channel shall be bounded by Equation (22-14) as shown in Figure 22-6.

- RL(f) >= 12 dB for $f_{min} < f \leq f_b/4$
- RL(f) >= 12 dB - 15 $Log_{10}(4f/f_b)$ for $f_b/4 < f < f_b$ (22-14)

Note: f_{min} is as defined in Table 22-8

Figure 22-6. CEI-56G-LR normative channel return loss at 37.5 Gsym/s



22.2.6.6 Channel integrated crosstalk noise

Using the Integrated crosstalk noise method of Section 12.2.1.2 and the parameters of Table 22-10, the total integrated crosstalk noise from neighboring aggressors into the ENRZ channel as measured on any subchannel of the ENRZ channel shall be less than the value specified by Equation (22-15) and illustrated in Figure 22-7.

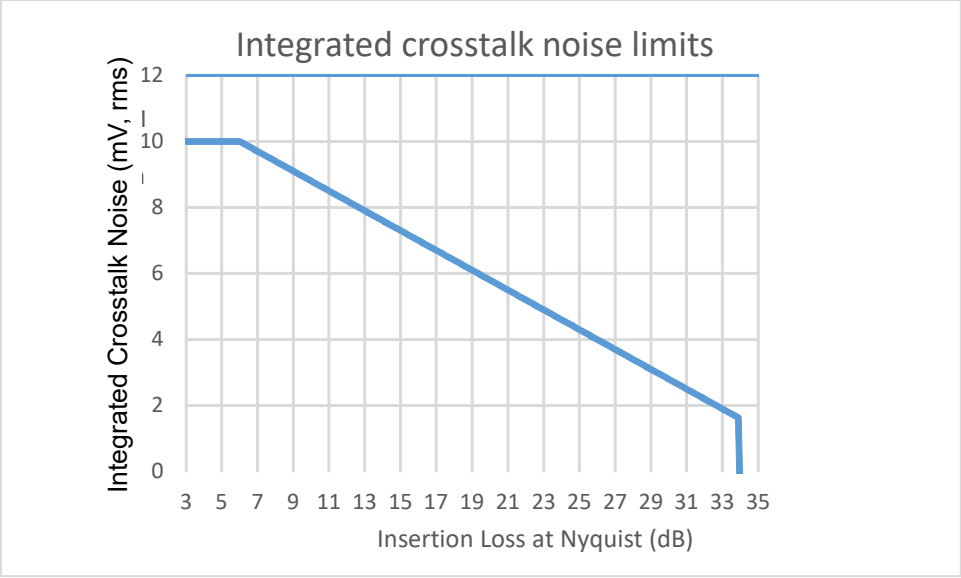
Table 22-10. Channel integrated crosstalk aggressor parameters

Parameter	Symbol	Value	Units
Baud rate	f_b	max. Baud Rate sup. by Channel	Gsym/s
Near-end aggressor peak to peak single-ended output amplitude	A_{nt}	600	mVpp
Far-end aggressor peak to peak single-ended output amplitude	A_{ft}	600	mVpp
Near-end aggressor 20% to 80% rise and fall times	T_{nt}	5.5	ps
Far-end aggressor 20% to 80% rise and fall times	T_{ft}	5.5	ps

$$\sigma_x \le \sigma_{x,\,max} = \begin{cases} 10\ (\text{mV,RMS}) & 3\ \text{dB} < IL \le 6.0\ \text{dB} \\ 11.8 - 0.30\ IL\,(\text{mV,RMS}) & 6.0\ \text{dB} < IL \le 33.9\ \text{dB} \end{cases} \quad (22\text{-}15)$$

In Equation (22-15), the *IL* denotes the value of the channel insertion loss in dB at 0.5 x baud rate (ENRZ).

Figure 22-7. Illustration of integrated crosstalk noise limits



22.2.6.7 Insertion Loss to Conversion Loss Ratio (IC_OR)

The Insertion Loss to Conversion Loss Ratio (IC_OR) of a subchannel, also called the ENRZ Mode Conversion, accounts for crosstalk of one subchannel into another subchannel of the same ENRZ channel.

The Insertion Loss (IL) and Conversion Loss (CL) of a subchannel can be calculated from the S-parameters of the channel as described in Annex 22.D.3. IC_OR is calculated as follows:

$$ICoR_{Di} = IL_{Di} - CL_{Di} \quad (22\text{-}16)$$

where *i* = 0, 1, or 2 is the subchannel designation.

Subchannels must meet the following requirement:

$$ICoR_{Di} > 20dB \qquad \left(0 \le f \le \frac{f_b}{2}\right) \quad (22\text{-}17)$$

for each subchannel *i* = 0 to 2.

22.3 Electrical Characteristics

The electrical signaling is based on high speed low voltage logic with a nominal impedance of 50 Ω between any signals of the quad channel and AC ground.

All devices shall work within the range from 33.16 Gsym/s to 37.50 Gsym/s as specified for the device, with the baud rate tolerance as per Section 3.2.11. Implementation of specific protocols will define the operating baud rate without affecting CEI compliance.

22.3.1 Transmitter Characteristics

Transmitter electrical specifications at compliance point T (see Figure 22-4) are given in Table 22-11. The transmitter shall satisfy jitter requirements specified in Table 22-12. Jitter is measured as specified in Annex 22.B.2, for a BER as specified in Section 22.2.4.

Link budgets in this document assume optimized TX FIR equalization as part of the system management function. Specific implementations are outside the scope of this document.

Table 22-11. Transmitter Electrical Output Specification.

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	T_Baud		33.16		37.50	Gsym/s
Output Max. Peak-to-Peak Voltage Swing (Single-Ended)	T_V_{SEpp}	See Note 1			600	mVpp
Output Common Mode Voltage	T_Vcm	See Note 2	-100		1700	mV
Common Mode Noise	T_Ncm	See Note 3			15	mV_{RMS}
Transmitter Skew	T_Skew	See Note 4			0.06	UI
Single-Ended Output Return Loss	T_S22	See Section 22.3.1.3				dB

NOTES:
1. See Equation (22-4) for definition of V_{SEpp}. These limits shall apply for all equalizer settings.
2. See Equation (22-1) for definition of VCM. Load is defined in Annex 22.B.1.1.
3. Tested using the test equipment setup defined in Annex 22.B.2.1 using the procedure defined in Section 12.3.
4. Time between zero crossings of any two wires of the multi-wire interface for the same baud symbol transition, measured with skew compensation disabled.

Table 22-12. Transmitter Output Jitter Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Clock Random Jitter, RMS	T_CRJrms	See Annex 22.B.2.2			0.005	UI
Clock Deterministic Jitter	T_CDJ	See Annex 22.B.2.2			0.05	UI
Even-Odd Jitter	T_EOJ	See Annex 22.B.2.3			0.03	UI
Signal to Noise Distortion Ratio	T_SNDR	See Annex 22.B.3			19	dB

22.3.1.1 Transmitter Baud Rate

All devices shall work within the range from 33.16 Gsym/s to 37.50 Gsym/s as specified for the device, with the baud rate tolerance as per Section 3.2.11. Note that implementation of specific protocols will define the operating baud rate without affecting CEI compliance.

22.3.1.2 Transmitter Amplitude and Swing

Transmitter single-ended peak-to-peak voltage swing as defined in Equation (22-3) shall not exceed 600 mVpp for any transmitter coefficient configuration. The single-ended transmitter output voltage shall be between -0.3V and 1.9 V with respect to local ground. Transmitter output amplitude shall additionally adhere to the requirements in Section 22.3.1.7.

22.3.1.3 Transmitter Return Loss

The single-ended return loss shall be better than A0 from f0 to f1 and better than A0 + slope*log10(f/f1) where f is the frequency from f1 to f2. Please refer to Figure 3-1 in Section 3.2.10 using the following parameters:

Table 22-13. Transmitter Single-Ended Return Loss Parameters

Parameter	Value	Units
A0	-12	dB
f0	50	MHz
f1	0.1714 x T_Baud	Hz
f2	T_Baud	Hz
Slope	12.0	dB/dec

22.3.1.4 Transmitter Quad-to-Quad Skew

Please refer to Section 3.2.7. For an ENRZ interface, this requirement restricts the skew between any two quad wiring groups.

22.3.1.5 Transmitter Wire-to-Wire Skew

The transmitter implements active skew compensation on each wire with a range of at least 0.40 T_Baud, and a step size no greater than 1 ps. Link budgets in this document assume optimized transmit skew compensation as part of the system management function. Specific implementations are outside the scope of this document.

22.3.1.6 Transmitter Short Circuit Current

Please refer to Section 3.2.9.

22.3.1.7 Transmitter output waveform requirements

The transmitter shall include an equalizer defined as:

$$H(Z) = C_{-1} + C_0 z^{-1} + C_1 z^{-2} \quad (22\text{-}18)$$

22.3.1.7.1 Summary of requirements

The normalized amplitudes of the coefficients of the transmitter equalizer (computed per Annex 22.B.1.5) shall meet the requirements in Table 22-14.

Table 22-14. Coefficient range and step size

Coefficient	Normalized Amplitude		Normalized Step Size (%)
	Min (%)	Max (%)	
C_{-1}	-20	0	1.25 to 5
C_1	-25	0	1.25 to 5
C_0	40	100	1.25 to 5

The amplitude of a coefficient can be computed by multiplying its normalized amplitude by v_f, which is defined in equation Equation (22-29). The "min" is defined as the minimum normalized amplitude of the coefficient that must be supplied by the transmitter to be compliant. The "max" is defined as the maximum normalized amplitude of the coefficient that must be supplied by the transmitter to be compliant.

The peak output voltage shall not exceed limits specified in Section 22.3.1.2 for any values of $|C_{-1}|+|C_0|+|C_1|$.

22.3.1.7.2 Requirements for Transmitter Linearity

The Linear Mismatch Ratio (R_{LM}) is calculated as described in Annex 22.B.1.2 and must meet the requirements specified in Table 22-15. The steady state output voltage (v_f) and linear fit pulse peak values ($p(k)$) are calculated as described in Annex 22.B.1.6 and must meet the requirements specified in Table 22-15. The normalized RMS linear fit error ($e(k)$) is calculated as described in Annex 22.B.1.7 and must meet the requirements specified in Table 22-15.

Table 22-15. Transmitter output waveform requirements

Parameter	Condition	Units	Value
Linear Mismatch Ratio, R_{LM}	min	-	0.92
Steady state output voltage, v_f	max	mVpp	600
Steady state output voltage, v_f	min	mVpp	400
Linear fit pulse peak, p_{max}	min	-	0.85 x v_f
Normalized RMS Linear Fit Error, σ_e	max	-	0.025

22.3.2 Receiver Characteristics

A compliant receiver shall operate at the specified BER when the input signal at compliance point R meets the electrical specifications given in Table 22-16. Jitter specifications at reference R are listed in Table 22-17.

Table 22-16. Receiver Electrical Input Specifications

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud rate	R_Baud		33.16		37.50	GSym/s
Single-ended input voltage	R_V_{SEpp}	See Note 1			600	mVpp
Input Impedance	R_Rdin	See Note 4	40	50	60	Ω
Input Impedance Mismatch	R_Rm				10	%
Single-Ended Input Return Loss	R_S11	See Section 22.3.2.3				
Input Common Mode Voltage	R_Vcm	See Note 2 and 3	-150		1750	mV

NOTES:
1. See Equation (22-4) for definition of V_{SEpp}. This specification applies to each wire of the quad channel.
2. Min. T_Vdiff, AC-Coupling or floating load. For floating load, input resistance shall be ≥ 1kΩ.
3. See Equation (22-1) for definition of V_{CM}.
4. Impedance is between any input of the quad receiver to AC ground.

Table 22-17. Receiver Input Jitter Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Sinusoidal Jitter, Maximum	R_SJ-max	See Note 1			5	UIpp
Sinusoidal Jitter, High Frequency	R_SJ-hf	See Note 1			0.05	UIpp

NOTES:
1. The Receiver shall tolerate the sum of these jitter contributions: Total transmitter jitter from Table 22-12;Sinusoidal jitter as defined in Table 22-17;The effects of a channel compliant to the Channel Characteristics (Section 22.2.6).

22.3.2.1 Input Baud Rate

All devices shall work within the range from 33.16 Gsym/s to 37.50 Gsym/s as specified for the device, with the baud rate tolerance as per Section 3.2.11.

22.3.2.2 Reference Input Signals

The receiver shall accept input signal amplitudes produced by a compliant transmitter connected with the minimum attenuation specified in Figure 22-5 to the receiver. This may be larger than the 600 mVpp maximum value of T_V_{SEpp} for the transmitter due to output/input impedances and reflections.

The minimum input amplitude is defined by the minimum transmitter amplitude, the actual receiver input impedance and the loss of the actual PCB. The receiver interference tolerance test defined in Section 22.3.2.6 tests receiver compliance under minimum amplitude conditions.

22.3.2.3 Input Resistance and Return Loss

The single-ended return loss shall be better than A0 from f0 to f1 and better than A0 + slope*log10(f/f1) where f is the frequency from f1 to f2. Please refer to Figure 3-1 in Section 3.2.10 using the following parameters.

Table 22-18. Receiver Single-Ended Return Loss Parameters

Parameter	Value	Units
A0	-12	dB
f0	50	MHz
f1	0.1714 x R_Baud	Hz
f2	R_Baud	Hz
Slope	12.0	dB/dec

22.3.2.4 Input Quad-to-Quad Skew

Please refer to Section 3.2.8. For an ENRZ interface, this requirement restricts the skew through receivers for any two quad groups.

22.3.2.5 Absolute Input Voltage

The absolute voltage levels with respect to the receiver ground at the input of the receiver are dependent on the transmitter implementation and the inter-ground difference. The voltage levels at the input of an AC coupled receiver (if the effective AC coupling is done within the receiver) or at the TX side of the external AC coupling cap (if AC coupling is done externally) will be between -0.3 to 2.0V with respect to local ground.

22.3.2.6 Receiver Interference Tolerance Test

The receiver interference tolerance shall consist of four separate tests as described in Annex 22.C.1 with the parameters specified in Table 22-19. The receiver shall satisfy the requirements for interface tolerance specified in Annex 22.C.1 for all tests.

Table 22-19. Receiver Interference Tolerance Test Parameters

Parameter	Test 1 Values	Test 2 Values	Test 3 Values	Test 4 Values	Units / Notes
Target BER (Test Requirement)	10^{-12}	10^{-12}	10^{-12}	10^{-12}	
m_{TC} (min.)	1.0	0.5	1.0	0.5	See Note 1
Amplitude of broadband noise (min. RMS)	5.2	12	5.2	12	mV
Applied Sinusoidal Jitter amplitude (min.)	R_SJ-max	R_SJ-max	R_SJ-hf	R_SJ-hf	See Note 2
Applied Sinusoidal Jitter frequency	(R_Baud / 10^6) ±10%		(R_Baud / 100) ±10%		
f_{ILmin}	See Table 22-9				See Note 3
f_{ILmax}	See Table 22-9				
f_{min}	See Table 22-8				

NOTES:
1. The m_{TC} parameter is defined in Annex 22.C.1.4, Equation (22-45).
2. SJ values are defined in Table 22-17.
3. Also see Section 22.2.6 for definitions of these parameters.

22.3.2.7 Receiver Imbalance Tolerance Test

The receiver imbalance tolerance shall consist of a total of sixteen separate tests as described in Annex 22.C.2. Test parameters are specified in Table 22-20 for four tests on wire *i*. These tests are repeated for each of the wires W3, W2, W1, and W0 of the quad channel, for a total of sixteen separate tests. The receiver shall satisfy the requirements for imbalance tolerance specified in Annex 22.C.2 for all tests.

Table 22-20. Receiver Imbalance Tolerance Test Parameters

Parameter	Test 1 Values	Test 2 Values	Test 3 Values	Test 4 Values	Units / Notes
Target BER (Test Requirement)	10^{-12}	10^{-12}	10^{-12}	10^{-12}	
m_{TC} (min.)	1.0	0.5	1.0	0.5	See Note 1
Amplitude of broadband noise (min. RMS)	5.2	12	5.2	12	mV
f_{ILmin}	See Table 22-9				See Note 2
f_{ILmax}	See Table 22-9				
f_{min}	See Table 22-8				
V_{bias} on wire *i*	$V_{cm} + (0.15 \times v_f)$		$V_{cm} - (0.15 \times v_f)$		See Note 3, 4
V_{bias} on other wires	V_{cm}				

NOTES:
1. The m_{TC} parameter is defined in Annex 22.C.1.4, Equation (22-45).
2. Also see Section 22.2.6 for definitions of these parameters.
3. Repeat the four tests for each of wires i = W3, W2, W1, and W0 of the ENRZ lane.
4. Parameter vf is calculated as described in Annex 22.B.1.6.

22.3.2.8 Receiver Skew Tolerance Test

The receiver skew tolerance shall consist of a total of eight separate tests as described in Annex 22.C.3. Test parameters are specified in Table 22-21 for each test. The receiver shall satisfy the requirements for imbalance tolerance specified in Annex 22.C.3 for all tests.

Table 22-21. Receiver Skew Tolerance Test Parameters

Parameter	Test 1	Test 2	Test 3	Test 4	Test 5	Test 6	Test 7	Test 8	Units / Notes
Target BER (Test Requirement)	10^{-12}	10^{-12}	10^{-12}	10^{-12}	10^{-12}	10^{-12}	10^{-12}	10^{-12}	
m_{TC} (min.)	1.0	0.5	1.0	0.5	1.0	0.5	1.0	0.5	See Note 1
Amplitude of broadband noise (min. RMS)	5.2	12	5.2	12	5.2	12	5.2	12	mV
f_{ILmin}	See Table 22-9								See Note 2
f_{ILmax}	See Table 22-9								
f_{min}	See Table 22-8								
Preskew on wire A	Nominal + 0.15 × (1 / R_Baud)		Nominal value.		Nominal value.		Nominal value.		See Note 3
Preskew on wire B	Nominal value.		Nominal + 0.15 × (1 / R_Baud)		Nominal value.		Nominal value.		
Preskew on wire C	Nominal value.		Nominal value.		Nominal + 0.15 × (1 / R_Baud)		Nominal value.		
Preskew on wire D	Nominal value.		Nominal value.		Nominal value.		Nominal + 0.15 × (1 / R_Baud)		

NOTES:
1. The m_{TC} parameter is defined in Annex 22.C.1.4, Equation (22-45).
2. Also see Section 22.2.6 for definitions of these parameters.
3. "Nominal value" represents any driver preskew setting such that the driver outputs are approximately aligned with minimal skew between wires. A setting of "Nominal + N ps" indicates the additional skew on this wire must be at least N ps.

22.A Annex - Test Patterns

The following patterns shall be used for the testing of transmitter and receiver compliance, including jitter tolerance and output jitter compliance.

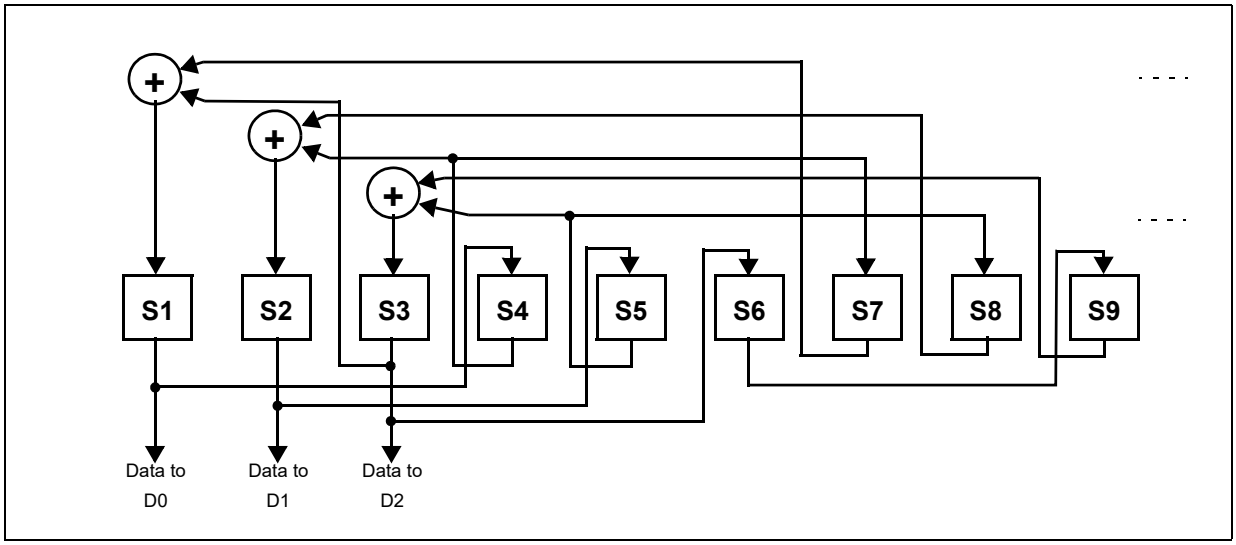
22.A.1 PRBS9 Polynomial

This pattern is a free running PRBS9 generator defined by the serial polynomial:

$$x^9 + x^5 + 1$$

Three bits of the polynomial are sent on ENRZ subchannels D2, D1, and D0 to generate each baud symbol, as shown in Figure 22-8:

Figure 22-8. PRBS9 Pattern Generation



22.A.2 Quad Short Stress Pattern Random (SSPR-Q)

The SSPR-Q pattern is similar to the SSPR pattern defined in Annex 2.D.2. SSPR-Q differs from SSPR in that the pattern contains an extra pad bits such that the pattern length is divisible by 3.

SSPR patterns were chosen to have baseline wander and timing content that are at least as stressful as 10,000 years of random binary. The pattern is described in this section and the pattern bit sequence is defined in Annex 22.A.5.

- The baseline wander was assessed with a cut-off frequency of baudrate/10,000.
- The clock content was assessed with a corner frequency of baudrate/1667.
- The period of 10,000 years was chosen on the basis of random binary exceeding the baseline wander timing content limits of the short pattern once in 10 years in a network containing 1000 random streams.

The SSPR-Q pattern is defined as described in Figure 22-9:

Figure 22-9. Quad Short Stress Pattern Random (SSPR-Q)

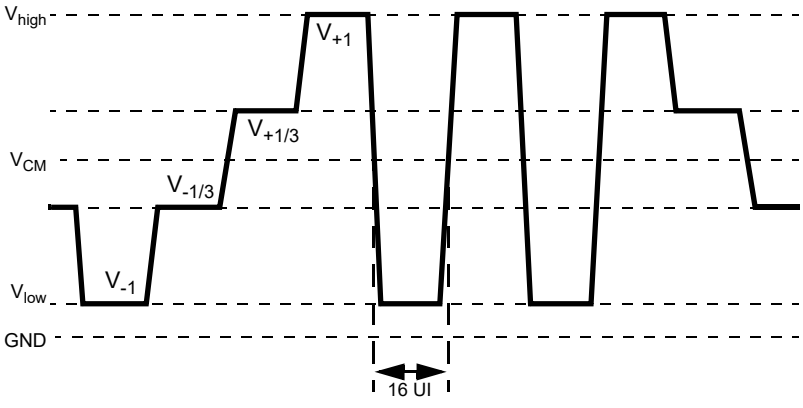
PRBS28 Seed=0080080	CID 1, 72 x0	PRBS28 Seed=FFFFFFF	PRBS28 Seed=0080080 Diff. Encoded	$\overline{\text{PRBS28}}$ Seed=0080080	$\overline{\text{CID}}$ 0, 72 x1	$\overline{\text{PRBS28}}$ Seed=FFFFFFF	$\overline{\text{PRBS28}}$ Seed=0080080 Diff. Encoded
5437 bits	73 bits	5437 bits	5469 bits	5437 bits	73 bits	5437 bits	5469 bits

- Total length 32,832 bits
- All 2^{28}-1 PRBS28 sequences are generated using taps 25 and 28
- Block 1 is 5437 bits of PRBS28 seed = 0x0080080 and begins with 8 x 0, 1, 11 x 0, 1, 12 x 0, 1, and so forth.
- Block 2 is 1 followed by 72 x 0
- Block 3 is 5437 bits of PRBS28 seed = 0xFFFFFFF and begins with 28 x 1, 25 x 0, 3 x 1, 22 x 0, and so forth.
- Block 4 takes the same sequence as block 1 (extended by 32 bits) and encodes it as follows:
  - — A zero causes a change of output
  - — A one causes no change of output
  - — The output before the first bit is assumed to have been zero
  - — This block begins 10101010010101010101101010101011011010 ...
- Blocks 5 to 8 are the inverse of blocks 1 to 4 respectively.

22.A.3 Linearity Test Pattern

The Linearity Test Pattern drives the waveform shown in Figure 22-10 on the driver leg (W3, W2, W1, or W0) that is being tested.

Figure 22-10. Linearity Test Pattern Waveform



This pattern is described as follows:

- The time between each transition of the waveform in Figure 22-10 is 16 UI.
- The data driven on subchannels (1, 2, 3) to produce these levels depends on the driver leg that is being tested as described below. The corresponding pattern bit sequences are defined in Annex 22.A.5.
  - Driver W3: (0, 1, 1), (1, 1, 1), (0, 0, 0), (1, 0, 0), (0, 1, 1), (1, 0, 0), (0, 1, 1), (1, 0, 0), (0, 0, 0), (1, 1, 1), and repeat.
  - Driver W2: (1, 1, 0), (0, 1, 0), (1, 0, 1), (0, 0, 1), (1, 1, 0), (0, 0, 1), (1, 1, 0), (0, 0, 1), (1, 0, 1), (0, 1, 0), and repeat.
  - Driver W1: (1, 0, 1), (0, 0, 1), (1, 1, 0), (0, 1, 0), (1, 0, 1), (0, 1, 0), (1, 0, 1), (0, 1, 0), (1, 1, 0), (0, 0, 1), and repeat.
  - Driver W0: (0, 0, 0), (1, 0, 0), (0, 1, 1), (1, 1, 1), (0, 0, 0), (1, 1, 1), (0, 0, 0), (1, 1, 1), (0, 1, 1), (1, 0, 0), and repeat.
- Signal voltage levels are measured at the points of the waveform labeled V_{-1}, $V_{-1/3}$, $V_{+1/3}$, and V_{+1} in Figure 22-10. Each measurement is performed 8 UI from the prior transition edge, with a tolerance of ±1 UI.

22.A.4 Clock Jitter Test Patterns

Test patterns defined in this section are used to ensure transmitter jitter specifications are met.

22.A.4.1 Clock Jitter Pattern A

Clock Jitter Pattern A drives alternating (-1, +1) states on the output driver.

The data driven on subchannels (D2, D1, D0) to produce these levels depends on the driver leg being tested as described below. The corresponding pattern bit sequences are defined in Annex 2.A.

- Driver W3: (0, 0, 0), (1, 1, 1), and repeat.
- Driver W2: (1, 1, 0), (0, 0, 1), and repeat.
- Driver W1: (1, 0, 1), (0, 1, 0), and repeat.
- Driver W0: (0, 1, 1), (1, 0, 0), and repeat.

22.A.4.2 Clock Jitter Pattern B

Clock Jitter Pattern B drives alternating (-1, +1) states on the output driver, repeated 15 times, and then drives alternating (+1, -1) states on the output driver, repeated 16 times, and so forth.

The data driven on subchannels (D2, D1, D0) to produce these levels depends on the driver leg being tested as described below. The corresponding pattern bit sequences are defined in Annex 22.A.5.

— Driver W3: Repeat (0, 0, 0), (1, 1, 1) 15 times; repeat (1, 1, 1), (0, 0, 0) 16 times; and repeat pattern.

— Driver W2: Repeat (1, 1, 0), (0, 0, 1) 15 times; repeat (0, 0, 1), (1, 1, 0) 16 times; and repeat pattern.

— Driver W1: Repeat (1, 0, 1), (0, 1, 0) 15 times; repeat (0, 1, 0), (1, 0, 1) 16 times; and repeat pattern.

— Driver W0: Repeat (0, 1, 1), (1, 0, 0) 15 times; repeat (1, 0, 0), (0, 1, 1) 16 times; and repeat pattern.

22.A.5 Test Pattern Definitions

CEI Short Stress Pattern Random (SSPR-Q)

Below is the definition of the test pattern described in Section 22.A.2 as hexadecimal digits with the most significant bit of each digit transmitted first. Blocks #1 to #4 of the pattern are shown below. Blocks #5 to #8 are the inverse of blocks #1 to #4.

```
00800800480480208208124924880000 0C8000068800032C8001A48800C80C8068868832
CB2C9A49248480000A080005A480028808016C8480A08A085A4DA4A882081EC9248E8800
0FAC80072C8803E48C81CC0E88FAC7ACF2CFACB64B2C904124812480088008004C8048228
820936C924080800448480260A081165A489A4880C480C86E0868B1E4B2D3EC1244C8C80
628E88376FAC98C12C85EC848AA88A0DFECDA6208A09724DA42E020855E124AFAE801D2D
A80F440E875647ABDE47AF52C7AD5C4FAC7BE32CFA4FA4B283281269A68812492C880004
8C80020E880127AC8081AC8848CC8CA0EA8E9A7BEFA49A492804800682080329248 1A600
08C96004E826023A91613EE1A68C9EC92E868805AB2C828F24896F600C214606D2B76304
70C7B27F6FA218412B2DA48724080BE044854E260AF3F165D6C7A4B60FA810672E8935E5
AC09AC8CC44C8EAE628FBDD76F2536C160C80CA668869952CB253C4920CDE0026A2E0113
B5E098E1AE45FECDC6A08A3F3A4DBC6E8205F1A922A7CE03799BE18B544EDD1F63835E47
F99AC78354CFB99F2B27566721DE55E2F2CFAF564B2D5E41247AC4807ACE083ACBE49EC9
4C068832C32C9A4DA48482080A092485A4000A884005ECA402A898417EC5A4A88E881ECF
AC8E8B2C8FAD248F2C400F64E407443C43D65DE5D64B2CB6412490448001260800816480
48A40820D8449261A60016C9600A082605A491628801A76C80C9C088687C4CB2B9E29277
6F601CC1460FACB7672C90C5E4816EAC08A1BCC4DAC5AE20CE8DF26BAE26136DF1688027
A2C811AB4889CF10CC7B796AFA0B23D2A523D478C3D77BEDD6CA4836098098645845B469
A681724928AE0006DDE003032E01B1A5E0C3C8AE6DD8DDD031E3351BEFA9DC492E73E005
DECE02B28BE1726D4EAE1073BDE93EE52A0C9CC7A687AFA92BAD2E076C45E3C400000000
0000000003FFFFFFC000001C00000FC000071C0003FFC001C01C00FC0FC071C71C3FFFFF
DC000013C00008DC0004E3C0023FDC013C13C08DC8DC4E38E3E3FFFFCFC0001B1C000C3F
C006DC1C0303CFC1B1DB1CC3F03FADC71C2C3FFFD4DC001723C00AE3DC05DFD3C2B214DD
722B236E372381F8E3F8E3FFC3FFC01DC01C0F3C0FC76DC71FC03FFE1C1C00EFCFC0791B
1C3B1C3FDE3FDC12FC13C851C8D8ADF8E1DC23FEF3D3C096D4DC420723E523E3CCC3CFDA
ADDB10FC303971DB1F2FF03E65071CD4D3FFA724C029E02C166E14CA51EB298DEB265E2B
214AF722B1D4E373F73F8EC4EC3F8E38DC3FFFE3DC000FD3C00714DC03FB23C1C223DCFD
33D3B14AD4E3B1C73FE3FFEC0FC008C71C04EFFFC239001D3F100F4C790752FB13DC5238
D3EC3FE4C8DC0C28E3C6D6FFDF0610127369081E82148EA92B0FBE073724E3E8E03FCAFE
1C19D0EFCD75791A6DEB1C902B3F81172C389AE4DFC4DC221E23D32EF3D4A596D7189206
FDC023113C13B98DC8E75E38FDDAFFF130D0078B6503BD04D1E55225ECFC30A8B1DB5ED3
F01A84C70CEA2FF6BBB5043661D25856F409AE15444DEBF6622B445737166EE8FA519AF2
8DD4D66E372651F8E14DE3FEB22FC0B2351C5239DFEC3F7208DC4E24E3E3F03FCFC71C1B
1FFFCC3E001ADCE00CC3BE06ADE4E33C2C3FADD4DC2C3723D4D8E3D721FFD6E2E0161F5E
0A6E5AE591C8DC91F8E381E3FFF8EFC003F91C01C31FC0FDBE1C7104EFFF923900303F10
1B1C790C3FFB16DC023A03C13EA1DC8CBAF38E96D6FFA206102B23691723821AE3F92CDF
```

```
C304A21DB21B2F022C257134D0EF8925793C00EB0DC07B363C3A287DDEB6B932B0370A73
18F59EBDF596B5259231C0903BFC411E41E49EC4EC068E38C32FFFEDA5000808D00484E5
020A3CD125BDA5808508984AD4C5A1C72E8AFFE5ADD00C8C35068ED9D32F8174A538AD18
D54AAB555B55B552B52B56DB6DB4AAAAABB55555CB555513B555724B5544ABB55CB5CB51
3B13B724924A4AAAAB2B55558DB55534AB5563B5B54D4B2B58DB8DB34AD4A83B6DB434AA
ABF3B555EC4B55024BB57BABCB40C5F3BEC40C4E24EC495A924A924AAB4AAB55BB55B52C
B52B6E3B6DAB54AAA5B5B5522B2B569D8DB48DB4ABA4ABB5C2B5CB17DB13903A925BB44A
A2CBCB51E3F3B7456C4A7C4A4B334B2B803B8DD2B4D49EDB8DAC2AD4A67D6DB3F3CAA86C
73541A5435E625F307DA0C193A0C67A40C5F02EC40DBF24ECAECA9237234A92493B4AAAA
4BB5552BCB556DF3B54A8C4B5B444BB2BCCBC8DF03F248DB6CAA4AAA352B55136DB5722A
AB449D55BCADD52F369D6FC28DCBB7C493CA34AA7313B534124B63E2ABAD65D5C6CE1D15
A145F1201C0D28A56CEC724A1254AB02A5B59BD22B3EFE9D863A0DB1D40CA95DEC349182
73AB73B445A44BCC22CBF079E3ED91C562BB544DDCB5C8993B126FA492BB82AADCD3D569
0E7D48BD73DA7FC47A32B4D010DB8FA3CAD581736D32042AE088FD74E65BC797E2F51825
FF773A0AE6440F77ECEDE6221287D982C13BF3E624EC67DA925F3A4AA0C42B50C4FDB7C4
9BAA34AEC513B724724A4AD4AB2B6DB58DAAAB34A55583B2553348A5603A724CB434A83B
F3B434EC4BF3924BEC5AABE24255E5AFA506278279DB13B1DA92495A4AAA922B554A9DB5
5B4DAB52B8A5B6DD722AA9C49D54D4ADD58DB69D34AA8DE3B544854B5CA05BB13082C921
E3E2A84565D40C4E1DEC4945824A9C33AB4D7045B8C58C2D44347EDCF3D2291C7E9CB552
0D3B568CE4B48416BBA0E09CC0D4ED06CD92F9A0BAF9E0FC79C4DB51D48AB75DA75A71A3
72356124934C2AAA387D551513D571727D4504B3DC78B879517D119703F3785B6C2102AA
783BD53134FD61239BCC295EF07C903D932BB7BA0DCA0C0C930C6C2A1C5A7D054233F85F
```

Linearity Test Pattern

Below is the definition of the test pattern described in Section 22.A.3. Every 3 bits are striped across subchannels 1, 2, and 3 respectively, and symbols are transmitted in the order from most significant bit to least significant bit. The pattern depends upon the driver leg being tested.

Driver W3:

```
000000000000 924924924924 6DB6DB6DB6DB FFFFFFFFFFFF 000000000000
FFFFFFFFFFFF 000000000000 FFFFFFFFFFFF 6DB6DB6DB6DB 924924924924
```

Driver W2:

```
DB6DB6DB6DB6 492492492492 B6DB6DB6DB6D 249249249249 DB6DB6DB6DB6
249249249249 DB6DB6DB6DB6 249249249249 B6DB6DB6DB6D 492492492492
```

Driver W1:

```
B6DB6DB6DB6D 249249249249 DB6DB6DB6DB6 492492492492 B6DB6DB6DB6D
492492492492 B6DB6DB6DB6D 492492492492 DB6DB6DB6DB6 249249249249
```

Driver W0:

```
6DB6DB6DB6DB FFFFFFFFFFFF 000000000000 924924924924 6DB6DB6DB6DB
924924924924 6DB6DB6DB6DB 924924924924 000000000000 FFFFFFFFFFFF
```

Clock Jitter Pattern A and B

Below is the definition of the test patterns described in Section 22.A.4. Every 3 bits are striped across subchannels D2, D1, and D0 respectively, and symbols are transmitted in the order from most significant bit to least significant bit. The pattern depends upon the driver leg being tested.

Since pattern A is 6 bits long (which is not divisible by 4), the two least significant bits of the last digit shown are not included in the sequence.

Since pattern B is 186 bits long (which is not divisible by 4), the two least significant bits of the last digit shown are not included in the sequence.

Driver W3:

```
Clock Jitter Pattern A: 1C

Clock Jitter Pattern B: 1C71C71C71C71C71C71C71F8E38E38E38E38E38E38E38E0
```

Driver W2:

```
Clock Jitter Pattern A: C4

Clock Jitter Pattern B: C71C71C71C71C71C71C71C4E38E38E38E38E38E38E38E38
```

Driver W1:

```
Clock Jitter Pattern A: A8

Clock Jitter Pattern B: AAAAAAAAAAAAAAAAAAAAAA955555555555555555555554
```

Driver W0:

```
Clock Jitter Pattern A: 70

Clock Jitter Pattern B: 71C71C71C71C71C71C71C7238E38E38E38E38E38E38E38C
```

22.B Annex - Transmitter Compliance Tests

Test procedures described in this annex are used to test transmitter compliance.

22.B.1 Transmitter Output Waveform Tests

This section describes measurements to ensure the transmitter output waveform meets specifications.

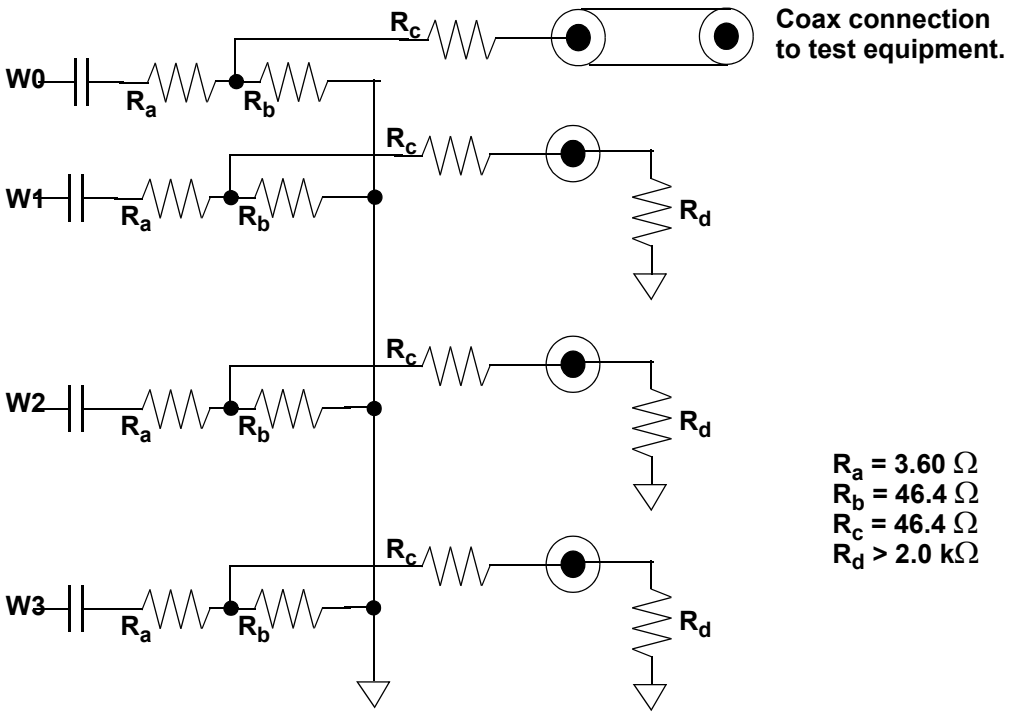
22.B.1.1 Test Equipment Setup

Test equipment used to measure the transmitter output for waveform tests is connected to test point T (either T_E or T_I) as defined in Section 22.2.6.1 using the termination network described in Figure 22-11. The driver being tested is connected to the test equipment, and the other drivers of the CEI quad are terminated as shown.

DC resistance values should have a tolerance of ±1%.

The return loss of the network should be better than 20 dB from baud rate divided by 1667 to 1.5 times the baud rate unless otherwise noted.

Figure 22-11. Driver Test Load



22.B.1.2 Linear Mismatch Ratio

Transmitter linearity is measured using the waveform described in Annex 22.A.3 and the test load described in Annex 22.B.1.1. Signal voltage levels measured at the points labeled V_{-1}, $V_{-1/3}$, $V_{+1/3}$, and V_{+1} in Figure 22-10 are used in the following calculations.

The minimum delta between voltage levels for signal states on the wire (S_{min}) is calculated as:

$$S_{min} = \frac{min((V_{+1} - V_{+1/3}), (V_{+1/3} - V_{-1/3}), (V_{-1/3} - V_{-1}))}{2} \quad (22\text{-}19)$$

and the linear mismatch ratio (R_{LM}) is calculated as:

$$R_{LM} = \frac{6 \times S_{min}}{(V_{+1} - V_{-1})} \quad (22\text{-}20)$$

Specifications for R_{LM} must be met on each of the W3, W2, W1, and W0 transmitters.

The voltage levels measured in this section are further used to calculate the average signal voltage (V_{avg}) and the effective voltage levels for the $V_{-1/3}$ and $V_{+1/3}$ wire states ($EV_{-1/3}$ and $EV_{+1/3}$) as follows:

$$V_{avg} = \frac{V_{+1} + V_{+1/3} + V_{-1/3} + V_{-1}}{4} \quad (22\text{-}21)$$

$$EV_{-1/3} = \frac{V_{-1/3} - V_{avg}}{V_{-1} - V_{avg}} \quad (22\text{-}22)$$

$$EV_{+1/3} = \frac{V_{+1/3} - V_{avg}}{V_{+1} - V_{avg}}$$

The $EV_{-1/3}$ and $EV_{+1/3}$ values are used in Annex 22.B.1.4.

22.B.1.3 Waveform acquisition for Linear Fit Measurements

The transmitter under test repetitively transmits the PRBS9 pattern defined in Annex 22.A.1. The waveform shall be captured with an effective sample rate that is *M* times the signaling rate of the transmitter under test. The value of *M* shall be an integer not less than 7. Averaging multiple waveform captures is recommended.

The captured waveform shall represent an integer number of repetitions of the test pattern totaling *N* bits. Hence the length of the captured waveform should be *M* x *N* samples. The waveform should be aligned such that the first *M* samples of waveform correspond to the first bit of the test pattern, the second *M* samples to the second bit, and so on.

For the PRBS9 pattern defined in Annex 22.A.1: N = 511.

22.B.1.4 Determining Linear Fit to Measured Waveform

Unless otherwise specified, waveforms for this procedure are measured as described in Annex 22.B.1.3 with the test setup described in Annex 22.B.1.1.

Given the captured waveform *y(k)* and corresponding aligned symbols *x(n)*, define the *M*-by-*N* waveform matrix *Y* as shown in Equation (22-23).

$$Y = \begin{bmatrix} y(1) & y(M+1) & \dots & y(M(N-1)+1) \\ y(2) & y(M+2) & \dots & y(M(N-1)+2) \\ \dots & \dots & \dots & \dots \\ y(M) & y(2M) & \dots & y(MN) \end{bmatrix} \quad (22\text{-}23)$$

Rotate the symbols vector *x* by the specified pulse delay T_D_p to yield x_r.

$$x_r = \left[x(\mathrm{T_D}_p + 1)\ x(\mathrm{T_D}_p + 2)\ \dots\ x(N)\ x(1)\ \dots\ x(\mathrm{T_D}_p) \right] \quad (22\text{-}24)$$

Define the matrix *X* to be an *N*-by-*N* matrix derived from x_r as shown in Equation (22-25).

$$X = \begin{bmatrix} x_r(1) & x_r(2) & \dots & x_r(N-1) & x_r(N) \\ x_r(N) & x_r(1) & \dots & x_r(N-2) & x_r(N-1) \\ \dots & \dots & \dots & \dots & \dots \\ x_r(2) & x_r(3) & \dots & x_r(N) & x_r(1) \end{bmatrix} \quad (22\text{-}25)$$

Define the matrix X_1 to be the first T_N_p rows of *X* concatenated with a row vector of 1's of length *N*. The *M*-by-(T_N_p + 1) coefficient matrix, *P*, corresponding to the linear fit is then defined by Equation (22-26).

$$P = Y{X_1}^T(X_1{X_1}^T)^{-1} \quad (22\text{-}26)$$

In Equation (22-26) the superscript "T" denotes the matrix transpose operator.

Define the error matrix *E* as shown Equation (22-27).

$$E = PX_1^T - Y = \begin{bmatrix} e(1) & e(M+1) & \dots & e(M(N-1)+1) \\ e(2) & e(M+2) & \dots & e(M(N-1)+2) \\ \dots & \dots & \dots & \dots \\ e(M) & e(2M) & \dots & e(MN) \end{bmatrix} \quad (22\text{-}27)$$

The error waveform, *e(k)*, is then read column-wise from the elements of *E*.

Define P_1 to be a matrix consisting of the first T_N_p columns of the matrix *P* as shown in Equation (22-28).

$$P_1 = \begin{bmatrix} p(1) & p(M+1) & \dots & p(M(\mathrm{T_N}_p-1)+1) \\ p(2) & p(M+2) & \dots & p(M(\mathrm{T_N}_p-1)+2) \\ \dots & \dots & \dots & \dots \\ p(M) & p(2M) & \dots & p(R(\mathrm{T_N}_p)) \end{bmatrix} \quad (22\text{-}28)$$

The linear fit pulse response, *p(k)*, is then read column-wise from the elements of P_1.

22.B.1.5 Transmitter Equalization Coefficients

The coefficients of the transmitter equalizer shall be determined from the measured waveform during the transmitter compliance test using the process described below.

1. The transmitter under test is preset such that C_0 is its maximum value (C_{0_max}) and all other coefficients are zero.
2. Capture at least one complete cycle of the PRBS9 pattern as described in Annex 22.B.1.3.
3. Compute the linear fit to the captured waveform (*p(k)*) per Annex 22.B.1.4 with parameter values T_D_p = 2 and T_N_p = 8.
4. Define t_x to be the time where the rising edge of the linear fit pulse, *p*, from step 3 crosses 50% of its peak amplitude.
5. Sample the linear fit pulse, *p*, at symbol-spaced intervals relative to the time $t_0 = t_x + 0.5$ UI, interpolating as necessary to yield the sampled pulse p_i.
6. Use p_i to compute the vector of coefficients, *w*, of a T_N_w-tap symbol-spaced transversal filter that equalizes for the transfer function from the transmit function to T per Annex 22.B.1.8.

For each configuration of the transmit equalizer:

7. Configure the transmitter under test as required.
8. Capture at least one complete cycle of the PRBS9 pattern as described in Annex 22.B.1.3.
9. Compute the linear fit to the captured waveform ($p(k)$) per Annex 22.B.1.4 with parameter values T_D_p = 2 and T_N_p = 8.
10. Define t_x to be the time where the rising edge of the linear fit pulse, p, from step 3 crosses 50% of its peak amplitude.
11. Sample the linear fit pulse, p, at symbol-spaced intervals relative to the time $t_0 = t_x + 0.5$ UI, interpolating as necessary to yield the sampled pulse p_i.
12. Equalize the sampled pulse, p_i, using the coefficient vector, w, computed in step 6 per Annex 22.B.1.8 to yield the equalized pulse q_i.

The normalized amplitude of coefficient C_{-1} is the value of q_i at time $t_0 + (T_D_w - 1)$ UI.
The normalized amplitude of coefficient C_0 is the value of q_i at time $t_0 + T_D_w$ UI.
The normalized amplitude of coefficient C_1 is the value of q_i at time $t_0 + (T_D_w + 1)$ UI.

Specifications for transmitter equalization coefficients shall be met for all for each of the W3, W2, W1, and W0 transmitters.

22.B.1.6 Steady State Voltage and Linear Fit Pulse Peak

For each configuration of driver equalization coefficients, capture at least one complete cycle of the PRBS9 pattern as described in Annex 22.B.1.3.

Compute the linear fit pulse response *p(k)* using the procedure in Annex 22.B.1.4 with parameter values T_D_p = 2 and T_N_p = 8. The aligned symbol values *x(n)* used to construct x_r should be values of either +1, $EV_{+1/3}$, $EV_{-1/3}$, or -1. The values of $EV_{+1/3}$ and $EV_{-1/3}$ were calculated in Annex 22.B.1.2.

The steady-state voltage v_f is defined as:

$$v_f = \frac{1}{M} \sum_{k=1}^{M \bullet \mathrm{T_Np}} p(k) \qquad (22\text{-}29)$$

Specifications for v_f and specifications for *p(k)* values relative to v_f shall be met for all transmitter configurations and for each of the W3, W2, W1, and W0 transmitters.

22.B.1.7 Linear Fit Error

For each configuration of driver equalization coefficients, capture at least one complete cycle of the PRBS9 pattern as described in Annex 22.B.1.3.

Compute the linear fit pulse response (*p(k)*) and the error between the linear fit and the measured waveform (*e(k)*) using the procedure in Annex 22.B.1.4 with parameter values T_D_p = 2 and T_N_p = 8. The aligned symbol values *x(n)* used to construct x_r should be values of either +1, $EV_{+1/3}$, $EV_{-1/3}$, or -1. The values of $EV_{+1/3}$ and $EV_{-1/3}$ were calculated in Annex 22.B.1.2.

Specifications for v_f and specifications for the RMS value of *e(k)* normalized to the peak value of *p(k),* designated σ_e, shall be met for all transmitter equalizer settings and for each of the W3, W2, W1, and W0 transmitters.

22.B.1.8 Removal of the Transfer Function between the Transmitter and T

Rotate sampled pulse response p_i by the specified equalizer delay T_D_w to yield p_r as shown in Equation (22-30).

$$p_r = \left[p_i(\mathrm{T_D}_w + 1)\ p_i(\mathrm{T_D}_w + 2)\ \ldots\ p_i(N)\ p_i(1)\ \ldots\ p_i(\mathrm{T_D}_w) \right] \qquad (22\text{-}30)$$

Define the matrix P_2 to be a T_N_p-by-T_N_p matrix derived from p_r as shown in Equation (22-31).

$$X = \begin{bmatrix} p_r(1) & p_r(\mathrm{T_N}_p) & \dots & p_r(3) & p_r(2) \\ p_r(2) & p_r(1) & \dots & p_r(4) & p_r(3) \\ \dots & \dots & \dots & \dots & \dots \\ p_r(\mathrm{T_N}_p) & p_r(\mathrm{T_N}_p - 1) & \dots & p_r(2) & p_r(1) \end{bmatrix} \quad (22\text{-}31)$$

Define the matrix P_3 to be the first T_N_w rows of P_2. Define a unit pulse column vector x_p of length T_N_p. The value of element $x_p(T_D_p + 1)$ is 1 and all other elements have a value of 0. The vector of filter coefficients w that equalizes p_i is then defined by Equation (22-32).

$$w = (P_3{}^T P_3)^{-1} P_3{}^T x_p \quad (22\text{-}32)$$

Given the column vector of equalizer coefficients, w, the equalized pulse response q_i is determined by Equation (22-33).

$$q_i = P_3 w \quad (22\text{-}33)$$

22.B.2 Transmitter Output Jitter

This section describes measurements to ensure transmitter jitter requirements are met.

22.B.2.1 Test Equipment Setup

Test equipment used to measure the transmitter output for jitter tests is connected to test point T (either T_E or T_I) as defined in Section 22.2.6.1 using the test load described in Annex 22.B.1.1.

22.B.2.2 Deterministic and Random Clock Jitter

Clock random jitter (CRJ_{rms}) and clock deterministic jitter (CDJ) are measured as specified in this section.

Both CRJ_{rms} and CDJ are measured with the driver transmitting the Clock Jitter Pattern A test pattern defined in Annex 22.A.4.1. Note that the test pattern varies based on which transmitter (W3, W2, W1, or W0) is being tested. The pattern length shall be at least 10^7 symbols. Using appropriate test equipment, the zero crossings $T_{ZC}(i)$ are captured.

The average pulse width ΔT_{avg} is calculated as follows:

$$\Delta T_{avg} = \frac{T_{ZC}(N) - T_{ZC}(1)}{N-1} \quad (22\text{-}34)$$

The jitter series τ(j) is calculated as follows:

$$\tau(j) = T_{ZC}(j) - ((j-1) \cdot \Delta T_{avg}) - T_{ZC}(1) \qquad j = 2, 3, \ldots, N \quad (22\text{-}35)$$

Filter the jitter samples with the effect of a single-pole high-pass filter (20 dB per decade low-frequency response) with -3 dB gain at 1.6 MHz and a peak gain of 3 dB at 6 MHz. The filtered jitter samples are designated $\tau_{HPF}(j)$.

Create a CDF as a function of $\tau_{HPF}(j)$. From this CDF, determine J_5 as the difference between τ_{HPF} at the (1 - 0.5 x 10^{-5}) and (0.5 x 10^{-5}) probabilities respectively. Determine J_6 as the difference between τ_{HPF} at the (1 - 0.5 x 10^{-6}) and (0.5 x 10^{-6}) probabilities respectively.

Using J_5 and J_6, calculate CRJ_{rms} and CDJ as follows:

$$\begin{bmatrix} CRJ_{rms} \\ CDJ \end{bmatrix} = \begin{bmatrix} 1.0538 & -1.0538 \\ -9.3098 & 10.3098 \end{bmatrix} \begin{bmatrix} J_6 \\ J_5 \end{bmatrix} \quad (22\text{-}36)$$

Specified limits for CRJ_{rms} and CDJ shall be met for all driver outputs (W3, W2, W1, W0).

Specifications for CRJ_{rms} and CDJ shall be met for all transmitter equalizer settings and for each of the W3, W2, W1, and W0 transmitters.

22.B.2.3 Even-Odd Jitter

Even-Odd Jitter (EOJ) is measured as specified in this section.

EOJ is measured with the driver transmitting the Clock Jitter Pattern B test pattern defined in Annex 22.A.4.2. Note that the test pattern varies based on which transmitter (W3, W2, W1, or W0) is being tested.

Using appropriate test equipment, the zero crossings $T_{ZC}(i)$ are captured for each of the 60 transitions. Averaging of the vertical waveform or of each zero-crossing time may be used to mitigate effects of uncorrelated noise and jitter. The zero-crossing times are denoted as $T_{ZC}(i)$, i = 1, 2, ... 60, where i = 1 corresponds to the V_{+1} to V_{-1} transition that follows the two consecutive V_{+1} wire states.

A set of 40 pulse widths is calculated using the following equation:

$$\Delta T(j) = \begin{cases} T_{ZC}(j+10) - T_{ZC}(j+9) & 1 \le j \le 20 \\ T_{ZC}(j+19) - T_{ZC}(j+18) & 21 \le j \le 40 \end{cases} \quad (22\text{-}37)$$

EOJ is then calculated as follows:

$$EOJ = \frac{\left| \sum_{j=1}^{20} \Delta T(2j) - \sum_{j=1}^{20} \Delta T(2j-1) \right|}{40} \quad (22\text{-}38)$$

Specifications for *EOJ* shall be met for all transmitter equalizer settings and for each of the W3, W2, W1, and W0 transmitters.

22.B.3 Transmitter Output Noise and Distortion

The signal-to-noise-and-distortion ratio (*SNDR*) is measured as described in this section.

For each configuration of driver equalization coefficients, capture at least one complete cycle of the PRBS9 pattern as described in Annex 22.B.1.3.

Compute the linear fit pulse response (*p(k)*) and the error between the linear fit and the measured waveform (*e(k)*) using the procedure in Annex 22.B.1.4 with parameter values T_D_p = 2 and T_N_p = 8. The aligned symbol values *x(n)* used to construct x_r should be values of either +1, $EV_{+1/3}$, $EV_{-1/3}$, or -1. The values of $EV_{+1/3}$ and $EV_{-1/3}$ were calculated in Annex 22.B.1.2.

Note that waveform averaging should not be used when calculating *p(k)* and *e(k)* for Determine the value of S_{min} using Equation (22-16) in Annex 22.B.1.2.

Let k_p be the index to the peak of the linear fit pulse response *p(k)* where $p(k_p)$ = max(*p(k)*). Error variance is for each *m* in the range $m = k_p - M/4$ to $k_p + M/4$ using the following equation:

$$\sigma_m^{\,2} = \frac{1}{M} \sum_{n=0}^{N-1} e^2(mod_N(m-1+nM)+1) \quad (22\text{-}39)$$

where *M* and *N* were defined in Annex 22.B.1.2. If *M*/4 is not an integer, then the value is rounded up to the next largest integer. The $mod_N(x)$ function returns *x* modulo *N*.

The *SNDR* is then calculated as follows:

$$SNDR = \frac{S_{min}}{max(\sigma_m)} \quad (22\text{-}40)$$

Specifications for *SNDR* shall be met for all transmitter equalizer settings and for each of the W3, W2, W1, and W0 transmitters.

22.C Annex - Receiver Compliance Tests

Test procedures described in this section are used to test receiver compliance.

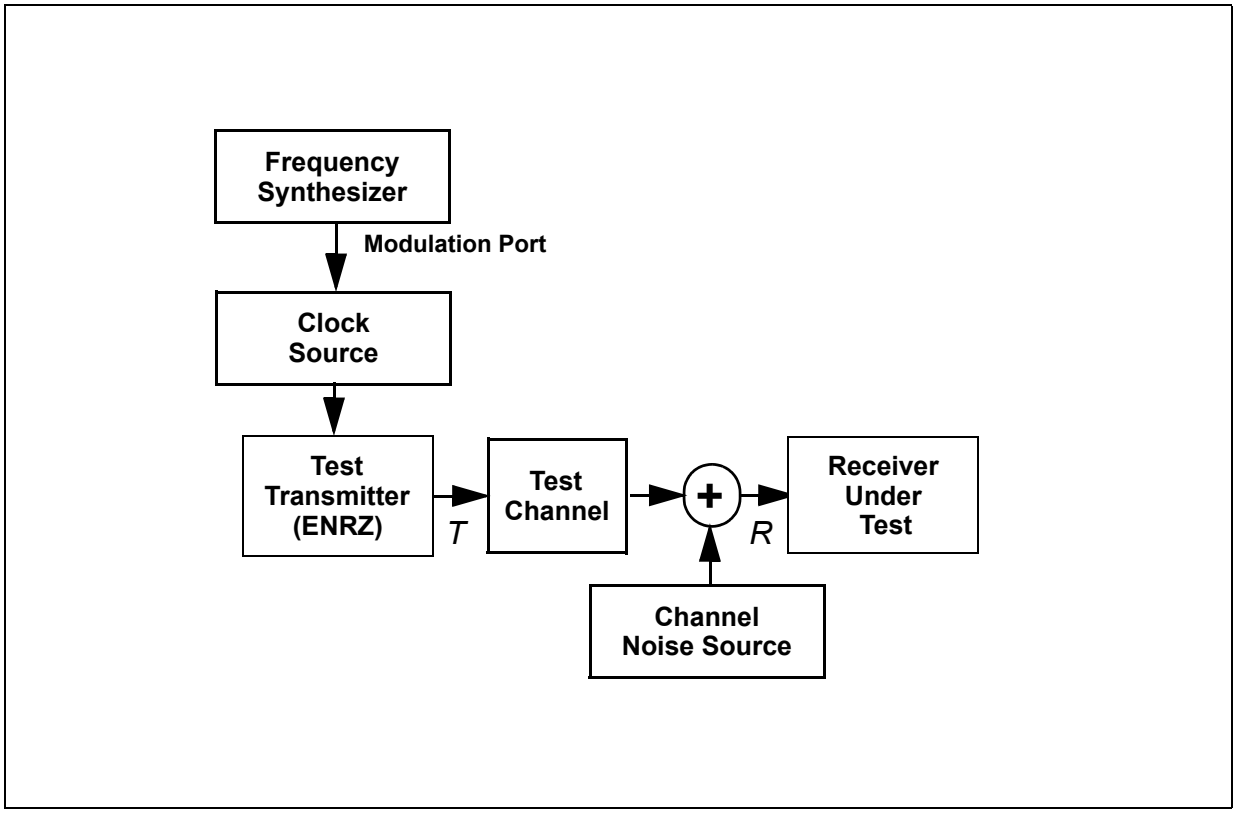
22.C.1 Receiver Interference Tolerance

This section defines the test setup and test procedures for testing interference tolerance of the receiver. The purpose of this test is to ensure interoperability of the receiver with any transmitter operating within specified limits.

22.C.1.1 Test Equipment Setup

The receiver interference tolerance test is performed using the test setup shown in Figure 22-12 or its equivalent.

Figure 22-12. Receiver Interference Tolerance Test Setup



Points *T* and *R* in Figure 22-12 are equivalent to the compliance points described in Section 22.2.6.1.

22.C.1.2 Test Transmitter

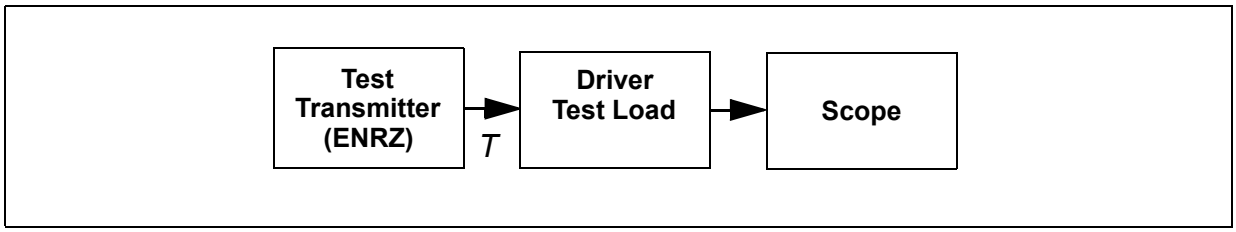
The test transmitter meets the transmitter specifications of the Section 22.3.1.

The test transmitter is configured as follows for receiver interference tolerance tests:

- The V_{SEpp} signal swing on any wire at point *T* shall not exceed the minimum value of the steady state output voltage (v_f) as defined in Table 22-15 of Section 22.3.1.7.2 when transmitting any of the test patterns defined in Annex 22.A.4.1 regardless of equalization settings.
- Transmit equalization shall be set to optimal values to maximize eye opening at sample points within the receiver. These settings may be determined through simulations using the Test Channel, or by measuring eye metrics and updating transmit equalization coefficients through a transmitter control method. The details of how the optimal transmit coefficient values are determined is outside the scope of this specification.

The test transmitter may be calibrated such that the signal at *T* meets the above requirements using the test equipment setup shown in Figure 22-13. The driver test load in this figure is implemented by the circuit shown in Figure 22-11 or its equivalent Calibration is performed such that the above conditions are met on each of the ENRZ wires W3, W2, W1, and W0. The scope in this figure measures the single-ended signal referenced to GND.

Figure 22-13. Configuration for Test Transmitter Calibration



22.C.1.3 Frequency Synthesizer and Clock Source

The purpose of the frequency synthesizer and clock source are to inject jitter on the clock used by the test transmitter. This jitter is presumed to transfer onto the output signals at point *T*.

The frequency synthesizer and clock source are configured as follows for receiver interference tolerance tests:

- The clock frequency of the clock source shall offset such that the baud rate of the test transmitter is offset by ±100 ppm relative to the baud rate at which the receiver is nominally set to operate.
- The frequency synthesizer shall modulate the clock source to generate sinusoidal jitter at point T with the amplitude and frequency specified by Section 22.3.2.6.

The frequency synthesizer and clock source may be calibrated such that the signal at *T* meets the above requirements using the test equipment setup shown in Figure 22-14. The ENRZ to differential NRZ conversion shown in this figure can be implemented by the resistor network shown in Figure 22-15 or its equivalent. Calibration is performed such that the above conditions are met on each of the ENRZ subchannels D2, D1, and D0. The scope in this figure measures the differential signal for the subchannel.

Figure 22-14. Configuration for Pattern Generator Calibration

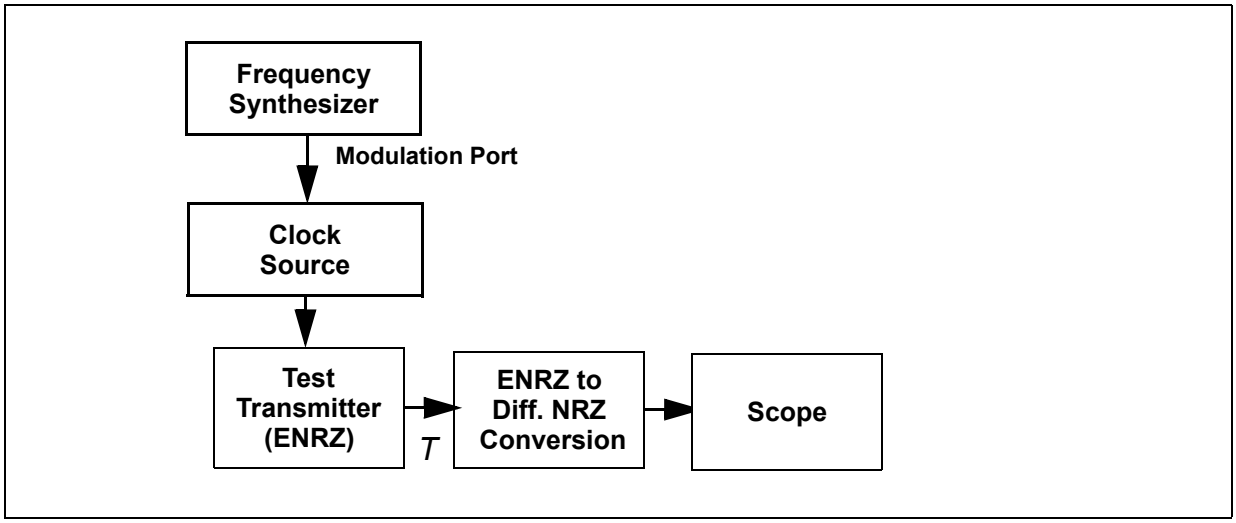
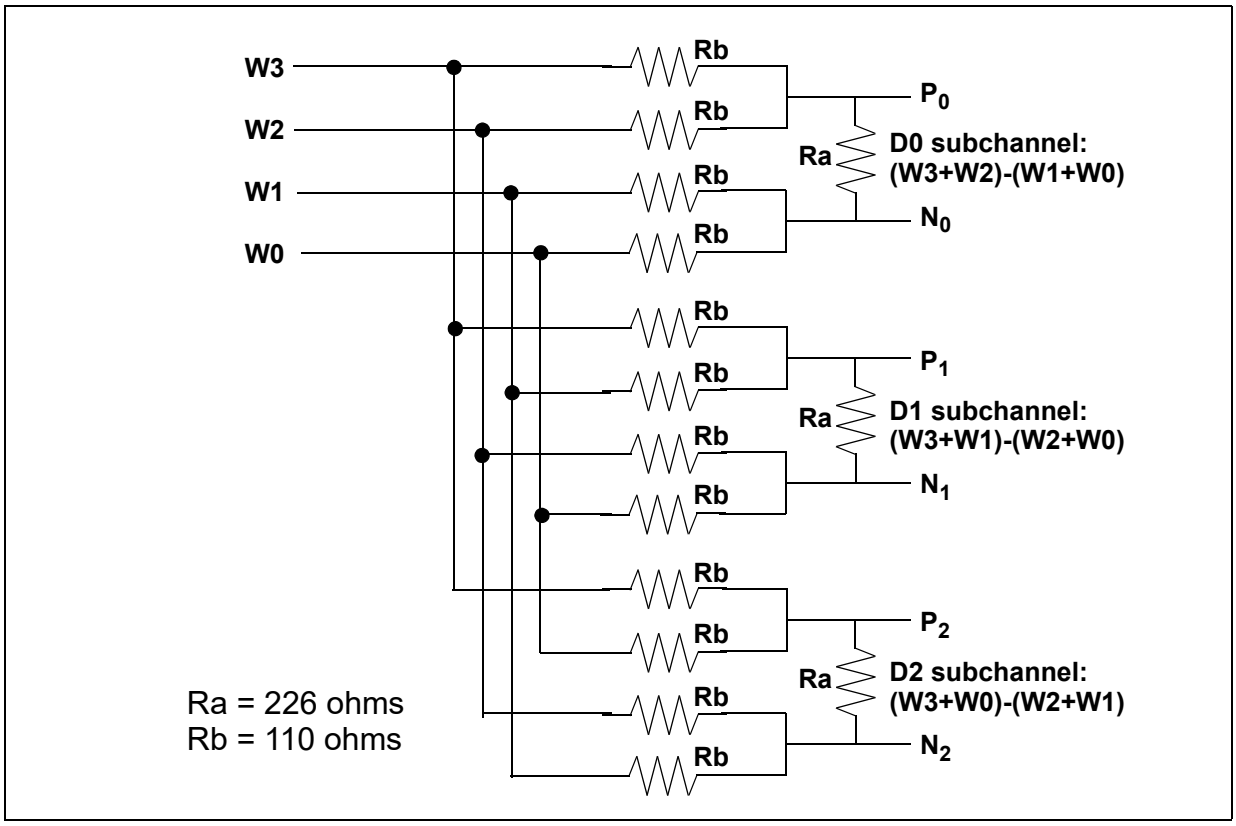


Figure 22-15. ENRZ to Differential Test Conversion Network



22.C.1.4 Test Channel

The test channel is a four wire ENRZ channel where traces are routed as two differential pairs (stripline). The reference PCB trace differential impedance is 100 Ω. for each differential pair, with loose coupling between the differential pairs. The test channel should be constructed such that it accurately represents the insertion loss and group delay characteristics of differential traces on an FR-4 printed circuit board.

The test channel is specified with respect to the insertion loss and return loss. Assume the insertion loss of the test channel (IL_{TC}) is measured at N uniformly-spaced frequencies f_n spanning f_{ILmin} to f_{ILmax} with a maximum frequency spacing of 10 MHz. The following equations calculate transmission magnitude parameters m_{TC} and b_{TC}:

$$m_X = \frac{1}{N}\sum_n IL_{max}(f_n) \quad \text{(22-41)}$$

$$m_Y = \frac{1}{N}\sum_n IL_{TC}(f_n) \quad \text{(22-42)}$$

$$m_{XY} = \frac{1}{N}\sum_n IL_{max}(f_n)IL_{TC}(f_n) \quad \text{(22-43)}$$

$$m_{XX} = \frac{1}{N}\sum_n IL_{max}(f_n)IL_{max}(f_n) \quad \text{(22-44)}$$

$$m_{TC} = \frac{m_{XY} - m_X m_Y}{m_{XX} - m_X m_X} \quad \text{(22-45)}$$

$$b_{TC} = m_Y - m_{TC} m_X \quad \text{(22-46)}$$

The values of f_{ILmin} to f_{ILmax} are specified by Section 22.3.2.6. IL_{max} is defined in Section 22.2.6.2. The test channel shall meet the following requirements:

- The value of m_{TC} shall be greater than the value specified by Table 22-19.
- The channel return loss at test points T and R shall be greater than or equal to 20 dB from f_{min} to f_{ILmax}, where f_{min} and f_{ILmax} are specified by Table 22-19.

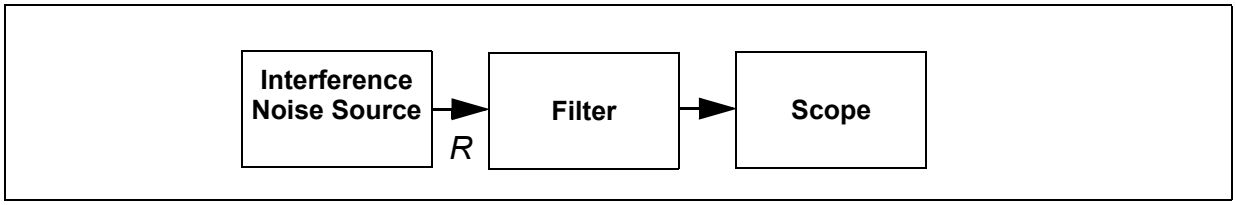
22.C.1.5 Interference Noise Source

The interference noise source emulates crosstalk and other noise which cannot be equalized by the receiver. It is sufficient in the test setup to connect the interference noise source to one wire of the ENRZ quad at a time since these distortions will be seen by all subchannels. If the noise source is connected to more than one wire of the ENRZ quad, then the noise for each wire must be uncorrelated to the other wires. If the noise source is connected to one wire at a time, then the test should be repeated for each of the four possible injection points.

The interference noise source generates white Gaussian noise with an adjustable amplitude. The power spectral density of the interference noise source shall be flat (within a tolerance of ± 3 dB) across the frequency range from f_{ILmin} to 0.5 times the baud rate.

The amplitude of the interference noise source may be calibrated using the test setup shown in Figure 22-16. The filter shown in the figure shall have a cutoff frequency that is greater than or equal to 0.5 times the baud rate, and a roll-off of 40 dB per decade or less.

Figure 22-16. Configuration for Interference Noise Source Calibration



22.C.1.6 Test Procedure

The receiver interference tolerance test is performed as follows:

- The test transmitter is configured as described in Annex 22.C.1.2.
- The frequency synthesizer and clock source are configured as described in Annex 22.C.1.3.
- The test transmitter drives the SSPR-Q test pattern defined in Annex 22.A.2.
- The amplitude of the noise injected by the interference noise source shall be greater than or equal to the amplitude specified by Table 22-19.
- The BER measured at the output of the receiver shall be less than the target BER specified by Table 22-19.

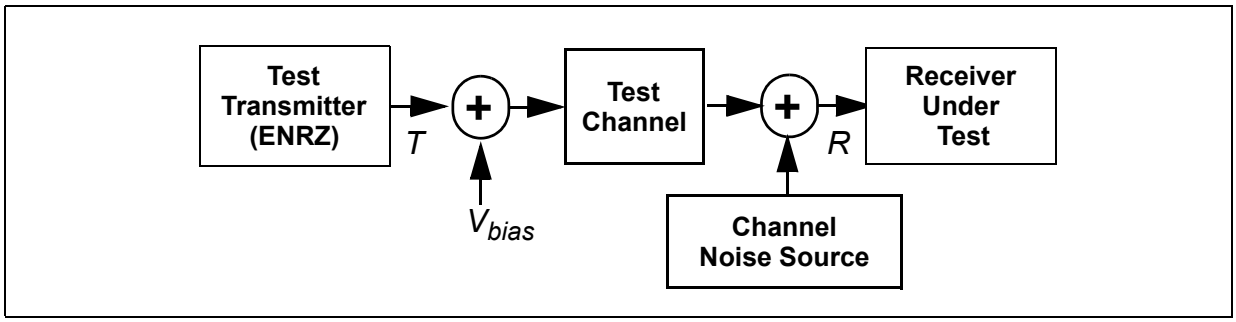
22.C.2 Receiver Imbalance Tolerance

This section defines the test setup and test procedures for testing imbalance tolerance of the receiver. The purpose of this test is to ensure interoperability of the receiver with any transmitter and channel operating within specified limits.

22.C.2.1 Test Equipment Setup

The receiver imbalance tolerance test is performed using the test setup shown in Figure 22-17 or its equivalent. Points *T* and *R* in Figure 22-17 are equivalent to the compliance points described in Section 22.2.6.1.

Figure 22-17. Receiver Imbalance Tolerance Test Setup



22.C.2.2 Test Transmitter

Refer to Annex 22.C.1.2 for a definition of the test transmitter used in this test.

22.C.2.3 Bias Voltage

The bias voltage in Figure 22-17 is intended to shift the V_{cm} voltage on one wire of the ENRZ quad relative to other wires. This will alter the switching points for the differential receivers in the receiver under test and induce skew between subchannels. The bias voltages that are to injected are specified by Section 22.3.2.7.

Figure 22-18. Configuration for Bias Voltage Calibration

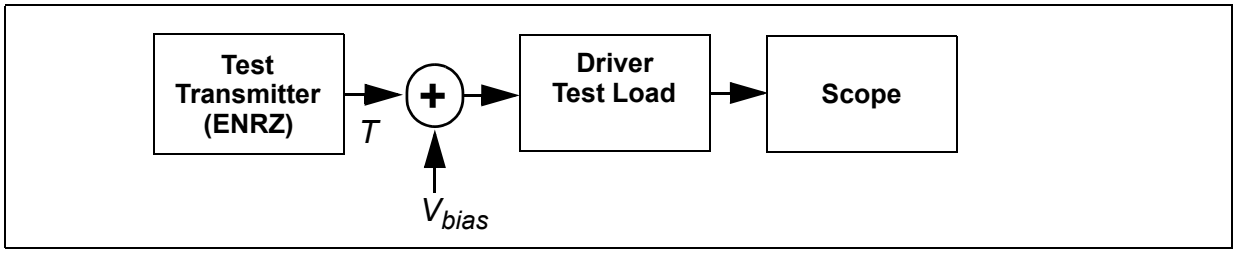
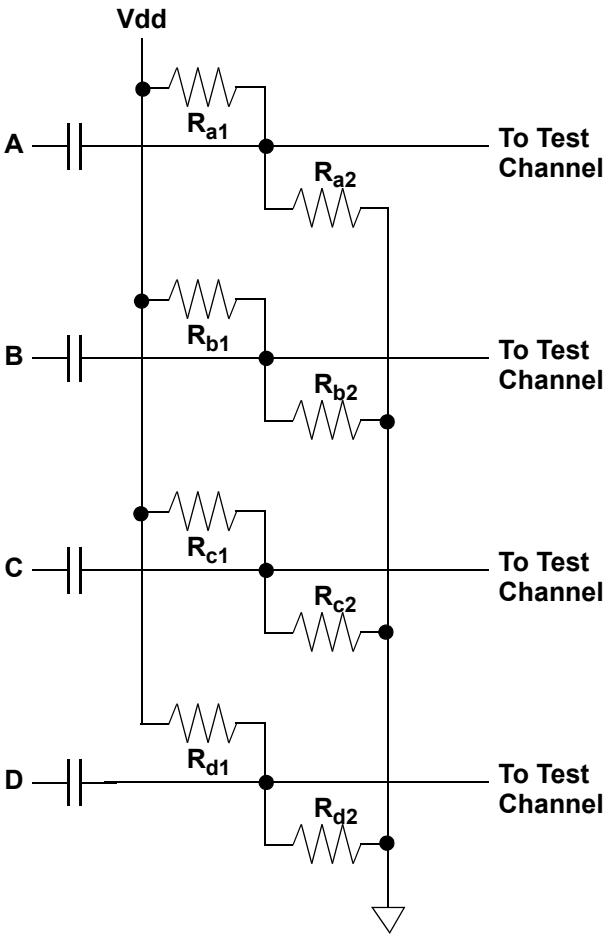


Figure 22-19. Bias Network



Bias voltages may be injected using the resistor network shown in Figure 22-19 or equivalent circuitry. The bias voltage may be calibrated using the test setup shown in Figure 22-18. The driver test load in this test setup is defined in Annex 22.C.1.1.

22.C.2.4 Test Channel

Refer to Annex 22.C.1.4 for a definition of the test channel used in this test.

22.C.2.5 Interference Noise Source

Refer to Annex 22.C.1.5 for a definition of the interference noise source used in this test.

22.C.2.6 Test Procedure

The receiver imbalance tolerance test is performed as follows:

- The test transmitter is configured as described in Annex 22.C.2.2.

- The bias voltages are configured as described in Annex 22.C.2.3. Bias voltage values are specified by Table 22-20.
- The test transmitter drives the SSPR-Q test pattern defined in Annex 22.A.2.
- The amplitude of the noise injected by the interference noise source shall be greater than or equal to the amplitude specified by Table 22-20.
- The BER measured at the output of the receiver shall be less than the target BER specified by Table 22-20.

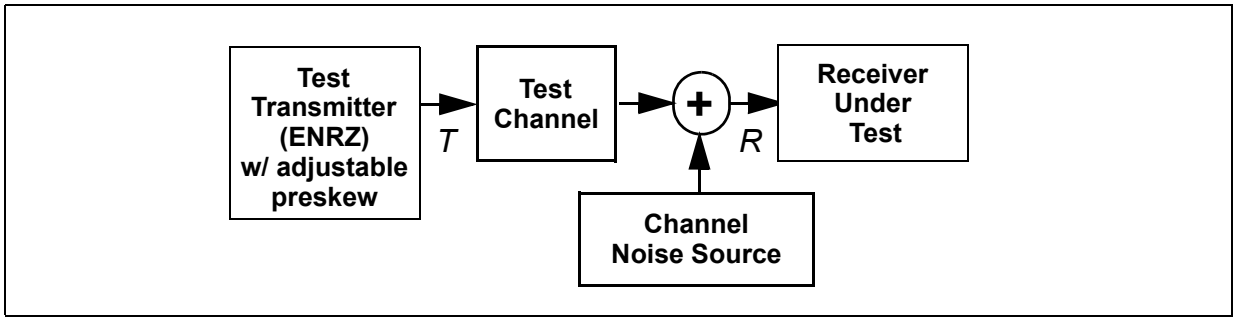
22.C.3 Receiver Skew Tolerance

This section defines the test setup and test procedures for testing skew tolerance of the receiver. The purpose of this test is to ensure interoperability of the receiver with any transmitter and channel operating within specified limits.

22.C.3.1 Test Equipment Setup

The receiver skew tolerance test is performed using the test setup shown in Figure 22-20 or its equivalent. Points *T* and *R* in Figure 22-20 are equivalent to the compliance points described in Section 22.2.6.1.

Figure 22-20. Receiver Skew Tolerance Test Setup



22.C.3.2 Test Transmitter

The test transmitter used for this test must meet all of the requirements described in Annex 22.C.1.2, and must additionally permit provisioning of preskew on individual drivers of the ENRZ quad. The preskew settings used for the test are specified by Section 22.3.2.8.

22.C.3.3 Test Channel

Refer to Annex 22.C.1.4 for a definition of the test channel used in this test.

22.C.3.4 Interference Noise Source

Refer to Annex 22.C.1.5 for a definition of the interference noise source used in this test.

22.C.3.5 Test Procedure

The receiver skew tolerance test is performed as follows:

- The test transmitter is configured as described in Annex 22.C.3.2.
- Transmitter preskew is configured as specified by Table 22-21.
- The test transmitter drives the SSPR-Q test pattern defined in Annex 22.A.2.
- The amplitude of the noise injected by the interference noise source shall be greater than or equal to the amplitude specified by Table 22-21.
- The BER measured at the output of the receiver shall be less than the target BER specified by Table 22-21.

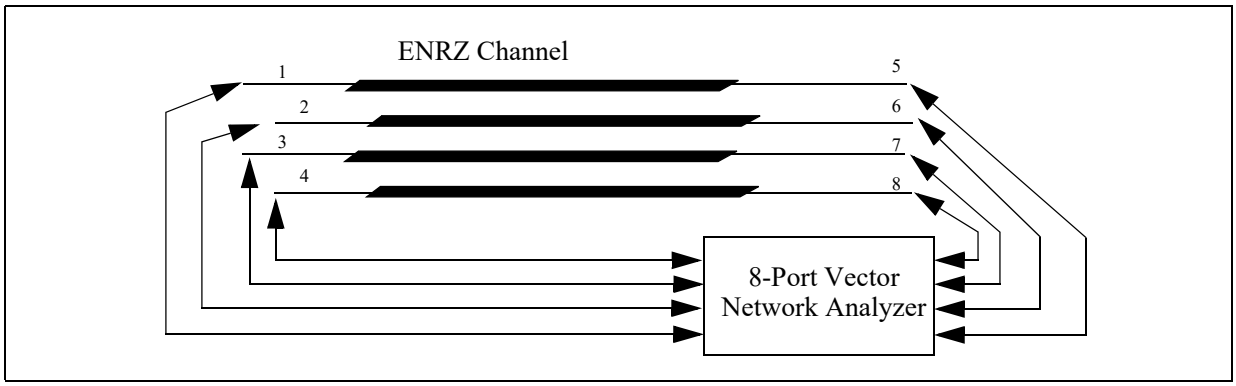
22.D Appendix - Network Analysis Measurement

This appendix describes methods of measuring 8-port S-parameters necessary for channel analysis.

22.D.1 Appendix - S-parameter Measurement with an 8-port VNA

An 8-port Vector Network Analyzer (VNA) can be used to measure the channel characteristics of an ENRZ Channel using the connections shown in Figure 22-21.

Figure 22-21. S-parameter Measurement Using an 8-port VNA



The single-ended response between each pair of connection points is expressed as S_{ji}, where j is the output port and i is the input port. The resulting responses are elements of an 8 by 8 matrix.

22.D.2 Appendix - S-parameter Measurement with an 4-port VNA

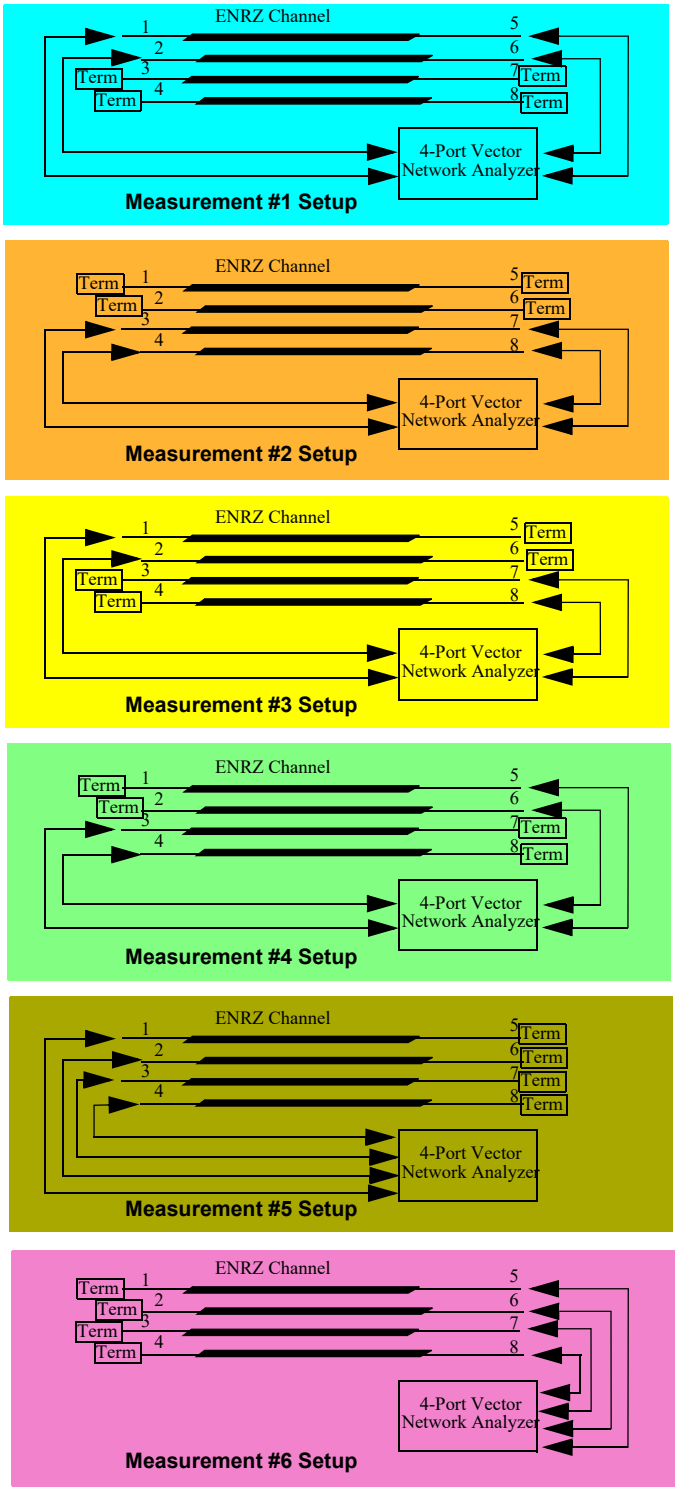
The S_{ji} responses measured in Appendix 22.D.1 can alternatively be measured using a 4-port VNA. Responses are measured using the 6 setup configurations shown in Figure 22-22. These responses are used to fill in the 8 port S-parameter matrix as follows:

$$S = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} & S_{15} & S_{16} & S_{17} & S_{18} \\ S_{21} & S_{22} & S_{23} & S_{24} & S_{25} & S_{26} & S_{27} & S_{28} \\ S_{31} & S_{32} & S_{33} & S_{34} & S_{35} & S_{36} & S_{37} & S_{38} \\ S_{41} & S_{42} & S_{43} & S_{44} & S_{45} & S_{46} & S_{47} & S_{48} \\ S_{51} & S_{52} & S_{53} & S_{54} & S_{55} & S_{56} & S_{57} & S_{58} \\ S_{61} & S_{62} & S_{63} & S_{64} & S_{65} & S_{66} & S_{67} & S_{68} \\ S_{71} & S_{72} & S_{73} & S_{74} & S_{75} & S_{76} & S_{77} & S_{78} \\ S_{81} & S_{82} & S_{83} & S_{84} & S_{85} & S_{86} & S_{87} & S_{88} \end{bmatrix}$$

Measurement #1 Setup
Measurement #2 Setup
Measurement #3 Setup
Measurement #4 Setup
Measurement #5 Setup
Measurement #6 Setup

(22-47)

Figure 22-22. S-parameter Measurement Using a 4-port VNA



22.D.3 Calculation of Insertion Loss and Conversion Loss

Given the 8-port S-parameters of a channel, the Insertion Loss and Conversion Loss terms for each subchannel can be calculated using the following equations:

$$\begin{bmatrix}0&0&0&0&1&1&-1&-1\end{bmatrix}\begin{bmatrix}S_{11}&S_{12}&\cdots&S_{18}\\S_{21}&S_{22}&\cdots&S_{28}\\\cdots&\cdots&\cdots&\cdots\\S_{81}&S_{82}&\cdots&S_{88}\end{bmatrix}\begin{bmatrix}1&1&1\\1&-1&-1\\-1&1&-1\\-1&-1&1\\0&0&0\\0&0&0\\0&0&0\\0&0&0\end{bmatrix} = \begin{bmatrix}SDD21_{D0}&FEXT_{D1\to D0}&FEXT_{D2\to D0}\end{bmatrix}$$

$$\begin{bmatrix}0&0&0&0&1&-1&1&-1\end{bmatrix}\begin{bmatrix}S_{11}&S_{12}&\cdots&S_{18}\\S_{21}&S_{22}&\cdots&S_{28}\\\cdots&\cdots&\cdots&\cdots\\S_{81}&S_{82}&\cdots&S_{88}\end{bmatrix}\begin{bmatrix}1&1&1\\1&-1&-1\\-1&1&-1\\-1&-1&1\\0&0&0\\0&0&0\\0&0&0\\0&0&0\end{bmatrix} = \begin{bmatrix}FEXT_{D0\to D1}&SDD21_{D1}&FEXT_{D2\to D1}\end{bmatrix} \quad (22\text{-}48)$$

$$\begin{bmatrix}0&0&0&0&1&-1&-1&1\end{bmatrix}\begin{bmatrix}S_{11}&S_{12}&\cdots&S_{18}\\S_{21}&S_{22}&\cdots&S_{28}\\\cdots&\cdots&\cdots&\cdots\\S_{81}&S_{82}&\cdots&S_{88}\end{bmatrix}\begin{bmatrix}1&1&1\\1&-1&-1\\-1&1&-1\\-1&-1&1\\0&0&0\\0&0&0\\0&0&0\\0&0&0\end{bmatrix} = \begin{bmatrix}FEXT_{D0\to D2}&FEXT_{D1\to D2}&SDD21_{D2}\end{bmatrix}$$

The insertion loss for each subchannel is:

$$\begin{aligned}IL_{D0} &= -SDD21_{D0}\\IL_{D1} &= -SDD21_{D1}\\IL_{D2} &= -SDD21_{D2}\end{aligned} \quad (22\text{-}49)$$

and the conversion loss for each subchannel is:

$$\begin{aligned}CL_{D0} &= \left|FEXT_{D1\to D0}\right| + \left|FEXT_{D2\to D0}\right|\\CL_{D1} &= \left|FEXT_{D0\to D1}\right| + \left|FEXT_{D2\to D1}\right|\\CL_{D2} &= \left|FEXT_{D0\to D2}\right| + \left|FEXT_{D1\to D2}\right|\end{aligned} \quad (22\text{-}50)$$

22.E Appendix - Printed Circuit Board Reference Geometry

Channels must be designed such that the S-parameters for each subchannel meet the requirements described in Clause 22.2.6, including requirements for insertion loss, insertion loss deviation (ILD), and return loss. This appendix describes an example reference geometry for printed circuit board routing which can meet these requirements, however there are many variations of this reference geometry that can also meet these requirements.

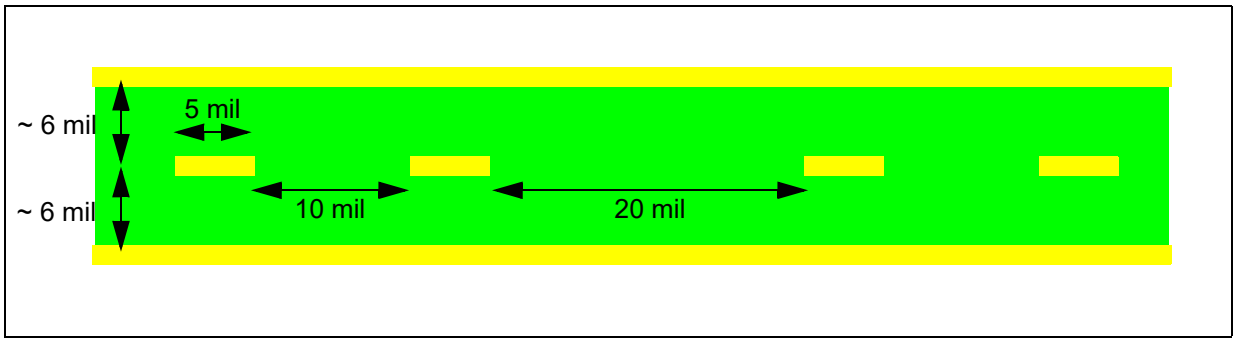
22.E.1 Appendix - Reference Geometry

Stripline configurations are recommended for PCB routing of ENRZ channels. While microstrip configurations are possible, stripline configurations exhibit better signal integrity performance.

A PCB routing reference geometry for an ENRZ channel using a stripline configuration is shown in Figure 22-23. The differential impedance (Zdiff) of each subchannel is $100\Omega \pm 10\%$. Each differential pair is routed as a loosely coupled stripline with 5/10/5 mil spacing. Spacing between differential pairs should be at least 20 mil to ensure minimal mutual inductance and capacitance between the wires of the two pairs.

These recommendations are based upon FR4 PCB material with the following characteristics: Ɛr = 3.7, and tanD = 0.019.

Figure 22-23. Reference PCB Routing Geometry for ENRZ Channel



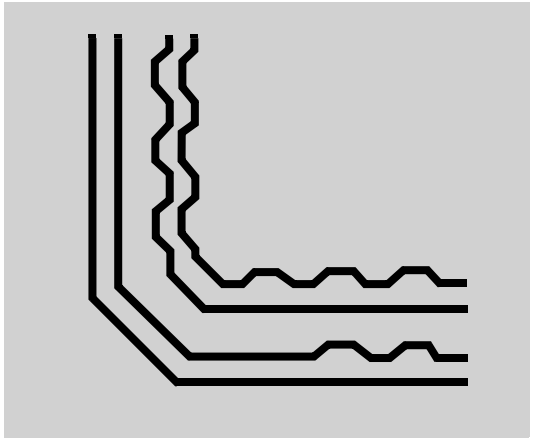
22.E.2 Appendix - Channel Skew

The transmitter is expected to actively compensate for skew on the interface, including channel skew, as defined in Section 22.3.1.5, and the receiver is expected to tolerate skew consistent with the test limits specified in Section 22.3.2.8. Skew in the channel must not be greater than the compensation range of the transmitter, and additionally should be minimized to avoid degradation of noise immunity or EMI. Excessive skew will also degrade ILD and return loss characteristics of the channel such that channel compliance may be impacted. Degradations are minimal if the channel meets the following guidelines:

- Maximum end-to-end channel skew across four ENRZ wires is less than 8 ps.
- Maximum routing length difference between wires of any single PCB segment is less than 5 mil.

If necessary, zigzag routing may be employed to minimize length mismatch of PCB traces. An example of zigzag routing to match lengths through a right angle turn is shown in Figure 22-24.

Figure 22-24. Length Matching Example Through a Right Angle Turn



The glass weave effect introduces additional skew which cannot be ignored for these skew ranges. Possible mitigation approaches include: using denser weave material; using glass material with a lower Dk value; using a wider trace; or employing angled routing at ~10 degree or zigzag routing. Because the skew mismatch due to glass weave may vary widely based on the PCB material characteristics and manufacturing process, specified guidelines cannot be provided in this appendix.

Note that all of the channel skew guidelines in this section are informative, and compliance is optional as long as the channel requirements in Section 22.2.6 are met.

23 CEI-112G-MCM-CNRZ Ultra Short Reach Interface

This clause details the requirements for the CEI-112G-MCM-CNRZ short-reach, high speed electrical interface between nominal data rates of 237.5 Gbit/s and 348.0 Gbit/s using CNRZ-5-EE coding across six wires. This throughput, normalized per wire, is equivalent to other CEI-112G variants which define signaling over two wires.

A compliant device must meet all of the requirements listed below. The electrical interface is based on high speed, low voltage DC-coupled logic. Connections are point-to-point balanced groups of six wires, and signaling is unidirectional.

The electrical IA is based on loss and jitter budgets and defines the characteristics required to communicate between a CEI-112G-MCM-CNRZ transmitter and a CEI-112G-MCM-CNRZ receiver using copper signal traces on a multi-chip module. The characteristic impedance of the signal traces is nominally 60 Ω between any wire of the channel to AC ground. A 'length' is effectively defined in terms of its attenuation and phase response rather than its physical length. Refer to Section 23.2.7 for the channel requirements.

23.1 Requirements

1. Support data rates within the range of 237.5 Gbit/s and 348.0 Gbit/s across six wires. Five bits are transmitted per baud rate symbol. Corresponding baud rates are within the range of 47.5 Gsym/s to 69.6 Gsym/s.
2. Capable of low bit error rate (10^{-15}, with a test requirement to verify 10^{-12}) without requiring a high-latency FEC.
3. Capable of driving 0 – 25 mm of package substrate
4. Shall support DC-coupled CMOS to CMOS operation.
5. Shall allow multiple CEI lanes (1 to n).
6. Shall minimize power (pJ/bit) requirements.

23.2 General Requirements

23.2.1 Data Patterns

Please refer to Section 3.2.1.

23.2.2 Signal levels

The signal is a low swing CNRZ-5 Equal Eye (CNRZ-5-EE) interface using six wires, designated W5, W4, W3, W2, W1, and W0. Low swing CNRZ-5 signaling provides noise immunity and improved electromagnetic interference (EMI) similar to the characteristics of differential NRZ signaling.

See Figure 23-1 and Figure 23-2 for an illustration of absolute driver output voltage limits and voltage levels. Drivers for wires W5, W3, W2, and W0 drive the six signal levels shown in Figure 23-1: V_{-1}, $V_{-1/2}$, $V_{-1/4}$, $V_{+1/4}$, $V_{+1/2}$, or V_{+1}. Drivers for wires W4 and W1 drive the four signal levels shown in Figure 23-2: $V_{-7/8}$, $V_{-1/8}$, $V_{+1/8}$, or $V_{+7/8}$.

Figure 23-1.Definition of Driver Amplitude and Swing (W5, W3, W2, W0)

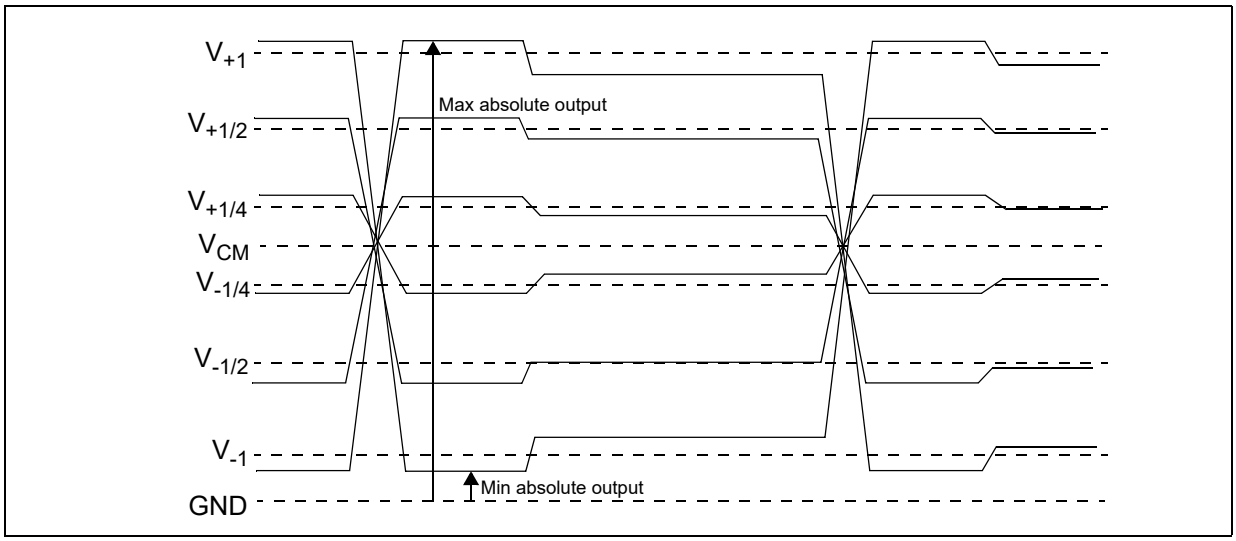


Figure 23-2.Definition of Driver Amplitude and Swing (W4, W1)

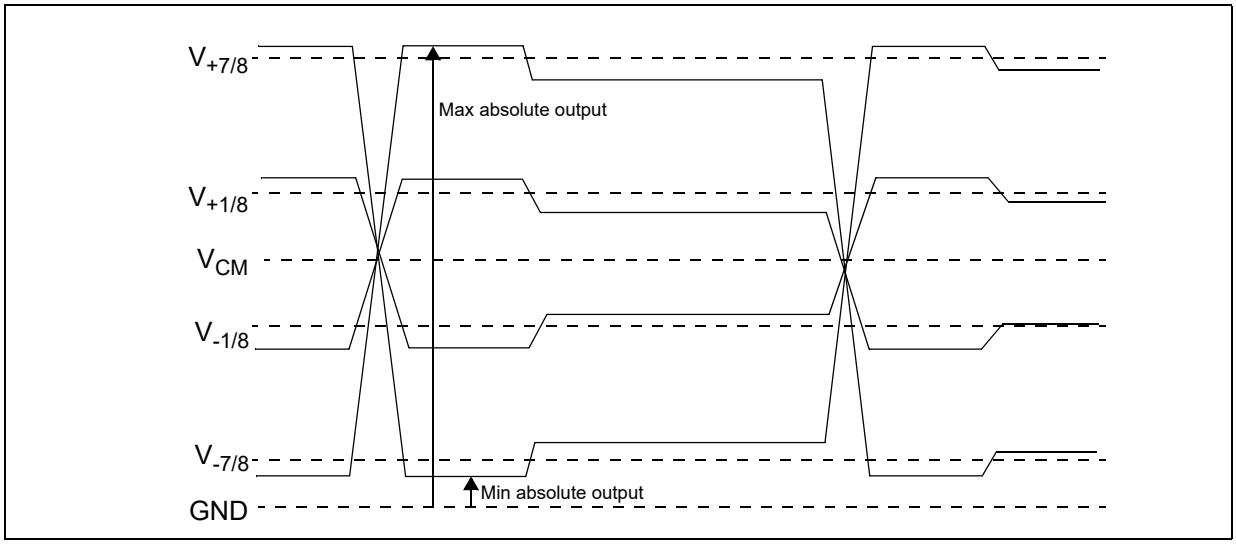
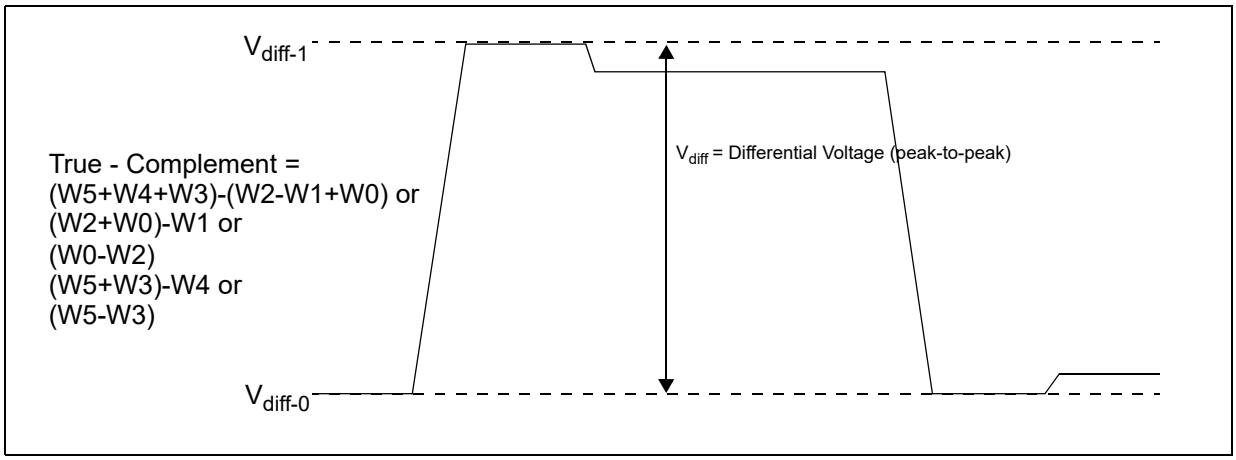


Figure 23-3.Definition of Driver Amplitude and Swing



See Figure 23-3 for a definition of differential peak-to-peak amplitude and differential voltages for bit values of 1 and 0 (V_{diff-1} and V_{diff-0}). The difference between these voltages is V_{diff}. The differential signal for a subchannel is obtained through linear combination of the signals on the wires in the proportion specified for the subchannel.

Given absolute voltages V_{W5}, V_{W4}, V_{W3}, V_{W2}, V_{W1}, and V_{W0} referenced to ground on the respective wires W5, W4, W3, W2, W1, and W0, the DC common mode voltage (V_{CM}) of the CNRZ-5-EE interface is defined as the average of the voltage on the six wires:

$$V_{CM} = \frac{V_{W5} + V_{W4} + V_{W3} + V_{W2} + V_{W1} + V_{W0}}{6} \quad (23\text{-}1)$$

The single-ended voltage on wire *i* with respect to V_{CM} is defined as:

$$V_{SE(i)} = V_i - V_{CM} \qquad (i = W5, W4, W3, W2, W1, W0) \quad (23\text{-}2)$$

The maximum and minimum single-ended voltages on any of the six wires are:

$$\begin{aligned} V_{SE\text{-}max} &= max(V_{SE(W5)}, V_{SE(W4)}, V_{SE(W3)}, V_{SE(W2)}, V_{SE(W1)}, V_{SE(W0)}) \\ V_{SE\text{-}min} &= min(V_{SE(W5)}, V_{SE(W4)}, V_{SE(W3)}, V_{SE(W2)}, V_{SE(W1)}, V_{SE(W0)}) \end{aligned} \quad (23\text{-}3)$$

The maximum peak-to-peak swing of V_{SE} is defined as:

$$V_{SEpp} = V_{SE\text{-}max} - V_{SE\text{-}min} \quad (23\text{-}4)$$

As illustrated in Figure 23-1 and Figure 23-2, the output driver may assume one of ten output states, where the nominal drive voltages of these states are defined in Table 23-1. Each of wires W5, W4, W3, W2, W1, and W0 can be driving different states, but only combinations of driver states which maintain a constant V_{CM} are allowed.

Table 23-1. CNRZ-5-EE Signal Drive States

Nomenclature for Signal State	Nom. V_{SE}	Nom. V_i
+1	+ (V_{SEpp} / 2)	+ (V_{SEpp} / 2) + V_{CM}
+(7/8)	+7 (V_{SEpp} / 16)	+ 7(V_{SEpp} / 16) + V_{CM}
+(1/2)	+ (V_{SEpp} / 4)	+ (V_{SEpp} / 4) + V_{CM}
+(1/4)	+ (V_{SEpp} / 8)	+ (V_{SEpp} / 8) + V_{CM}
+(1/8)	+ (V_{SEpp} / 16)	+ (V_{SEpp} / 16) + V_{CM}
-(1/8)	- (V_{SEpp} / 16)	- (V_{SEpp} / 16) + V_{CM}
-(1/4)	- (V_{SEpp} / 8)	- (V_{SEpp} / 8) + V_{CM}
-(1/2)	- (V_{SEpp} / 4)	- (V_{SEpp} / 4) + V_{CM}
-(7/8)	- 7(V_{SEpp} / 16)	- 7(V_{SEpp} / 16) + V_{CM}
-1	- (V_{SEpp} / 2)	- (V_{SEpp} / 2) + V_{CM}

The six wire CNRZ-5-EE interface carries data over five differential subchannels designated as D4, D3, D2, D1, and D0. Each CNRZ-5-EE symbol conveys one data bit on each of the five subchannels. The corresponding code map is described in Table 23-2.

Table 23-2. CNRZ-5-EE Signaling Code Map

Data Value (Subchannels D4, D3, D2, D1, D0)	Wire States (W5, W4, W3, W2, W1, W0)	Data Value (Subchannels D4, D3, D2, D1, D0)	Wire States (W5, W4, W3, W2, W1, W0)
0 0 0 0 0	{-1, +1/8, -1/4, +1/2, +7/8, -1/4}	1 0 0 0 0	{-1/4, +1/8, -1, +1/2, +7/8, -1/4}
0 0 0 0 1	{-1/4, +7/8, +1/2, -1/4, +1/8, -1}	1 0 0 0 1	{+1/2, +7/8, -1/4, -1/4, +1/8, -1}
0 0 0 1 0	{-1, +1/8, -1/4, +1, -1/8, +1/4}	1 0 0 1 0	{-1/4, +1/8, -1, +1, -1/8, +1/4}
0 0 0 1 1	{-1/4, +7/8, +1/2, +1/4, -7/8, -1/2}	1 0 0 1 1	{+1/2, +7/8, -1/4, +1/4, -7/8, -1/2}
0 0 1 0 0	{-1, +1/8, -1/4, -1/4, +7/8, +1/2}	1 0 1 0 0	{-1/4, +1/8, -1, -1/4, +7/8, +1/2}
0 0 1 0 1	{-1/4, +7/8, +1/2, -1, +1/8, -1/4}	1 0 1 0 1	{+1/2, +7/8, -1/4, -1, +1/8, -1/4}
0 0 1 1 0	{-1, +1/8, -1/4, +1/4, -1/8, +1}	1 0 1 1 0	{-1/4, +1/8, -1, +1/4, -1/8, +1}
0 0 1 1 1	{-1/4, +7/8, +1/2, -1/2, -7/8, +1/4}	1 0 1 1 1	{+1/2, +7/8, -1/4, -1/2, -7/8, +1/4}
0 1 0 0 0	{-1/2, -7/8, +1/4, +1/2, +7/8, -1/4}	1 1 0 0 0	{+1/4, -7/8, -1/2, +1/2, +7/8, -1/4}
0 1 0 0 1	{+1/4, -1/8, +1, -1/4, +1/8, -1}	1 1 0 0 1	{+1, -1/8, +1/4, -1/4, +1/8, -1}
0 1 0 1 0	{-1/2, -7/8, +1/4, +1, -1/8, +1/4}	1 1 0 1 0	{+1/4, -7/8, -1/2, +1, -1/8, +1/4}
0 1 0 1 1	{+1/4, -1/8, +1, +1/4, -7/8, -1/2}	1 1 0 1 1	{+1, -1/8, +1/4, +1/4, -7/8, -1/2}
0 1 1 0 0	{-1/2, -7/8, +1/4, -1/4, +7/8, +1/2}	1 1 1 0 0	{+1/4, -7/8, -1/2, -1/4, +7/8, +1/2}
0 1 1 0 1	{+1/4, -1/8, +1, -1, +1/8, -1/4}	1 1 1 0 1	{+1, -1/8, +1/4, -1, +1/8, -1/4}
0 1 1 1 0	{-1/2, -7/8, +1/4, +1/4, -1/8, +1}	1 1 1 1 0	{+1/4, -7/8, -1/2, +1/4, -1/8, +1}
0 1 1 1 1	{+1/4, -1/8, +1, -1/2, -7/8, +1/4}	1 1 1 1 1	{+1, -1/8, +1/4, -1/2, -7/8, +1/4}

Each subchannel is decoded by a comparator which implements linear combination Equation (23-5), where the weights of each wire for decoder c_i is defined in Table 23-3.

$$c_i = \sum_{j=0}^{m-1} (\text{weight of wire j})(\text{signal level on wire j}) \quad (23\text{-}5)$$

Table 23-3. CNRZ-5-EE Linear Combination Table

	Contribution of each wire to comparator decode					
Comparator	**w_5**	**w_4**	**w_3**	**w_2**	**w_1**	**w_0**
d_0	+1/3	+1/3	+1/3	-1/3	-1/3	-1/3
d_1				+1/2	-1	+1/2
d_2				-1		+1
d_3	+1/2	-1	+1/2			
d_4	+1		-1			

If c_i is greater than 0, then d_i = 1; if c_i is less than 0, then d_i = 0. The differential amplitude at the comparator in the absence of any gain in the receiver is:

$$V_{ppd} = 0.75(V_{SEpp}) \quad (23\text{-}6)$$

23.2.3 Signal Definitions

The signal paths of CEI channels are unidirectional point-to-point connections. Each hex channel for CEI-112G-MCM-CNRZ is made up of six balanced electrical connections. Figure 23-4 illustrates two hex channels comprising a full duplex CEI lane. However the CEI specification does not preclude use for unidirectional protocol applications.

A single clock signal is shared between the transmitting and receiving devices in the ingress direction and another clock signal is shared between the transmitting and receiving devices in the egress direction, avoiding the need for a clock recovery circuit

at the receiver. Although the specification in this clause is optimized for the Forwarded Clock Architecture described in Annex 18.A.1 (as shown in Figure 23-4), use of the Common Clock Architecture described in Annex 18.A.2 is not precluded.

Figure 23-4.Signal Diagram

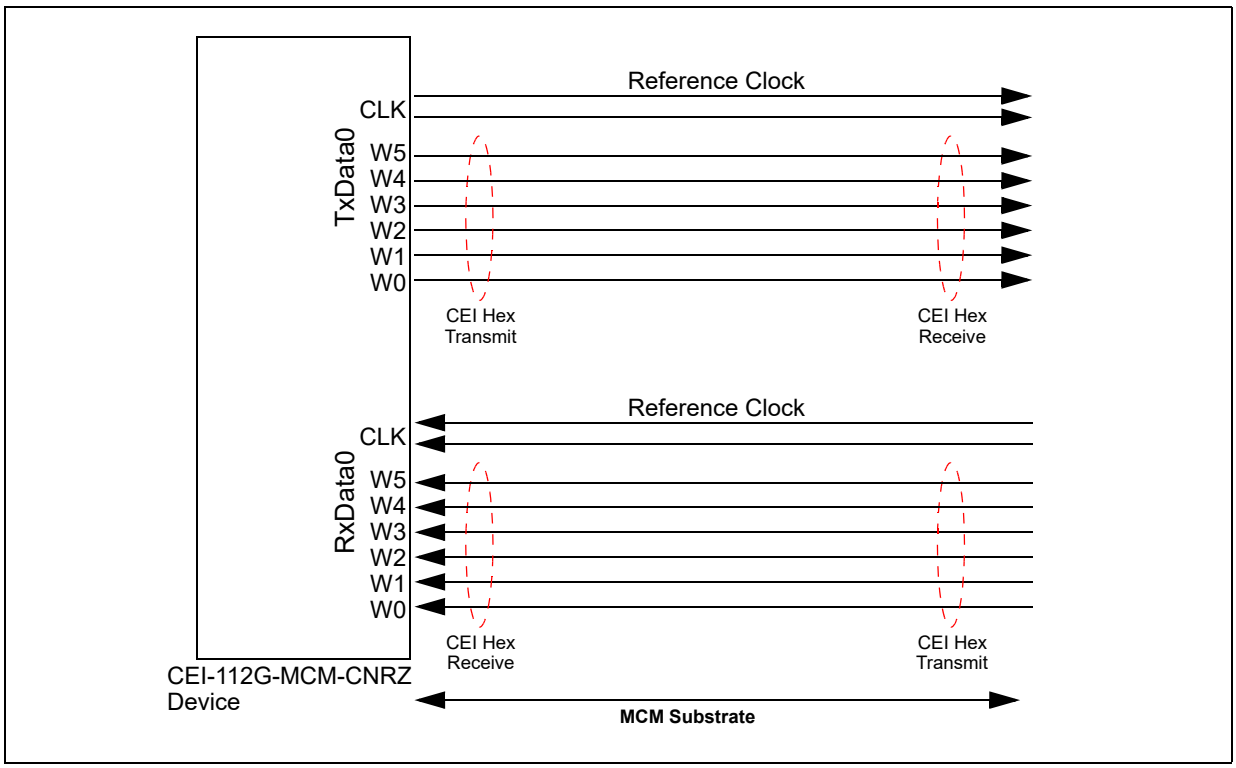


Table 23-4. Receive Signal Summary

Signal Name	Direction	Function
RXDATA[n..0]	Input to SERDES Component	The Receive Data (RXDATA[n]) signals are the inputs to the SERDES component.

Table 23-5. Transmit Signal Summary

Signal Name	Direction	Function
TXDATA[n..0]	Output of SERDES Component	The Transmit Data (TXDATA[n]) signals are the outputs of the SERDES component.

23.2.4 Bit Error Ratio

Please refer to Section 3.2.3.

23.2.5 Ground Differences

As the driver and receiver are in the package substrate (with no intervening connectors), then the ground difference is approximately 0 mV.

23.2.6 Cross Talk

Please refer to Section 3.2.5.

23.2.7 Channel Compliance

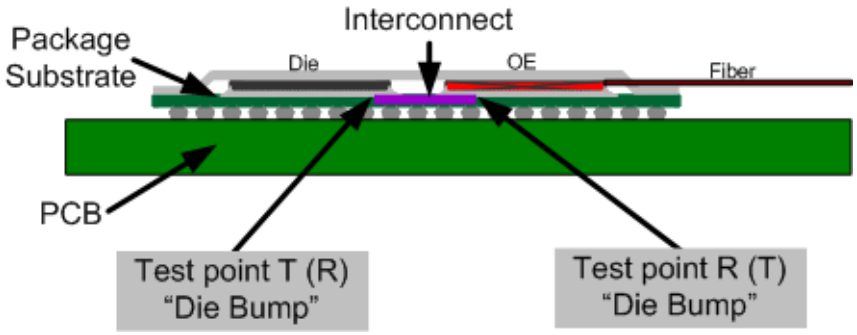
A forward channel and associated dominant crosstalk channels are deemed compliant if the channel characteristics conform to the requirements in this section.

23.2.7.1 Reference Model

The channel consists of a package substrate trace and any required vias. The reference package substrate trace impedance is 60 Ω (single-ended) and all channel specifications are referenced to this impedance. The S-parameters of each CNRZ-5 subchannel must meet the requirements described in Section 23.2.7.2, Section 23.2.7.3, Section 23.2.7.4, Section 23.2.7.5, Section 23.2.7.6, and Section 23.2.7.7.

Figure 23-5 shows a diagram of the intended application.

Figure 23-5.CEI-112G-MCM-NRZ Reference Model



Test points *T* and *R* are defined in Figure 23-5. Several channel characteristics are parametrized according to Table 23-6 at these test points and are used for calibration of the channel parameters found in Table 23-7.

Table 23-6. Measured Channel Parameters

Symbol	Description
IL(*f*)	Single-ended insertion loss, -S21 magnitude (dB)
$RL_1(f)$	Single-ended input return loss, -S11 magnitude (dB)
$RL_2(f)$	Single-ended output return loss, -S22 magnitude (dB)
$NEXT_m(f)$	Single-ended near-end crosstalk loss (m^{th} aggressor), -S21 magnitude (dB)
$FEXT_n(f)$	Single-ended far-end crosstalk loss (n^{th} aggressor), -S21 magnitude (dB)

Table 23-7. Calculated Channel Parameters

Symbol	Description
$IL_{fitted}(f)$	Fitted insertion loss (dB)
ILD(f)	Insertion loss deviation (dB)
ICN(f)	Integrated crosstalk noise (mVRMS)
FOM_{ILD}	Channel Figure of merit - Weighted insertion loss deviation (dB)

23.2.7.2 Insertion Loss

Insertion losses for each wire of the CNRZ-5 channel, including package substrate traces and vias, shall comply with the single-ended limits specified by Equation (23-7) and plotted in Figure 23-6. Note that the variable f_b is the maximum symbol rate to be supported by the channel under test (47.5 Gsym/s < f_b < 69.6 Gsym/s).

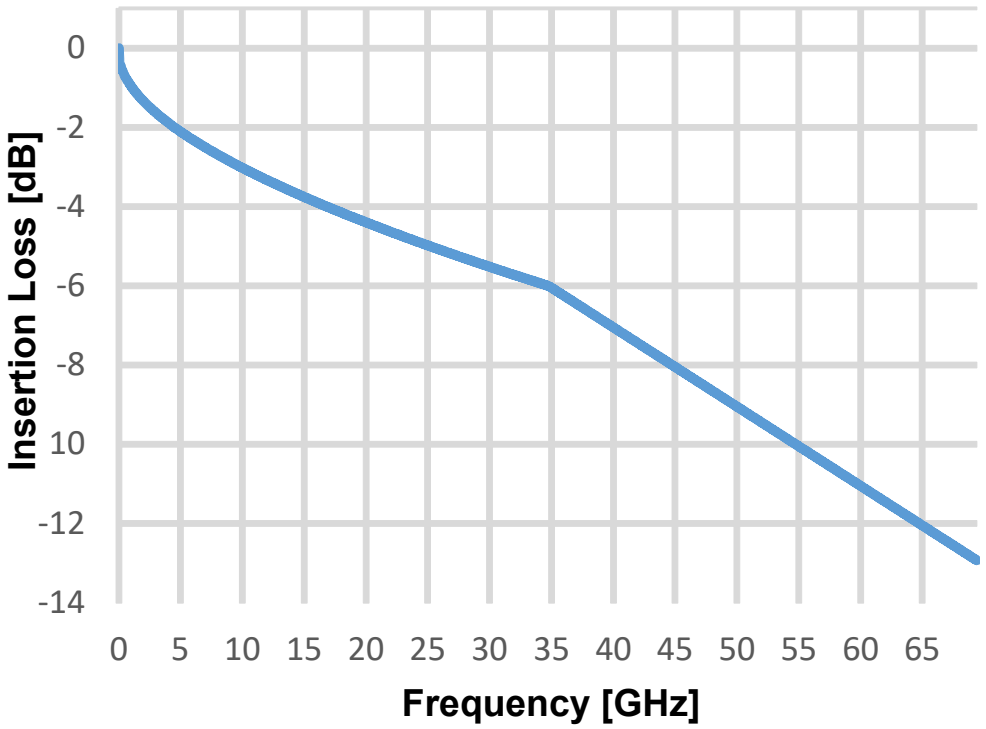
Table 23-8. Channel Insertion Loss Frequency Range

Parameter	Value	Units
f_{min}	50	MHz
f_{max}	f_b	GHz

$$IL_{max} = \begin{cases} 0.095 + 0.837\sqrt{\frac{f \times 69.6}{f_b}} + 0.028\frac{f \times 69.6}{f_b} & f_{min} \le f < \frac{f_b}{2} \\ -0.953 + 0.2\frac{f \times 69.6}{f_b} & \frac{f_b}{2} \le f \le f_b \end{cases} \quad (23\text{-}7)$$

Note: f in Equation (23-7) is in GHz.

Figure 23-6.CEI-112G-MCM-CNRZ normative channel insertion loss at 69.6 Gsym/s



23.2.7.3 Fitted Insertion Loss

For fitted insertion loss definitions, please refer to Section 12.2.1.1.

Insertion losses for each wire of the CNRZ-5 channel shall meet the single-ended insertion loss requirements defined in Table 23-9 and also meet the IL mask in Equation (23-7). Note that the variable f_b is the maximum symbol rate to be supported by the channel under test.

Table 23-9. Channel fitted insertion loss characteristics

Parameter	Units	Min Value	Max Value
Min frequency, f_{ILmin}	GHz	0.05	-
Max frequency, f_{ILmax}	GHz	-	fb
Fitted insertion loss at Nyquist	dB	-	6.0
Fitted insertion loss, a_0	dB	-1	2
Fitted insertion loss, a_1	dB	0	8.1
Fitted insertion loss, a_2	dB	0	12.0
Fitted insertion loss, a_4	dB	0	5.7

23.2.7.4 Insertion Loss Deviation (ILD)

The insertion loss deviation ILD is the difference between the measured insertion IL and the fitted insertion loss IL_{fitted} as defined in Equation (23-8) where f_{ILmin} and f_{ILmax} are given in Table 23-9.

$$ILD = IL - IL_{fitted} \qquad f_{ILmin} \le f \le (3/4) \times f_{ILmax} \tag{23-8}$$

The insertion loss deviation ILD shall be within the region defined by Equation (23-9).

$$-1.0 \le ILD \le 1.0 \tag{23-9}$$

A Figure Of Merit (FOM_{ILD}) for the channel is the weighted insertion loss deviation from f_{ILmin} to (3/4)*f_{ILmax}. FOM_{ILD} is calculated as indicated below. Note FOM_{ILD} is called ILD_{RMS} in OIF-CEI-03.0 clauses 10 & 11 and OIF-CEI-03.1 clauses 10, 11, 13 & 14.

Define the weight at each frequency *f* using Equation (23-10) below.

$$W(f) = \mathrm{sinc}^2(f/f_b)\left[\frac{1}{1+(f/f_t)^4}\right]\left[\frac{1}{1+(f/f_r)^8}\right] \tag{23-10}$$

Note that -3 dB transmit filter bandwidth f_t is inversely proportional to the minimum 20 to 80% rise and fall times T_*tr* and T_*tf*. The constant of proportionality is 0.2365 (i.e. T_*tr* x f_t = 0.2365, T_*tr* is in ns when f_t is in GHz). In addition, f_r is the -3 dB reference receiver bandwidth, which should be set at (3/4)f_b, where f_b is the maximum symbol rate to be supported by the channel.

FOM_{ILD} is calculated using Equation (23-11) where N is the number of frequency points. The summation is done over the frequency range of ILD with *f* in GHz. FOM_{ILD} shall be less than 0.2 dB for valid channels.

$$FOM_{ILD} = \sqrt{\frac{\sum W(f) \times ILD(f)^2}{N}} \tag{23-11}$$

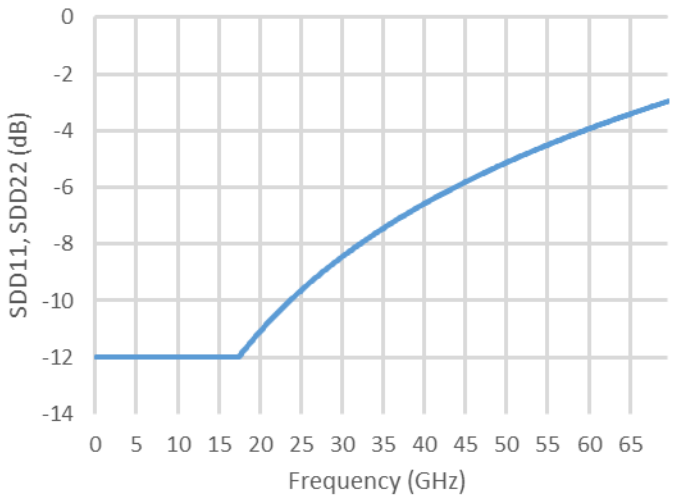
23.2.7.5 Channel Return Loss

The Return Loss for each wire of the CNRZ-5 channel shall be bounded by Equation (23-12) as shown in Figure 23-7.

$$\begin{aligned} RL(f) &> 12 \qquad f_{min} \le f \le \frac{f_b}{4} \\ RL(f) &> 12 - 15\log_{10}\left(\frac{4f}{f_b}\right) \qquad \frac{f_b}{4} < f \le f_b \end{aligned} \tag{23-12}$$

Note: f_{min} is as defined in Table 23-8.

Figure 23-7.CEI-112G-MCM-CNRZ normative channel return loss at 69.6 Gsym/s



23.2.7.6 Channel Crosstalk

The CNRZ-5 hex channel consists of six data wires plus two wires for a forwarded clock. These eight wires are defined as a “chord”. Note that the two wires for the forwarded clock may be members of more than one chord.

Crosstalk limits depend on whether the aggressor and victim wires are members of the same chord or a different chord. Table 23-10 specifies crosstalk limits for both the intra-chord and inter-chord cases.

- Inter-chord specifications apply to crosstalk measured in any wire of the CNRZ-5 hex channel from an aggressor wire in an adjacent CNRZ-5 hex channel. If the aggressor and victim CNRZ-5 hex channels have different forwarded clocks, then crosstalk to and from the clock wires must also meet these specifications.
- Intra-chord specifications apply to crosstalk measured in any wire of the CNRZ-5 hex channel from an aggressor wire in the same CNRZ-5 hex channel, including the wires for the forwarded clock associated with the hex channel.

Table 23-10 specifies crosstalk limits and parameters for aggressor signals.

Table 23-10. Channel integrated crosstalk aggressor parameters

Parameter	Symbol	Value	Units	Conditions
Far-end crosstalk (FEXT) limit for inter-chord crosstalk	$FEXT_{ext}$	-40	dB	$0 \le f \le f_b$ GHz
Near-end crosstalk (NEXT) limit for inter-chord crosstalk	$NEXT_{ext}$	-40	dB	$0 \le f \le f_b$ GHz
Far-end crosstalk (FEXT) limit for intra-chord crosstalk	$FEXT_{int}$	-35	dB	$0 \le f \le f_b$ GHz
Near-end crosstalk (NEXT) limit for intra-chord crosstalk	$NEXT_{int}$	-20	dB	$0 \le f \le f_b$ GHz

23.2.7.7 Channel Intra-Hex Wire Skew

The definition of skew in Section 1.6.2 is applied to the hex channel such that Lane X and Lane Y are illustrating the difference in propagation delay between two wires of the same hex channel. The channel is required to limit the skew between any two wires of the hex channel to a maximum of 0.05 UI.

The intra-hex wire skew is the result of differences in the length of wire traces within the hex channel. The distance delta limit imposed by the above requirement is dependent on implementation. Assuming the stripline implementation described in Section 23.A.1.1, the delta in routing distance is limited to approximately 0.125 mm at 69.6 Gsym/s. Additional guidelines for limiting skew are provided in Section 23.A.1.3.

23.3 Electrical Characteristics

The electrical interface is based on high speed, low voltage DC-coupled logic with nominal impedance of 60 Ω between any signals of the hex channel and AC ground.

All devices shall work within the range 47.5 Gsym/s to 69.6 Gsym/s as specified for the device, with all ingress lanes synchronous to a common reference frequency which can vary by ± 100ppm from nominal and all egress lanes synchronous to a common reference frequency which can vary by ± 100ppm from nominal.The reference clocks of the ingress and egress directions are not necessarily synchronous to each other. Note that implementation of specific protocols will define the operating baud rate without affecting CEI compliance.

23.3.1 Reference Clock

The reference clock is set to be 1/4th of the baud rate. This clock is typically "forwarded" from the driver side to the receiver side as described in Annex 18.A.1. When using a forwarded clock architecture, the clock is driven by output drivers that are similar to the output drivers used for the data path. The electrical specifications at R_C are given in Table 23-11.

Table 23-11. Reference Clock Electrical Specification.

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Reference Clock Rate	Ref_Baud			$f_b/4$		GHz
Input Differential Voltage	Ref_Vdiff		266		667	mVppd
Input Single Ended Voltage	Ref_Vse		0.1		1.2	V
Differential Termination Resistance Mismatch	Ref_Rdm				5	%
Input Clock Rise and Fall Time (20% to 80%)	Ref_tr, Ref_tf		4		200	ps
Differential Input Return Loss	Ref_SDD11	at $f_b/8 \le f \le f_b$ Note 1			-6	dB
Input Clock Duty Cycle	Ref_DC		40		60	%
High Frequency Uncorrelated Unbounded Gaussian Jitter	Ref_UUGJ_hf	Note 2, Note 3			0.009	UI rms
Reference Clock Single Side Band Phase Noise	Ref_PN	@ 1kHz offset			-70	dBc/Hz
		@10kHz offset			-93	
		@100kHz offset			-113	
		@1MHz offset			-133	
		≥10MHz offset			-143	

NOTES:
1. Return loss is referenced to 100 Ohm.
2. UUGJ measured using the methodology defined in Appendix 2.E.1 with a golden clock multiplier as described in Annex 18.A.4 observing with a bandwidth of 43 GHz. The golden clock multiplier has a cut-off frequency of fb/384.
3. 1 UI = 1/fb.

23.3.2 Transmitter Characteristics

The transmitter electrical specifications at compliance point T (see Figure 23-5) are given in Table 23-12. The transmitter shall satisfy jitter requirements specified in Table 23-13.

Transmit amplitudes and jitter eye measurements on subchannel signals are measured as described in Section 23.3.2.5. Jitter is measured relative to the reference clock timing source as described in Section 23.3.2.4, using a golden clock multiplier as detailed in Annex 18.A.4, for a BER as specified in Section 3.2.3. The waveform is observed through a fourth-order Bessel-Thomson response with a bandwidth of 43 GHz using a PRBS31 pattern. Since the data is sampled using the forwarded clock, any jitter that is common to the clock and data will cancel, and any residual jitter on either signal affects the eye opening in Table 23-13.

The link budget in this document assumes no Tx emphasis.

Table 23-12. Transmitter Electrical Output Specification.

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	T_Baud		47.5		69.6	Gsym/s
Output Differential Voltage See Note 3.	T_Vdiff		100		250	mVppd
Output Differential Voltage of Forwarded Clock	Ref_TVdiff		266		667	mVppd
Single Ended Transmitter Output Voltage See Note 4.	T_Vse		67		166	mV
Absolute Limit of Transmitter Output Voltage See Note 1.	T_Vabs		0.1		1.2	V
Termination Resistance Mismatch	T_Rdm				5	%
Output Rise and Fall Time (20% to 80%)	T_tr, T_tf		4			ps
Single-Ended Output Return Loss	T_S22	0 GHz $\le f \le f_b/2$ Note 2			-15	dB
		$f_b/2 \le f \le f_b$ Note 2			-10	dB
Transmitter Common Mode Noise	T_Ncm				15	mVrms

NOTES:
1. DC Coupling compliance is mandatory.
2. Return loss is referenced to 60 Ohm.
3. See Figure 23-3 for definition.
4. Relative to Vcm.

Table 23-13. Transmitter Output Jitter Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Uncorrelated Unbounded Gaussian Jitter	T_UUGJ				0.24	UIpp
Uncorrelated Bounded High Probability Jitter	T_UBHPJ				0.25	UIpp
Even Odd jitter (component of UBHPJ)	T_EOJ	Note 2			0.035	UIpp
Total Jitter	T_TJ	Note 1			0.44	UI
Eye Mask	T_X1	See 23.3.2.4			0.22	UI
Eye Mask	T_X2	See 23.3.2.4			0.4	UI
Eye Mask	T_Y1	See 23.3.2.4	50			mV
Eye Mask	T_Y2	See 23.3.2.4			125	mV

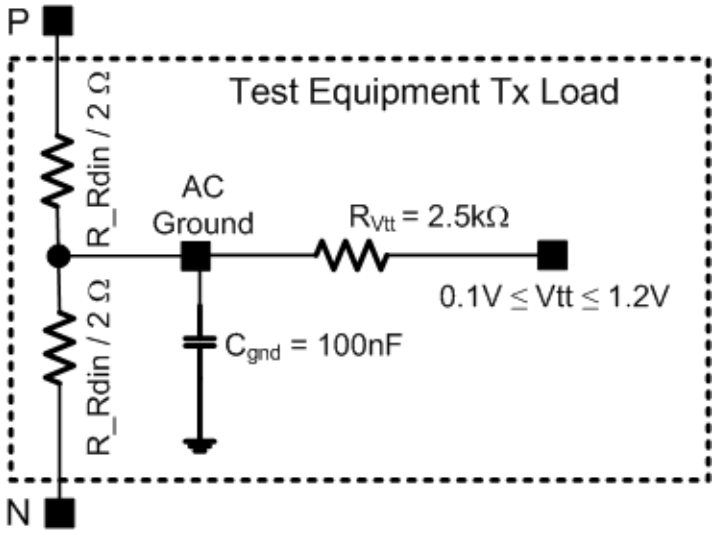
NOTES:
1. T_TJ includes all of the jitter components measured without any transmit equalization.
2. included in T_UBHPJ. Even-odd jitter is defined in Table 1-3.

23.3.2.1 Transmitter Amplitude and Swing

Transmitter differential output amplitude of the forwarded clock (Ref_TVdiff) shall be able to drive between 266 to 667 mVppd. The single-ended voltage on any wire must be between 0.1 and 1.2 V. The test load shown in Figure 23-8 is used for testing the transmitter for the differential Reference Clock, where R_Rdin = 120 ohms.

Transmitter differential output amplitude (T_Vdiff) of the subchannel (as defined in Figure 23-3) shall be able to drive between 100 to 250 mVppd. The single-ended voltage on any wire must be between 0.1 and 1.2 V. See Section 23.3.2.5 for methods of performing subchannel signal measurements.

Figure 23-8.Driver load



23.3.2.2 Transmitter Lane-to-Lane Skew

If an interface consists of more than one six-wire lane, lane-to-lane skew is defined as the skew between signal transitions on different groups of six wires. Please refer to Section 3.2.7 for requirements.

23.3.2.3 Transmitter Short Circuit Current

Not defined.

23.3.2.4 Transmitter Template and Jitter

When provided with the reference clock meeting the specifications in Section 23.3.1 as a timing source, using a golden clock multiplier as detailed in Annex 18.A.4, for a BER as specified in Section 3.2.3, the transmitter shall satisfy the eye template and jitter requirements given in Table 23-13 and Figure 1-4. The measurement of jitter and eye diagram is to be relative to the “forwarded” clock.

23.3.2.5 Transmitter Subchannel Amplitude and Jitter Measurements

The eye for each subchannel D4 to D0 of the CNRZ-5 interface may be determined by connecting all wires of the interface to a multi-channel oscilloscope, and configuring the oscilloscope to perform the linear combination defined in Table 23-3 for the subchannel being tested. The oscilloscope shall terminate each wire through a 60 ohm resistor to ground.

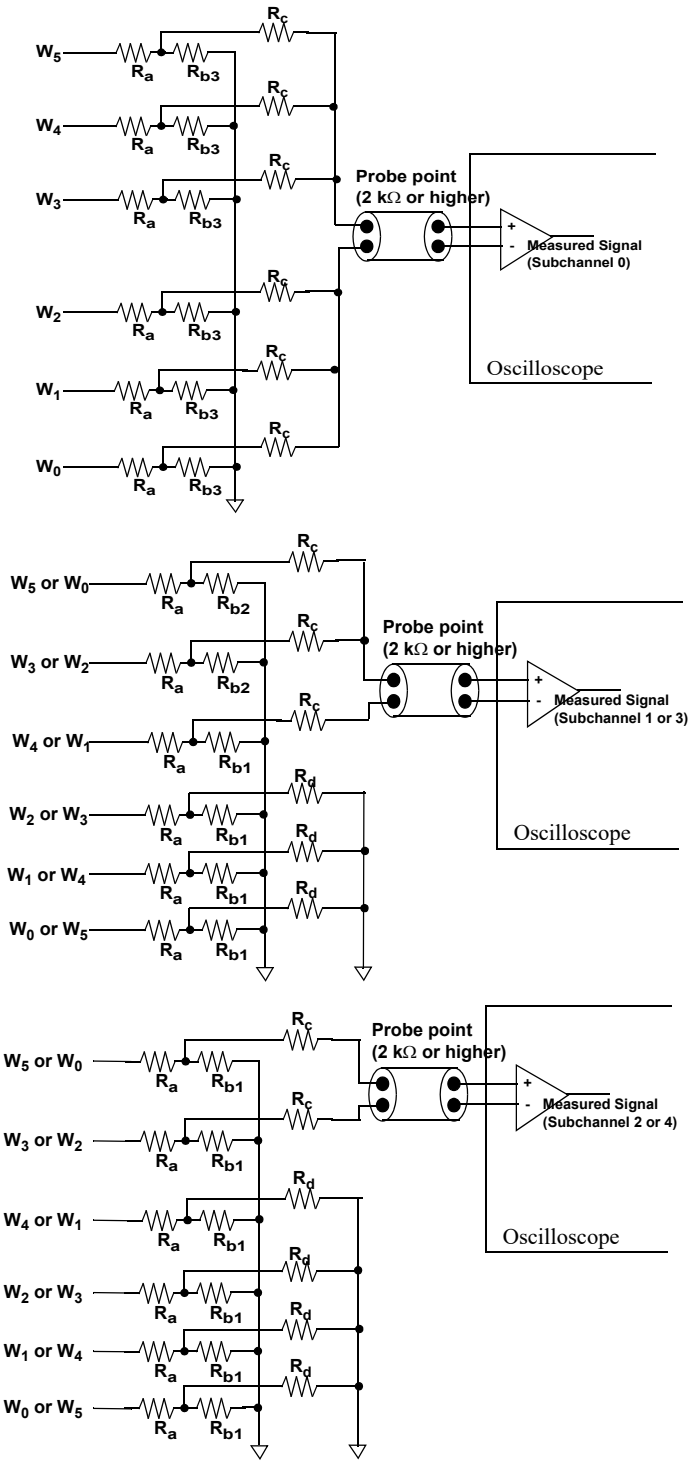
Alternatively, if a multi-channel oscilloscope is not available then passive averaging circuits may be used to average signals prior to the oscilloscope inputs. Passive averaging circuits are shown in Figure 23-9. All wires are connected through the passive averaging circuit to the oscilloscope when performing measurements on subchannel D0. When measuring subchannel 1 (or 3), wires W5, W4, and W3 (or w0, W1, and W2) are connected through the passive averaging circuit to the oscilloscope, and the remaining wires are terminated. When measuring subchannel 2 (or 4), wires W5 and W3 (or W0 and W2) are connected through the passive averaging circuit to the oscilloscope, and the remaining wires are terminated.

The recommended resistor values in Figure 23-9 are provided in Table 23-14. Note that these resistor networks provide the 60 ohm termination on each wire. The resulting resistor network has an inherent loss of 0.35 dB; measurements must be adjusted to account for this loss.

Table 23-14. Passive Averaging Circuit Resistor Values

Parameter	Value	Units
R_a	2.37	Ω
R_{b1}	57.6	Ω
R_{b2}	80.6	Ω
R_{b3}	100	Ω
R_c	57.6	Ω
R_d	4.02	Ω

Figure 23-9.Passive Averaging Circuits for CNRZ-5 Interface Eye Measurements



23.3.3 Receiver Characteristics

A compliant receiver shall operate at the specified BER with the worst case combination of a compliant transmitter and a compliant channel.

Receiver electrical specifications are given in Table 23-15 and measured at compliance point R.

The link budget in this document assumes no Rx equalization.

Table 23-15. Receiver Electrical Input Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	R_Baud		47.5		69.6	Gsym/s
Input Differential Voltage	R_Vdiff	Note 1			250	mVppd
Receiver Common Mode Noise	R_Ncm				25	mVrms
Input Resistance Mismatch	R_Rm				5	%
Single-Ended Input Return Loss	R_S11	0 GHz ≤ f ≤ f_b/2 Note 2			-15	dB
		f_b/2 ≤ f ≤ f_b Note 2			-10	dB
Rx Input Single Ended Voltage	R_V_{inSE}		0.1		1.2	V

NOTES:
1. The receiver shall have a differential input voltage range sufficient to accept a signal produced at point R by the combined transmitter and channel. The channel response shall include the worst case effects of the return losses at the transmitter and receiver.
2. Return loss is referenced to 60 Ohm.

When provided with the reference clock meeting the specifications in Section 23.3.1 as a timing source, the receiver shall tolerate the sum of these jitter contributions and meet the BER as per Section 3.2.3: the total transmitter jitter from Table 23-13 and the effects of a channel compliant to the Channel Characteristics (Section 23.2.7).

23.3.3.1 Reference Receiver Input Signals

The receiver shall accept differential input signal amplitudes produced by a compliant transmitter connected directly to the receiver. This may be larger than the 250 mVppd maximum of the transmitter due to output/input impedances and reflections.

The minimum input amplitude is defined by the minimum transmitter amplitude, the actual receiver input impedance and the loss of the actual package substrate. Note that the minimum transmitter amplitude is defined using a well controlled load impedance, however the real receiver's impedance may differ, which can leave the receiver input signal smaller than expected. Additionally the real receiver may be affected by environmental noise.

23.3.3.2 Input Lane-to-Lane Skew

If an interface consists of more than one six-wire lane, lane-to-lane skew is defined as the skew between signal transitions on different groups of six wires. Please refer to Section 3.2.8 for requirements.

23.A Appendix - Channel Routing Guidelines

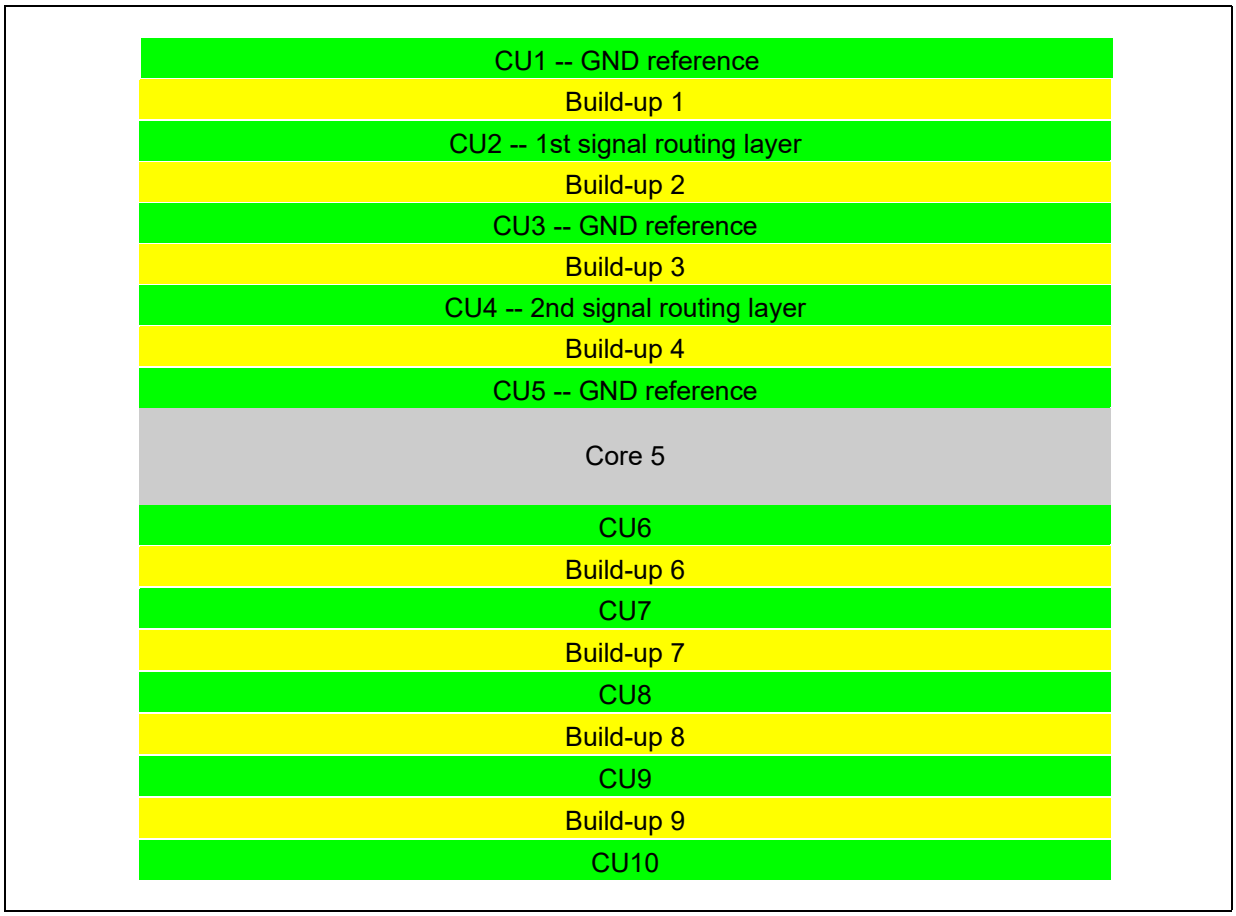
Channels must be designed such that the S-Parameters for each wire meet the requirements described in Clause 23.2.7, including requirements for insertion loss, insertion loss deviation (ILD), and return loss. This appendix describes signal routing guidelines which meet these requirements, however there are many variations of these guidelines that can also meet these requirements.

23.A.1 Appendix - Trace Routing

A recommended 4/2/4 stack-up is shown in Figure 23-10 that supports an implementation using two layers of CNRZ-5 channels along the chip edge. This allows the high speed traces to be routed as stripline traces on CU2 and CU4. CU1, CU3, and CU5 should provide as much continuous GND reference for the high speed traces as possible.

The high speed signals should not be routed on layers below the Core region. The large plated-through-hole vias required in the Core region can create large impedance discontinuities to the high speed signals.

Figure 23-10. Reference 4/2/4 Stack-Up



23.A.1.1 Appendix - Stripline vs. Microstrip

CNRZ-5 signaling is more sensitive to differences in the propagation speeds among various transmission modes than differential signaling. Stripline routing is preferred over microstrip because the homogeneous environment ensures uniform propagation speeds. If necessary, short microstrip channels can be considered with a proper soldermask layer applied.

Using a typical MCM as an example:

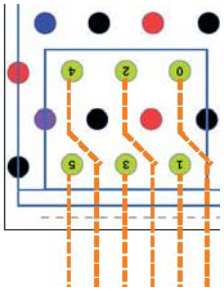
- The soldermask thickness is 20 um above CU1.
- The soldermask material is AUS703; at 10 GHz: εr = 3.3 and tanD = 0.027.
- In comparison, the organic substrate material is GX13; at 10 GHz:εr = 3.1 and tanD = 0.019.

This configuration yields a very small propagation delay difference between odd and even modes: 5.755 ps/mm and 5.749 ps/mm respectively. However, if air replaces the soldermask layer, then the propagation delay difference between odd and even modes are 4.61 ps/mm and 5.07 ps/mm. The modes will have a total of 2.3 ps difference over a 5 mm channel.

23.A.1.2 Appendix - Trace Width and Spacing

Preferred center-to-center trace pitch depends on the floorplan of the CNRZ-5 macro. Assuming a floorplan where the CNRZ-5 pins have been arranged in 2 rows by 3 columns, Figure 23-11 illustrates trace routing to escape both rows of signals. If the horizontal pitch between bumps on the macro is 150 um, then the preferred center-to-center trace pitch should be 75 um to avoid any unnecessary fan-out. High speed wires should also be shielded or kept far away from other signals to minimize unwanted noise.

Figure 23-11. Trace Routing for 2 row by 3 column Floorplan

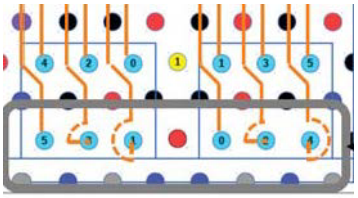


23.A.1.3 Appendix - Skew

The bump location and bit order assignments of macro implementations should be designed to enable direct wiring between Tx and Rx with minimal skew. However, if the Tx and Rx dies are not directly facing each other, skew may result from turns and

corners. In these cases, skew compensation can be implemented at the bump escape by hugging the signal trace around the circumference of the via pad as shown in Figure 23-12. Caution is needed to not create excess coupling when implementing skew compensation.

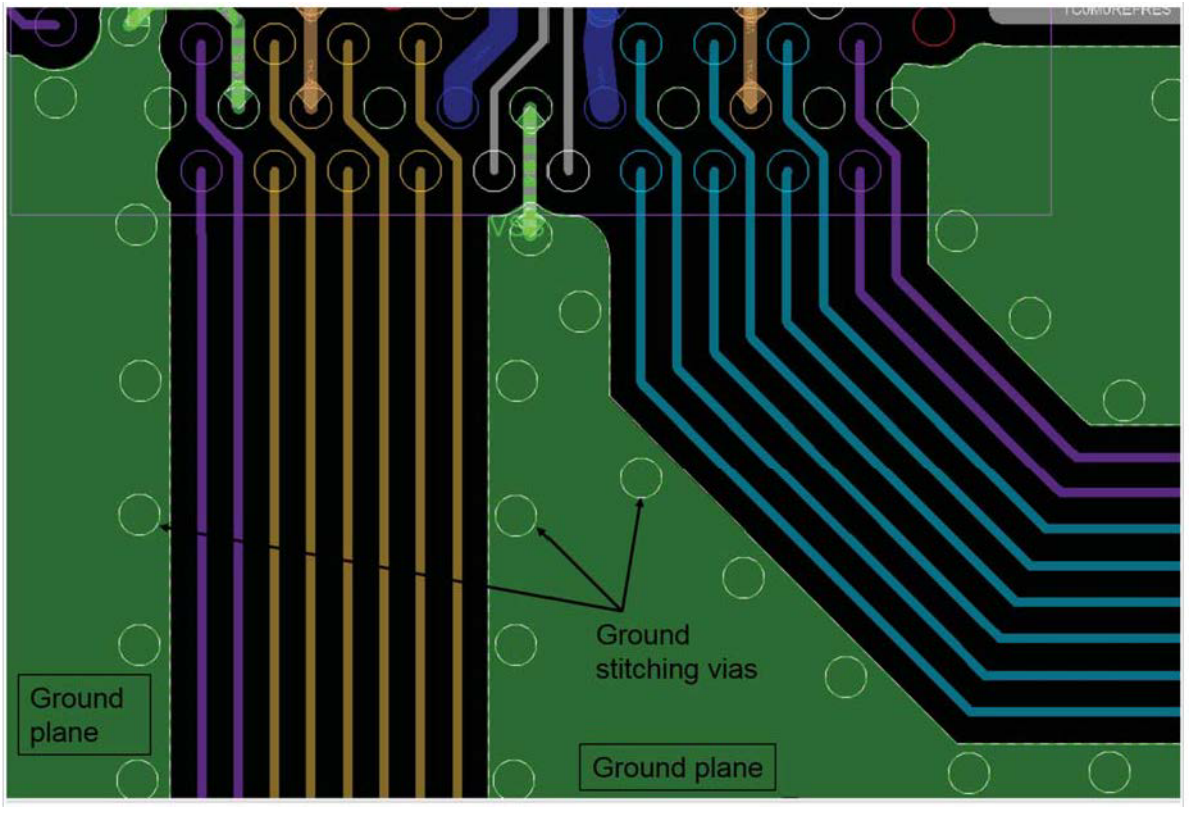
Figure 23-12. Skew Compensation



23.A.2 Appendix - Ground Stitching Vias

If ground planes are adjacent to the high speed traces, ground stitching vias are recommended to avoid unwanted resonances. Ground stitching vias should be placed less than 1 mm apart to ensure the resonance is well above the signal frequency. An example is shown in Figure 23-13.

Figure 23-13. Example of Ground Stitching Vias



23.A.3 Appendix - Ground Cutout

The larger landing pads of the bumps and vias can create extra capacitance, which introduce impedance discontinuity to the channel. To minimize the impedance discontinuity created by the larger pads, cutouts of the ground layer underneath the signal layer can be helpful. In these cases, the signal would reference a ground layer which is further away.

Note however that if the CNRZ-5 channels are stacked two deep as was assumed for the stack-up example in Figure 23-10, a ground cutout underneath the CU2 layer is not recommended. A ground cutout underneath CU2 can create noise coupling from CU4 signals to CU2.

The optimum size of the ground cutout depends on the via pad size and dielectric height. It should be simulated and optimized for each package design.

24 CEI-112G-XSR-PAM4 Extra Short Reach Interface

This clause details the requirements for the CEI-112G-XSR-PAM4 extra short reach high speed electrical interface between nominal baud rates of 36 Gsym/s and 58 Gsym/s using PAM4 coding. A compliant device shall meet all of the requirements listed below. The electrical interface is based on high speed, low voltage logic. Connections are point-to-point balanced differential pairs and signaling is unidirectional.

The electrical IA is based on loss and jitter budgets and defines the characteristics required to communicate between a CEI-112G-XSR-PAM4 transmitter and a CEI-112G-XSR-PAM4 receiver using copper signal traces on a system in a package (SIP). The characteristic impedance of the signal traces is nominally 92.5Ω differential. However, the reference impedance of the channel S-parameters is 100Ω. The signal trace or channel between a transmitter and a receiver shall meet the channel operating margin (COM), a method and a threshold quantity used for channel compliance.

CEI-112G-XSR-PAM4 assumes using forward error correction (FEC) to achieve the bit error ratio (BER) target.

Extra short reach CEI-112G-XSR-PAM4 devices from different manufacturers shall be inter-operable.

This Clause assumes recovered clock, not forwarded clock.

24.1 Requirements

1. Support serial baud rates (f_b) within the range from 36 Gsym/s to 58 Gsym/s as specified for the device using PAM4 coding. A CEI implementation complies to the specifications of this clause over the range of baud rates stated for the implementation within this range.
2. Capable of achieving a raw Bit Error Ratio (BER) of <= 10^{-9} per lane for 8 dB channel (see CAT3 of Table 24-1), or <= 10^{-8} per lane for 10 dB channel (see CAT2 of Table 24-1), or <= 10^{-6} per lane for 10 dB channel (see CAT1 of Table 24-1). FEC is assumed to be used in the system to achieve corrected BER of 10^{-15} better per lane. The baud rate includes the overhead required for FEC. The definition of FEC is outside the scope of this IA.
3. Capable of driving up to 50 mm of package substrate trace, or package (one or two package of the link) on package. The channel may include a connector.
4. Shall support DC-coupled operation. AC coupling can be supported by capacitors implemented on die.
5. Shall allow multi-lanes (1 to n).

24.2 General Requirements

24.2.1 Data Patterns

See Appendix 16.C.5.

24.2.2 Bit Error Ratio

A raw Bit Error Ratio (BER) better than or equal to 10^{-9} for 8 dB channel, or 10^{-8} for 10 dB channel, or 10^{-6} for 10 dB channel, is required on each lane, as shown in Table 24-1

Table 24-1. Channel Categories

Category	IL at Nyquist (Max, dB)	BER (Max)
CAT1	10	1e-6
CAT2	10	1e-8
CAT3	8	1e-9

A compliant receiver, when receiving from a compliant transmitter over a compliant channel, shall deliver the specified raw BER to the subsequent FEC decoder. Error bursts with length more than 7 PAM4 symbols delivered to the PAM4 decoder shall occur with a probability of less than 1 in 10^{20} PAM4 symbols. To enable a more practical test, the error bursts with length more than 3 PAM4 symbols delivered to the PAM4 decoder should occur with a probability of less than 1 in 10^{12} PAM4 symbols.

24.2.3 Ground Differences

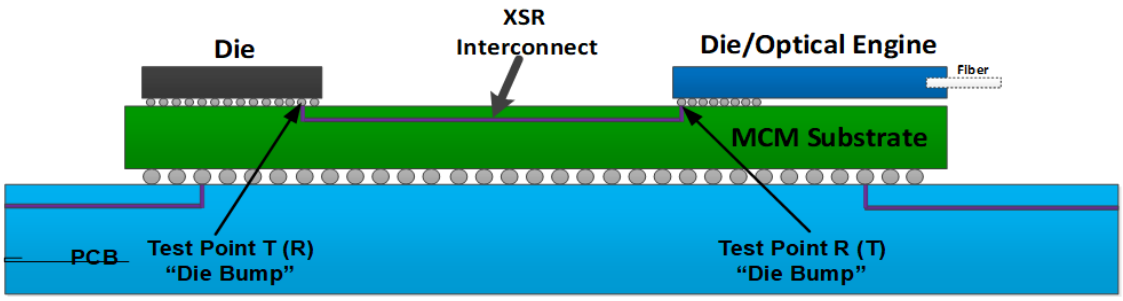
As the driver and receiver are on the same package, the ground difference is approximately 0 mV.

24.2.4 Channel Compliance

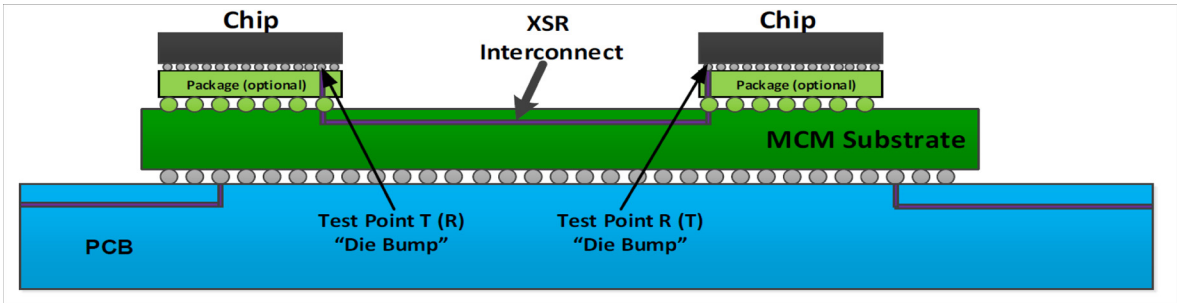
A forward channel and associated dominant crosstalk channels are deemed compliant if the channel characteristics conform to the requirements defined in this section.

24.2.4.1 Reference Model

Figure 24-1. CEI-112G-XSR Reference Model

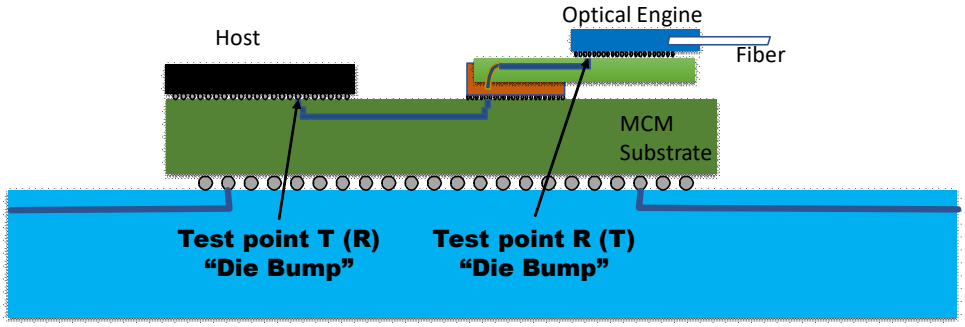


Use Model A: Die-to-Die/OE



Use Model B: Chip-to-Chip (or Package on Package)

Note that in the use model B, package is part of the channel.



Use Model C: Die-to-Die/OE with separable interconnect

Note that in the use model C, all the relevant substrates and the separable interconnects are part of the channel.

The channel is defined between test point T and test point R, and bump is not part of the channel, and may include a connector provided the channel meets the specification in this section.

24.2.4.2 Channel Operating Margin

For an informative introduction into the Channel Operating Margin method, please refer to Appendix 25.D. The Channel Operating Margin (COM) of the channel is computed using the procedure in Annex 93A of IEEE Std 802.3 [27] as modified by IEEE Std 802.3ck [29]. Using T_r = 0.3984 UI, for $H_f(f)$ in Equation (93A–19), COM shall be greater than or equal to 2.6 dB for each test. This minimum value allocates margin for practical limitations on the receiver implementation and the largest step size allowed for transmitter equalizer coefficients.

Table 24-2. COM Parameter Values

Parameter	Symbol	Value	Units
Signaling rate	f_b	36 - 58	Gsym/s
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device die model Single-ended die capacitance Single-ended die series inductance Single-ended die bump capacitance (Note 1)	 C_d L_s C_b	 100 120 30	 fF pH fF
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	45	Ω
Receiver 3 dB bandwidth	f_r	0.75 × f_b	GHz
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.60	—
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.14 0 0.02	 — — —
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.18 0 0.02	 — — —
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –8 0 1	 dB dB dB
Continuous time filter, DC gain2 Minimum value Maximum value Step size	g_{DC2}	 –2 0 1	 dB dB dB
Continuous time filter, scaled zero frequency	f_z	f_b /2.5	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	f_b /2.5 f_b	GHz GHz

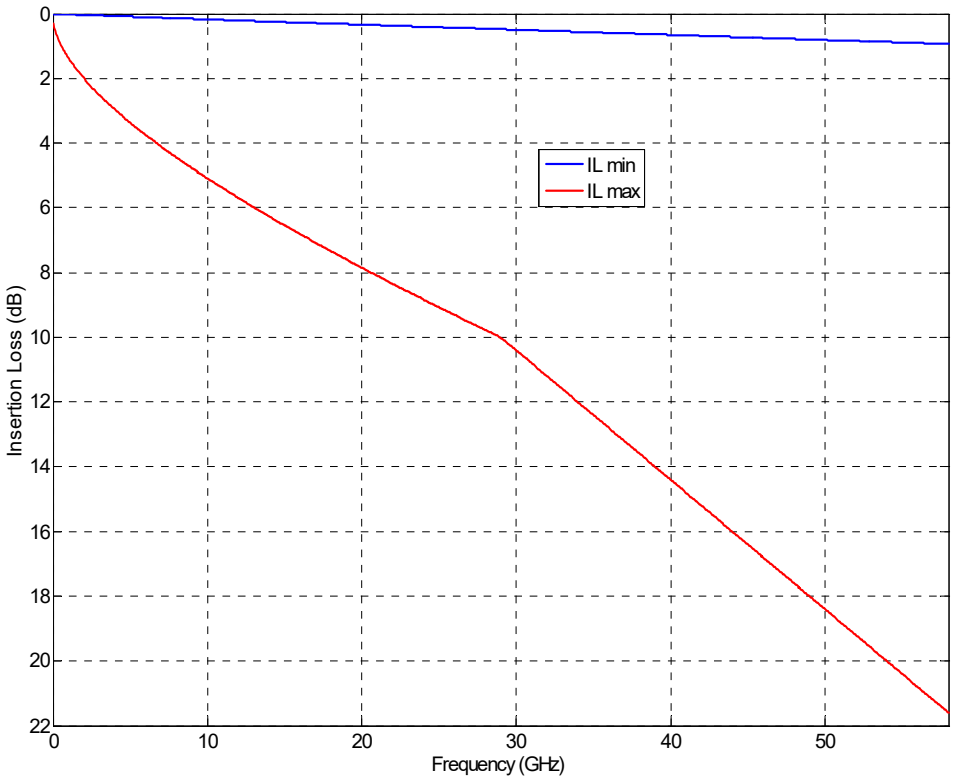
Table 24-2. COM Parameter Values

Continuous time filter, low frequency pole/scaled zero	f_{LF}	$f_b/80$	GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.275 0.275 0.375	 V V V
Number of signal levels	L	4	—
Level separation mismatch ratio	R_{LM}	0.95	—
Transmitter signal-to-noise ratio	SNR_{TX}	32.5	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	0	UI
Normalized DFE coefficient magnitude limit for n = 2 to N_b	$b_{max(1)}$ $b_{max(2-Nb)}$	0 0	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.02	UI
One-sided noise spectral density	η_0	1.23×10^{-7}	V^2/GHz
Target detector error ratio (Note 2)	DER_0	10^{-9}, or 10^{-8}, or 10^{-6}	—
Channel operating margin, min	COM	2.6	dB

NOTES:
1. This includes die and die bump capacitance.
2. The DER0 is 1e-9 for 8 dB channel, or 1e-8 for 10 dB channel, or 1e-6 for 10 dB channel.

24.2.4.3 Informative Channel Insertion Loss

Figure 24-2. Channel Insertion Loss Limit for 58.0 Gsym/s



$$IL_{max} = \begin{bmatrix} 0.01 + 1.25\sqrt{\frac{f \times 58}{f_b}} + 0.1125\frac{f \times 58}{f_b} & f_{min} \le f < \frac{f_b}{2} \\ -1.6 + 0.4\frac{f \times 58}{f_b} & \frac{f_b}{2} \le f < f_b \end{bmatrix} \quad (24\text{-}1)$$

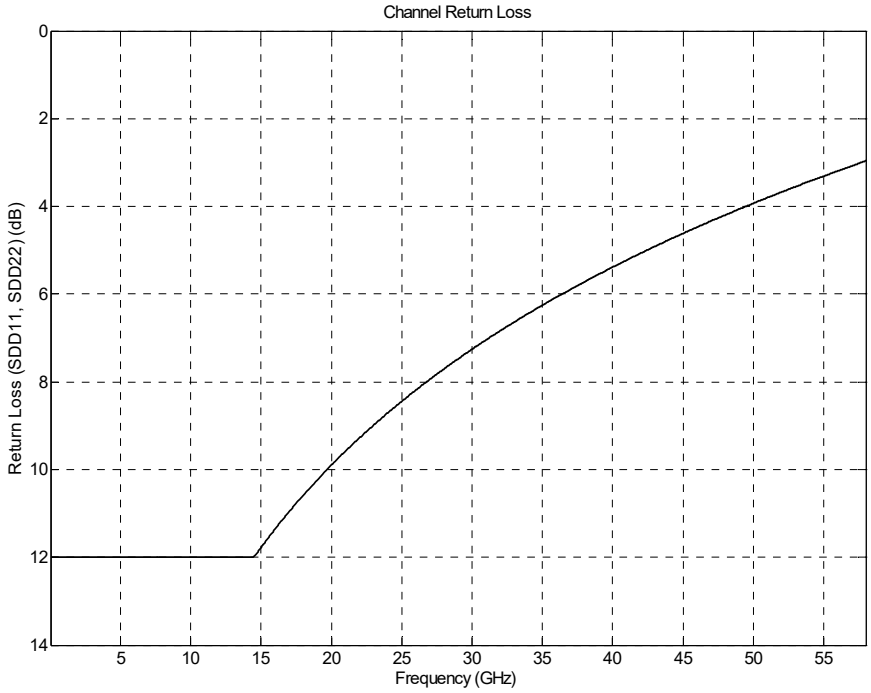
$$IL_{min} = \begin{bmatrix} 0.009\sqrt{f} + 0.015f & f_{min} \le f < f_b \end{bmatrix} \quad (24\text{-}2)$$

Channel insertion loss is an informative recommendation. For 8 dB channel, max loss (ILmax) parameters are scaled appropriately, ILmin remains unchanged.

The channel must comply with the normative specification in Section 24.2.4.2

24.2.4.4 Channel Return Loss

Figure 24-3. Channel Return Loss Limit for 58.0 Gsym/s (Informative)



Channel Return Loss shall be bounded by Equation (24-3) (informative) as shown in Figure 24-3.

$$RL_{max} = \begin{bmatrix} 12, & f_{min} \le f < \frac{f_b}{4} \\ 12 - 15\log_{10}\left(\frac{4f}{f_b}\right), & \frac{f_b}{4} \le f \le f_b \end{bmatrix} \quad (24\text{-}3)$$

24.2.4.5 Channel Effective Return Loss (ERL)

The background of ERL is described in the informative Appendix 25.E. ERLs of the channel (between test points T and R) are computed at test point T and at test point R using the procedure in 93A.5 [27] with the values in Table 24-3. Parameters that do not appear in Table 24-3 take values from Table 24-2. The value of T_{fx} is 0. N_{bx} is set to the value of N_b in Table 24-2.

Channel ERLs shall be greater than or equal to 7.35 dB for CAT1, 7.5 dB for CAT2, and 8 dB for CAT3 channels.

Table 24-3. Channel ERL Parameter Values

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	0.531	UI
Incremental available signal loss factor	β_x	0	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.618	-
Length of the reflection signal	N	400	UI

24.2.4.6 Channel DC-coupling

The transmitter shall be connected with DC-coupled package substrate traces to the receiver. AC-coupling can be supported, if the DC-blocking capacitor is implemented in the transmitter or receiver IC on the die. The low-frequency 3 dB cutoff of the AC-coupling shall be less than 100 kHz.

24.3 Electrical Characteristics

The electrical signaling is based on high speed low voltage logic with a nominal differential impedance of 100 Ω.

24.3.1 Transmitter Characteristics

The transmitter electrical requirements at compliance point T (see Figure 24-1) are specified in Table 24-4, and the jitter requirements are specified in Table 24-5.

Table 24-4. Transmitter Electrical Output Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	T_Baud		36		58	Gsym/s
Output Differential Voltage	T_Vdiff	See Note 2, 3.			750	mVppd
Output AC Common Mode Voltage	T_VcmAC	See Note 2, 3.			15	mVrms
Single-ended Transmitter Output Voltage	T_Vse	See Note 2, 3.	0.1		1.2	V
Effective return loss (ERL)		See Section 24.3.1.3	11			dB
Common Mode Output Return Loss	T_SCC22	200 MHZ to fb/2			-6	dB
Level Separation Mismatch Ratio	T_RLM	See Note 2, 3, 4, 5	0.95			-
Steady-state Voltage	T_Vf		0.275		0.375	V
Linear Fit Pulse Peak	T_Pk		0.85× T_Vf			V
Signal-to-Noise-and-Distortion-Ratio	T_SNDR		32.5			dB

NOTES:
2. Signals are specified as measured through a fourth-order Bessel-Thomson low-pass response with 43 GHz 3 dB bandwidth. Sampling oscilloscopes will not be able to pattern lock and may substitute the 40 GHz bandwidth limit with compensation for the reduced bandwidth.
3. Measured as described in Section 24.3.1.2. T_Vdiff min is set by the steady-state voltage T_Vf min.
4. Measured as described in Section 24.3.1.6.
5. T_RLM is defined in Appendix 16.C.4.3.

Table 24-5. Transmitter Output Jitter Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Uncorrelated Jitter (time interval from 0.0000005% to 99.9999995% of the probability distribution)	T_J_{8u}	See Note 1			0.1546	UI
Uncorrelated jitter RMS (standard deviation of the probability distribution)	T_J_{RMS}				0.0224	UIrms
Even-Odd Jitter	T_EOJ				0.025	UIpp

NOTES:
1. Measured as described in Section 24.3.1.7.

24.3.1.1 Transmitter Baud Rate

All devices shall work within the range from 36 Gsym/s to 58 Gsym/s as specified for the device, with the baud rate tolerance as per Section 3.2.11. A CEI implementation complies to the specifications of this clause over the range of baud rates stated for the implementation within this range.

24.3.1.2 Transmitter Amplitude and Swing

The differential output voltage T_Vdiff is defined to be True minus Complement. The common-mode output voltage T_Vcm is defined to be one half of the sum of True and Complement. These definitions are illustrated in Section 1.6.1.

For a QPRBS13-CEI test pattern (Appendix 16.C.3.1), the peak-to-peak value of the differential output voltage (T_Vdiff) shall be less than or equal to the limit given in Table 24-4 regardless of the transmit equalizer setting.

The DC common-mode output voltage (T_Vcm) shall be within the limits in Table 24-4 with respect to local ground.

The AC common-mode output voltage (T_VcmAC) shall be less than or equal to the limit given in Table 24-4 with respect to local ground. Common-mode output voltage requirements shall be met regardless of the transmit equalizer setting.

The single-ended transmitter output voltage (T_Vse) shall be within the limits in Table 24-4 with respect to local ground.

The transmitter shall be capable of providing a differential steady state output amplitude (2xT_V_f) between 550 and 750 mVppd with transmit emphasis disabled.

Transmitter differential output amplitude shall additionally adhere to the requirements in Section 24.3.1.6.

Power-down behavior is beyond the scope of CEI IA.

24.3.1.3 Transmitter Return Loss

ERL of the transmitter at compliance point T is computed using the procedure in 93A.5 [27] with the values in Table 24-6. Parameters that do not appear in Table 24-6 take values from Table 24-2. The value of T_{fx} is 0. N_{bx} is set to the value of N_b in Table 24-2.

Table 24-6. Transmitter and Receiver ERL Parameter Values

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	0.531	UI
Incremental available signal loss factor	β_x	0	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.618	-
Length of the reflection signal	N	100	UI

Transmitter ERL at T shall be greater than or equal to 11 dB.

This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements shall be 100 Ω.

24.3.1.4 Transmitter Lane-to-Lane Skew

Refer to Section 3.2.7, but expect that limit needs to be changed.

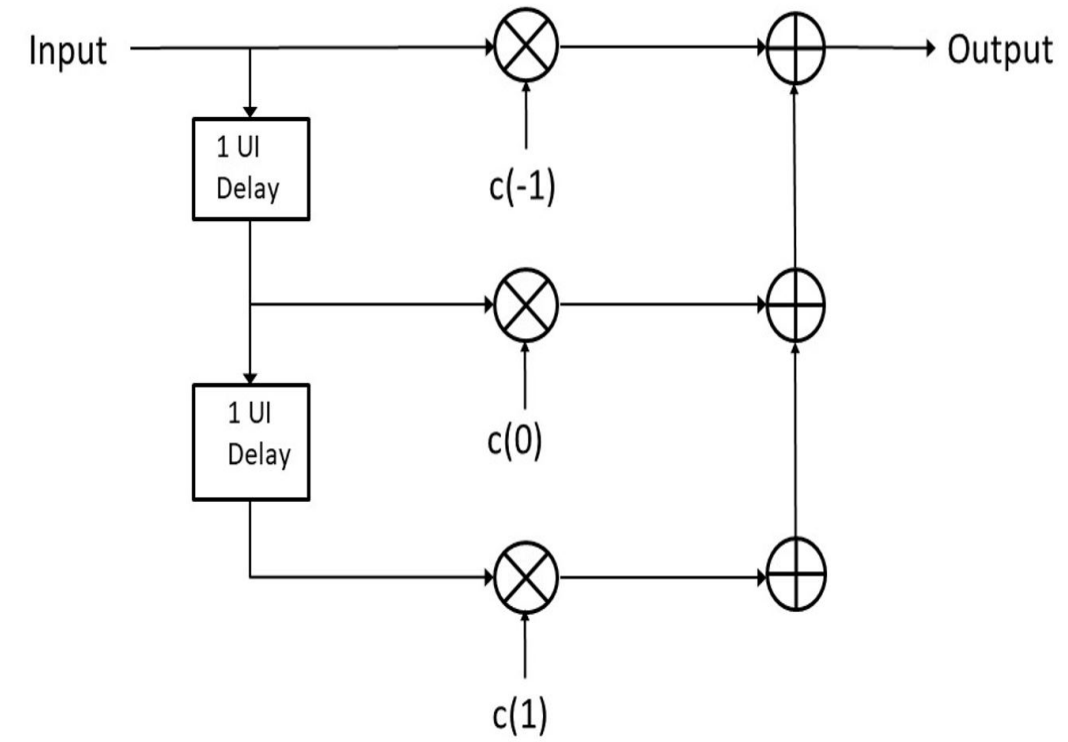
24.3.1.5 Transmitter Short Circuit Current

Please refer to Section 3.2.9.

24.3.1.6 Transmitter output waveform requirements

The transmitter function includes programmable equalization to compensate for the frequency-dependent loss of the channel and facilitate data recovery at the receiver. The functional model for the transmit equalizer is the three tap transversal filter shown in Figure 24-4.

Figure 24-4. Transmit equalizer functional model



Link budgets in this document assume optimized TX FIR equalization that is part of the system management function. The specific implementation is outside the scope of this document.

24.3.1.6.1 Linear fit to the measured waveform

The following test procedure defines linear fit pulse response, linear fit error e(k) (see Section 11.3.1.6.4), and normalized transmitter coefficient values.

For each configuration of the transmit equalizer, capture at least one complete cycle of the QPRBS13-CEI test pattern (Appendix 16.C.3.1) at the TX bump (see Figure 24-1).

Compute the linear fit pulse response p(k) from the captured waveform per Section 11.3.1.6.2 using Np = 4 and Dp = 2. Note that Np, Dp are equivalent to T_Np, T_Dp defined in Section 11.3.1.6.2, and are used for T_Nw and T_Dw defined in Section 11.3.1.6.2. For aligned symbol values x(n) use -1, -ES1, ES2, and 1 to represent symbol values of -1, -1/3, 1/3, and 1, respectively, and where ES1 and ES2 are the effective symbol levels determined in Appendix 16.C.4.3.

For each configuration of the transmit equalizer, compute the normalized transmit equalizer coefficients, c(i), according to Section 11.3.1.6.2 - Section 11.3.1.6.5.

24.3.1.6.2 Steady-state voltage and linear fit pulse peak

The linear fit pulse, p(k), is determined according to the linear fit procedure in Section 11.3.1.6.2 - Section 11.3.1.6.5, as modified by Section 24.3.1.6.1. The steady-state voltage T_Vf is defined to be the sum of the linear fit pulse p(k) divided by M, as shown in Equation (11-12).

The steady-state voltage, T_Vf, shall satisfy the requirements in Table 24-4.

The linear fit pulse peak, T_Pk, is the highest value of p(k). It shall satisfy the requirement in Table 24-4.

24.3.1.6.3 Transmitter equalizer coefficients

Table 24-7. Coefficient Range and Step Size

Coefficients	Normalized Amplitude		Normalized Step Size (%)
	Min (%)	Max (%)	
c(-1)	-14	0	0.2 to 2.5
c(1)	-18	0	0.2 to 2.5
c(0)	60	100	0.2 to 2.5

The normalized amplitudes of the coefficients of the transmitter equalizer (computed per Section 24.3.1.6.1) shall meet the requirements in Table 24-7. "min" is defined as the minimum normalized amplitude of the coefficient that must be supplied by the transmitter to be compliant. "max" is defined as the maximum normalized amplitude of the coefficient that must be supplied by the transmitter to be compliant.

The amplitude of a coefficient can be computed by multiplying its normalized amplitude by T_Vf, which is defined in Section 24.3.1.6.2.

The peak-to-peak output voltage is approximated by

$$(|c(-1)| + |c(0)| + |c(1)|) * 2 * T_Vf \quad (24\text{-}4)$$

and should not exceed the limit for T_Vdiff given in Table 24-4.

24.3.1.6.4 Transmitter Output Noise and Distortion

Signal-to-noise-and-distortion ratio (SNDR) is measured at the transmitter output using the following method, with the transmitter on the lane under test transmitting QPRBS13-CEI and transmitters on lanes not under test enabled and transmitting QPRBS31-CEI test pattern as defined in Appendix 16.C.3.2, or a valid CEI signal, or transmitting the same pattern with a slightly different Baud rate on each lane so that lane to lane signals are asynchronous. These transmitters shall have identical transmit equalizer settings to the transmitter under test.

Compute the linear fit to the captured waveform and the linear fit pulse response, p(k), and error, e(k), according to Section 24.3.1.6.1. Denote the standard deviation of e(k) as σ_e.

With the QPRBS13-CEI pattern and the same configuration of the transmit equalizer, measure the RMS deviation from the mean voltage at a fixed point in a run of at least 6 consecutive identical PAM4 symbols. The RMS deviation is measured for a run of each of the four PAM4 symbol levels.The average of the four measurements is denoted as σ_n.

SNDR is defined by Equation (24-5) where p_{max} is the maximum value of p(k).

$$SNDR = 10\log_{10}\left(\frac{p_{max}^2}{\sigma_e^2 + \sigma_n^2}\right)(dB) \quad (24\text{-}5)$$

SNDR shall be greater than 32.5 dB for any allowable transmit equalizer setting.

24.3.1.7 Transmitter output jitter

Jitter measurements in this sub-clause are performed with transmitters on physical lanes not under test enabled and transmitting QPRBS31-CEI test pattern as defined in Appendix 16.C.3.2, or a valid CEI signal, or transmitting the same pattern with a slightly different Baud rate on each lane so that lane to lane signals are asynchronous. These transmitters shall have identical transmit equalizer settings to the transmitter under test.

J_{8u}, J_{RMS}, and EOJ are defined by measurements of 12 specific transitions in a QPRBS13-CEI pattern in order to exclude correlated jitter. The 12 transitions represent all possible combinations of four identical symbols followed by two different identical symbols as shown in Table 24-8. The sequences are located by the symbol indices given in the table where symbols 1 to 7 are the run of seven +1s.

Alternatively, EOJ can be defined by measurements of 12 specific transitions in a QPRBS9-CEI pattern (see Appendix 25.G) in order to exclude short-term correlated jitter. The 12 transitions represent all possible combinations of two to five identical symbols followed by two different identical symbols as shown in Table 24-9. The sequences are located by the symbol indices given in the table where symbols 1 to 5 are the run of five +1s.

The threshold used to define each transition is given in Table 24-8 and Table 24-9 where V_{-1}, $V_{-1/3}$, $V_{1/3}$, and V_1 are as defined in Appendix 16.C.4.3.

The jitter is measured with a clock from a clock recovery unit (CRU) (i.e., a first order golden PLL, with corner frequency at f_b/13280, and a 20 dB/decade slope, see Section 1.6) as the trigger or reference clock.

J_{8u}, J_{RMS}, and EOJ specifications shall be met regardless of the transmit equalization setting.

Table 24-8. QPRBS13-CEI Pattern Symbols Used for Jitter Measurement

Label	Description	Gray Coded PAM4 Symbols	Index of First Symbol	Index Transition Begins	Index Transition Ends	Index of Last Symbol	Threshold Level
REF	Reference for symbol index	3333333	1	--	--	7	--
R03	0 to 3 rise	10000 330	1830	1834	1835	1837	$(V_{-1}+V_1)/2$
F30	3 to 0 fall	23333 001	1269	1273	1274	1276	
R12	1 to 2 rise	0111111 2222221	3638	3644	3645	3651	$(V_{-1/3}+V_{1/3})/2$
F21	2 to 1 fall	022222 113	1198	1203	1204	1206	
R01	0 to 1 rise	100000 113	6835	6840	6841	6843	$(V_{-1}+V_{-1/3})/2$
F10	1 to 0 fall	21111 003	2992	2996	2997	2999	
R23	2 to 3 rise	32222 330	6824	6828	6829	6831	$(V_{1/3}+V_1)/2$
F32	3 to 2 fall	033333 2222223	7734	7739	7740	7746	
R02	0 to 2 rise	10000 223	3266	3270	3271	3273	$(V_{-1}+V_{1/3})/2$
F20	2 to 0 fall	122222 0000002	7282	7287	7288	7294	
R13	1 to 3 rise	011111 331	133	138	139	141	$(V_{-1/3}+V_1)/2$
F31	3 to 1 fall	23333 112	7905	7909	7910	7912	

Table 24-9. QPRBS9-CEI Pattern Symbols Used for Jitter/EOJ Measurement

Label	Description	Gray Coded PAM4 Symbols	Index of First Symbol	Index Transition Begins	Index Transition Ends	Index of Last Symbol	Threshold Level
REF	Reference for symbol index	33333	1	--	--	5	--
R03	0 to 3 rise	1000 331	260	263	264	266	$(V_{-1}+V_1)/2$
F30	3 to 0 fall	233333 001	511	5	6	8	
R12	1 to 2 rise	311 2221	464	466	467	470	$(V_{-1/3}+V_{1/3})/2$
F21	2 to 1 fall	122 11110	254	256	257	261	
R01	0 to 1 rise	200 113	503	505	506	508	$(V_{-1}+V_{-1/3})/2$
F10	1 to 0 fall	21111 0003	256	260	261	264	
R23	2 to 3 rise	3222 330	210	213	214	216	$(V_{1/3}+V_1)/2$
F32	3 to 2 fall	133 223	507	509	510	1	
R02	0 to 2 rise	200 22223	63	65	66	70	$(V_{-1}+V_{1/3})/2$
F20	2 to 0 fall	12222 001	321	325	326	328	

R13	1 to 3 rise	0111 331	166	169	170	172	$(V_{-1/3}+V_1)/2$
F31	3 to 1 fall	033 1112	263	265	266	269	

24.3.1.7.1 J_{8u} and J_{RMS} Jitter

For each transition i, 1 ..i ..12, of the transitions specified in Table 24-8, obtain a set S_i = {$t_i(1)$, $t_i(2)$, ...} of transition times modulo the period of the pattern. The 12 sets should be of equal size and the size of all sets should be chosen to enable calculation of J_{8u} (as defined below) with sufficient accuracy.

Calculate the average of each set Si, Tavgi, and subtract it from all elements of that set, to create a set $S0_i$ = {$t_i(1)$ - $Tavg_i$, $t_i(2)$ - $Tavg_i$, ...}.

Combine the sets $S0_i$, i=1 to 12, to create an estimated probability distribution $f_J(t)$.

J_{8u} is defined as the time interval that includes all but 10^{-8} of $f_J(t)$, from the 0.0000005th to the 99.9999995th percentile of $f_J(t)$.

J_{RMS} is defined as the standard deviation of $f_J(t)$.

24.3.1.7.2 Even-Odd Jitter (EOJ)

For one of the 12 specific transitions in QPRBS13-CEI in Table 24-8 or QPRBS9-CEI in Table 24-9:

a) Trigger once in 3 repeats of the QPRBS13-CEI or QPRBS9-CEI test pattern.

Obtain the mean time (T3) for this transition in the first QPRBS13-CEI or QPRBS9-CEI.

Obtain the mean time (T4) for the same transition in the second QPRBS13-CEI or QPRBS9-CEI.

b) The difference between the two means (T4 – T3), is the estimated period of the repeating pattern.

For each of the 12 specific transitions in QPRBS13-CEI in Table 24-8 or QPRBS9-CEI in Table 24-9:

1) Trigger once in 2 repeats of the QPRBS13-CEI or QPRBS9-CEI test pattern.

Obtain the mean time (T1) for the specific transition in the first QPRBS13-CEI or QPRBS9-CEI.

Obtain the mean time (T2) for the same transition in the second QPRBS13-CEI or QPRBS9-CEI.

2) Calculate EOJ for this transition as |(T2 – T1) – (T4 – T3)|.

EOJ is the maximum of the 12 measurements.

NOTE 1—Both of (T2 - T1) and (T4 - T3) are about 8191 UI for QPRBS13-CEI, or 511 UI for QPRBS9-CEI, which is much larger than the EOJ value. Hence, each of T1 through T4 should have high precision.

24.3.2 Receiver Characteristics

A compliant receiver shall autonomously operate at the specified BER with the worst case combination of a compliant transmitter and a compliant channel. The receiver also shall not cause error propagation that violates the error burst length requirement as defined in Section 24.2.2. Further receiver electrical requirements at compliance point R (see Figure 24-1) are specified in Table 24-10, with the receiver interference tolerance parameters specified in Table 24-11. Lanes not under test should be enabled and transmitting or receiving asynchronous or uncorrelated signals.

Table 24-10. Receiver Electrical Input Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	R_Baud		36		58	Gsym/s
Effective return loss (ERL)		See Section 24.3.1.3	11			dB
Common Mode Input Return Loss	R_SCC11	0.2-10 GHz			-6	dB
		10 GHz-fb			-4	dB
Interference Tolerance		Table 24-11				
Jitter Tolerance		Table 24-12				

Table 24-11. Receiver interference tolerance parameters (Note 1)

Parameter	Test 1 values				Test 2 values				Units
	Min	Max (CAT1)	Max (CAT2)	Max (CAT3)	Min	Max (CAT1)	Max (CAT2)	Max (CAT3)	
Pre-FEC Bit Error Ratio (BER), Note 3		10^{-6}	10^{-8}	10^{-9}		10^{-6}	10^{-8}	10^{-9}	
COM, including effects of broadband noise		2.6	2.6	2.6		2.6	2.6	2.6	dB
Insertion loss at Nyquist, Note 2		2	2	2		10	8	8	dB

NOTES:
1. Definition can be found in Annex 93A of IEEE Std 802.3 [1]. See Section 24.3.2.4.
2. Measured between TX and RX bumps (see Figure 24-1).
3. Pre-FEC BER of 1e-9 for 8 dB channel; or 1e-8 for 10 dB channel, or 1e-6 for 10 dB channel.

24.3.2.1 Input Baud Rate

All devices shall work within the range from 36 Gsym/s to 58 Gsym/s as specified for the device, with the baud rate tolerance as per Section 3.2.11. A CEI implementation complies to the specifications of this clause over the range of baud rates stated for the implementation within this range.

24.3.2.2 Reference Input Signals

The receiver shall accept differential input signal amplitudes produced by a compliant transmitter connected with the minimum attenuation specified in Figure 24-2 to the receiver. This may be larger than the 750 mVppd maximum of the transmitter due to output/input impedances and reflections.

The minimum input amplitude is defined by the minimum transmitter amplitude, the actual receiver input impedance and the loss of the actual package trace. Note that the minimum transmitter amplitude is defined using a well controlled load impedance, however the real receiver is not, which can leave the receiver input signal smaller than expected.

24.3.2.3 Receiver Input Return Loss

ERL of the receiver at compliance point R is computed using the procedure in 93A.5 [27] with the values in Table 24-6. Parameters that do not appear in Table 24-6 take values from Table 24-2. The value of T_{fx} is 0. N_{bx} is set to the value of Nb in Table 24-2.

The specification for the minimum value of the receiver ERL at compliance point R is the same as the specification for the minimum value of the transmitter at compliance point T.

The reference impedance for differential return loss measurements shall be 100 Ω.

24.3.2.4 Receiver Interference Tolerance

The receiver interference tolerance test is based on the test defined in Annex 120D.3.2.1 of IEEE Std 802.3 [27].

The receiver on each lane shall meet the pre-FEC BER requirement with channels matching the Channel Operating Margin (COM) and loss parameters for Test 1 and Test 2 in Table 24-11.

The test channel should be created using multiple chip module (MCM) with short interconnecting cables.

The following considerations apply to the interference tolerance test. The transmitter package is omitted in the COM calculation. The test transmitter's measured SNDR should be used for SNR_{TX} in the COM calculation. The transmitter output levels are set such that R_{LM} is equal to 0.95. The test transmitter meets the specifications in Section 24.3.1. The test transmitter is constrained such that for any transmitter equalizer setting the differential peak-to-peak voltage is less than 550 mV, and the normalized amplitudes of the coefficients of the transmitter equalizer c(-1), c(0) and c(1) are between the minimum and maximum limits given in Table 24-7.

The lower frequency bound for the noise spectral density constraints, f_{NSD1}, is 1 GHz. The ERL of the test channel at test point R (as defined in Annex 93A of IEEE Std 802.3 [27], IEEE Std 802.3cd [28], IEEE Std 802.3ck [29]) shall meet the requirements in Section 24.2.4.5, and be 3 dB better. The test transmitter's jitter parameters J_{8u} and J_{RMS} are measured. A_{DD} and σ_{RJ} are calculated from the measured values of J_{8u} and J_{RMS} using Equation (24-6), and Equation (24-7), respectively and used for COM parameters. Other COM parameters are set according to the values in Table 24-2. The broadband noise is added and adjusted to achieve the COM value in Table 24-11. The test pattern to be used is QPRBS31-CEI defined in Appendix 16.C.3.2. A test system with a fourth-order Bessel-Thomson low-pass response with 43 GHz 3 dB bandwidth is to be used for measurement of the signal applied by the pattern generator and for measurements of the broadband noise.

$$A_{DD} = \left(\frac{J_{8u}}{2} + Q_{8d} \sqrt{(Q_{8d}^2 + 1) \times J_{RMS}{}^2 - \left(\frac{J_{8u}}{2} \right)^2} \right) / (Q_{8d}^2 + 1) \quad \text{(24-6)}$$

$$\sigma_{RJ} = \left(\frac{J_{8u}}{2} - A_{DD} \right) / Q_{8d} \quad \text{(24-7)}$$

where Q_{8d} = 5.612001.

Note 1: Q_{8d} is an approximated solution of $Q(Q_{8d}) = 10^{-8}$. Q(x) is the complement of the standard Normal cumulative distribution function (CDF).

Note 2: Calculation of ADD requires that the term in the square-root in Equation (24-6) be positive. If this does not hold, a different transmitter should be used in the test setup.

24.3.2.5 Receiver Jitter Tolerance

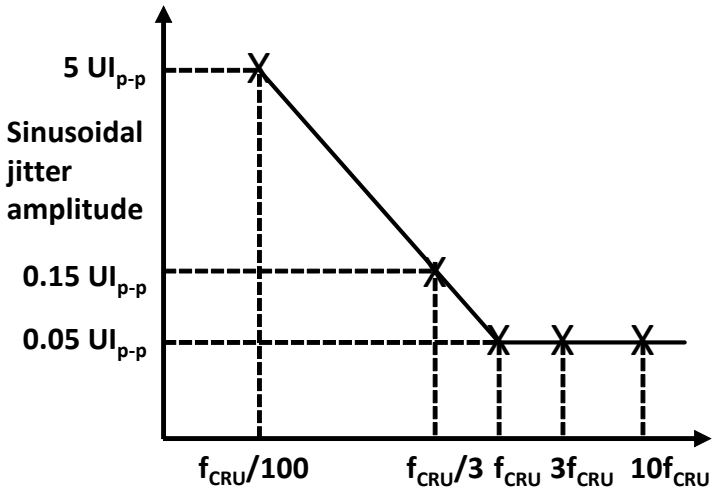
Receiver jitter tolerance shall meet conditions and parameters defined in Table 24-12. This sinusoidal jitter is part of the jitter applied in the stressed input test. The sinusoidal jitter is calibrated at 10x the reference CRU's bandwidth and must be tested at $f_{CRU}/100$, $f_{CRU}/3$, f_{CRU}, $3f_{CRU}$, and $10f_{CRU}$, where f_{CRU} is the jitter corner frequency

given by f_b/13280, with sinusoidal jitter of 5 UI, 0.15 UI, 0.05 UI, 0.05 UI and 0.05 UI respectively. For this test the channel used is as for the receiver interference tolerance described in Section 24.3.2.4. Note that the values measured for J_{8u} and JRMS include the effects of this added sinusoidal jitter. Noise is added to obtain a COM of 2.6 dB with these measured jitter values using the same procedure as for calibrating the noise for the interference tolerance test. The receiver bit error ratio (BER) shall meet the requirements of Section 24.2.2 for each pair of jitter frequency and peak-to-peak amplitude values listed above and shown in Figure 24-5.

Table 24-12. Receiver Jitter Tolerance Parameters

Frequency Range	Sinusoidal jitter, peak-to-peak (UI)
f < f_b/1328000	Not Specified
f_b/1328000 < f ≤ f_b/13280	5*f_b/(1328000*f)
f_b/13280 < f ≤ 10f_{CRU}	0.05

Figure 24-5. Receiver Jitter Tolerance Mask



24.3.2.6 Single Ended Input Voltage

The single ended voltage levels with respect to the receiver ground at the input of the receiver are dependent on the transmitter implementation. The voltage levels at the input of an AC coupled receiver (if the effective AC coupling is done within the receiver) will be between 0.1 V and 1.2 V with respect to local ground.

24.3.2.7 Input Lane-to-Lane Skew

Refer to Section 3.2.8, but expect that limit needs to be changed.

25 CEI-112G-VSR-PAM4 Very Short Reach Interface

This clause details the requirements for the CEI-112G-VSR-PAM4 very short reach high speed chip-to-module electrical interface of nominal baud rates of 36.0 Gsym/s to 58.0 Gsym/s. A compliant host or module shall meet all of the relevant requirements listed below. The electrical interface is based on high speed, low voltage logic, and connections are point-to-point balanced differential pairs.

This clause defines the characteristics required to communicate between CEI-112G-VSR-PAM4 integrated circuits using copper signal traces on a printed circuit board or cables, a mated connector pair and copper signal traces inside an optical module. These specifications are normative at the test points shown in Figure 25-1. A 'length' is effectively defined in terms of its attenuation and phase response rather than its physical length.

Hosts and modules compliant to CEI-112G-VSR-PAM4 from different manufacturers shall be inter-operable.

25.1 Requirements

The objectives and requirements for the CEI-112G-VSR-PAM4 implementation agreement are given by the project definition as follows:

- Support baud rates (f_b) within the range from 36.0 Gsym/s to 58.0 Gsym/s as specified for the device using PAM4 coding. A CEI implementation complies to the specifications of this clause over the range of baud rates stated for the implementation within this range.
- Capable of driving up to a minimum of 200 mm of host PCB trace plus one connector and a minimum of 20 mm of module PCB trace. The use of cables to replace or partially replace the copper signal traces on the printed circuit board is acceptable and may extend the physical length of the connection.
- Capable of achieving a raw Bit Error Ratio (BER) of 10^{-6} or better per lane. FEC is assumed to be used to achieve a corrected BER of 10^{-15} or better per lane. The baud rate includes the overhead required for FEC. The definition of FEC is outside the scope of this IA (see Appendix 16.D).
- Module electrical input to be self-adaptive and autonomous.
- Shall support AC-coupled operation.
- Shall allow multi-lanes (1 to n).
- Shall support hot plug.

25.2 General CEI Requirements

25.2.1 Data Patterns

See Appendix 16.C.5

25.2.2 Transmitter equalizer function

Both host and module Tx FIR (or equivalent) are likely to be required to meet TP1a and far-end TP4 eye requirements respectively for a high loss channel (see Figure 25-1).

25.2.3 Bit Error Ratio

A raw Bit Error Ratio (BER) better than or equal to 10^{-6} is required on each lane. A compliant host or module, when receiving from a compliant module or host, shall deliver the specified raw BER to the subsequent FEC decoder. Error bursts with length more than 15 PAM4 symbols delivered to the PAM4 decoder shall occur with a probability of less than 1 in 10^{20} PAM4 symbols. To enable a more practical test, error bursts with length more than 6 PAM4 symbols delivered to the PAM4 decoder should occur with a probability of less than 1 in 10^{12} PAM4 symbols. See also Appendix 16.D.

25.2.4 Ground Differences

The maximum ground difference between the host and module shall be ±50 mV. The common mode voltage limits are set taking this difference into account.

25.3 Electrical Characteristics

Hosts and modules shall meet the specifications defined in Table 25-1, Table 25-2, Table 25-3, Table 25-4, Table 25-5 and Table 25-6 as applicable. The direction of a signal (host-to-module or module-to-host) determines which table is applicable.

AC coupling is required in the module for both Tx and Rx.

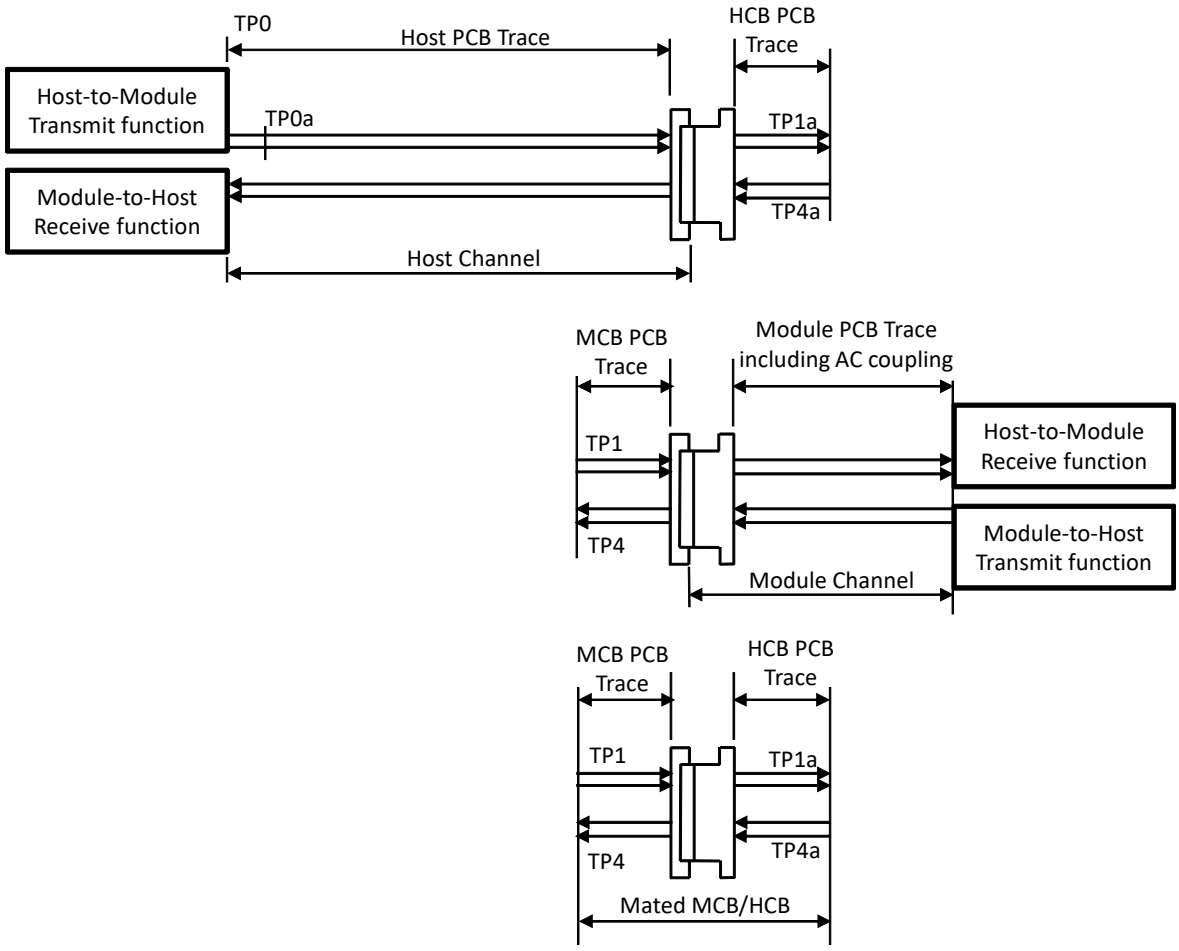
25.3.1 Compliance Point Specifications

Figure 25-1 below gives the reference model and test points associated with host-to-module and module-to-host lanes.

Reference test fixtures, called compliance boards, are used to access the electrical specification parameters. The output of the Host Compliance Board (HCB) provides access to the host-to-module electrical signal (host electrical output) defined at TP1a. Additional module electrical input specifications, for host-to-module communication, are defined at TP1, the input of the Module Compliance Board (MCB). The output of the MCB provides access to the module-to-host electrical signal (module electrical output)

defined at TP4. Additional host electrical input specifications, for module-to-host communication, are defined at TP4a, the input of the HCB. Informative recommendations for the host transmit function at TP0a are given in Appendix 25.C.

Figure 25-1. Measurement points using compliance boards



25.3.2 Host-to-Module Electrical Specifications

Each host-to-module lane shall meet the specifications of Table 25-1 and Table 25-2. Definitions and methodologies can be found in Sections 25.3.4 to 25.3.12.

Table 25-1. Host-to-Module Electrical Specifications at TP1a (host output)

Parameter	Min.	Max.	Unit	Conditions
Differential Voltage pk-pk	-	860	mV	See 25.3.4
Common Mode Voltage (Vcm)	-0.3	2.8	V	Referred to host ground See Note 1
Common Mode Noise RMS	-	17.5	mV	See 25.3.5
Differential Termination Resistance Mismatch	-	10.0	%	At 1 MHz. See 13.3.6
Common Mode to Differential Mode Conversion (SDC22)	-	Equation (25-2)	dB	See Note 2
Common Mode Return Loss (SCC22)	-	-2 -1.6 - 0.1*f -8.5 + 0.13*f	dB dB dB	0.25 ≤ f ≤ 4 4 < f ≤ 30 30 < f ≤ min(0.8*f_b,43GHz) f is in GHz, see Note 2
Effective Return Loss (ERL)	8.5	-		See Note 3
Transition Time (short mode)	10		ps	See 16.C.4.1 except use a Bessel-Thomson filter bandwidth of 43 GHz
Transition Time (long mode)	15		ps	
Eye Height in the region from Ts -50 mUI to Ts + 50 mUI	10	-	mV	See 25.3.11 See Note 4
Vertical Eye Closure (VEC) in the region from Ts -50 mUI to Ts + 50 mUI	-	12	dB	See 16.C.4.2 except use the reference receiver of 25.3.11.4.

NOTES:
1. Vcm is defined in Table 1-2 of Section 1.6
2. S-parameter specifications are based on a differential reference impedance of 100 Ω and a common mode reference impedance of 25 Ω
3. ERL is based on the methodology in IEEE 802.3 [27] clause 95A.5. See Section 25.3.7.
4. Open eye is generated through the use of a reference Continuous Time Linear Equalizer (CTLE) and DFE applicable to all three PAM4 eyes (See 25.3.11.4)

Table 25-2. Host-to-Module Electrical Specifications (module input)

Parameter	Test Point	Min.	Max.	Unit	Conditions
Overload Differential Voltage pk-pk	TP1a	900	-	mV	See 25.3.12
Common Mode Voltage (Vcm)	TP1	-350	2850	mV	See Notes 1, 2
Differential Termination Resistance Mismatch	TP1	-	10	%	At 1 MHz. See 25.3.6
Differential Mode to Common Mode Conversion (SCD11)	TP1	-	Equation (25-1)	dB	See Note 3
Effective Return Loss (ERL)		9	-	dB	See Note 4
Stressed Input Test	TP1a	See Section 25.3.11.3			

NOTES:
1. Vcm is defined in Table 1-2 General Definitions of Section 1.6
2. Vcm is generated by the host. Specification includes effects of ground offset voltage
3. S-parameter specifications are based on a differential reference impedance of 100 Ω and a common mode reference impedance of 25 Ω
4. ERL is based on the methodology in IEEE 802.3 [27] clause 95A.5. See Section 25.3.7.

Table 25-3. Crosstalk parameters for host output test and module stressed input test calibration at TP4

Parameter	Target value	Unit	Conditions
Crosstalk Amplitude Differential Voltage pk-pk	860	mV	
Crosstalk Slew Time	10	ps	between -270 mV and +270 mV, see Note 1

NOTES:
1. See Appendix 16.C.4.1 Transition Time and Slew Time except use a Bessel-Thomson filter bandwidth of 43 GHz

25.3.3 Module-to-Host Electrical Specifications

Each module-to-host lane shall meet the specifications of Table 25-4 and Table 25-5. Definitions and methodologies can be found in Sections 25.3.4 to 25.3.12.

Table 25-4. Module-to-Host Electrical Specifications at TP4 (module output)

Parameter	Min.	Max.	Unit	Conditions
Differential Voltage, pk-pk	-	860	mV	See 25.3.4
Common Mode Voltage (Vcm)	-350	2850	mV	See Note 1, Note 2
Common Mode Noise, RMS	-	17.5	mV	See 25.3.5
Differential Termination Resistance Mismatch	-	10	%	At 1 MHz. See 13.3.6
Common Mode to Differential Mode Conversion (SDC22)	-	Equation (25-2)	dB	See Note 3
Effective Return Loss (ERL)	9.0	-	dB	See Note 4
Common Mode Return Loss (SCC22)	-	-2 -1.6 - 0.1*f -8.5 + 0.13*f	dB dB dB	0.25 ≤ f ≤ 4 4 < f ≤ 30 30 < f ≤ min(0.8*f_b,43GHz) See Note 3
Transition Time	8.0		ps	See 16.C.4.1 except use a Bessel-Thomson filter bandwidth of 43 GHz
Near-end Vertical Eye Closure over ± 50 mUI (VEC)	-	12	dB	See 25.3.11 See Note 5
Near-end Eye Height over ± 50 mUI	20	-	mV	See 25.3.11 See Note 5
Far-end Vertical Eye Closure over ± 50 mUI (VEC)	-	12	dB	See 25.3.11 See Note 5
Far-end Eye Height over ± 50 mUI	15	-	mV	See 25.3.11 See Note 5

NOTES:
1. Vcm is defined in Table 1-2 General Definitions of Section 1.6
2. Vcm is generated by the host. Specification includes effects of ground offset voltage.
3. S-parameter specifications are based on a differential reference impedance of 100 Ω and a common mode reference impedance of 25 Ω
4. ERL is based on the methodology in IEEE 802.3 [27] clause 95A.5. See Section 25.3.7.
5. Open eye is generated through the use of a reference Continuous Time Linear Equalizer (CTLE) and Decision Feedback Equalizer (DFE) applicable to all three PAM4 eyes (See 25.3.11.4)

Table 25-5. Module-to-Host Electrical Specifications (host input)

Parameter	Test Point	Min.	Max.	Unit	Conditions
Overload Differential Voltage pk-pk	TP4	900	-	mV	See 25.3.12
Differential Termination Resistance Mismatch	TP4a	-	10	%	At 1 MHz. See 13.3.6
Effective Return Loss (SDD11)	TP4a	8.5	-	dB	See Note 1
Differential Mode to Common Mode Conversion (SCD11)	TP4a	-	Equation (25-1)	dB	See Note 1
Stressed Input Test	TP4	See 25.3.11.3			
Common Mode Voltage (Vcm)	TP4a	-0.3	2.8	V	See Note 1, Note 3

NOTES:
1. ERL is based on the methodology in IEEE 802.3 [27] clause 95A.5. See Section 25.3.7.
2. Vcm is defined in Table 1-2 General Definitions of Section 1.6
3. Referred to host ground. Common mode voltage is generated by host

Table 25-6. Crosstalk parameters for module output test and host stressed input test calibration at TP1a

Parameter	Target value	Unit	Conditions
Crosstalk Amplitude differential voltage pk-pk	860	mV	
Crosstalk Slew Time, module in short mode	10.0	ps	between -270 mV and +270 mV, see Note 1
Crosstalk Slew Time, module in long mode	15.0	ps	

NOTES:
1. See Appendix 16.C.4.1 Transition Time and Slew Time except use a Bessel-Thomson filter bandwidth of 43 GHz.

25.3.4 Output Differential Voltage, peak-peak

The differential voltage, peak-peak, (see Section 1.6.1 for definition of differential voltage peak-peak) shall meet the specifications given in Table 25-1 or Table 25-4 for the respective communication direction. Host and module Tx FIRs (or equivalent) are expected to be required to meet TP1a eye requirements for high loss channels and TP4 far-end eye requirements. AC coupling is required in the module for both Tx and Rx. The waveform is observed through a fourth-order Bessel-Thomson response with a 3 dB bandwidth of 43 GHz using a QPRBS13-CEI pattern (see Appendix 16.C.3.1). The differential voltage measured using a QPRBS13-CEI pattern is less than the in-service differential voltage due to frequency-dependent loss and length of the QPRBS13-CEI pattern.

25.3.5 Common Mode Noise

See Section 12.3 with the exception that the oscilloscope bandwidth shall be 43 GHz. As pattern lock is not used, sampling oscilloscopes may substitute 40 GHz bandwidth with compensation for the reduced bandwidth.

25.3.6 Differential Termination Resistance Mismatch

See Section 13.3.6.

25.3.7 Effective Return Loss

The background of ERL is described in the informative Appendix 25.E.
When measured at the respective test point the effective return loss shall not exceed the limit given in the appropriate table Table 25-1, Table 25-2, Table 25-4 or Table 25-5. The ERL of the host or module output or input at the appropriate test point is computed using the procedure in IEEE Std 802.3 [27] Annex 93A.5 (see IEEE P802.3ck [29] Annex 95A.5) with the values shown in Table 25-7.

Table 25-7. Transmitter and receiver ERL parameter values

Parameter	Symbol	Transmitter and Receiver	Mated Test Fixture	Units
Transition time associated with a pulse	T_r	10	10	ps
Length of the reflection signal for module	N	400	400	UI
Length of the reflection signal for host	N	800	400	UI
Time-gated propagation delay	T_{fx}	Note 1	0	ns
Equalizer length associated with reflection signal	N_{bx}	4	4	UI
Incremental available signal loss factor	β_x	0	0	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.618	0.618	-
Tukey ('raised cosine') window	tw	True	True	
Target detector error ratio	DER_0	10^{-6}	10^{-6}	-

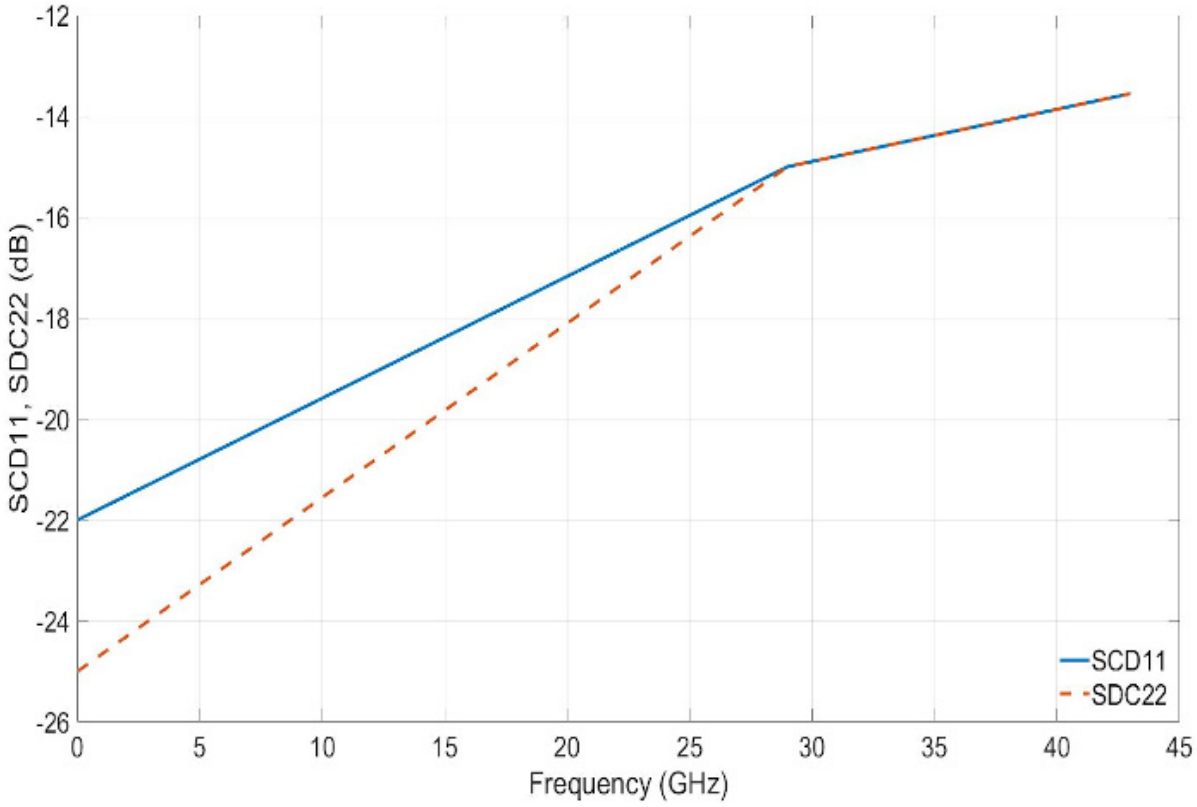
NOTES:
1. Twice the delay between the compliance board test connector and the host-facing or module-facing connection minus 0.2 ns

The test points are TP1a for host output, TP4a for host input, TP1 for module input and TP4 for module output.

25.3.8 Common to differential mode and differential to common mode conversion

The common mode to differential mode and differential mode to common mode conversion specifications are intended to limit the amount of unwanted signal energy that is allowed to be generated due to conversion of common mode voltage to differential mode voltage or vice versa. When measured at the respective input or output test point, common mode to differential mode or differential mode to common mode conversion shall not exceed the limits given in Equation (25-1) and Equation (25-2) (illustrated in Figure 25-2 for f_b=58 GHz). The common mode to differential mode conversion specification for the host and module outputs is more stringent than for the inputs to take into account the lack of a common mode input return loss specification.

Figure 25-2. SCD11 for module input (TP1) and host input (TP4a), and SDC22 for module output (TP4) and host output (TP1a) (for f_b=58 GHz)



$$\begin{aligned} &\text{SCD11} < \text{-22+14*}(f/f_b)\ \text{dB} \quad \text{for } 0.05\ \text{GHz} \le f \le f_b/2 \\ &\text{SCD11} < \text{-18+6*}(f/f_b)\ \text{dB} \quad \text{for } f_b/2 < f \le \min(0.8 * f_b, 43\ \text{GHz}) \end{aligned} \tag{25-1}$$

$$\begin{aligned} &\text{SDC22} < \text{-25+20*}(f/f_b)\ \text{dB} \quad \text{for } 0.05\ \text{GHz} \le f \le f_b/2 \\ &\text{SDC22} < \text{-18+6*}(f/f_b)\ \text{dB} \quad \text{for } f_b/2 < f \le \min(0.8 * f_b, 43\ \text{GHz}) \end{aligned} \tag{25-2}$$

25.3.9 Common Mode Return Loss

The common mode output return loss specification is intended to limit the amount of common mode energy that can be reflected by the host and module outputs. This has an effect on EMI radiation and differential mode signals generated via common mode to differential mode conversion.

25.3.10 Module near-end and far-end Eye Height and VEC

For each of two module output modes, short and long, the module output signal is defined with both a near-end channel and a far-end channel as shown in Table 25-8. The near-end and far-end channels are intended to emulate the host receiver Printed Circuit Board (PCB) signal path. Note that the Channel Insertion loss for the near-end and far-end channels does not include the MCB loss (See Appendix 25.4.1).

Table 25-8. Emulated Host Channels as shown in Figure 25-3 and Figure 25-4

Module Output Mode	Host Channel Type	Channel Insertion Loss (dB)	Zp (mm)
Short	near-end	0	0
Short	far-end	7.5	89.8
Long	near-end	4.5	53.8
Long	far-end	11.9	142.4

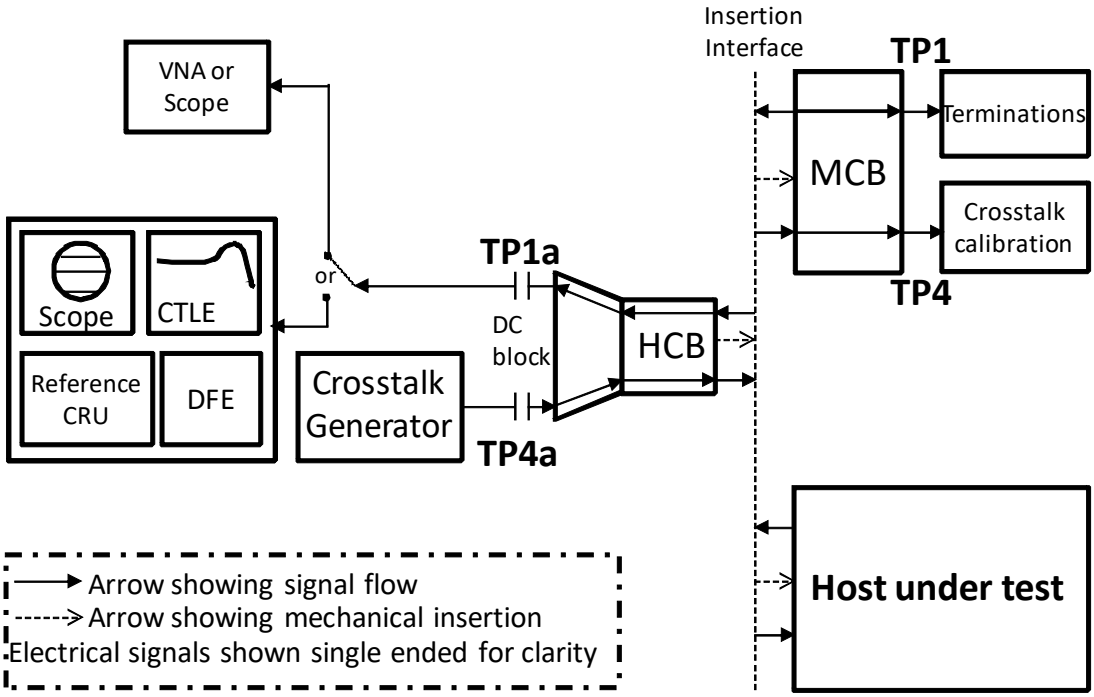
25.3.11 Eye Height, Vertical Eye Closure and Stressed Input tests

Eye Height and Vertical Eye Closure (VEC) are specified in Table 25-1 (host output) and Table 25-4 (module output). Compliance is verified using the test setup shown in Figure 25-3 (host) and Figure 25-4 (module). For example, the Eye Height measurement could include a total of 32 million captured PAM4 symbols, at a rate of one sample per symbol, with 16 million samples per individual eye (with the two middle levels (i.e. +1/3 and -1/3) used for the outer eyes and the middle eye). The 10^{-6} vertical eye points would have 8 samples at the top of each of the sub-eyes and 8 samples at the bottom of each of the sub-eyes. Compliance to the input specifications defined in Table 25-2 and Table 25-5 is verified using the test setup shown in Figure 25-8 (host) and Figure 25-9 (module).

25.3.11.1 Host and Module output Eye Height and Vertical Eye Closure test

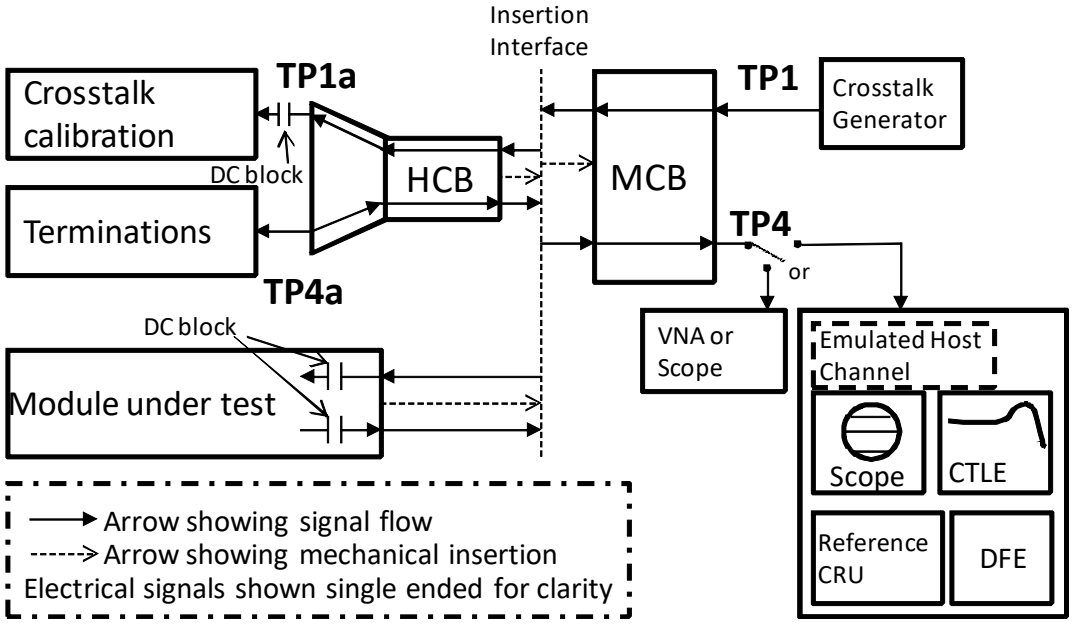
The host output Eye Height and Vertical Eye Closure (VEC) are defined for a signal at TP1a of Figure 25-1, the output of a Host Compliance Board as defined in Section 25.4.1, processed by the reference receiver of Section 25.3.11.4. The test setup is shown in Figure 25-3.

Figure 25-3. Host output test setup



The module output Eye Height and Vertical Eye Closure (VEC) is defined for a signal at TP4 of Figure 25-1, the output of a Module Compliance Board as defined in Section 25.4.1, processed by the emulated channel of Section 25.3.10 and the reference receiver of Section 25.3.11.4. The test setup is shown in Figure 25-4.

Figure 25-4. Module output test setup



25.3.11.1.1 Host and Module output test method

The signal at TP1a may appear as a closed eye, therefore a reference receiver with a Continuous Time Linear Equalizer (CTLE) and a 4-tap DFE (see Section 25.3.11.4) is used to equalize the host output signal and open the eye for Eye Height and VEC measurements. The reference receiver is also used to equalize the module output signal. For Eye Height and VEC measurements, this reference receiver is used instead of the Bessel-Thomson filter specified for other parameters. The signal after the reference receiver shall meet the specifications listed in Section 25.3.2 for host to module and Section 25.3.3 for module to host. All co-propagating and counter-propagating lanes are active as crosstalk sources, using a QPRBS13-CEI test pattern as defined in Appendix 16.C.3.1, or a QPRBS31-CEI test pattern as defined in Appendix 16.C.3.2, or a valid CEI signal. If the QPRBS13-CEI is used for the co-propagating lanes they should be asynchronous to the lane under test or sufficiently delayed to remove correlation from the lane under test. If the QPRBS13-CEI or QPRBS31-CEI patterns are used, any pairs of aggressor lanes should also be asynchronous to each other or sufficiently delayed. Amplitude and slew times for counter-propagating lanes are defined in Table 25-3 and Table 25-6. The lanes under test are asynchronous to the lanes in the opposing direction within the limits for the protocol in use.

Note: Co- and counter-propagating crosstalk generators based on valid NRZ CEI signals could be used but may over-stress the system as crosstalk from such generators may be greater than from PAM4 generators.

The test method for measuring either host or module output Eye Height and VEC as illustrated in Figure 25-5 is as follows:

1) Set the host or module to QPRBS13-CEI pattern (see Appendix 16.C.3.1).

-This allows the use of a sampling oscilloscope with a pattern lock.

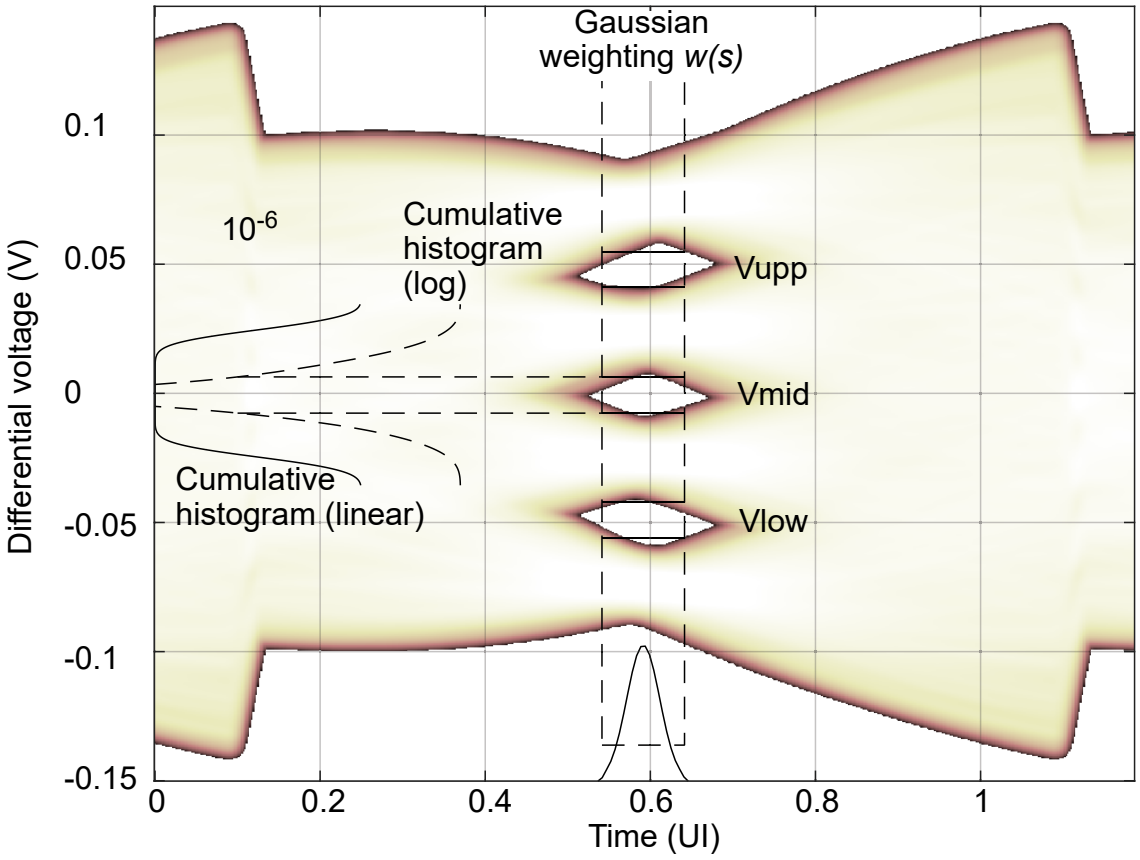
2) Capture the differential signal at TP1a or TP4 with a scope triggered with a clock from a reference clock recovery unit (CRU) with a first order transfer function with a 3 dB tracking bandwidth of f_b/13280 Hz.

-For TP1a, the scope shall be AC coupled.

-The reference CRU can be a software CRU in case of a real time scope.

-Sample the signal with a minimum of 3 samples per symbol or equivalent. Collect sufficient samples in order to construct normalized cumulative distribution functions (normalized CDFs) (see Figure 25-5) of the post-processed captured signals to a probability of 10^{-6} (without extrapolation) as described below. Depending on the sampling rate, careful interpolation using a method such as sin(x)/x or cubic spline may be needed for good accuracy.

Figure 25-5. TP1a and TP4 Eye Height parameters



3) Apply the reference receiver as defined in Section 25.3.11.4 to equalize the captured signal in step 2.

-For TP4 near-end compliance test of the module output in short mode, CTLE peaking and a 4-tap DFE is required in the reference receiver. Any reference receiver equalizer setting listed in Table 25-10 and Table 25-12 for short mode that meets both the Eye Height and VEC settings defined for TP4 in Table 25-4 is acceptable. Eye Height is the minimum value from the set of Vlow, Vmid and Vupp measurements (see Section 25.3.11.2 for these eye parameter definitions).

-For TP4 near-end compliance test of the module output in long mode and far-end compliance test in either mode, the signal measured at TP4 is first convolved with an emulated loss channel (see Table 25-8) that represents the additional loss present in a maximum loss channel including 1.5 dB package loss. The loss channel is a host trace as defined in Section 16.3.10.1.1 using Equation (16-4) to Equation (16-9) with the transmission line parameters listed in Table 16-7 except that Z_p is given in Table 25-8. The response of these channels are illustrated in Figure 25-15. Any reference receiver equalizer

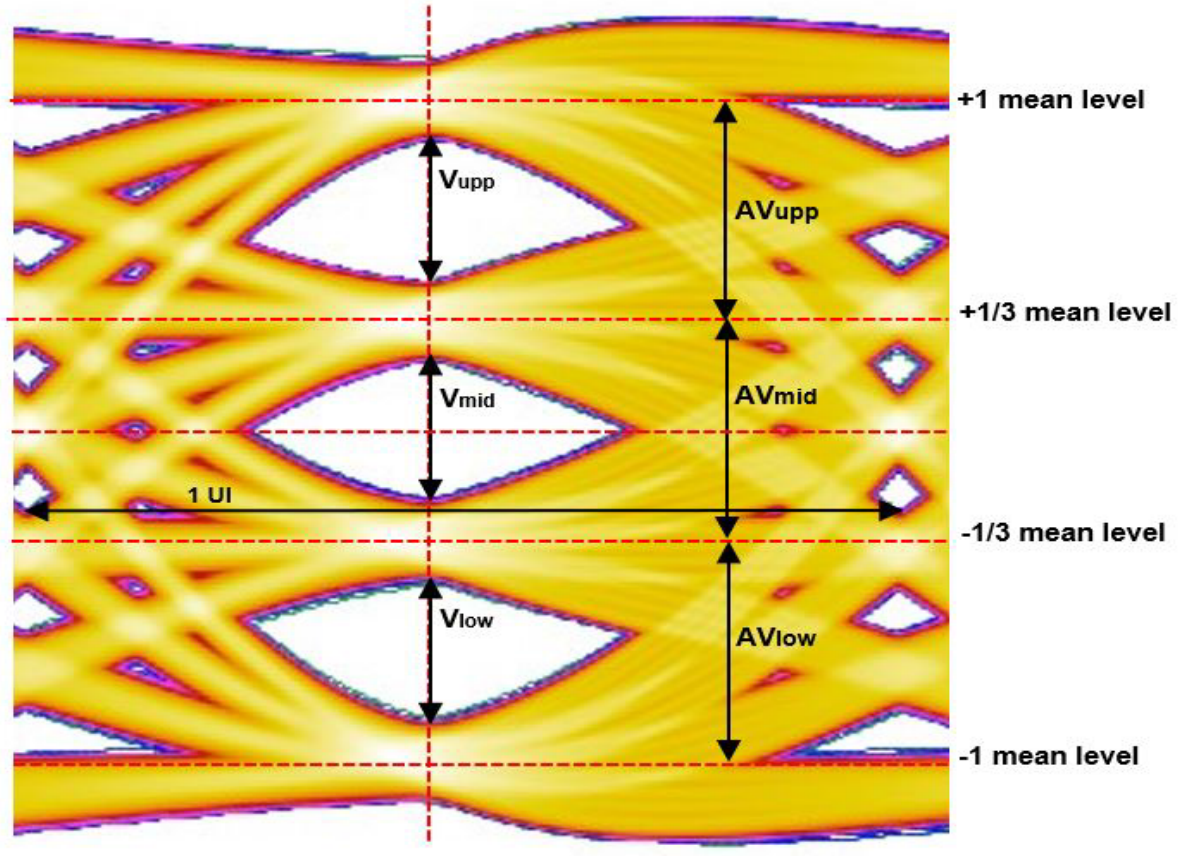
setting listed in Table 25-10 and Table 25-12 for short or long mode, as applicable, that meets both the VEC and Eye Height requirements defined for near-end or far-end TP4 in Table 25-4, as applicable, is acceptable.

-For TP1a compliance test the reference receiver equalization shall be set to one of the values in Table 25-10 and one of the settings in Table 25-12. Any reference receiver equalization setting listed in Table 25-10 and Table 25-12 for TP1a that meets the Eye Height and VEC requirements defined for TP1a in Table 25-1 is acceptable. Eye Height and VEC have the same meaning as in the previous paragraph.

4) At TP1a, passing is defined as at least one reference receiver equalizer setting that meets the Eye Height, VEC specifications defined in Table 25-1 for the lower, upper and middle eyes. At TP4, for each of the short and long module output modes, passing is defined as at least one equalizer setting that meets the near-end Eye Height and VEC specifications given in Table 25-4 and at least one potentially different equalizer setting that meets the far-end Eye Height and VEC specifications given in Table 25-4.

25.3.11.2 Measured PAM4 Eye Parameter Definitions

Figure 25-6. TP1a and TP4 Eye Height and Vertical Eye Closure (VEC)



All the relevant PAM4 eye parameters are based on 10^{-6} probability (see Figure 25-6 and Figure 25-7). The voltage measurements include all samples within the windows used to create the CDF. The CDF is computed with the probability for each sample weighted by the function w(t) according to the following steps and as defined by Equation (25-3) to Equation (25-7).

Perform the following step once:

Capture the PRBS13-CEI signal $\boldsymbol{y_1}(k)$ with the effect of low-pass response equivalent to the specified receiver noise filter with associated parameter f_r in Table 25-14, and using a clock recovery unit with a corner frequency of $f_b/13280$ Hz and slope of 20 dB/decade. The capture includes a minimum of 3 samples per symbol, or equivalent. Collect sufficient samples equivalent to at least 1.2 million PAM4 symbols to allow for construction of a normalized cumulative distribution function (CDF) to a probability of 10^{-6} without extrapolation.

Perform the following steps for each valid combination of g_{DC} and g_{DC2} as specified in Table 25-10:

1. Compute the response $\boldsymbol{y_2}(k)$ by applying the effect of the continuous time filter to $\boldsymbol{y_1}(k)$ using the associated parameters in Table 25-10.
2. Compute the linear fit pulse response $\boldsymbol{p2}(k)$ using the method defined in IEEE Std 802.3ck [29], Section 162.9.4.1.1 with parameter M (see [29]) the same as for Step 1, Dp equal to 3, and Np equal to 200.
3. Compute the DFE sampling phase t_s and tap weights $\boldsymbol{b}(n)$ for $\boldsymbol{p2}(k)$ according to the methodology in Annex 93.A.1.6 of IEEE Std 802.3ck [29] using the associated parameters in Table 25-10. This is illustrated in Section 25.3.11.2.1.
4. Compute the signal after the DFE $\boldsymbol{y_{rx}}(k)$ by applying the effect of the DFE to $\boldsymbol{y_2}(k)$ using the sampling phase t_s and tap weights $\boldsymbol{b}(n)$ determined in the previous step.
5. Compute the variance of the noise at the output of the receive equalizer based on the one-sided spectral density eta0 given in Section 25.3.11.4, referred to the receiver noise filter input per IEEE Std 802.3ck [29], Annex 93.A.1.6, Equation 93A-35.
6. Compute an eye diagram from $\boldsymbol{y_{rx}}(k)$, including the effect of Gaussian noise with variance calculated in the previous step, but taking into account that some noise from the measurement instrument is already in $\boldsymbol{y_{rx}}(k)$.
7. Compute Vmid, Vupp, Vlow from the eye diagram using Section 25.3.11.2.2 steps 1) through 6) with the probability for each sample weighted by the function w(t) defined by Equation (25-3). As an example, UPPCDF1 may be calculated using Equation (25-5) from a set of N samples $\{v_i, t_i\}$.
8. The eye height is the minimum of Vmid, Vupp, and Vlow.
9. Compute VEC using Equation (16-15) and the values computed in Step 8 with the exception that +1, +1/3, -1/3, -1 mean levels are the average values over the time interval $t_s \pm 0.05$ UI instead of “within 0.025 UI of time TCmid”.

The values of Eye Height and VEC are the values obtained with the combination of g_{DC} and g_{DC2} that produces the minimum value of VEC where eye height also complies with the specification for eye height (min) as specified for the interface.

$$w(t) = \begin{cases} \frac{1}{\sqrt{2\pi}\sigma_r}\exp\left(-\frac{1}{2}\left(\frac{x(t)}{\sigma_r}\right)^2\right) & |x(t)| \le 0.05 \\ 0 & |x(t)| > 0.05 \end{cases} \quad (25\text{-}3)$$

$$x(t) = (t - t_s)f_b \quad (25\text{-}4)$$

$$UPPCDF1(v) = \frac{1}{A}\sum_{i=1}^{N} w(t_i)u(v_i, VCupp, v) \quad (25\text{-}5)$$

$$u(x, a, b) = \begin{cases} 1 & a \le x \le b \\ 0 & \text{otherwise} \end{cases} \quad (25\text{-}6)$$

$$A = \sum_{i=1}^{N} w(t_i) \quad (25\text{-}7)$$

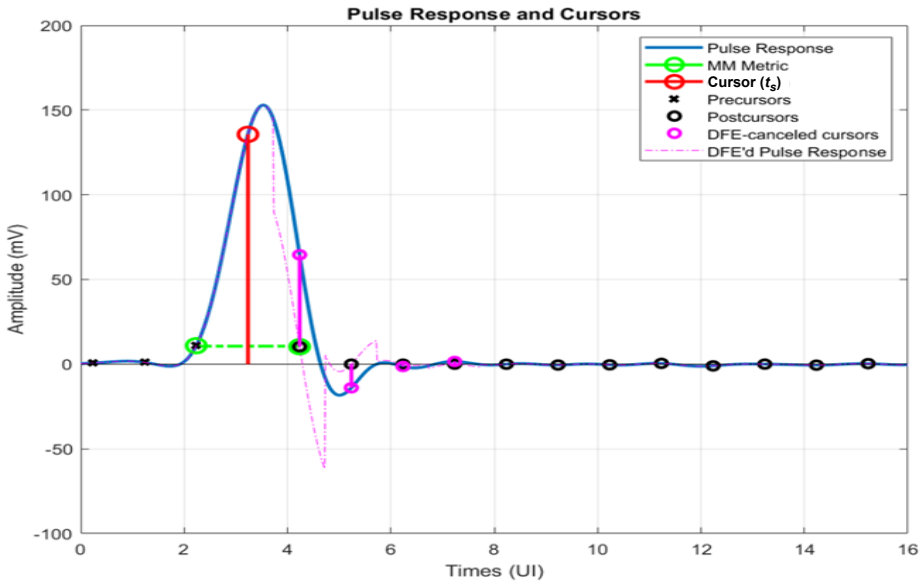
where:

$w(t)$	is the weighting function
$x(t)$	is the deviation from the sampling time t_s in UI
σ_r	is the standard deviation in UI and is equal to 0.02 UI
f_b	is the signaling rate in Hz
t	is time in seconds
A	is a factor to normalize the weighting function over the sample set

25.3.11.2.1 Method for finding the sampling phase t_s

The approach described in this clause is based upon first locating t_s, the time that satisfies the Mueller-Müller equation (Annex 93.A.1.6 of IEEE Std 802.3 [27], Equation (93A-25) with parameters determined in IEEE Std 802.3ck [29]).

Figure 25-7. Visualization of t_s in Mueller-Müller equation



25.3.11.2.2 Definitions of Vmid, Vupp, Vlow, AVmid, Avupp and Vlow

1. Vmid - the 10^{-6} inner Eye Height of the middle eye determined from voltage CDFs in a ± 0.05 UI time window centered on t_s

2. Vupp - the 10^{-6} inner Eye Height of the upper eye determined from voltage CDFs in a ± 0.05 UI time window centered on t_s

3. Vlow - the 10^{-6} inner Eye Height of the lower eye determined from voltage CDFs in a ± 0.05 UI time window centered on t_s

4. AVmid, the Eye Amplitude of the middle eye, is the difference of the mean levels of the +1/3 level and -1/3 level voltage histograms in a ± 0.05 UI time window centered on t_s

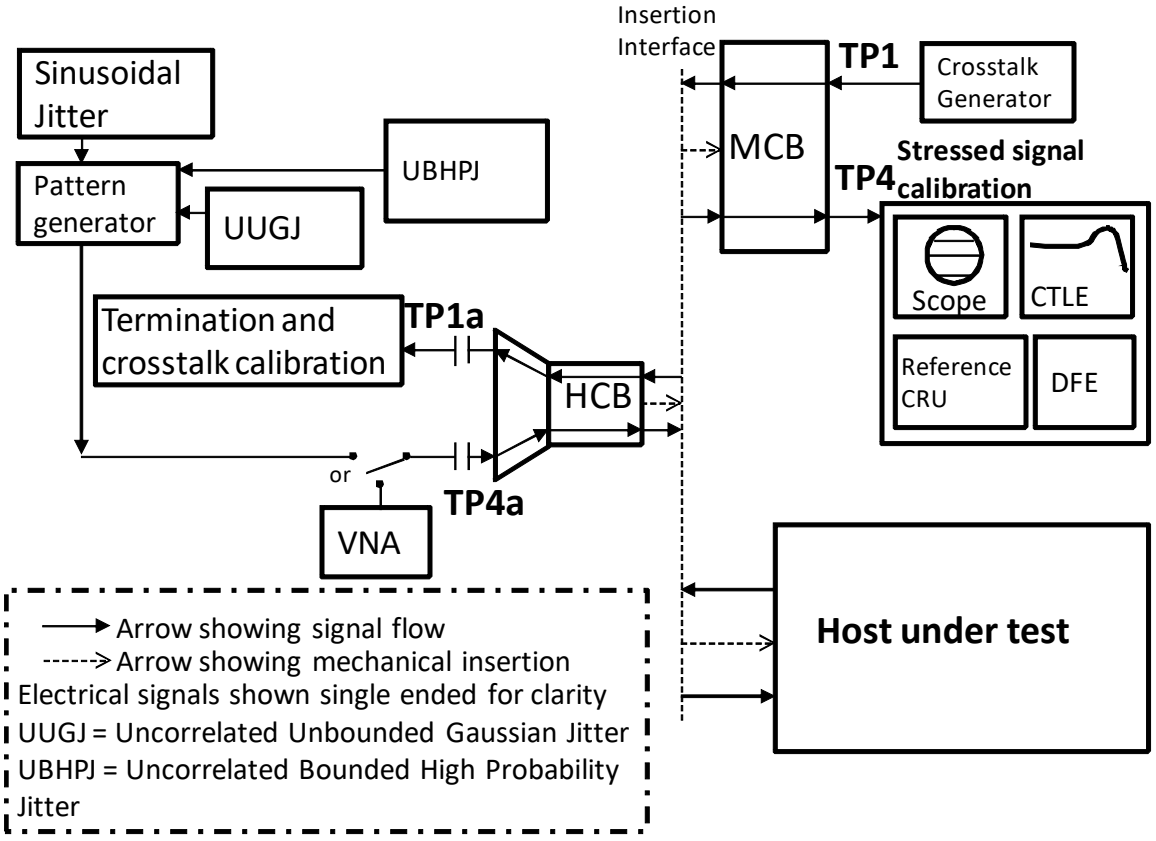
5. AVupp, the Eye Amplitude of the upper eye, is the difference of the mean levels of the +1 level and +1/3 level voltage histograms in a ± 0.05 UI time window centered on t_s

6. AVlow, the Eye Amplitude of the lower eye, is the difference of the mean levels of the -1/3 level and -1 level voltage histograms in a ± 0.05 UI time window centered on t_s

25.3.11.3 Host and Module stressed input test

The ability of the host input to tolerate the Eye Height and VEC specified in Table 25-4 and the sinusoidal jitter specified in Table 25-9 is tested using a stressed input test. There are two stressed signals, representing a worst compliant module in short and long output modes. The host chooses which of the two settings it is tested with. Each test signal is applied at TP4a of Figure 25-1 and calibrated at TP4, using a Host Compliance Board and Module Compliance Board specified in Section 25.4.1 The test setup is shown in Figure 25-8. The UBHPJ block is used to create non-compensable DJ in addition to sinusoidal jitter.

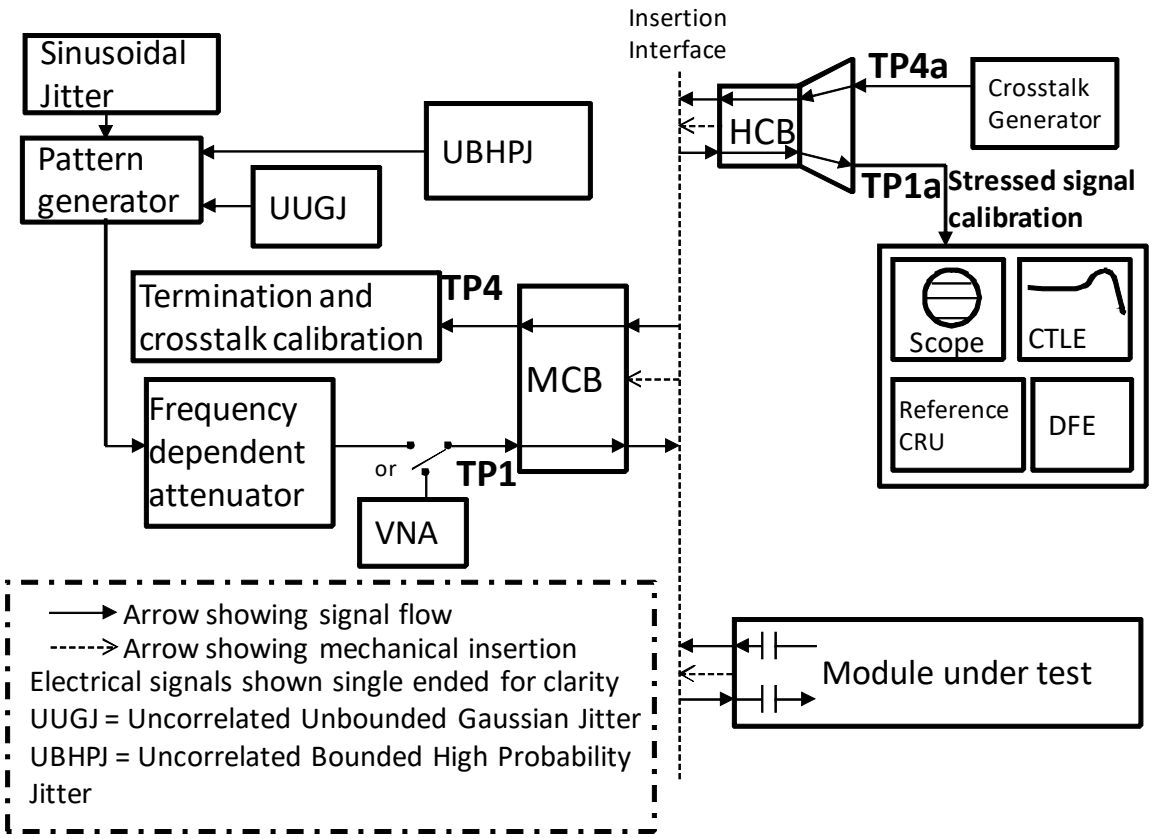
Figure 25-8. Host input test setup



The ability of the module input to tolerate the Eye Height and VEC specified in Table 25-1 and the sinusoidal jitter specified in Table 25-9 is tested using a stressed input test. The test signal is applied at TP1 of Figure 25-1, and calibrated at TP1a using a Host Compliance Board and Module Compliance Board specified in Section 25.4.1. The test setup is shown in Figure 25-9. The module stressed input test represents the worst case high loss host. Modules are also expected to operate at the BER specified in Section 25.1 when presented with lower loss channels that require different equalization settings as long as the signal complies with the specifications in Table 25-1. The module input shall tolerate these various channels in an autonomous manner

with no recommended equalization settings being provided by the host. The host may provide the module with a recommended CTLE peaking value as a starting point for optimizing input equalization.

Figure 25-9. Module input test setup



25.3.11.3.1 Host (TP4a) and Module (TP1) stressed input test method

The host and module input shall tolerate sinusoidal jitter with the frequency and amplitude defined by the mask of Figure 25-10 and Table 25-9. This sinusoidal jitter is part of the jitter applied in the stressed input test. The sinusoidal jitter is calibrated at 10x the reference CRU's bandwidth. f_{CRU} is the jitter corner frequency given by $f_b/13280$.

The reference CRU and reference receiver as defined in Section 25.3.11.4 are used to calibrate the stressed input test signal at TP4 (per Table 25-4) or TP1a (per Table 25-1) using a QPRBS13-CEI pattern. The pattern is changed to QPRBS31-CEI for the stressed input test.

The crosstalk source is asynchronous to the main pattern generator. The amplitude and rise/fall time of the crosstalk source are given in Table 25-3 and Table 25-6. The crosstalk signal is calibrated at TP4 or TP1a using a QPRBS13-CEI pattern, then the

pattern is changed to QPRBS31-CEI for the test. For multi-lane implementations additional lanes shall be active with either uncorrelated QPRBS31-CEI or QPRBS13-CEI patterns or valid CEI signals, using the above calibration methods.

Figure 25-10. Host input and Module input Sinusoidal Jitter

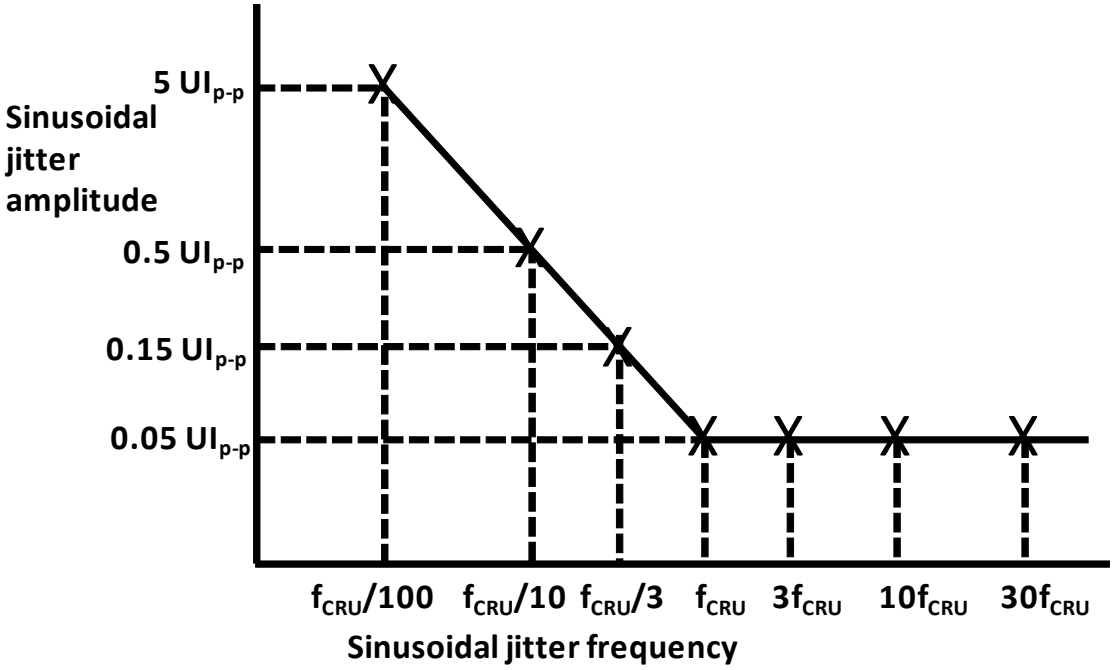


Table 25-9. Sinusoidal jitter frequency for TP4 and TP1a testing

Frequency	Sinusoidal jitter, peak-to-peak (UI)
$f_{CRU}/100$	5
$f_{CRU}/10$	0.5
$f_{CRU}/3$	0.15
f_{CRU}	0.05
$3f_{CRU}$	0.05
$10f_{CRU}$	0.05
$30f_{CRU}$	0.05

25.3.11.3.1.1 Host input test signal calibration

The host input is tested at TP4a of Figure 25-1 using a Host Compliance Board as defined in Section 25.4.1. The host input test setup is shown in Figure 25-8.

1. The functional model for the pattern generator is a 3-tap FIR with two precursor taps and tap spacing of 1 UI. With the precursor taps set to zero, UBHPJ, UUGJ and sinusoidal jitter are added to a clean test pattern until the jitter (except for EOJ) at the output of the pattern generator approximates the informative transmit recommendations given in Appendix 25.C.
2. With the crosstalk generator calibrated to meet the specifications in Table 25-6, the far-end Eye Height and far-end VEC at TP4 are measured using the reference receiver defined in Section 25.3.11.4 with the optimal receiver equalizer settings and the methodology defined in Section 25.3.11.1.
3. The pattern generator FIR is adjusted to minimize far-end VEC. UUGJ is adjusted to give the maximum far-end VEC specified for the module output in Table 25-4. The pattern generator amplitude is adjusted to give the minimum far-end Eye Height specified for the module output in Table 25-4. The procedure of this Step 3 is iterated as necessary.

This calibrated signal must also equal or exceed the near-end Eye Height and near-end VEC in Table 25-4 measured using the reference receiver defined in Section 25.3.11.4 with at least one of the reference receiver settings allowed for near-end eye measurement.

25.3.11.3.1.2 Module input test signal calibration

The module input is tested at TP1 of Figure 25-1 using a Module Compliance Board as defined in Section 25.4.1. The module input test setup is shown in Figure 25-9.

The functional model for the pattern generator is a 3-tap FIR with two precursor taps and tap spacing of 1 UI. With the precursor taps set to zero, UBHPJ, UUGJ and sinusoidal jitter are added to a clean test pattern until the jitter (except for EOJ) at the output of the pattern generator approximates the informative transmit recommendations given in Appendix 25.C.

The frequency-dependent attenuator is intended to represent the host channel and package. The frequency-dependent attenuator may be implemented with PCB traces. The frequency-dependent attenuation is added such that the loss at Nyquist from the output of the pattern generator to TP1a is consistent with Appendix 25.A that is 16 dB (worst case host channel insertion loss) plus an additional allowance of 2.2 dB allocated for the difference between the host Tx package loss and the equivalent loss in the pattern generator. The complete path from the output of the pattern generator to TP1a should also meet the return loss specifications given for the mated HCB and MCB (see Section 25.4.1 and 13.4.1.2). The crosstalk generator is calibrated to meet the specifications in Table 25-3. The Eye Height and VEC at TP1a are measured using the reference receiver (defined in Section 25.3.11.4) with the reference receiver equalizer setting and the methodology defined in Section 25.3.11.1. The reference

receiver equalizer setting is based on pattern generator and receiver settings meeting the minimum VEC specification that also passes the Eye Height specification. UUGJ and the pattern generator FIR, PAM4 levels and amplitude are adjusted in the manner of 25.3.11.3.1.1 to the specifications of Table 25-1. The optimum CTLE setting for a correctly calibrated signal is such that g_{DC} + g_{DC2} is less than or equal to -10.5 dB.

25.3.11.4 Reference receiver

The waveform is observed through a reference receiver which includes receiver input referred noise eta0 of 4.1x10^{-8} V^2/GHz, a fourth-order Butterworth filter with a bandwidth of 0.75f_b concatenated with a continuous time linear equalizer (CTLE) and 4-tap Decision Feedback Equalizer (DFE). The filters may be implemented in software; however, the signal is not averaged. The reference receiver provides a standardized way of assessing a signal and is not intended to impose constraints on the design of product inputs.The CTLE is defined by Equation (25-8),

$$H_{ctf}(f) = \frac{\left(10^{\frac{g_{DC}}{20}} + j\frac{f}{f_z}\right)\left(10^{\frac{g_{DC2}}{20}} + j\frac{f}{f_{LF}}\right)}{\left(1 + j\frac{f}{f_{p1}}\right)\left(1 + j\frac{f}{f_{p2}}\right)\left(1 + j\frac{f}{f_{LF}}\right)} \quad (25\text{-}8)$$

where:

g_{DC}+ g_{DC2} is the low-frequency gain,

f_{p1}, f_{p2} and f_{LF} are the frequencies of the CTLE poles,

f_z along with g_{DC} determine the high frequency zero,

f_{LF} along with g_{DC2} determine the low frequency zero of the CTLE.

The values of f_{p1}, f_{p2}, f_z, f_{LF} shall be implemented according Table 25-11. Figure 25-11 shows the CTLE response of the reference CTLE with 0 dB of low frequency gain for a baud rate of 50 GBd with g_{DC} = 2 dB to 12 dB in 1 dB steps, g_{DC2} = 0 dB and f_{p1}, f_{p2}, f_z, f_{LF} as listed in Table 25-10 and Table 25-11. Figure 25-12 shows the frequency response of the reference CTLE used for module far-end and host output testing for a baud rate of 50 GBd with values for g_{DC} = 12 dB, g_{DC2} = 0 dB to 3 dB in 0.5 dB steps and f_{p1}, f_{p2}, f_z, f_{LF} as listed in Table 25-10 and Table 25-11. Figure 25-13 and Figure 25-14 show the frequency response of the reference CTLE used for the module near-end and far-end, respectively, output testing for a baud rate of 50 GBd with values for g_{DC}, g_{DC2}, f_{p1}, f_{p2}, f_z, f_{LF} as listed in Table 25-10 and Table 25-11. The CTLE peaking value is the approximate difference between the low-frequency response (1 MHz) and the maximum high-frequency response in dB.

Table 25-10. CTLE Low-frequency Gain Range

g_{DC2}	g_{DC}		Location
	max.	min.	
0	0	-5	Short
-1	-2	-5	Short
-2	-4	-4	Short
0	-8	-12	Long
-1	-7	-11	Long
-2	-6	-10	Long
-3	-5	-9	Long
0	-2	-11	TP1a
-1	-2	-11	TP1a
-2	-4	-10	TP1a
-3	-4	-9	TP1a
Note: For non-integer values of g_{DC2} round down to nearest whole value except that for TP1a values of g_{DC2} greater than -3dB the value should be rounded up to the nearest whole value.			

Table 25-11. Reference CTLE Poles and Zeros

Parameter	Value
f_{p1}	f_b / 1.8839
f_{p2}	f_b
f_z	f_b / 2.862
f_{LF}	f_b / 40

Figure 25-11. Host output reference CTLE transfer function for 2 to 12 dB of high frequency gain and 0 dB of low frequency gain at 50 Gsym/s

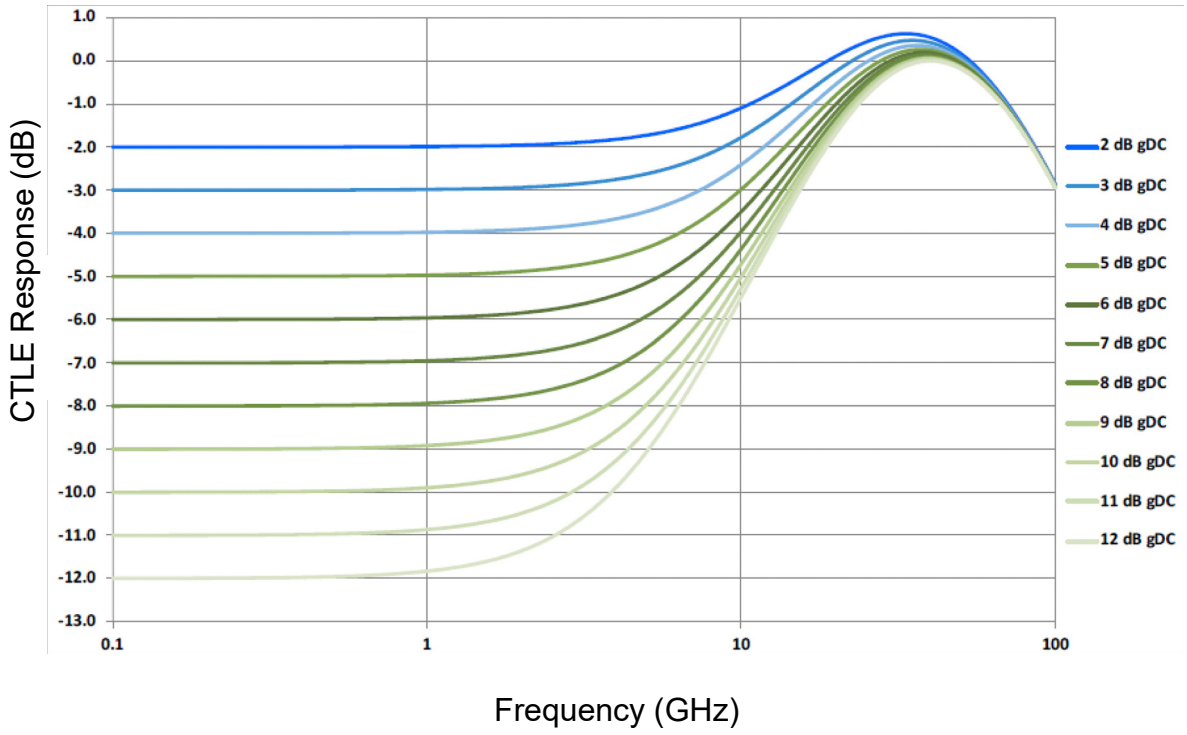


Figure 25-12. Host output reference CTLE transfer function for 12 dB of high frequency gain and 0 dB to 2.5 dB of low frequency gain at 50 Gsym/s

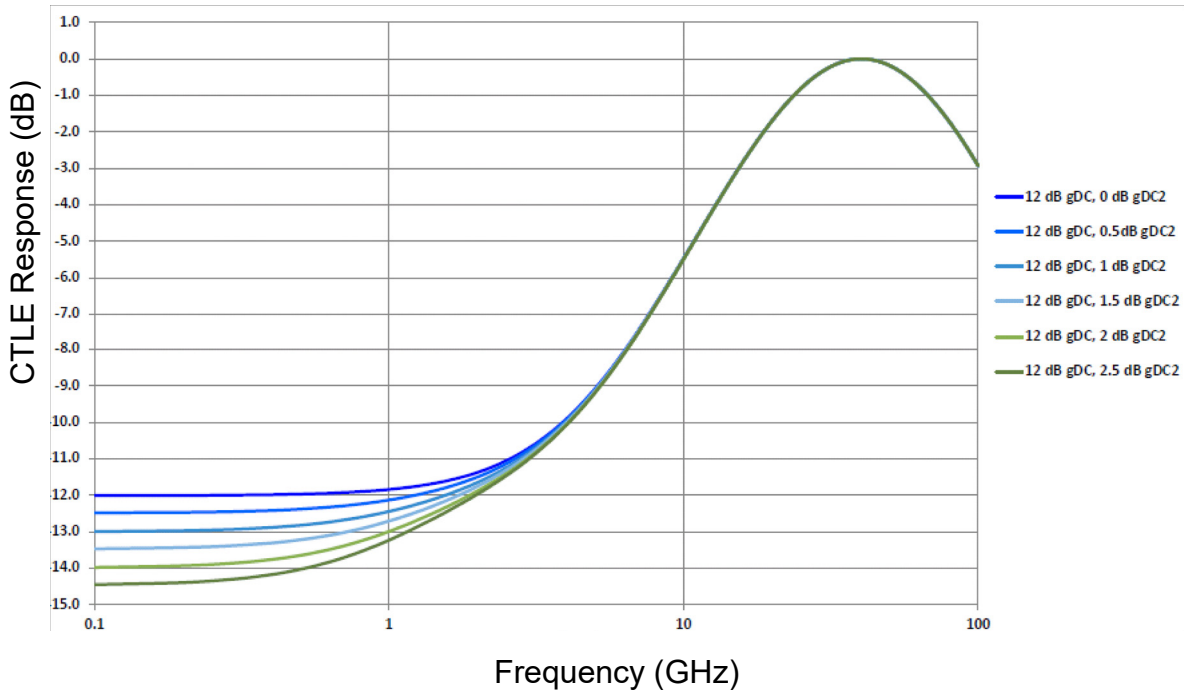


Figure 25-13. Module near-end output reference CTLE transfer function for 2 dB to 5 dB of high frequency gain and 0 dB of low frequency gain at 50 Gsym/s

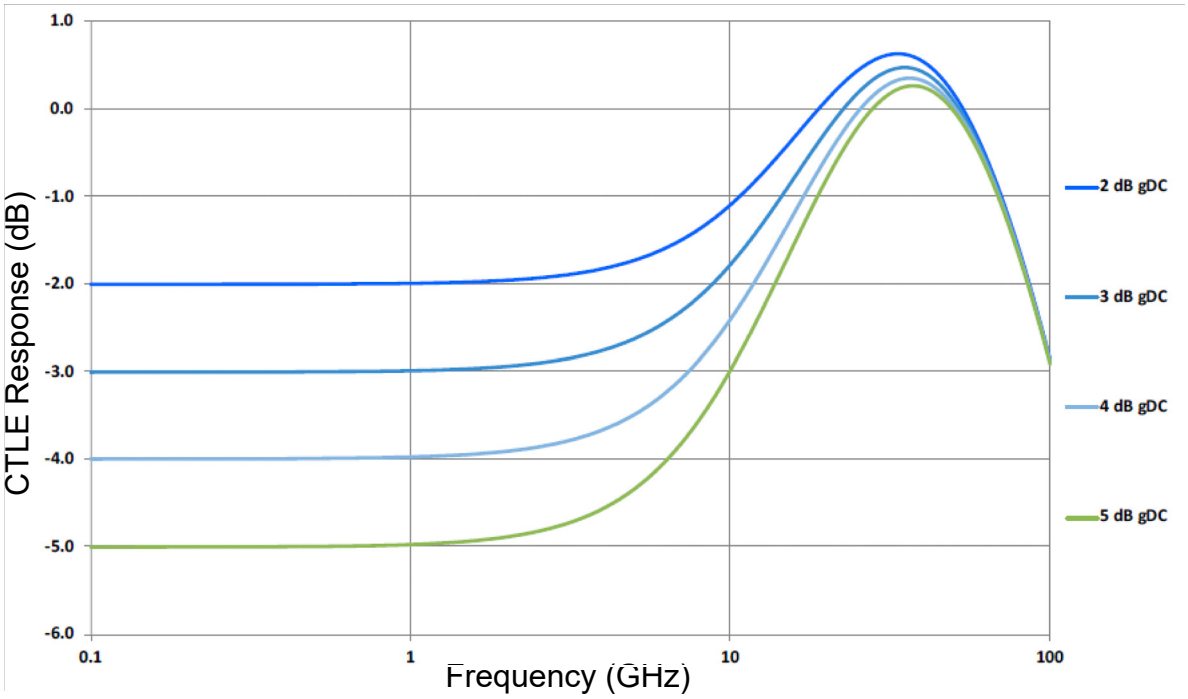
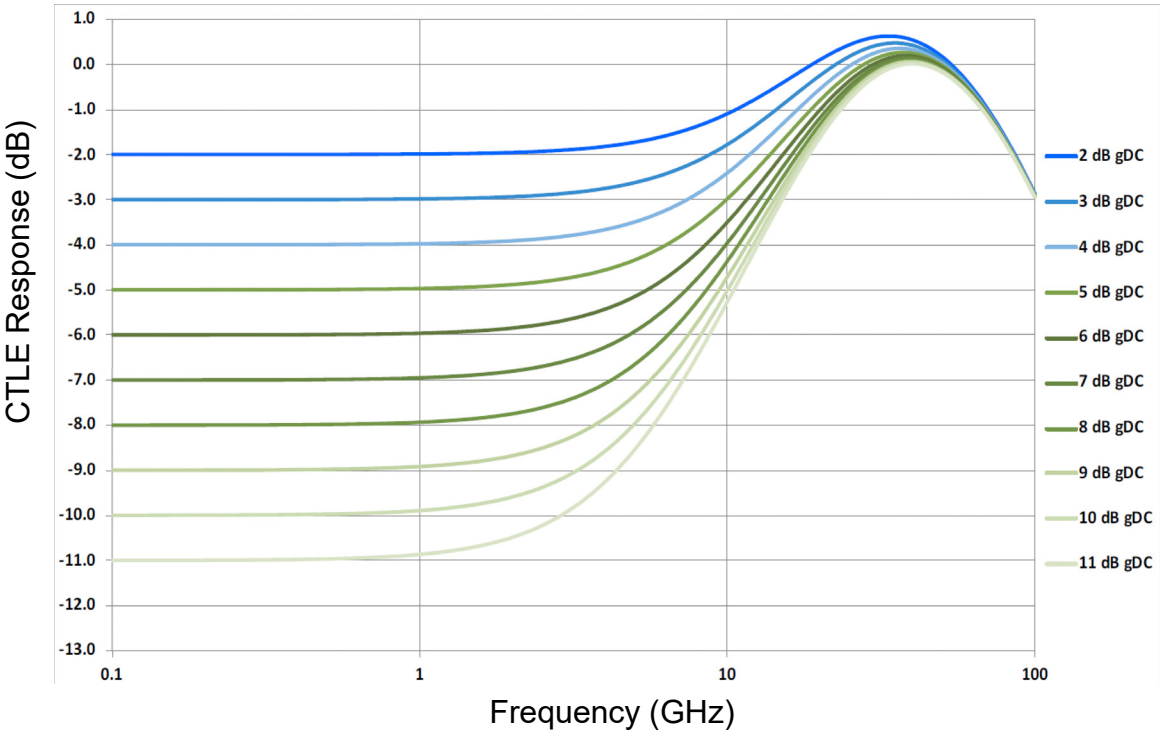


Figure 25-14. Module output far-end reference CTLE transfer function for 11 dB of high frequency gain and 0 dB of low frequency gain at 50 Gsym/s



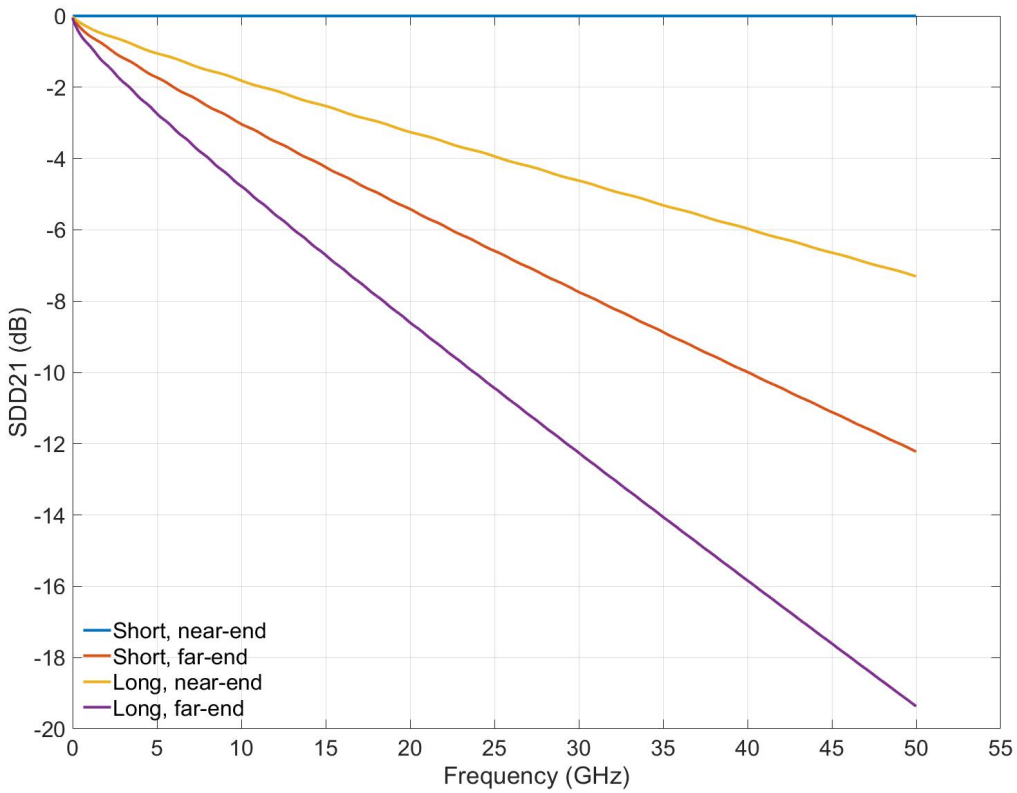
The reference DFE is a four-tap DFE with taps b1, b2, b3 and b4. The DFE tap weight ranges are defined in Table 25-12. Please note that the actual device implementation is allowed to deviate from these values.

Table 25-12. 4-tap Reference DFE Characteristics

Parameter	Min Value	Max Value
Range of b1 tap	0.1	0.4
Range of b2 and b3 taps	-0.1	0.15
Range of b4 tap	-0.05	0.1

TP4 module output tests use emulated host channels specified by Table 25-8 and illustrated in Figure 25-15. See Section 25.3.11.1.1.

Figure 25-15. TP4 far-end Host Channel SDD21 for f_b= 58 GHz



25.3.12 Input Overload Voltage Tolerance

The input voltage tolerance tests the acceptance of differential input peak-peak amplitudes produced by the extremes of operation from the host output (for host-to-module communication) or module output (for module-to-host communication).

The maximum voltage at an IC input can be larger than the maximum at the compliance point due to output/input impedances and reflections.

The input overload voltage tolerance specification is to be met for any valid CEI pattern. The differential voltage specified in Table 25-1 is somewhat smaller than the module input voltage tolerance due to host loss and the QPRBS13-CEI's pattern length.

25.4 Compliance Boards

25.4.1 Compliance Boards and measurement points

Use of compliance boards for testing is assumed for the parameters defined in Table 25-1 through Table 25-6. Figure 25-1 shows the test setup for making S-parameter measurements of the mated compliance boards. The test results for test and calibration at TP1a should be corrected for any deviations between the Host Compliance Board's loss and the Host Compliance Board's reference loss. The test results for test and calibration at TP4 should be corrected for any deviations between the mated compliance board loss minus the Host Compliance Board's loss and the mated compliance board reference loss minus the Host Compliance Board's reference loss. If the compliance boards do not meet the specified S-parameters, the test results should be corrected for the difference. The requirements in this section are not connector specifications for a CEI-112G-VSR-PAM4 product design.

25.4.1.1 HCB and MCB reference trace insertion loss

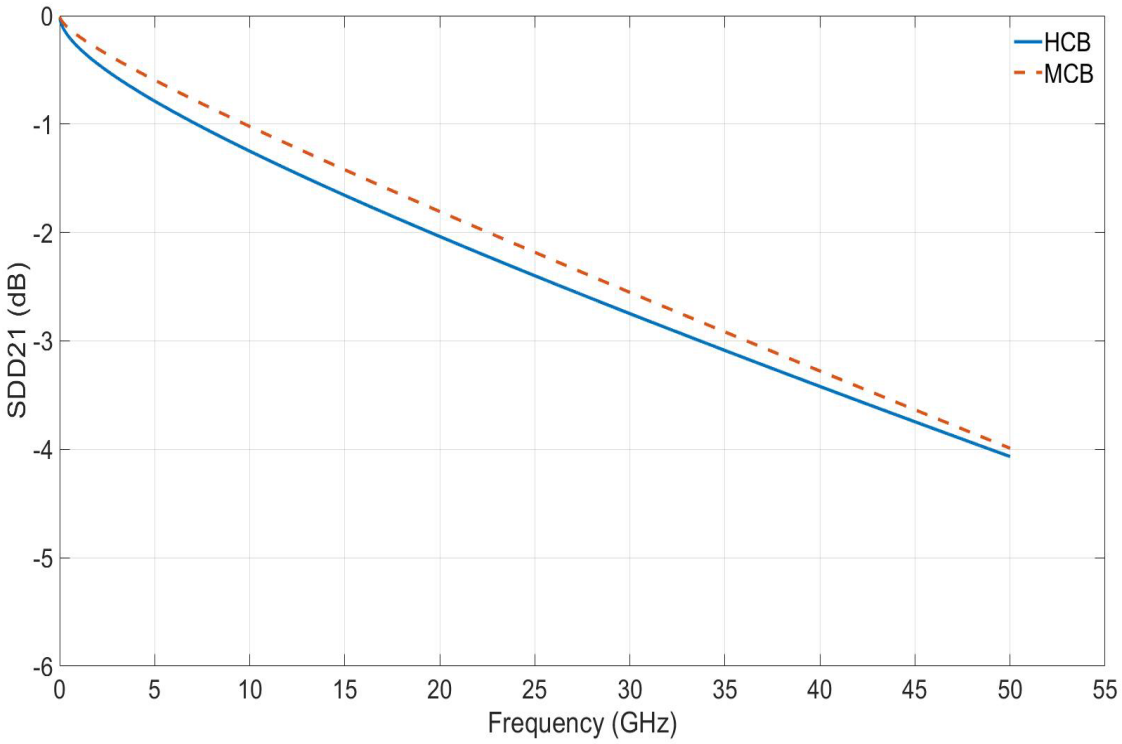
The reference differential insertion loss of the HCB printed circuit board trace follows Equation (25-9). The reference differential insertion loss of the MCB printed circuit board trace follows Equation (25-10). Both the HCB and MCB equations are illustrated in Figure 25-16 below.

$$\text{HCB ref SDD21} = 1.00*(0.001 - 0.250*\sqrt{f} - 0.046*f)\ \text{dB} \quad (25\text{-}9)$$

$$\text{MCB ref SDD21} = 1.34*(0.001 - 0.096*\sqrt{f} - 0.046*f)\ \text{dB} \quad (25\text{-}10)$$

for 0.001 GHz< f < 50 GHz

Figure 25-16. Reference Differential Insertion Losses of HCB and MCB traces



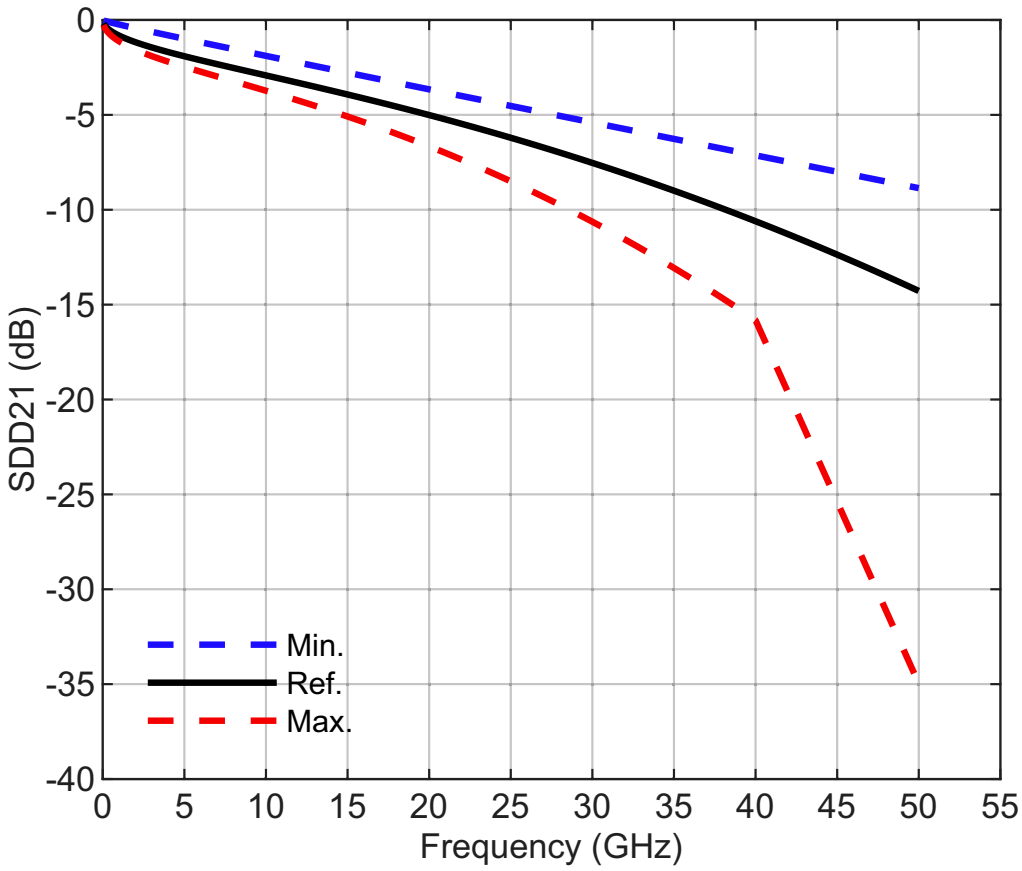
25.4.1.2 Mated HCB and MCB S-parameters

The specifications given for the HCB and MCB S-parameters apply in both directions. (exception being differential insertion loss can be in either direction)

25.4.1.2.1 Mated HCB and MCB Insertion loss

The minimum differential insertion loss and mated insertion loss for a mated HCB and MCB is given in Equation (25-11). The maximum differential insertion loss for a mated HCB and MCB pair is given in Equation (25-12). The reference mated MCB-HCB loss is given in Equation (25-13) and Equation (25-14). The minimum, maximum and reference insertion loss are all shown in Figure 25-17 below.

Figure 25-17. Mated HCB-MCB Differential Insertion Loss



$$\text{Min mated HCB-MCB SDD21, SDD12} < -1.0225(0.0656\sqrt{f} + 0.164f) \text{ dB} \quad \text{(25-11)}$$

$$\text{Ref mated HCB-MCB SDD21, SDD12} = -0.8153\sqrt{f} - 0.003405f^2 \text{ dB} \quad \text{(25-12)}$$

for 0.05 GHz ≤ *f* ≤ 50 GHz, where *f* is frequency in GHz.

$$\text{Max mated HCB-MCB SDD21, SDD12} > -1.185\sqrt{f} + 0.072f - 0.007f^2 \text{ dB} \quad \text{(25-13)}$$

for 0.05 GHz ≤ *f* < 40 GHz

$$\text{Max mated HCB-MCB SDD21, SDD12} > 60.78 - 1.915f \text{ dB} \quad \text{(25-14)}$$

for 40 GHz ≤ *f* ≤ 50 GHz-

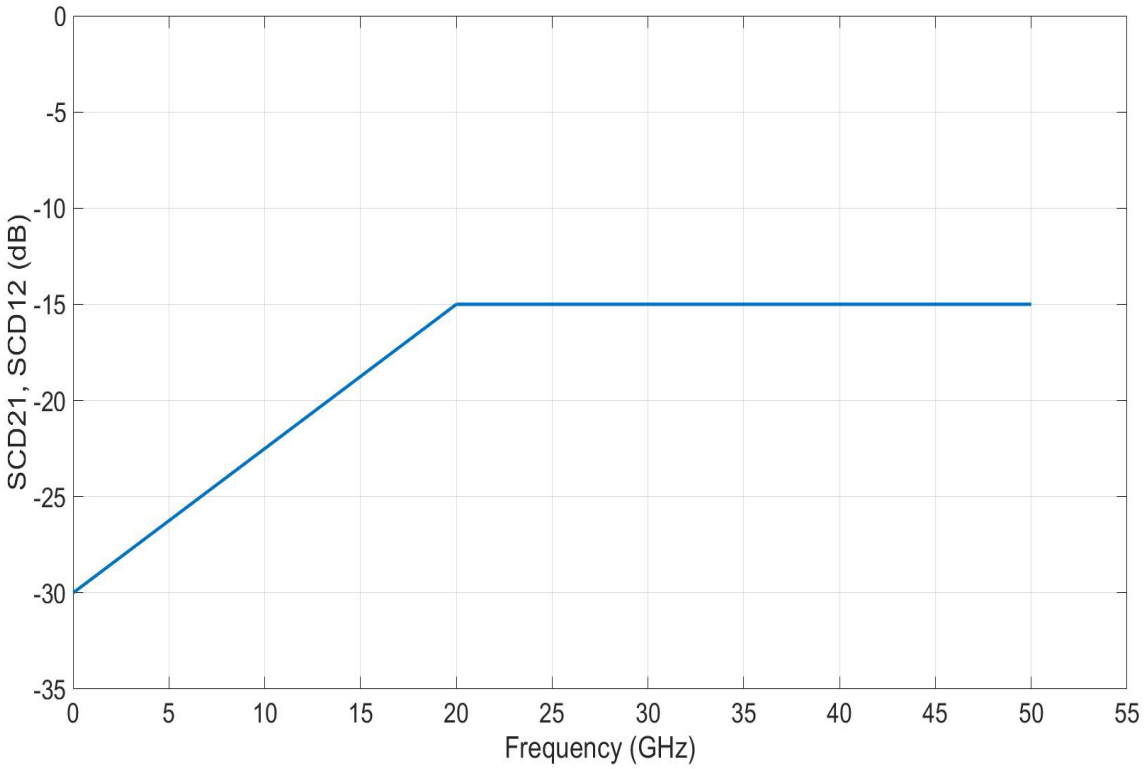
25.4.1.2.2 Mated HCB and MCB Effective Return Loss (ERL)

The Effective Return Loss of the mated HCB and MCB pair shall be calculated using the method shown in IEEE Std 802.3 [27] clause 93A.5 as modified by IEEE Std 802.3ck [29] using the specifications in Table 25-7. The minimum ERL for mated MCB-HCB shall be 10.3 dB.

25.4.1.2.3 Differential to Common Mode Conversion

The differential to common mode conversion for a mated HCB and MCB pair is given in Equation (25-15) and shown in Figure 25-18 below. Note that SCD and SDC should be the same.

Figure 25-18. Mated HCB-MCB SCD21, SCD12



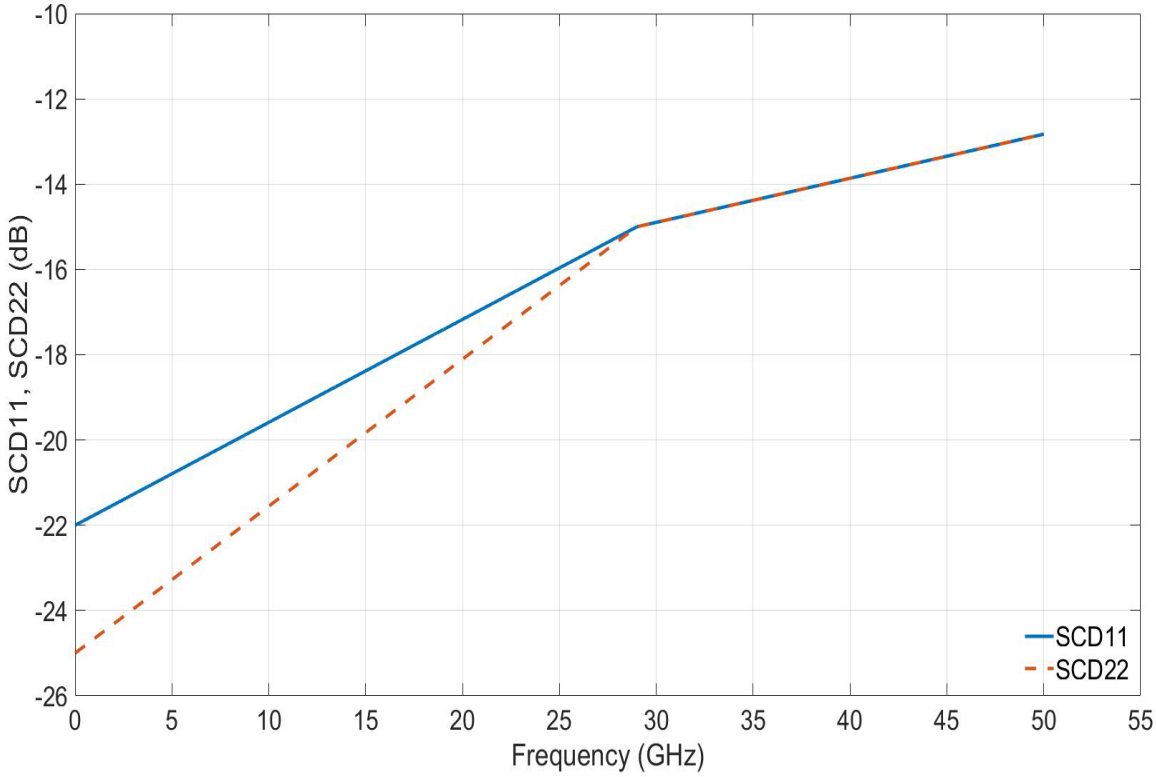
$$\text{Mated HCB–MCB SCD21, SCD12} \le -30 + \frac{21}{28} f \text{ dB} \quad \text{for } 0.05 \text{ GHz} \le f < 20 \text{ GHz} \tag{25-15}$$

$$\text{Mated HCB–MCB SCD21, SCD12} \le -15 \text{ dB} \quad \text{for } 20 \text{ GHz} \le f \le 50 \text{GHz}$$

25.4.1.2.4 Differential to Common Mode (SCD11) and Common Mode to Differential (SCD22) Return Loss

The differential to common mode (SCD11) and Commom Mode to Differential (SDC22) return loss for a mated HCB and MCB pair is given in Equation (25-16) and shown in Figure 25-19 below.

Figure 25-19. Mated HCB-MCB SCD11, SCD22



$$\text{Mated HCB–MCB SCD11} \quad \leq -22 + \frac{1}{4} f \text{ dB}$$

$$\text{Mated HCB–MCB SCD22} \quad \leq -25 + \frac{5}{14} f \text{ dB} \qquad \text{(25-16)}$$

for 0.05 GHz ≤ f < 28 GHz

$$\text{Mated HCB–MCB SCD11, SCD22} \leq -18 + \frac{3}{28} f \text{ dB}$$

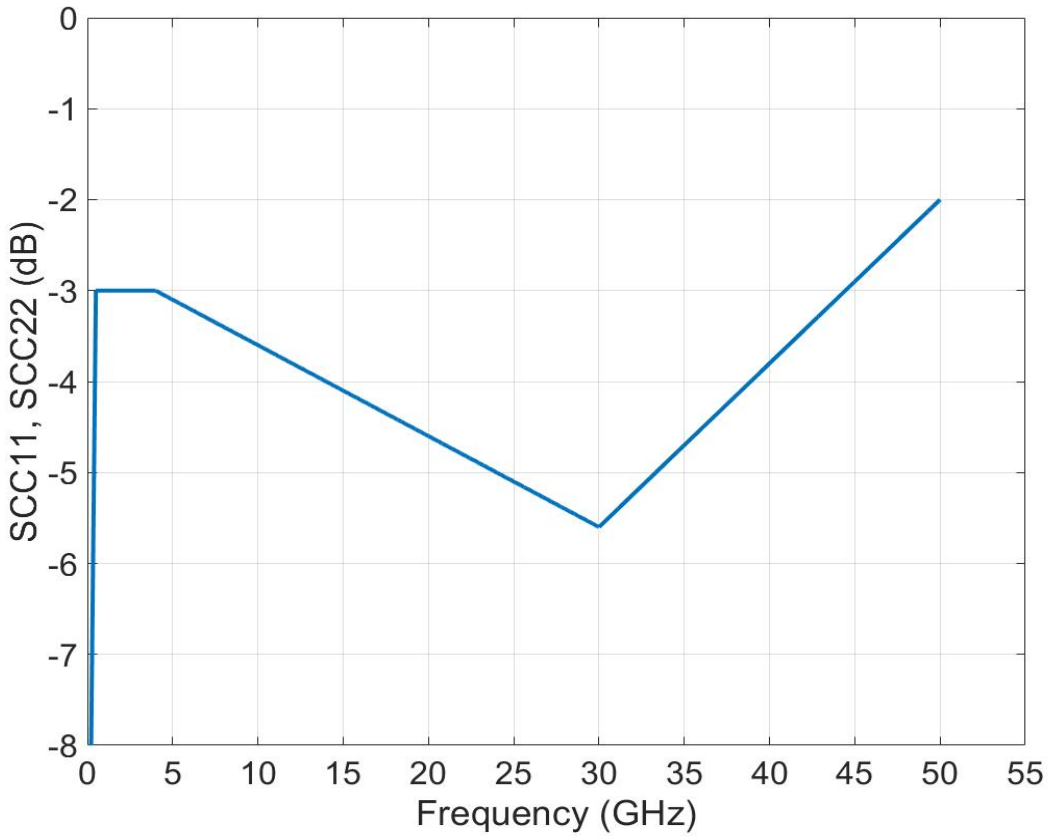
for 28 GHz ≤ f ≤ 50 GHz

Where port 2 is TP1a and TP4, port 1 is TP1 and TP4a

25.4.1.2.5 Common Mode Return Loss

The maximum common mode return loss for a mated HCB-MCB pair is given in Equation (25-17) and shown in Figure 25-20 below.

Figure 25-20. Mated HCB-MCB SCC11, SCC22



$$\begin{aligned}
&\text{HCB-MCB SCC11 and SCC22} \le -12 + 18f \text{ dB} && \text{for } 0.05\text{ GHz} \le f < 0.5\text{ GHz} \\
&\text{HCB-MCB SCC11 and SCC22} \le -3 \text{ dB} && \text{for } 0.5\text{ GHz} \le f < 4\text{ GHz} \\
&\text{HCB-MCB SCC11 and SCC22} \le -2.6 - 0.1f \text{ dB} && \text{for } 4\text{ GHz} \le f < 30\text{ GHz} \\
&\text{HCB-MCB SCC11 and SCC22} \le -11 + 0.18f \text{ dB} && \text{for } 30\text{ GHz} \le f \le 50\text{ GHz}
\end{aligned} \qquad (25\text{-}17)$$

25.4.1.3 Figure of Merit ILD (FOM_{ILD})

The FOM_{ILD} (as calculated using the method defined in Section 10.2.6.4 (with the exception that there are no restrictions on the fitting coefficients) and the curve fit method defined in Clause 12 with f_{ILmax} of 43.5 GHz, f_{ILmin} of 50 MHz and rise time of 8.0 ps) for the mated HCB and MCB pair is ≤ 0.15 dB.

25.4.1.4 Crosstalk

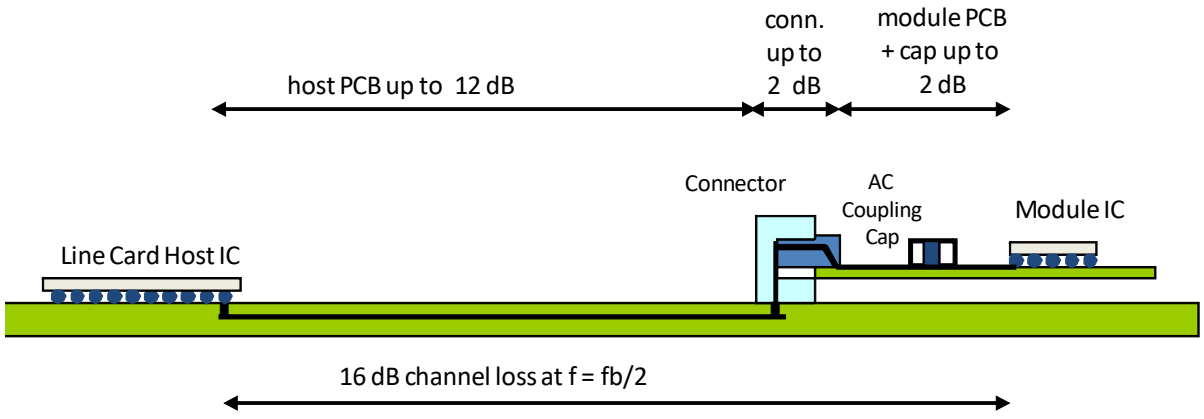
The Integrated Crosstalk Noise (ICN) is defined by the method of Section 12.2.1.2, with the exception that the measurements and summations extend up to 43.5 GHz, while Equation (12-12) and Equation (12-13) for the weights use Fb = 58 GHz with the aggressor amplitudes as listed in Table 25-3, the rise/fall times equal to the slew time listed in Table 25-3. ICN shall be less than 3.85 mV RMS. MDNEXT shall be less than 1.35 mV RMS. MDFEXT shall be less than 3.6 mV RMS.

25.A Appendix - Recommended Electrical Channel

This Appendix contains recommended electrical channels as described in Section 25.1.

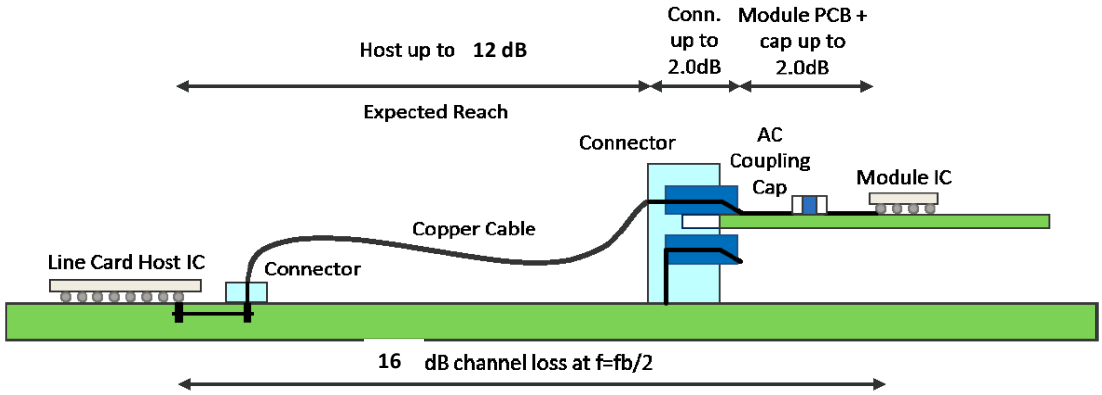
The first recommended channel includes a host that consists of a majority of PCB trace with an expected host trace reach of up to at least 200 mm. The end to end channel consists of host PCB trace, module PCB trace, vias, AC coupling capacitor and one connector, not in this order. The recommended PCB trace differential impedance is 100 ± 10 Ω. This full channel model is shown in Figure 25-21 below.

Figure 25-21. CEI-112G-VSR-PAM4 PCB Channel Reference Model



The second recommended channel includes an extended reach host that consists of a majority of cable routing with an expected host cable reach of up to at least 600 mm. The end to end channel consists of host PCB trace, module PCB trace, vias, AC coupling, two connectors and copper cable, not in this order. This full channel model is shown in Figure 25-22 below.

Figure 25-22. CEI-112G-VSR-PAM4 Cabled Channel Reference Model



Note that in practice the host channel is not measurable as appropriate test points are not accessible. However, Appendix 25.B contains recommended host channel performance.

The expected reach is greatly influenced by the attenuation of the interconnect media used on the host. To illustrate this, Table 25-13 contains a comparison of several material class categories and the expected reach if the host consisted only of this media and no other interconnect pieces.

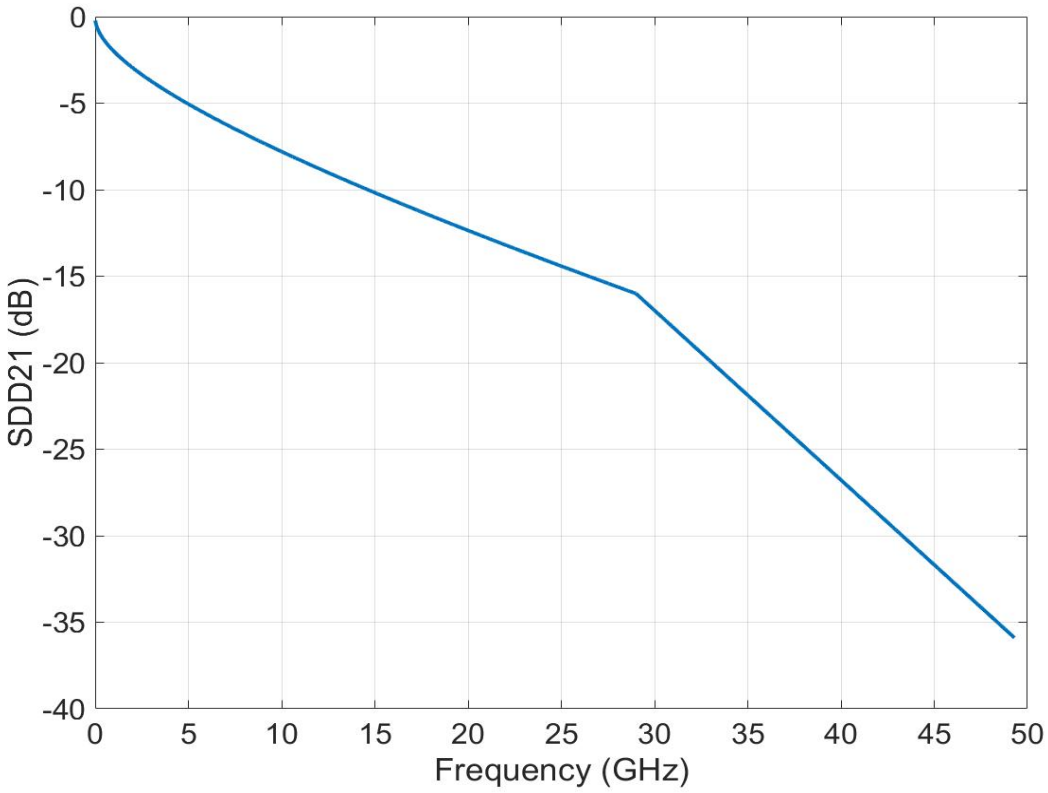
Table 25-13. Expected Reach of Different Material Classes

Material Class	Attenuation per mm (dB/mm)	Reach at 12 dB (mm)
Medium Loss PCB	0.1	120
Low Loss PCB	0.08	150
Ultra Low Loss PCB	0.05	240
TwinAx Cable	0.02	600

25.A.1 Insertion Loss

Host insertion loss and module insertion loss are recommended limits only. Achieving these recommended limits does not signify compliance nor guarantee successful communication between two devices. Equation (25-18) (illustrated in Figure 25-23) represents the highest recommended insertion loss (see SDD21) of the end-to-end channel.

Figure 25-23. Recommended minimum SDD21 of the end-to-end channel (for f_b= 58 GHz)



$$\mathrm{SDD21} = -0.05 - 13.1196\sqrt{\frac{f}{f_b}} - 13.3503\frac{f}{f_b} \qquad \text{for } f < \frac{f_b}{2}$$

$$\mathrm{SDD21} = 12.421875 - 56.84375\frac{f}{f_b} \qquad \text{for } \frac{f_b}{2} < f < 0.85 f_b \tag{25-18}$$

In addition it is recommended that the VSR channel have an $\mathrm{FOM_{ILD}}$ less than or equal to 0.25 dB and an ERL (Effective Return Loss) greater than or equal to 10 dB. This recommended host channel when used with a host transmitter meeting the recommendations in Appendix 25.C is expected to meet the VEC, Eye Height and Eye Width specifications in Table 25-1. ERL parameter values are given in Table 25-7, "Transmitter and Receiver" column.

25.B Appendix - Channel Operating Margin to TP1a

For an informative introduction into the Channel Operating Margin method, please refer to Appendix 25.D.The Channel Operating Margin (COM) of the host channel plus host compliance board can be computed using the procedure in Annex 93A of IEEE Std 802.3 [27] as modified by IEEE Std 802.3ck [29], with the Test 1 and Test 2 values in Table 25-14. Test 1 and Test 2 differ in the value of the device package model transmission line length *zp*. For engineered links, the length of the package for Test 2 can be modified to the actual package length and material.

Table 25-14. COM Parameter Values

Parameter	Symbol	Value	Units	Conditions
Signaling rate	f_b	36.0 - 58.0	Gsym/s	
Maximum start frequency	f_{min}	0.05	GHz	
Maximum frequency step	Δf	0.01	GHz	
Transmitter device package Single-ended device capacitance Single-ended device inductance Single-ended device capacitance at the device-to-pkg IF Transmission line length, Test 1 Transmission line length. Test 2 Transmission line 2 length Single-ended PKG capacitance at package-to-board IF	 C_d L_s C_b z_p z_p z_{p1} C_p	 100 120 30 15 30 1.8 87	 fF pH fF mm mm mm fF	See Note 1
Receiver device package Single-ended device capacitance Single-ended device inductance Single-ended device capacitance at the device-to-pkg IF Transmission line length, Test 1 Transmission line length. Test 2 Transmission line 2 length Single-ended PKG capacitance at package-to-board IF	 C_d L_s C_b z_p z_p z_{p1} C_p	 0 0 0 0 0 0 0	 fF pH fF mm mm mm fF	
Transmission line characteristic impedance	Z_c	87.5	Ω	
Transmission line 2 characteristic impedance	Z_{c1}	92.5	Ω	
Single-ended reference resistance	R_0	50	Ω	
Single-ended termination resistance	R_d	50	Ω	
Receiver 3 dB bandwidth	f_r	0.75 × f_b	GHz	
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.65	—	
Transmitter equalizer, 2nd pre-cursor coefficient Minimum value Maximum value Step size	$c(-2)$	 0 0.10 0.020	 — — —	
Transmitter equalizer, 1st pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.2 0 0.020	 — — —	
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.1 0 0.020	 — — —	

Table 25-14. COM Parameter Values

Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 -11 -2 1.0	 dB dB dB	See Note 2
Continuous time filter, DC gain2 Minimum value Maximum value Step size	g_{DC2}	 -3 0 0.5	 dB dB dB	See Note 2
Parameter-sets for G_{Qual} (min, max), $G2_{Qual}$ (see Table 25-10)	G_{Qual}, $G2_{Qual}$	(-2, -11), 0 (-2, -11), -1 (-4, -10), -2 (-4, -9), -3	dB dB dB dB	
Continuous time filter, pole frequencies	f_{p1} f_{p2}	f_b /1.8839 f_b	GHz GHz	
Continuous time filter, scaled zero frequency	f_z	f_b /2.862	GHz	
Continuous time filter, low frequency pole/scaled zero	f_{LF}	f_b /40	GHz	See Note 3
Transmitter rise time	T_r	0.3984	UI	
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.413 0.413 0.489	 V V V	
Number of signal levels	L	4	—	
Level separation mismatch ratio	R_{LM}	0.95	—	
Transmitter signal-to-noise ratio	SNR_{TX}	32.5	dB	
Number of samples per unit interval	M	32	—	
Decision feedback equalizer (DFE) length	N_b	4	UI	
Range of b1 tap	$b_{(1)}$	0.1 to 0.4		See Note 4
Range of b2 and b3 taps	$b_{(2-3)}$	-0.1 to 0.15		See Note 4
Range of b4 tap	$b_{(4)}$	-0.05 to 0.1		See Note 4
Random jitter, RMS	σ_{RJ}	0.01	UI	
Dual-Dirac jitter, peak	A_{DD}	0.02	UI	
One-sided noise spectral density	eta0	4.1×10^{-8}	V^2/GHz	
Target detector error ratio	DER_0	$1x10^{-6}$	—	See Note 5
One half of the histogram window	T_O	50	mUI	
Eye Height	Eye_Height	10	mV	
Vertical Eye Closure	VEC	12	dB	

Notes:

1. C_d includes die bump, ESD and additional parasitic effects as modified by any T-coils or other structures
2. Not all combinations are allowed, See Table 25-10.
3. f_{LF} is called f_HP_PZ in Appendix 25.D.3.
4. See Table 25-12 and Appendix 25.D.3 for reference.
5. Equivalent to a BER of 1x10-6 with an average error extension probability of 0.5.

25.C Appendix - Informative Host Transmitter output Electrical Recommendations

Informative host Tx output recommendations are given in Table 25-15.

25.C.1 Host Transmitter output test point

Figure 25-1 gives the reference model and test points associated with host-to-module and module-to-host CEI-112G-VSR-PAM4 lanes. The informative host transmitter output electrical recommendations are defined to be measured at TP0a. TP0a is defined to be separated from TP0, the ball of the package performing the host-to-module transmit function, by 4 dB of PCB attenuation at 28 GHz.

25.C.2 Host-to-Module transmitter output Electrical Recommendations

It is recommended that each host-to-module lane meet the limits of Table 25-15.

Table 25-15. Host-to-Module Electrical Recommendations at TP0a

Parameter	Symbol	Min.	Max.	Unit	Conditions
Baud Rate		36.0	58.0	Gsym/s	
Differential Voltage, pk-pk	T_Vdiff	750	-	mV	See Note 1
DC Common Mode Voltage	T_Vcm	-0.3	2.8	V	See Note 2
Differential Termination Resistance Mismatch	T_Rdm	-	10	%	at 1 MHz
Differential Return Loss	T_SDD22	-	Equation 25-3	dB	at TP0
Transition Time: 20% to 80%	T_tr, T_tf	6.5	-	ps	With emphasis off
Common-mode return loss	T_SCC22	$-6 + 3*f/f_b$	-	dB	
Common Mode Noise, RMS	T_Ncm	-	12	mV	
Uncorrelated Jitter RMS (standard deviation of the probability distribution)	T_J_{RMS}		0.023	UI_{RMS}	See Note 3
Uncorrelated Jitter (time interval from 0.0005% to 99.9995% of the probability distribution)	T_J_{5u}		0.128	UI	See Note 3
Even-Odd Jitter (EOJ)	T_EOJ		0.025	UI	
Signal-to-noise-and-distortion ratio		32.5	-	dB	See Section 17.3.1.6.4 for definition

NOTES:
1. Max voltage is limited by specifications at TP1a. Minimum voltage can be lower for low loss channels. Signals are specified as measured through a fourth-order Bessel-Thomson low-pass response with 43 GHz 3 dB bandwidth. Sampling oscilloscopes may substitute the 40 GHz bandwidth limit with compensation for the reduced bandwidth.
2. Load type 0 with min. T_Vdiff, AC-Coupling or floating load.
3. As defined for CEI-112G-MR-PAM4 in Section 26.3.1.7

25.D Appendix - Informative Introduction to Channel Operating Margin

25.D.1 Introduction

Channel Operating Margin, COM, has emerged at high data rates as a single measure of channel performance that includes the effects of both signal impairments and the techniques used to compensate for those impairments. CEI-LR interoperability agreements have used COM as a normative specification to define the limits of the interconnect used for passive copper cables and backplanes. COM may be used as an informative tool to evaluate CEI-112G-VSR host and module channel design including impairments from:

Host or Module package

HCB or MCB with mated connectors

PCB trace or cabled interconnect

COM is a normative computation for CEI-LR which begins with S-parameters defined for an interconnect between the BGA balls of a transmitter device and receiver device. The COM computation establishes a closed budget between crosstalk, ISI, and channel loss, using parameters from transmitter and device specifications.

COM predicts the performance margin of an interconnect, but it can also be used to examine the interoperability margin of a high-speed serial system. Since COM includes the calculation of the ISI (inter-symbol interference) that remains after equalization and the effects of noise, jitter, and crosstalk, the derivation of COM itself can offer insights into the strengths and weaknesses of a design.

A COM value can be translated to an estimate of Vertical Eye Closure (VEC), which is more closely related to the output specification, using Equation (25-19).

$$VEC = -20\ log_{10}\left(1 - 10^{\frac{-COM}{20}}\right) \quad (25\text{-}19)$$

This allows designers to choose how they optimize signal impairments and equalization schemes while meeting BER specifications. While a channel that passes or fails the recommended COM limits is not guaranteed to pass or fail the normative specification limits, it provides guidance to designers.

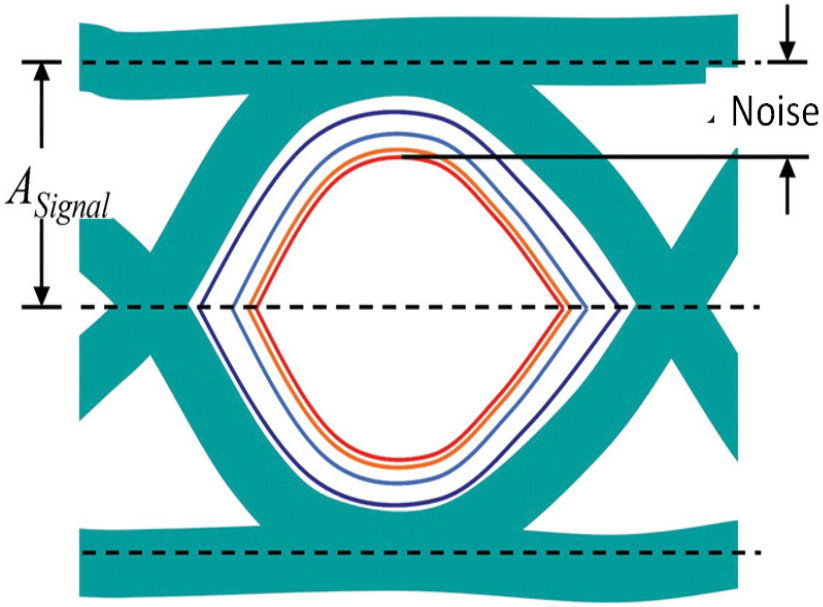
Since COM is a function of many signal integrity variables, it introduces the concept of a “design space.” The best design should correspond to the maximum value of COM in this multidimensional design space.

Figure 25-24 gives the concept of COM using a traditional NRZ eye diagram. The eye diagram used in COM is calculated from measurements of S-parameters, jitter, and noise along with models of SERDES (serializer-deserializer) response. The calculated

eye diagram includes the insertion loss and return loss of the channel, crosstalk, and random jitter and noise with equalization schemes at both the transmitter and receiver. COM (Equation (25-20)) is given by the dB ratio of the signal amplitude available at the reference sampler, A_s to the noise defined with respect to symbol error ratio.

$$COM = 20\ log_{10}\left(\frac{A_s}{Noise}\right) \quad (25\text{-}20)$$

Figure 25-24. Graphical depiction of COM. The eye diagram and SER contours include the effects of both transmitter and receiver equalization.



25.D.2 Deriving COM from S-parameters

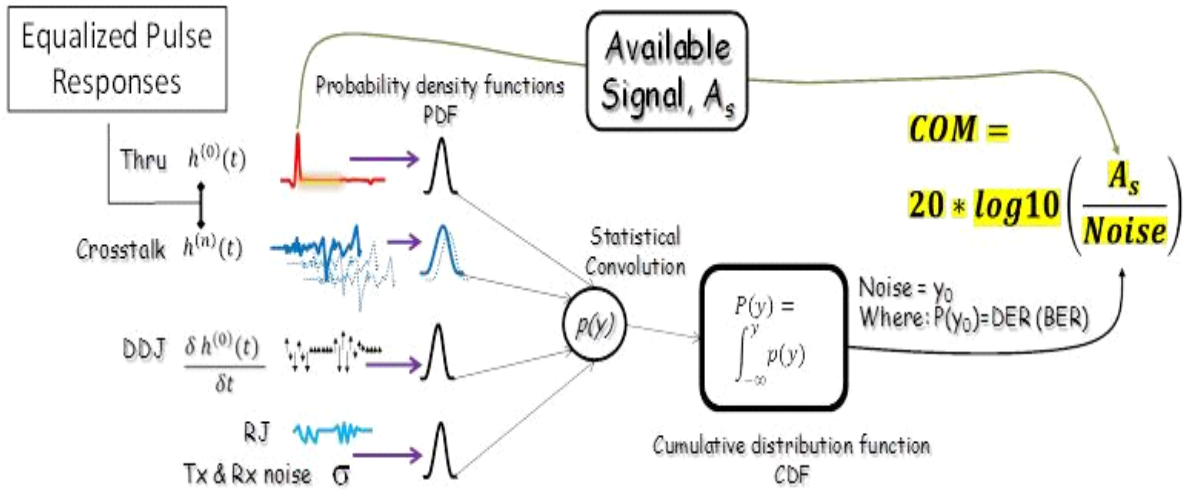
COM cannot be measured directly. It is derived from a combination of measurements and assumptions from device specifications.

The transfer functions of the channel, its crosstalk aggressors, the transmitter output, and receiver input are calculated under the assumption that they are LTI (linear time invariant). The system transfer function (in the frequency domain) is then used to calculate the pulse response in the time domain, which is the response to an isolated rectangular pulse of 1 UI in duration. Even in PAM4, any symbol stream can be considered as the superposition of such pulses with appropriate amplitudes.

The equalized pulse response and all the signal impairments are used to calculate a vertical slice of the eye diagram. For some digital architectures an eye diagram may not normally be generated, nevertheless the sampling point exists. DER is a generalized term that is equivalent to the BER for NRZ systems and the SER (symbol error rate) for PAM4 systems.

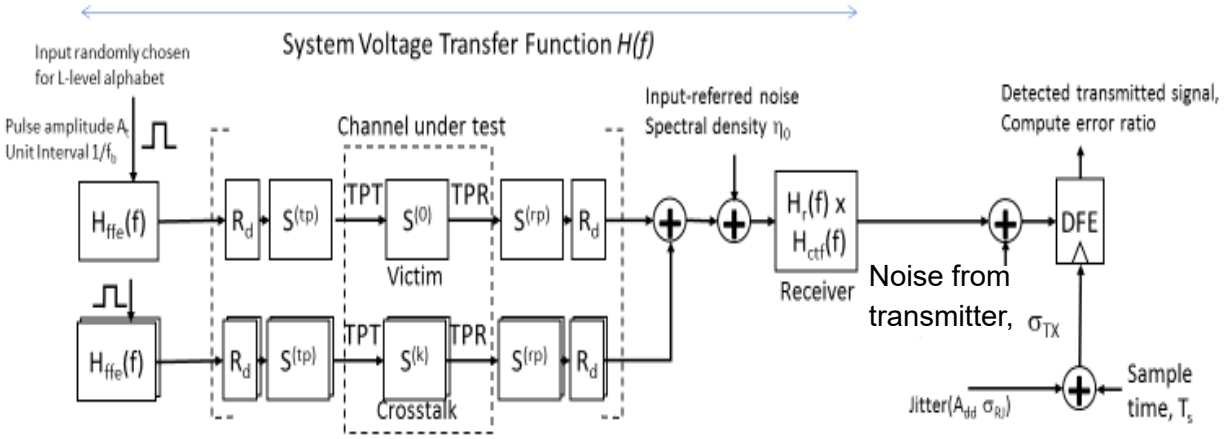
The peak signal amplitude, A_s, is the signal level and the noise-crosstalk amplitude, Noise, is related to the vertical eye closure defined with respect to DER0, the DER prescribed by the standard as in Figure 25-25.

Figure 25-25. Block diagram of the system operational elements



ISI, crosstalk, jitter and other noises are combined as probability density functions (PDF). The resulting PDF is converted to a cumulative distribution function (CDF) from which the total noise at DER0 is determined.

Figure 25-26. COM Block diagram of the transfer functions of the system elements

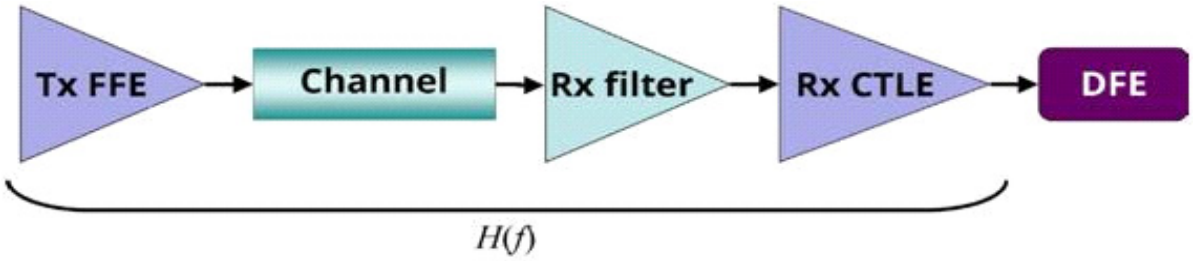


Pulse responses are derived from H(f), the system voltage transfer functions as shown in Figure 25-26. The measured channel is TPT to TPR for LR but for VSR, TP0a to TP1a is used for host output computations. Notice that transmit package, $S^{(tp)}$ and receive package $S^{(rp)}$, are reference S-parameters which may be cascaded to the channel under test. For LR both are used but for VSR, only the transmit package is used.

25.D.2.1 Calculate the System Transfer Function, H(f)

The transfer function of a circuit element represents its loss properties and its frequency and phase response. It is also the frequency domain representation of the impulse response. We build the system transfer function, H(f), from the transfer functions of each element from the transmitter through the channel to the receiver, including transmitter FFE (feed-forward equalization), receiver CTF (continuous time function) equalizer and receiver DFE (decision feedback equalizer), Figure 25-27. The CTF may be a CTLE (continuous time linear equalizer). The system transfer function is given by the product of the individual transfer functions in the frequency domain.

Figure 25-27. Block diagram of the system elements



The transmitter output transfer function includes two terms: first, the package response, $H_{Tx}(f)$, comes from a minimal model specified by the standard or the output response of the transmitter under consideration and, second, the transfer function of the transmitter FFE scheme, $H_{TxFFE}(f)$. The values of the FFE tap weights may be optimized in the next step, Section 25.D.2.2.

The transfer function of the channel, $H_{Channel}(f)$, is derived from the S-parameters of everything from the transmitter to the receiver. Since current COM implementations ignore common-mode noise and differential-to-common-mode conversion, we only need the differential terms: the through term, SDD21, the reflection terms SDD11 and SDD22, the FEXT terms, SDD23, SDD25, and SDD27, and the NEXT terms, SDD24, SDD26, and SDD28.

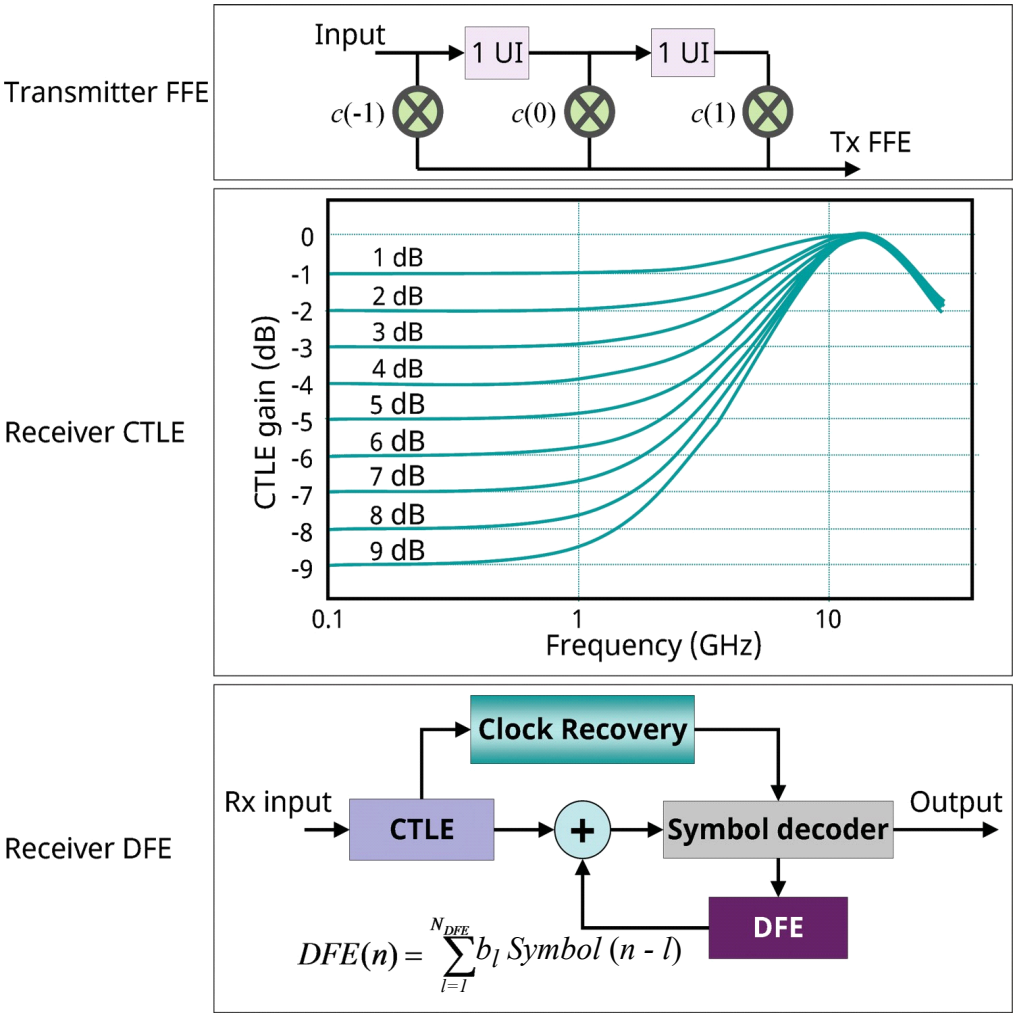
The receiver transfer function, $H_{Rx}(f)$, is usually specified as a 4th order Butterworth filter with bandwidth at $0.75f_b$, where fb is the baud rate, and the CTLE response, $H_{RxCTLE}(f)$. The CTLE gain is a free parameter whose value will be optimized in the next step.

Since the receiver DFE is a nonlinear device (i.e., it is not LTI) its effects are included separately. The resulting transfer function,

$$H(f) = H_{Tx}(f) \times H_{TxFFE}(f) \times H_{Channel}(f) \times H_{Rx}(f) \times H_{RxCTLE}(f),$$

is a function of frequency that depends on the still-to-be-determined values of the FFE taps and CTLE gain, Figure 25-28.

Figure 25-28. Diagrams of typical FFE, CTLE and DFE



25.D.2.2 Optimize Transmitter FFE and Receiver CTLE

The next step is to optimize the equalization parameters. Think of the equalization parameters geometrically as though they span a configuration space. For example, if we have three transmitter FFE taps {c (–1), c (0), c(1)}, one CTLE gain g_{DC}, and 4 DFE taps {b(0), b(1), b(2), b(3)}, then it's an 8 dimensional space. To find the best combination of the 8 parameters we need a function of those 8 parameters that reaches a maximum when the equalization schemes are optimized. That function is a figure of merit: FoM(c (–1), c (0), c(1), g_{DC}, b(0),…, b(3)). To find the optimal set of parameters we can perform a full grid search that steps through the possible values allowed by the specification and the implementation. The optimal value of FOM determines the best equalization settings. The equation for FOM is provided in Equation (25-21).

$$FOM = 10\log_{10}\left(\frac{A_s^2}{\sigma_{TX}^2 + \sigma_{ISI}^2 + \sigma_J^2 + \sigma_{XT}^2 + \sigma_N^2}\right) \quad (25\text{-}21)$$

where

A_s is the peak signal amplitude (computed in COM),

σ_{TX} is the transmitter noise (derived from SNR_TX in COM table),

σ_{ISI} is the noise contribution of the residual ISI (computed in COM),

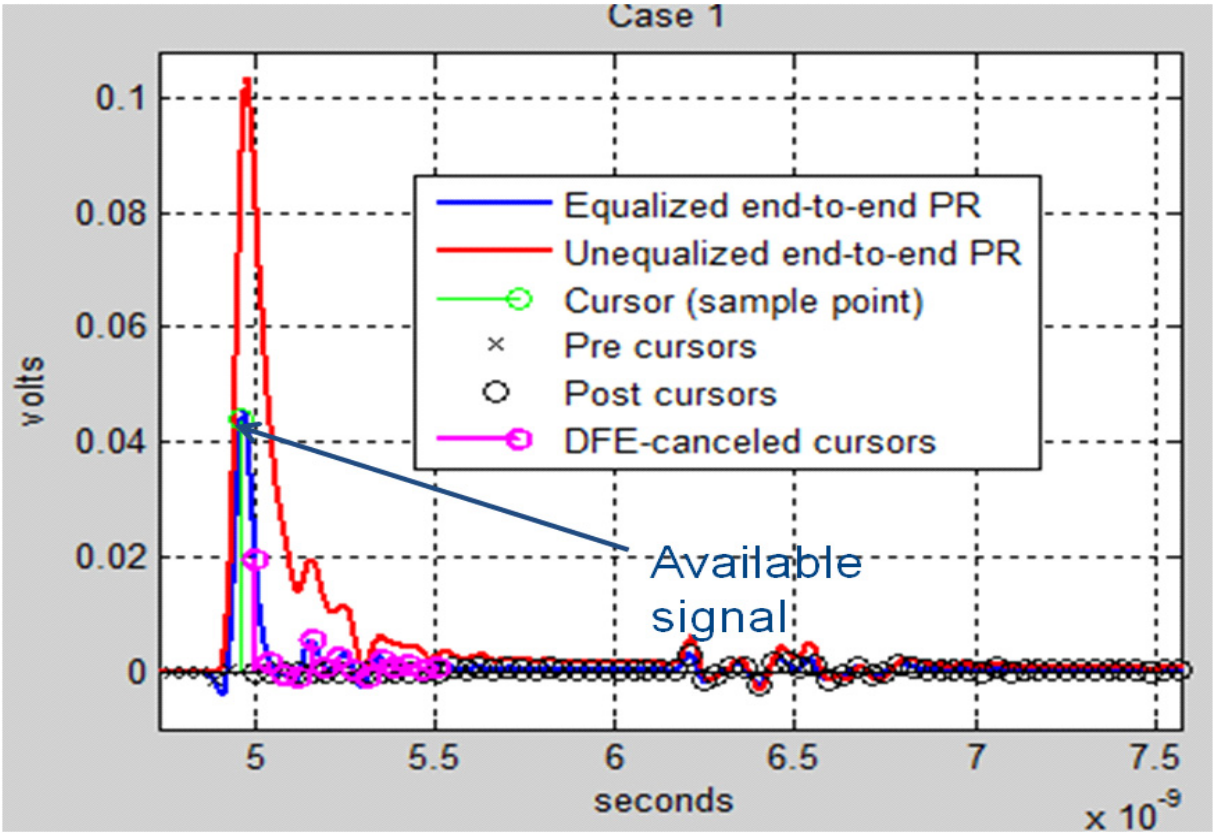
σ_J is the jitter contribution to amplitude noise (derived from sigma_RJ and A_DD in COM table; i.e., Gaussian jitter and half of High Probability jitter (W), respectively: see Annex 2.C.4)

σ_{XT} is the peak crosstalk noise (computed in COM) and

σ_N is the spectral noise at the receiver (input parameter, eta0 in COM table).

The value of A_s is determined using the equalized pulse response as shown in Figure 25-29.

Figure 25-29. Pulse response used to calculate A_s



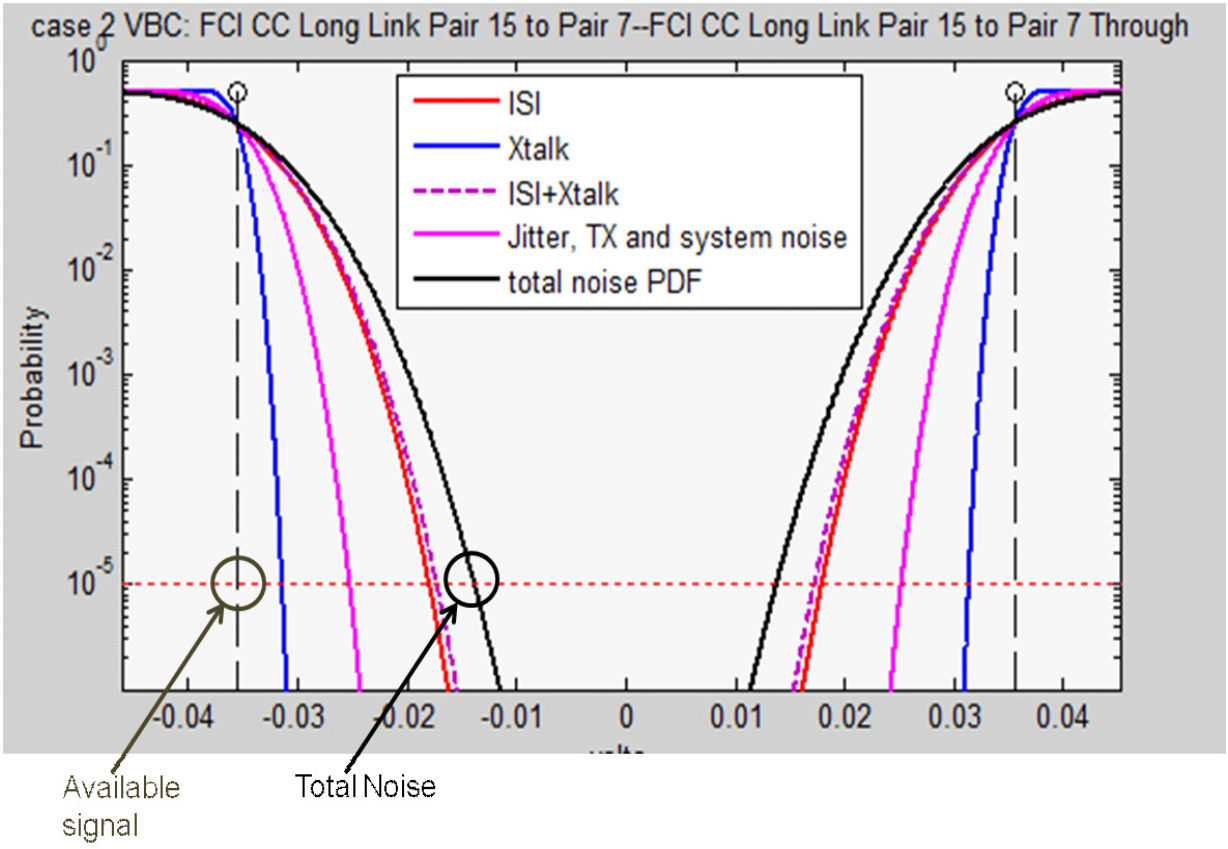
25.D.2.3 Calculate the Noise and Crosstalk Interference

With the equalization scheme set and the numerator, A_S, in Equation (25-20) determined, we turn to the noise and interference-crosstalk terms to get *Noise* and then complete the calculation of COM.

We acquire the noise and crosstalk PDF (probability density function) by modeling a vertical slice of the eye diagram.

Eye diagrams consist of overlaid waveforms of individual symbols. The key ingredients to each symbol-waveform can be separated into deterministic and random components. The deterministic components consist of discrete shifts in the level of each symbol-waveform and the random components cause statistical fluctuations about those levels. Figure 25-30 shows an example of noise components and their effect on the total noise PDF.

Figure 25-30. Block diagram of the system elements



25.D.3 Tables for COM parameters, outputs, results

The following table provides the definition of the parameters found in the COM report (saved in csv file in row format). Not all parameters are used.

Table 25-16. Definition of COM Implementation Parameters

Parameter	Definition
--- Testcase xx results ---	This report is produced for each package case. These parameters are reported in the report mat and cvs files.
file_names	This is the tag used for the channel run set - it contains the thru file name
config_file	The configuration xls files used for the report
levels	Number of symbols levels (PAM-4 is 4, NRZ is 2)
Pkg_len_TX	Victim transmitter package trace length in mm (integer only) cases
Pkg_len_NEXT	NEXT aggressor transmitter package trace length in mm (integer only) for this cases
Pkg_len_FEXT	FEXT aggressor transmitter package trace length in mm (integer only) for this cases
Pkg_len_RX	victim receiver package trace length in mm (integer only) for this cases
baud_rate_GHz	Baud (Signaling) rate (GHz) i.e. f_b
f_Nyquist_GHz	f_b/2
channel_operating_margin_dB	COM value in dB for this case
peak_interference_mV	The total noise at probability DER_0. This is used in COM calculation
peak_channel_interference_mV	The noise at probability DER_0 for the combined uncompensated ISI and crosstalk. This is used in the diagnosis of a channel design.
peak_ISI_mV	The noise at probability DER_0 for only uncompensated ISI. This is used in the diagnosis of a channel design.
peak_MDXTK_interference_mV	The noise at probability DER_0 for only all the crosstalk. This is used in the diagnosis of a channel design.
peak_MDNEXT_interference_mV	The noise at probability DER_0 or only all NEXT crosstalk. This is used in the diagnosis of a channel design.
peak_MDFEXT_interference_mV	The noise at probability DER_0 for only all FEXT crosstalk. This is used in the diagnosis of a channel design.
available_signal_after_eq_mV	The amplitude of the available signal (A_s). This is used in COM calculation and Eye Height calculations. It is essentially defined at the sample point.
steady_state_voltage_mV	Steady state voltage
Eye_Height_mV	Eye Height at the sample point.
Eye_Height_normalized	Normalized Eye Height at the sample point.
VEC_dB	dB of normalized Eye Height at the sample point.
T_O	One half of the histogram window

fit_loss_dB_at_Fnq	Fitted insertion loss at f_b/2. Not intended to couple with any particular standard or method.
IL_dB_at_Fnq	Insertion loss at f_b/2 of tp0-tp5 which includes host boards if applicable
FOM_ILD	RMS over f_b/2 span of insertion loss deviation. This may used in the diagnosis of a channel design. Not intended to couple with any particular standard or method.
ICN_mV	RMS over f_b/2 span of power sum of the crosstalk. This may used in the diagnosis of a channel design. Not intended to couple with any particular standard or method.
equivalent_ISI_ICN	RMS over f_b/2 span of power sum of the crosstalk and ISI. This may used in the diagnosis of a channel design. Not intended to couple with any particular standard or method.
sci_noise_FD_RMS	Obsolete
CTLE_zero_poles	List of zero pole1 and pole2 in Hz used for the CTLE in the COM calculations
CTLE_DC_gain_dB	Relative DC gain in decibels used for the CTLE in the COM calculations
TXLE_taps	List of transmitter FFE taps used for the CTLE in the COM calculations
DFE_taps	List of transmitter DFE taps used for the CTLE in the COM calculations
cci_noise_TD_BER	Obsolete
peak_interference_at_BER	Same as peak_channel_interference_mV but in volts
FOM	Best figure of merit result from the CTLE and Tx FFE optimization.
DFE2_RSS	Root sum squared of DFE taps 2 to last DFE tap
DFE4_RSS	Root sum squared of DFE taps 4 to last DFE tap
error_propagation_probability	Sequential list of error propagation probabilities for each DFE tap
burst_probabilities	Sequential list of burst error probabilities for each burst length.
peak_uneq_pulse_mV	Peak value of the unequalized SBR
cable_loss	Cable assembly loss report when include PCB is not 0 in the config file
COM Pass threshold	The pass fail threshold for COM in dB
CSV_REPORT	When set to 1 a CSV report is created in the results directory. The name contains the name of the thru file and case number. 0 suppressed this
DIAGNOSTICS	When set to 0 a limited set of results are reported. When set to 1 a fuller set of results are reported. This extra parameters can be useful for diagnosing contributions and other aspects of channel design. In addition a mat file is written to the result
Display frequency domain	When set to 1 a figure containing IL, RL, PST, ILD, and ICR is displayed. 0 suppresses this.
DISPLAY_WINDOW	When set to 0 the display windows are suppressed. Set to 1 may be useful when running in a batch.

Enforce Causality	When set to 1 causality is enforced for the FD to TD conversion. If set to zero a IFFT using extrapolated low and high frequency data is used to convert to time domain. Look at the SBR in figure 100. If a small amount of precursor exists set to 1.
Enforce Causality DIFF_TOL	Tolerance parameter for causality, Hard enforcement, 1e-4,Soft enforcement, 1e-3
Enforce Causality pulse start tolerance	Tolerance parameter for causality, Hard enforcement, 0.05, Soft enforcement, 02
Enforce Causality REL_TOL	Tolerance parameter for causality, Hard enforcement, 1e-3, Soft enforcement, 1e-2
Error propagation COM margin	Unsupported. Set to 0
Force PDF bin size	Normally set to 0. This forces a PDF bin size when set to 1.
IDEAL_RX_TERM	Normally set to 0. When set to 1 an ideal termination replaces the Tx package.
IDEAL_TX_TERM	Normally set to 0. When set to 1 an ideal termination replaces the Rx package.
T_r	Rise time of transmitter, converted to a TX filter per Equation 93A-46 if IDEAL_TX_TERM is true.
INC_PACKAGE	When set to 1 the package is added to the channel model. If the channel model contains a package set this to 0. When set to 0 C_d, z_p select, z_p (TX), z_p (NEXT), z_p (FEXT), z_p (RX), C_p, R_0, and R_d are ignored.
Include PCB	This is normally set to 0. Set to 1 for CR4. When set to 1 a PCB board is concatenated on both sides of the tested channel as specified in 92.10.7.1.1.
INCLUDE_CTLE	Normally set to 1. When set to 0 the CTLE is omitted from analysis.
INCLUDE_TX_RX_FILTER	Normally set to 1. If set to 0 the Tx and Rx filter are omitted. However Tx FFE and CTLE are no affect by this parameter.
Max burst length calculated	Used for calculation of probabilities of error bursts due to DFE error propagation.
PDF bin size	The value in volts which is the size of PDF voltage bins. Essentially can be used a noise filter as any value lower than this voltage is considered as 0 V.
Port Order	Order for S-parameter ports [tx+, tx-, Rx+, Rx-]. Normally set to [1 3 2 4]
RESULT_DIR	The name of the results directory. May use relative references. If contains the string {date} todays date replaces {date}
RX_CALIBRATION	Set to 0 for regular channel analysis. Set to 1 for calibrating the noise source in RX compliance test (Annex 93C.2).
Sigma BBN step	Initial step used for noise adjustment in Rx calibration.
SAVE_FIGURE_to_CSV	Set to one to save figure contents in csv files in RESULTS_DIR.
SAVE_FIGURES	Set to one to save fig files in RESULTS_DIR.
COM_CONTRIBUTION	When set to 1 a rough approximation of COM contributions chart replaces the bathtub curves. When set to 0 the bathtub curves are displayed
BREAD_CRUMBS	When set to 1 then a mat file with the structures “params” and “OP” is created in the results directory

Table 25-17. New parameters for rev 162a

Parameter	Definition
c(-2)	TX equalizer pre cursor tap -2 individual settings or range. If not present, ignored
c(2)	TX equalizer post cursor tap 2 individual settings or range. If not present, ignored
c(3)	TX equalizer post cursor tap 3 individual settings or range. If not present, ignored
g_DC_HP	Sweepable AC-DC gain
f_HP_PZ	Pole-zero location

Table 25-18. Param MATLAB® structure (Output if BREAD_CRUMBS is set)

Param MATLAB® Structure		
fb	specBER	z_p_rx_cases
max_start_freq	pass_threshold	pkg_gamma0_a1_a2
max_freq_step	sigma_RJ	pkg_tau
tx_ffe_c0_min	A_DD	pkg_Z_c
tx_ffe_cm1_values	eta0	brd_gamma0_a1_a2
tx_ffe_cp1_values	SNDR	brd_tau
ndfe	R_LM	brd_Z_c
ctle_gdc_values	samples_per_ui	z_bp_tx
CTLE_fp1	bmax	z_bp_next
CTLE_fp2	C_pkg_board	z_bp_fext
CTLE_fz	C_diepad	z_bp_rx
a_thru	R_diepad	snpPortsOrder
a_fext	Z0	f_v
a_next	z_p_tx_cases	f_f
levels	z_p_next_cases	f_n
	z_p_fext_cases	f_r

Table 25-19. OP MATLAB® structure (Output if BREAD_CRUMBS is set)

OP MATLAB® Structure		
include_pcb	BREAD_CRUMBS	PHY
INCLUDE_CTLE	ENFORCE_CAUSALITY	RUNTAG
INCLUDE_FILTER	EC_REL_TOL	use_simple_EP_model
force_pdf_bin_size	EC_DIFF_TOL	nburst
BinSize	EC_PULSE_TOL	COM_EP_margin
DEBUG	pkg_len_select	
DISPLAY_WINDOW	RX_CALIBRATION	
CSV_REPORT	sigma_bn_STEP	
SAVE_FIGURES	BBN_Q_factor	
SAVE_FIGURE_to_CSV	force_BBN_Q_factor	
GET_FD	transmitter_transition_time	
INC_PACKAGE	LIMIT_JITTER_CONTRIB_TO_DFE_SPAN	
IDEAL_RX_TERM	impulse_response_truncation_threshold	
IDEAL_TX_TERM	interp_sparam_mag	
EXTERNAL	interp_sparam_phase	
RESULT_DIR		

25.D.4 References

Anritsu white paper: Measuring Channel Operating Margin: https://dl.cdn-anritsu.com/en-us/test-measurement/files/Technical-Notes/White-Paper/11410-00989A.pdf

Original IEEE proposal: http://www.ieee802.org/3/bj/public/jul12/mellitz_01_0712.pdf
R Mellitz, C Moore, M Dudek, M Li, A Ran, "Time-Domain Channel Specification: Proposal for Backplane Channel Characteristic Sections", IEEE Std 802.3bj July 2012 Meeting, San Diego, CA

IEEE Std 802.3 [27, 28, 29] Clause 93A.1

DesignCon 2014 Paper: http://www.ee.sc.edu/classes/Spring14/elct861/Class_Notes/8-TH6%20state%20of%20IEEE%20802%203bj%20100G%20Backplane%20Ethernet.pdf
M Brown, M Dudek, A Healey, E Kochuparambil, L Ben-Artsi, R Mellitz, C Moore, A Ran, P Zivny, "The state of IEEE 802.3bj 100 Gb/s Backplane Ethernet", DesignCon 2014, January 2014, Santa Clara, SC

A Healey, C Moore, R Mellitz, A Ran, L Ben-Artsi, "Proposal for a causal transmission line model" IEEE 802 Plenary March 2014 Meeting, Beijing, China: http://www.ieee802.org/3/bj/public/mar14/healey_3bj_01_0314.pdf

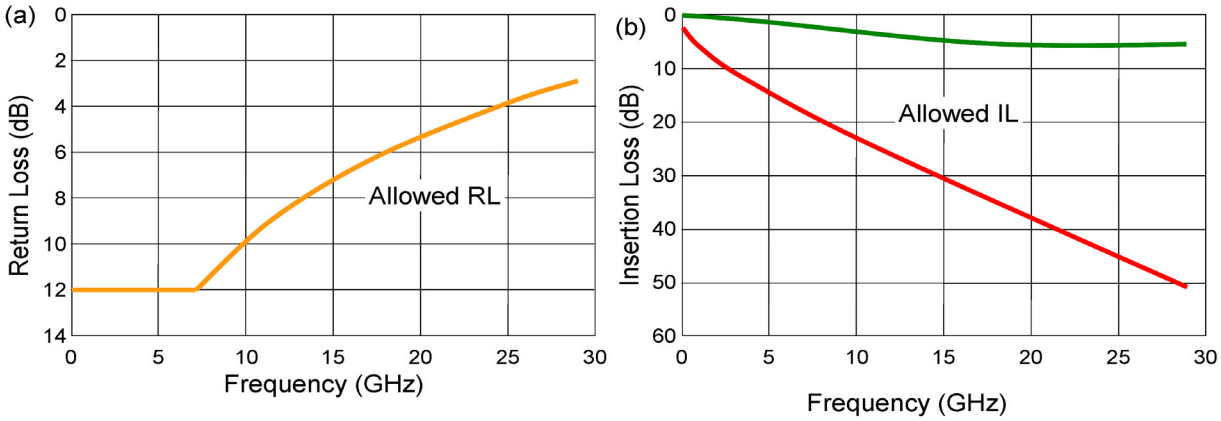
Nov 2016 version of COM for 50 Gb/s per lane PAM4 IEEE work: http://www.ieee802.org/3/cd/public/channel/mellitz_3cd_01_1116_COM.zip

Multiple versions of COM for 100 Gb/s per lane in IEEE working group: https://ieee802.org/3/ck/public/tools/index.html#tools

25.E Appendix - Informative introduction to effective return loss

ERL was developed for noise-limited PAM4 (4-level pulse amplitude modulation) signals where it was found that S-parameter mask requirements (Figure 25-31) could not assure serdes-channel-serdes interoperability. Many cases where found in which a channel that fails the return loss template performed just fine in a system with equalization. In particular, decision feedback equalization (DFE) can equalize the effects of reflections that occur within the number of unit intervals (UI) over which the DFE extends; that is, if the DFE has N_{bx} taps, then it can equalize reflections over N_{bx} UI.

Figure 25-31. (a) Sdd22 or RL(f), and (b) Sdd21 or IL(f) masks for a typical PAM4 28 Gsym/s link (graphic courtesy of 'Ransom's Notes')



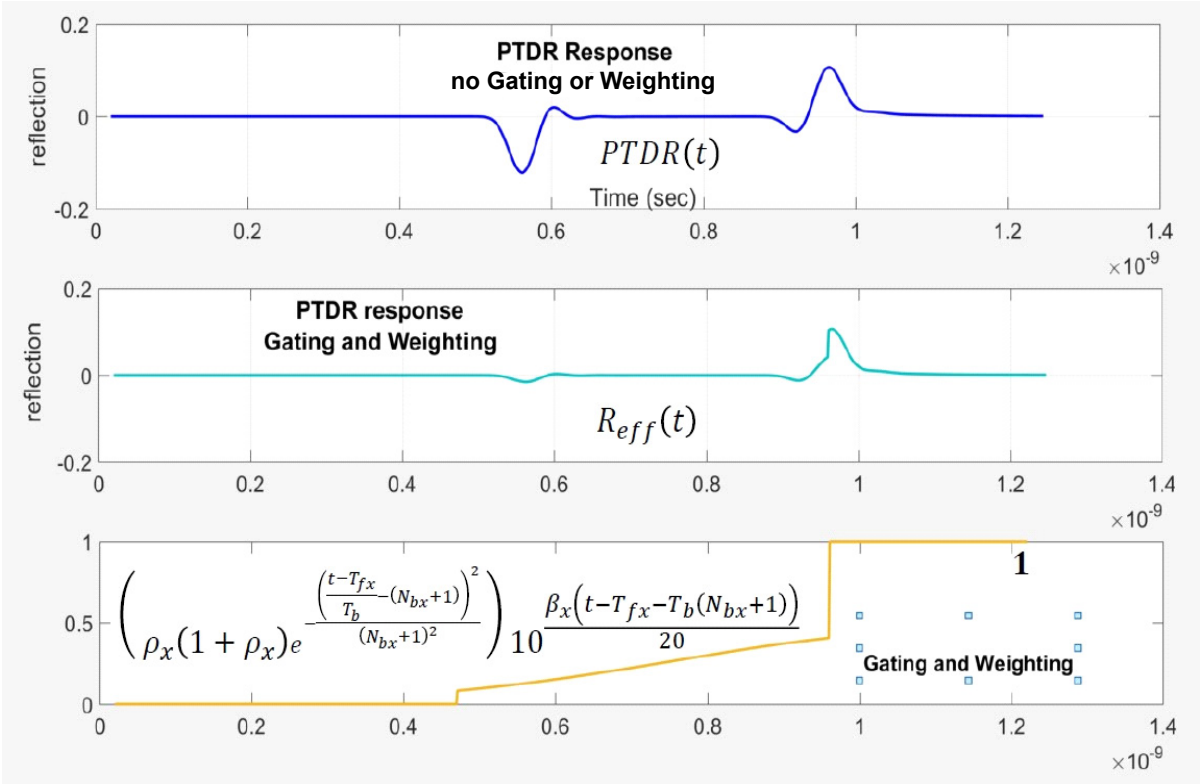
The ultimate performance question must be defined with respect to the error ratio which, for PAM4 systems, is symbol error ratio (SER). Effective return loss (ERL) was introduced by Rich Mellitz, a Distinguished Engineer at Samtec, to combine return loss and equalization into a figure of merit that is traceable to SER.

Like channel operating margin (COM), ERL is derived from the pulse response of a channel under specific assumptions about the quality of the transmitted signal. With ERL, we now consider the pulse response's reflection.

Think of a pulse as a long string of NRZ zeros (or PAM4 S1's) followed by a one (or a PAM4 S2) followed by another long string of zeros (or PAM4 S1s). The pulse response is the waveform that results from the transmission of a pulse through a channel. The reflected pulse response consists of the combination of all reflections due to a transmitted pulse. It can be calculated from TDR (time domain reflectometry) by using an incident pulse (PTDR) rather than the usual voltage step. The result is pulse time domain reflection, PTDR(t) is the reflected waveform. PTDR(t) can also be calculated from the channel's S-parameters. A Tukey filter may be applied to S-parameters prior to calculating PTDR(t).

R_{eff} (t), the "effective reflection waveform," is calculated from PTDR(t) by applying time gating multiplied by weighting functions (Figure 25-32). The time gating function is simple: zero prior to signal transmission and one thereafter. Two weighting functions are applied; one eliminates reflections within the N_{bx} unit interval range of the DFE, and the other accounts for how insertion loss dampens reflections. Both of the weighting functions are only applied over N_{bx} unit intervals.

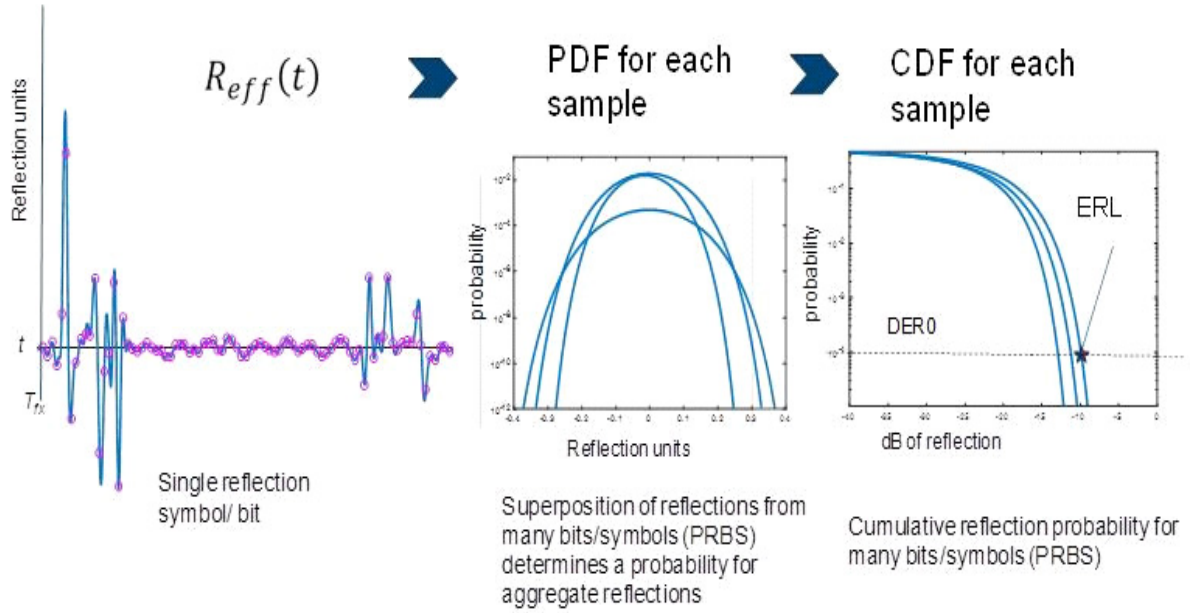
Figure 25-32. Examples: Top, PTDR(t); middle, R_{eff}(t); bottom, time gating and weighting function



R_{eff} (t) is sampled *M* times per UI over *N* UI resulting in R_{eff} (*n*, *m*) with a total of *NM* samples.

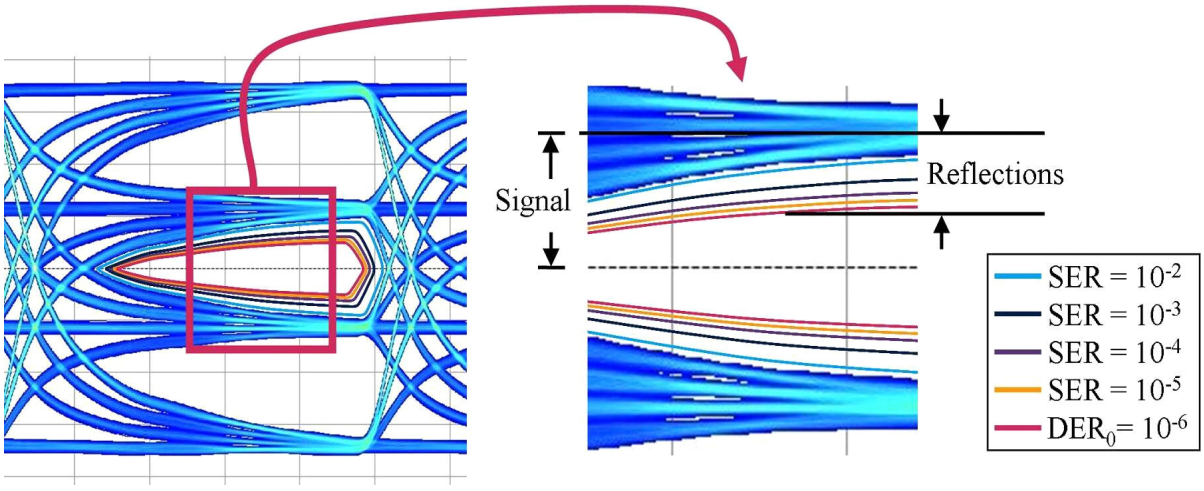
The sampled response is convolved with all possible pulse positions and PAM4 levels in *N* UI. The result gives the probability density functions (PDFs) for vertical eye closure caused by reflections (Figure 25-33). The worst variance of the *M* samples in each UI is used in the ERL calculation.

Figure 25-33. Block diagram of the system elements



Similar to how COM is calculated, ERL is given by the *ratio of the signal amplitude to the amount of eye closure caused by reflections, defined with respect to a prescribed SER*. The prescribed SER is called the detector error ratio (DER_0). (Figure 25-34).

Figure 25-34. Depiction of signal amplitude and eye closure defined with respect to an SER (courtesy Rhode and Schwarz)



The advantage of a requirement like ERL > minimum value prescribed in a specification rather than S-parameter mask requirements is that ERL incorporates the effects of equalization and S-parameter masks do not. In addition S-parameter mask do not address the SER.

As ERL is the dB ratio of an incident signal to reflected signal, larger values of ERL correspond to *smaller* amounts of reflection!

Example of parameters used to compute ERL are illustrated in Table 25-20

Table 25-20. Example of parameters used to compute ERL

Parameter Info	Default	Parameter Name	Unit
Signaling rate	Per section	f_b	GBd
Transition time associated with a pulse	Per section	T_r	ns
Receiver 3 dB bandwidth for the applied Butterworth Filter	Per section	f_r	GHz
Number of signal levels	4	L	—
Length of the reflection signal. The time in UI which ERL is computed for the signal R_{eff} (and TDR)	Per section	N	UI
Fixture delay time in UI to start the ERL computation	Per section	T_{fx}	UI
Number of samples per unit interval	32	M	—
Equalizer length associated with reflection signal	N_b	N_{bx}	UI
Incremental available signal loss factor	0	β_x	GHz
Permitted reflection from a transmission line external to the device under test	0.618	ρ_x	—
Target detector error ratio	Per section	DER_0	—

25.E.1 References

What's effective return loss, anyway? (Part 1, Part 2) EDN Ransom Stephens http://edn.com/electronics-blogs/eye-on-standards/4461625/what-s-effective-return-loss--anyway---part-1-

Effective Return Loss for 112G and 56G PAM 4: Richard Mellitz, Distinguished Engineer, Samtec, 2018 Central PA Signal Integrity Symposium, Apr 13, 2018

IEEE Std 802.3 [27, 28, 29] Clause 93A.5

25.F Appendix - Informative package model overview for COM

The value of COM is dependent on the package parameters. These parameters can be specified by the interoperability agreement, the user or they can be unused when the package is included in the channel S-parameters.

The package model used in COM is based on a T-coil model as shown in Figure 25-35. The circuit model is an un-coupled single lane of a differential pair except for the transmission lines which are specified in differential impedance. The values for the components of the T-coil model are entered into the appropriate COM location as shown in Table 25-21.

Figure 25-35. Die termination and package model used by COM

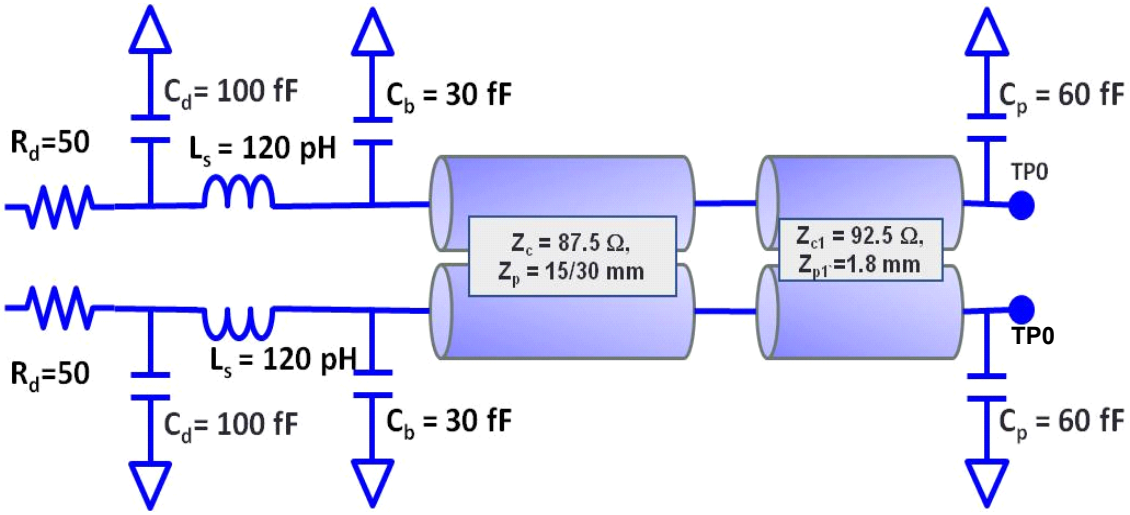


Table 25-21. Default die termination and parameter entries for CEI-112G-VSR COM

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
C_d	[1.0e-4 0]	nF	[TX RX]
L_s	[0.12, 0]	nH	[TX RX]
C_b	[0.3e-4 0]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[15 30; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]
z_p (FEXT)	[15 30; 1.8 1.8]	mm	[test cases]
z_p (RX)	[0 0; 0 0]	mm	[test cases]
C_p	[0.6e-4 0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm

It is also possible to calculate COM on a channel with S21 measurements that include packages as depicted in Figure 25-36. In this case the COM spreadsheet package parameters need to be adjusted according to Figure 25-37.

Figure 25-36. COM channel S-parameters including package

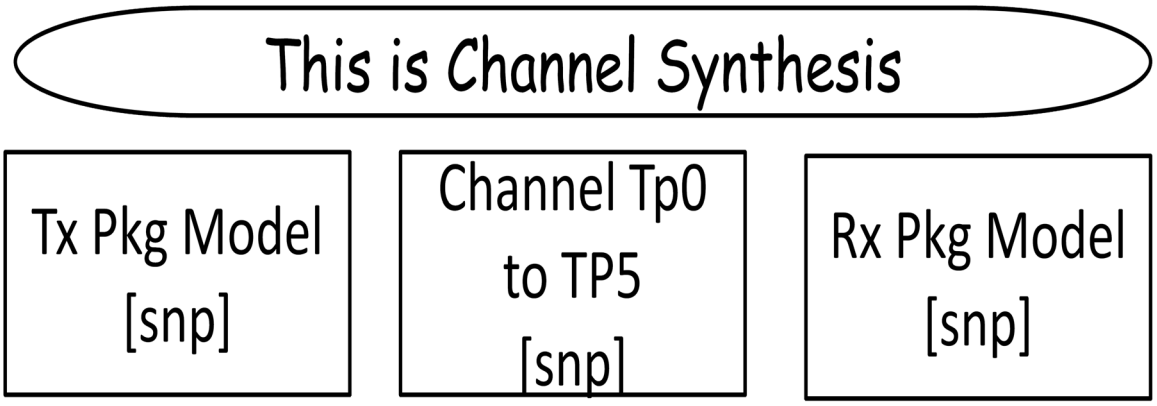


Figure 25-37. Adjusted COM spreadsheet package parameters for a measured channel that includes packages

C_d	[1.8e-4 1.8e-4]	nF	[TX RX]
z_p select	[1]		[test cases to run]
z_p (TX)	[0]	mm	[test cases]
z_p (NEXT)	[0]	mm	[test cases]
z_p (FEXT)	[0]	mm	[test cases]
z_p (RX)	[0]	mm	[test cases]
C_p	[0 0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[42.5]	Ohm	[TX RX] or selected

- C_d and R_d need to be provided by Rx Tx device manufacturers

- Zero length to remove the package addition
- C_p is already in the system model

25.G Appendix - Quaternary PRBS9 Test Pattern - QPRBS9-CEI

The QPRBS9-CEI test pattern is the 4-level pattern created by encoding the PRBS9 test pattern defined in [21] using the Gray Coding and PAM4 encoding described in Appendix 16.C.

26 CEI-112G-MR-PAM4 Medium Reach Interface

This clause details the requirements for the CEI-112G-MR-PAM4 medium reach high speed electrical interface between nominal baud rates of 36.0 Gsym/s and 58.0 Gsym/s using PAM4 coding. A compliant device shall meet all of the requirements listed below. The electrical interface is based on high speed, low voltage logic. Connections are point-to-point balanced differential pairs and signaling is unidirectional.

The electrical IA is based on loss and jitter budgets and defines the characteristics required to communicate between a CEI-112G-MR-PAM4 transmitter and a CEI-112G-MR-PAM4 receiver using copper signal traces on a printed circuit board. The use of cables to replace or partially replace the copper signal traces on the printed circuit board is acceptable and may extend the physical length of the connection. The characteristic impedance of the signal paths is nominally 100 Ω differential. The signal path or channel between a transmitter and a receiver shall meet the channel operating margin (COM), a method and a threshold quantity used for channel compliance.

CEI-112G-MR-PAM4 assumes using forward error correction (FEC) to achieve the bit error ratio (BER) target. The FEC guidances are described in Appendix 16.D.

Medium reach CEI-112G-MR-PAM4 devices from different manufacturers shall be interoperable.

26.1 Requirements

1. Support serial baud rates (f_b) within the range from 36.0 Gsym/s to 58.0 Gsym/s as specified for the device using PAM4 coding. A CEI implementation complies to the specifications of this clause over the range of baud rates stated for the implementation within this range.
2. Capable of achieving a raw Bit Error Ratio (BER) of 10^{-6} or better per lane. FEC is assumed to be used in the system to achieve corrected BER of 10^{-15} or better per lane. The baud rate includes the overhead required for FEC. The definition of FEC is outside the scope of this IA (see Appendix 16.D).
3. Capable of driving up to 500 mm of PCB and up to 1 connector.
4. Shall support AC-coupled operation.
5. Shall allow multi-lanes (1 to n).
6. Shall support hot plug.

26.2 General Requirements

26.2.1 Data Patterns

See Appendix 16.C.5.

26.2.2 Bit Error Ratio

A raw Bit Error Ratio (BER) better than or equal to 10^{-6} is required on each lane. A compliant receiver, when receiving from a compliant transmitter over a compliant channel, shall deliver the specified raw BER to the subsequent FEC decoder. Error bursts with length more than 94 PAM4 symbols delivered to the PAM4 decoder shall occur with a probability of less than 1 in 10^{20} PAM4 symbols. To enable a more practical test, the error bursts with length more than 38 PAM4 symbols delivered to the PAM4 decoder should occur with a probability of less than 1 in 10^{12} PAM4 symbols. See Appendix 16.D.

26.2.3 Ground Differences

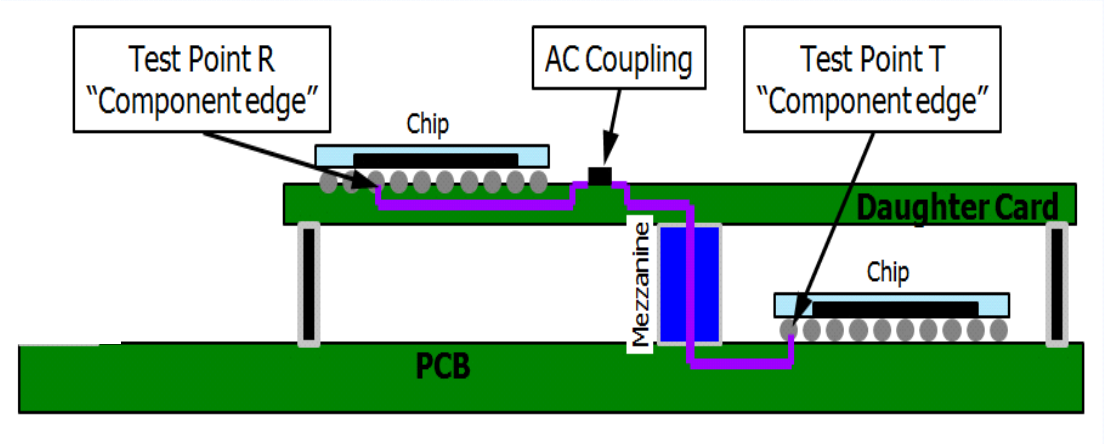
Please refer to Section 3.2.4.

26.2.4 Channel Compliance

A forward channel and associated dominant crosstalk channels are deemed compliant if the channel characteristics conform to the requirements defined in this section.

26.2.4.1 Reference Model

Figure 26-1.CEI-112G-MR-PAM4 Reference Model



Note: Test points differ from definitions in Section 1.8, as an AC-coupling capacitor, if physically located outside of the package, is part of the channel.

The channel is defined between test point T and test point R.

26.2.4.2 Channel Operating Margin

For an informative introduction into the Channel Operating Margin method, please refer to Appendix 25.D. The Channel Operating Margin (COM) of the channel is computed using the procedure in Annex 93A of IEEE Std 802.3 [27] as modified by IEEE Std 802.3ck [29], with the Tests 1,2,3,4 Table 26-1. Tests 1,2, 3, 4 differ in the value of the device package model transmission line length z_p. An informative package model overview can be found in Appendix 25.F. For engineered links, the length of the package for Test can be modified to the actual package length and material.

Using Tr = 0.3984 UI, in Equation (93A–46) [27]. COM shall be greater than or equal to 3.0 dB for each test. This minimum value allocates margin for practical limitations on the receiver implementation, and the largest step size allowed for transmitter equalizer coefficients.

Table 26-1. COM Parameter Values

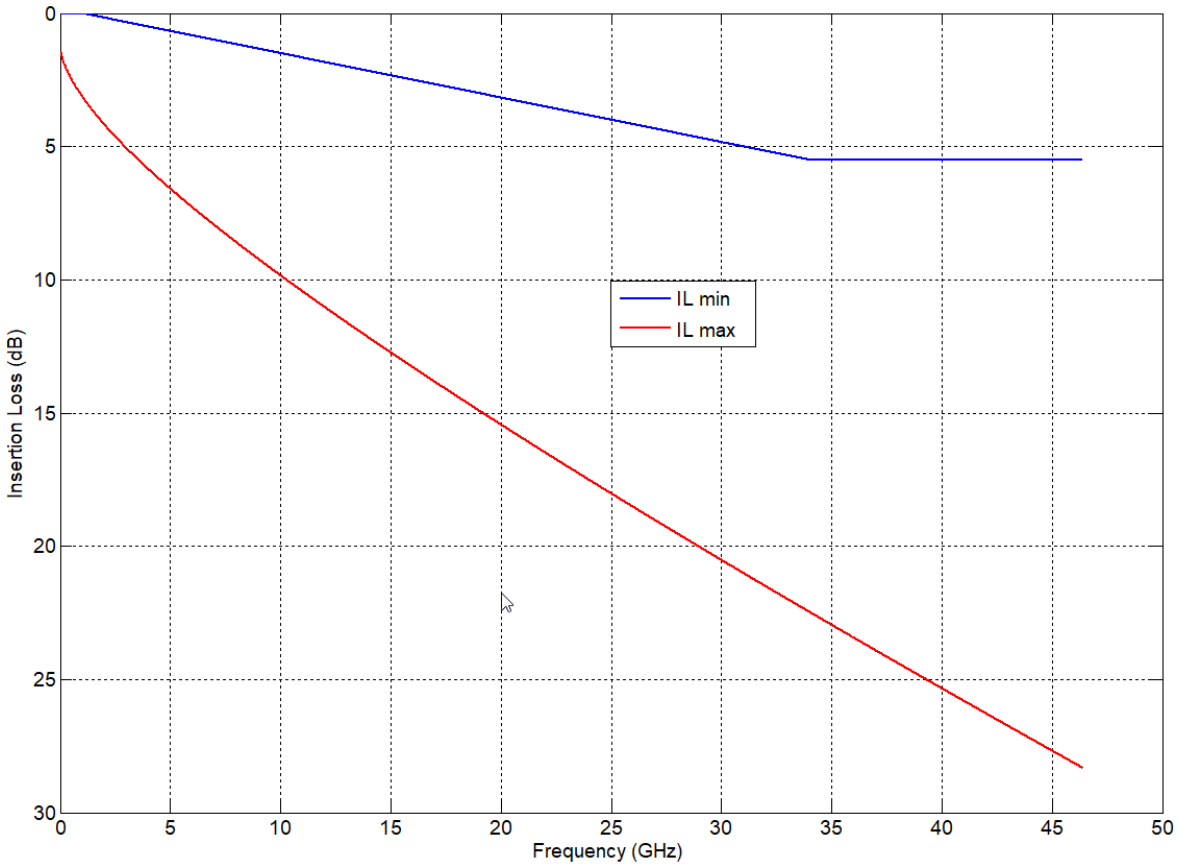
Parameter	Symbol	Value	Units
Signaling rate	f_b	36.0 - 58.0	Gsym/s
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package (PKG) model Single-ended device capacitance Single-device series inductance Single-ended capacitance at the device-to-pkg IF Transmission line length, Tx Test 1, 2, 3, 4 Transmission line length, Rx Test 1, 2, 3, 4 Transmission line 2 length Single-ended PKG capacitance at pkg-to-board IF Transmission line characteristic impedance Transmission line 2 characteristic impedance	 C_d L_s C_b Z_p Z_p Z_{p2} C_p Z_c Z_{c2}	 120 120 30 13,13,31,31 7,11,13,29 1.8 87 87.5 92.5	 fF pH fF mm mm mm fF Ω Ω
Transmission line parameter Transmission line parameter Transmission line parameter Transmission line parameter	γ_0 τ a_1 a_2	0 6.141×10^{-3} 9.909×10^{-4} 2.772×10^{-4}	1/mm ns/mm $ns^{1/2}/mm$ ns/mm
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	50	Ω
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.54	—
Transmitter equalizer, 3rd pre-cursor coefficient Minimum value Maximum value Step size	$c(-3)$	 -0.06 0 0.02	 — — —
Transmitter equalizer, 2nd pre-cursor coefficient Minimum value Maximum value Step size	$c(-2)$	 0 0.12 0.02	 — — —

Table 26-1. COM Parameter Values

Transmitter equalizer, 1st pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.34 0 0.02	 — — —
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.2 0 0.02	 — — —
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –20 -2 1	 dB dB dB
Continuous time filter, DC gain2 Minimum value Maximum value Step size	g_{DC2}	 –6 0 1	 dB dB dB
Continuous time filter, scaled zero frequency	f_z	f_b /2.5	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	f_b /2.5 f_b	GHz GHz
Continuous time filter, low frequency pole/scaled zero	f_{LF}	f_b /80	GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.413 0.413 0.608	 V V V
Number of signal levels	L	4	—
Level separation mismatch ratio	R_{LM}	0.95	—
Transmitter signal-to-noise ratio	SNR_{TX}	33	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	14	UI
Normalized DFE coefficient maximum limit for n = 1 to Nb	$b_{max}(1)$ $b_{max}(2\text{-}N_b)$	0.85 0.2	— —
Normalized DFE coefficient minimum limit for n = 1 to Nb	$b_{min}(1)$ $b_{min}(2\text{-}N_b)$	0.3 - 0.03	— —
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.02	UI
One-sided noise spectral density	η_0	8.2×10^{-9}	V^2/GHz
Target detector error ratio	DER_0	10^{-6}	—
Channel operating margin, min	COM	3.0	dB

26.2.4.3 Informative Channel Insertion Loss

Figure 26-2.Channel Insertion Loss Limit for 58.0 Gsym/s



$$IL_{max} = \left[1.083 + 1.696\sqrt{\frac{f \times 58}{f_b}} + 0.338\frac{f \times 58}{f_b}, \quad f_{min} \le f \le 0.8 f_b \right] \quad \text{(26-1)}$$

$$IL_{min} = \begin{bmatrix} 0, & f_{min} \le f \le 1GHz \\ \frac{1}{6}(f-1), & 1GHz < f \le 34GHz \\ 5.5, & 34GHz < f \le 0.8 f_b \end{bmatrix} \quad \text{(26-2)}$$

Channel insertion loss is an informative recommendation.

The channel must comply with the normative specification in Section 26.2.4.2.

26.2.4.4 Channel Effective Return Loss (ERL)

The background of ERL is described in the informative Appendix 25.E. ERLs of the channel (between test points T and R) are computed at test point T and at test point R using the procedure in 93A.5 [28] with the values in Table 26-2. Parameters that do not appear in Table 26-2 take values from Table 26-1. The value of T_{fx} is 0. N_{bx} is set to the value of N_b in Table 26-1.

Channel ERLs shall be greater than or equal to 11.9 dB.

Table 26-2. Channel ERL Parameter Values

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	0.531	UI
Incremental available signal loss factor	β_x	0	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.618	-
Length of the reflection signal	N	2000	UI

26.2.4.5 Channel AC-coupling

The transmitter shall be AC-coupled to the receiver. The impact of an AC-coupling capacitor implemented in the channel between the package balls of the transmitter and receiver (i.e., between compliance points T and R) is accounted for within the channel specifications. Common-mode specifications are defined as if the AC-coupling capacitor is implemented in the channel between compliance points T and R. Should the capacitor not be implemented between compliance point T and compliance point R, it is the responsibility of implementers to consider any necessary modifications to common-mode and channel specifications required for interoperability as well as any impact on the verification of transmitter and receiver compliance. In particular the common-mode specifications for the transmitter in Table 26-3 may not be appropriate.

The low-frequency 3 dB cutoff of the AC-coupling shall be less than 100 kHz.

26.3 Electrical Characteristics

The electrical signaling is based on high speed low voltage logic with a nominal differential impedance of 100 Ω.

26.3.1 Transmitter Characteristics

The transmitter electrical requirements at compliance point T (see Figure 26-1) are specified in Table 26-3, and the jitter requirements are specified in Table 26-4.

Table 26-3. Transmitter Electrical Output Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	T_Baud		36		58	Gsym/s
Output Differential Voltage	T_Vdiff	. See Note 1, 3.			1200	mVppd
DC Common mode Voltage	T_Vcm	See Note 3.	0		1.9	V
Output AC Common Mode Voltage	T_VcmAC	See Note 2, 3.			30	mVrms
Single-ended Transmitter Output Voltage	T_Vse	See Note 1, 3.	-0.3		1.9	V
Effective return loss (ERL)		See Section 26.3.1.3	9			dB
Common Mode Output Return Loss	T_SCC22	Equation (26-3)				dB
Level Separation Mismatch Ratio	T_RLM	See Note 1, 3, 4. 5	0.95			-
Steady-state Voltage	T_Vf		0.4		0.6	V
Linear Fit Pulse Peak	T_Pk		0.69 × T_Vf			V
Signal-to-Noise-and-Distortion-Ratio	T_SNDR		32.5			dB

NOTES:
1. Signals are specified as measured through a fourth-order Bessel-Thomson low-pass response with 43 GHz 3 dB bandwidth.
2. Sampling oscilloscopes will not be able to pattern lock and may substitute 40GHz bandwidth limit with compensation for the reduced bandwidth.
3. Measured as described in Section 26.3.1.2. T_Vdiff min is set by the steady-state voltage T_Vf min.
4. Measured as described in Section 26.3.1.6
5. T_RLM is defined in Appendix 16.C.4.3.

Table 26-4. Transmitter Output Jitter Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Uncorrelated Jitter (time interval from 0.0005% to 99.9995% of the probability distribution)	T_J_{5u}	See Note 1			0.128	UI
Uncorrelated jitter RMS (standard deviation of the probability distribution)	T_J_{RMS}				0.023	UIrms
Even-Odd Jitter	T_EOJ				0.025	UIpp

NOTES:
1. Measured as described in Section 26.3.1.7.

26.3.1.1 Transmitter Baud Rate

All devices shall work within the range from 36 Gsym/s to 58 Gsym/s as specified for the device, with the baud rate tolerance as per Section 3.2.11. A CEI implementation complies to the specifications of this clause over the range of baud rates stated for the implementation within this range.

26.3.1.2 Transmitter Amplitude and Swing

The differential output voltage T_Vdiff is defined to be True minus Complement. The common-mode output voltage T_Vcm is defined to be one half of the sum of True and Complement. These definitions are illustrated in Section 1.6.1.

For a QPRBS13-CEI test pattern (Appendix 16.C.3.1), the peak-to-peak value of the differential output voltage (T_Vdiff) shall be less than or equal to the limit given in Table 26-3 regardless of the transmit equalizer setting.

The DC common-mode output voltage (T_Vcm) shall be within the limits in Table 26-3 with respect to local ground.

The AC common-mode output voltage (T_VcmAC) shall be less than or equal to the limit given in Table 26-3 with respect to local ground. Common-mode output voltage requirements shall be met regardless of the transmit equalizer setting.

The single-ended transmitter output voltage (T_Vse) shall be within the limits in Table 26-3 with respect to local ground.

The transmitter shall be capable of providing a differential steady state output amplitude ($2xT_V_f$) between 800 and 1200 mVppd with transmit emphasis disabled.

Transmitter differential output amplitude shall additionally adhere to the requirements in Section 26.3.1.6.

Power-down behavior is beyond the scope of CEI IA.

26.3.1.3 Transmitter Return Loss

ERL of the transmitter at compliance point T is computed using the procedure in 93A.5 [28] with the values in Table 26-5. Parameters that do not appear in Table 26-5 take values from Table 26-1. The value of T_{fx} is 0. N_{bx} is set to the value of N_b in Table 26-1.

Table 26-5. Transmitter and Receiver ERL Parameter Values

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	0.531	UI
Incremental available signal loss factor	β_x	0	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.618	-
Length of the reflection signal	N	200	UI

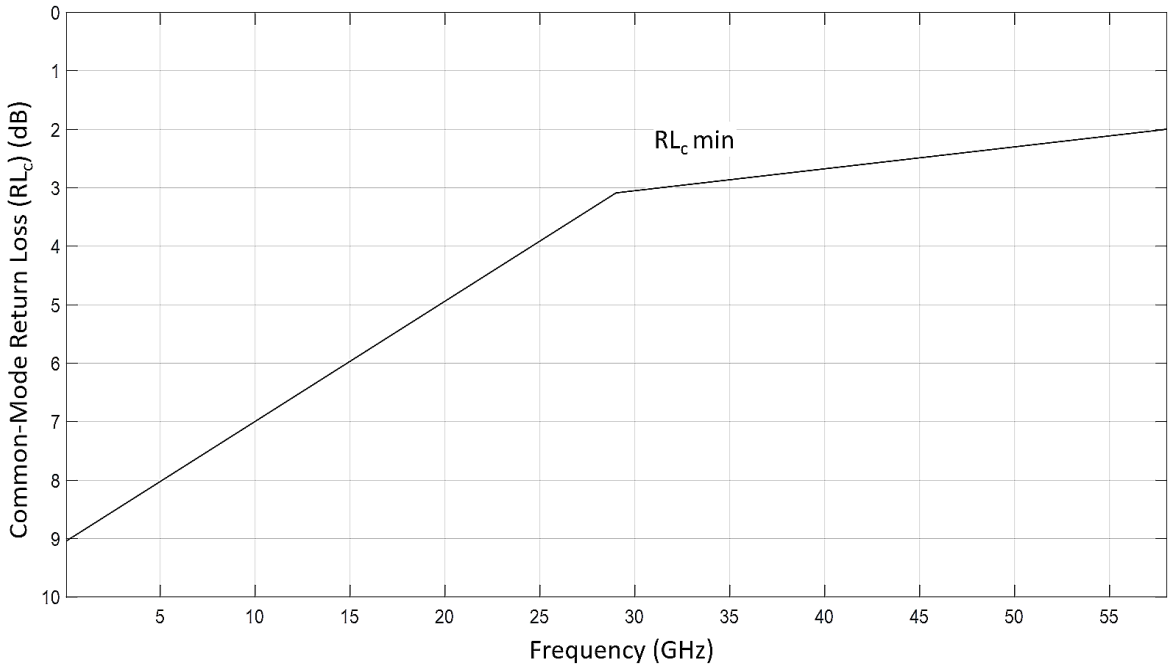
Transmitter ERL at T shall be greater than or equal to 9 dB.

This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements shall be 100 Ω.

The common-mode output return loss, in dB, of the transmitter shall meet Equation (26-3), where f is the frequency in GHz. The common-mode return loss limit $RL_C(f)$ is shown in Figure 26-3. This output impedance requirement applies to all valid output levels. The reference impedance for common-mode return loss measurements shall be 25 Ω.

$$RL_C(f) \geq RL_c min(f) = \begin{cases} 9.05 - 0.2056\left(\frac{f \times 58}{f_b}\right), & 0.05 \leq f \leq 0.5 f_b \\ 4.175 - 0.0375\left(\frac{f \times 58}{f_b}\right), & 0.5 f_b < f \leq f_b \end{cases} \quad (dB) \qquad (26\text{-}3)$$

Figure 26-3.Transmitter common mode return loss limit for 58 Gsym/s.



26.3.1.4 Transmitter Lane-to-Lane Skew

Please refer to Section 3.2.7.

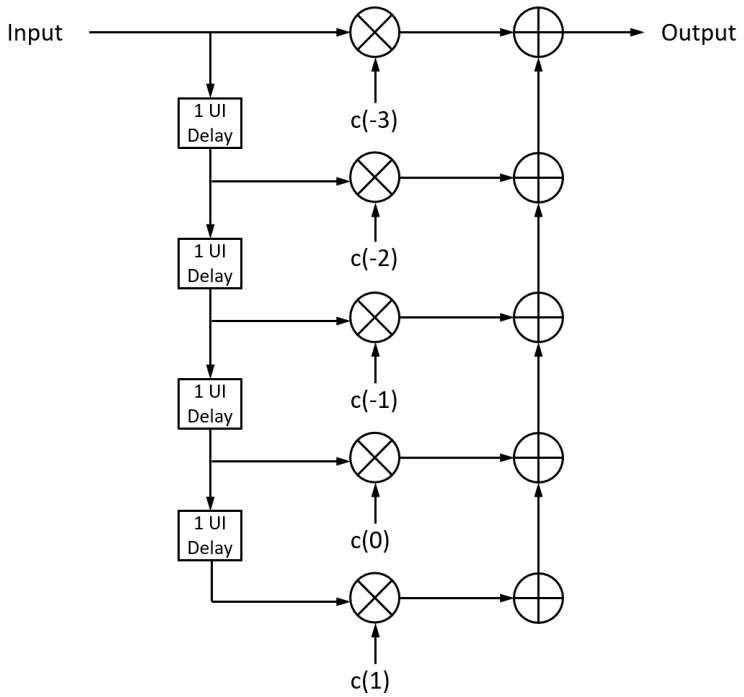
26.3.1.5 Transmitter Short Circuit Current

Please refer to Section 3.2.9.

26.3.1.6 Transmitter output waveform requirements

The transmitter function includes programmable equalization to compensate for the frequency-dependent loss of the channel and facilitate data recovery at the receiver. The functional model for the transmit equalizer is the five tap transversal filter shown in Figure 26-4.

Figure 26-4.Transmit equalizer functional model



Link budgets in this document assume optimized TX FIR equalization that is part of the system management function. The specific implementation is outside the scope of this document.

26.3.1.6.1 Linear fit to the measured waveform

The following test procedure defines linear fit pulse response, linear fit error e(k) (see Section 11.3.1.6.4) and normalized transmitter coefficient values.

For each configuration of the transmit equalizer, capture at least one complete cycle of the QPRBS13-CEI test pattern (Appendix 16.C.3.1) at the TX package ball (see Figure 26-1).

Compute the linear fit pulse response p(k) from the captured waveform per Section 11.3.1.6.2 using Np = 19 and Dp = 4. For aligned symbol values x(n) use -1, -ES1, ES2, and 1 to represent symbol values of -1, -1/3, 1/3, and 1, respectively, and where ES1 and ES2 are the effective symbol levels determined in Appendix 16.C.4.3.

Define r(k) to be the linear fit pulse response when transmit equalizer coefficients have been set to the “preset” values (see Section 11.3.1.6.1).

For each configuration of the transmit equalizer, compute the normalized transmit equalizer coefficients, c(i), according to Section 11.3.1.6.2 - Section 11.3.1.6.5.

26.3.1.6.2 Steady-state voltage and linear fit pulse peak

The linear fit pulse, p(k), is determined according to the linear fit procedure in Section 11.3.1.6.2 - Section 11.3.1.6.5, as modified by Section 26.3.1.6.1. The steady-state voltage T_Vf is defined to be the sum of the linear fit pulse p(k) divided by M, as shown in Equation (11-12). However, Np=18 for this calculation.

The steady-state voltage, T_Vf, shall satisfy the requirements in Table 26-3.

The linear fit pulse peak, T_Pk, is the highest value of p(k). It shall satisfy the requirement in Table 26-3.

26.3.1.6.3 Transmitter equalizer coefficients

Table 26-6. Coefficient Range and Step Size

Coefficients	Normalized Amplitude		Normalized Step Size (%)
	Min (%)	Max (%)	
c(-3)	-6	0	0.5 to 2.5
c(-2)	0	12	0.5 to 2.5
c(-1)	-34	0	0.5 to 2.5
c(1)	-20	0	0.5 to 2.5
c(0)	54	100	0.5 to 2.5

The normalized amplitudes of the coefficients of the transmitter equalizer (computed per Section 26.3.1.6.1) shall meet the requirements in Table 26-6. "min" is defined as the minimum normalized amplitude of the coefficient that must be supplied by the transmitter to be compliant. "max" is defined as the maximum normalized amplitude of the coefficient that must be supplied by the transmitter to be compliant.

The amplitude of a coefficient can be computed by multiplying its normalized amplitude by T_Vf, which is defined in Section 26.3.1.6.2.

The peak-to-peak output voltage is approximated by

$$(|c(-3)| + |c(-2)| + |c(-1)| + |c(0)| + |c(1)|) * 2 * T_Vf \quad (26\text{-}4)$$

and should not exceed the limit for T_Vdiff given in Table 26-3.

26.3.1.6.4 Transmitter Output Noise and Distortion

Signal-to-noise-and-distortion ratio (SNDR) is measured at the transmitter output using the following method, with the transmitter on the lane under test transmitting QPRBS13-CEI and transmitters on lanes not under test enabled and transmitting QPRBS31-CEI test pattern as defined in Appendix 16.C.3.2, or a valid CEI signal, or transmitting the same pattern with a slightly different Baud rate on each lane so that lane to lane signals are asynchronous. These transmitters shall have identical transmit equalizer settings to the transmitter under test.

Compute the linear fit to the captured waveform and the linear fit pulse response, p(k), and error, e(k), according to Section 26.3.1.6.1. Denote the standard deviation of e(k) as σ_e.

With the QPRBS13-CEI pattern and the same configuration of the transmit equalizer, measure the RMS deviation from the mean voltage at a fixed point in a run of at least 6 consecutive identical PAM4 symbols. The RMS deviation is measured for a run of each of the four PAM4 symbol levels.The average of the four measurements is denoted as σ_n.

SNDR is defined by Equation (26-5) where p_{max} is the maximum value of p(k).

$$SNDR = 10\log_{10}\left(\frac{p_{max}^2}{\sigma_e^2 + \sigma_n^2}\right)(dB) \quad (26\text{-}5)$$

SNDR shall be greater than 32.5 dB for any allowable transmit equalizer setting.

26.3.1.7 Transmitter output jitter

Jitter measurements in this sub-clause are performed with transmitters on physical lanes not under test enabled and transmitting QPRBS31-CEI test pattern as defined in Appendix 16.C.3.2, or a valid CEI signal, or transmitting the same pattern with a slightly different Baud rate on each lane so that lane to lane signals are asynchronous. These transmitters shall have identical transmit equalizer settings to the transmitter under test.

J_{5u}, J_{RMS}, and EOJ are defined by measurements of 12 specific transitions in a QPRBS13-CEI pattern in order to exclude short-term correlated jitter. The 12 transitions represent all possible combinations of four identical symbols followed by two different identical symbols as shown in Table 26-7. The sequences are located by the symbol indices given in the table where symbols 1 to 7 are the run of seven +1s.

Alternatively, EOJ can be defined by measurements of 12 specific transitions in a QPRBS9-CEI pattern (see Appendix 25.G) in order to exclude short-term correlated jitter. The 12 transitions represent all possible combinations of two to five identical symbols followed by two different identical symbols as shown in Table 26-8. The sequences are located by the symbol indices given in the table where symbols 1 to 5 are the run of five +1s.

The threshold used to define each transition is given in Table 26-7 and Table 26-8 where V_{-1}, $V_{-1/3}$, $V_{1/3}$, and V_1 are as defined in Appendix 16.C.4.3.

The jitter is measured with a clock from a clock recovery unit (CRU) (i.e., a first order golden PLL, with corner frequency at f_b/13280, and a 20 dB/decade slope, see Section 1.6) as the trigger or reference clock.

Table 26-7. QPRBS13-CEI Pattern Symbols Used for Jitter Measurement

Label	Description	Gray Coded PAM4 Symbols	Index of First Symbol	Index Transition Begins	Index Transition Ends	Index of Last Symbol	Threshold Level
REF	Reference for symbol index	3333333	1	--	--	7	--
R03	0 to 3 rise	10000 330	1830	1834	1835	1837	$(V_{-1}+V_1)/2$
F30	3 to 0 fall	23333 001	1269	1273	1274	1276	
R12	1 to 2 rise	0111111 2222221	3638	3644	3645	3651	$(V_{-1/3}+V_{1/3})/2$
F21	2 to 1 fall	022222 113	1198	1203	1204	1206	
R01	0 to 1 rise	100000 113	6835	6840	6841	6843	$(V_{-1}+V_{-1/3})/2$
F10	1 to 0 fall	21111 003	2992	2996	2997	2999	
R23	2 to 3 rise	32222 330	6824	6828	6829	6831	$(V_{1/3}+V_1)/2$
F32	3 to 2 fall	033333 2222223	7734	7739	7740	7746	
R02	0 to 2 rise	10000 223	3266	3270	3271	3273	$(V_{-1}+V_{1/3})/2$
F20	2 to 0 fall	122222 0000002	7282	7287	7288	7294	
R13	1 to 3 rise	011111 331	133	138	139	141	$(V_{-1/3}+V_1)/2$
F31	3 to 1 fall	23333 112	7905	7909	7910	7912	

Table 26-8. QPRBS9-CEI Pattern Symbols Used for Jitter/EOJ Measurement

Label	Description	Gray Coded PAM4 Symbols	Index of First Symbol	Index Transition Begins	Index Transition Ends	Index of Last Symbol	Threshold Level
REF	Reference for symbol index	33333	1	--	--	5	--
R03	0 to 3 rise	1000 331	260	263	264	266	$(V_{-1}+V_1)/2$
F30	3 to 0 fall	233333 001	511	5	6	8	
R12	1 to 2 rise	311 2221	464	466	467	470	$(V_{-1/3}+V_{1/3})/2$
F21	2 to 1 fall	122 11110	254	256	257	261	
R01	0 to 1 rise	200 113	503	505	506	508	$(V_{-1}+V_{-1/3})/2$
F10	1 to 0 fall	21111 0003	256	260	261	264	
R23	2 to 3 rise	3222 330	210	213	214	216	$(V_{1/3}+V_1)/2$
F32	3 to 2 fall	133 223	507	509	510	1	
R02	0 to 2 rise	200 22223	63	65	66	70	$(V_{-1}+V_{1/3})/2$
F20	2 to 0 fall	12222 001	321	325	326	328	
R13	1 to 3 rise	0111 331	166	169	170	172	$(V_{-1/3}+V_1)/2$
F31	3 to 1 fall	033 1112	263	265	266	269	

It is acceptable to meet the EOJ requirement with either QPRBS13 or QPRBS9 test pattern.

26.3.1.7.1 J_{5u} and J_{RMS} Jitter

For each transition i, 1 ..i ..12, of the transitions specified in Table 26-7, obtain a set S_i = {$t_i(1)$, $t_i(2)$, ...} of transition times modulo the period of the pattern. The 12 sets should be of equal size and the size of all sets should be chosen to enable calculation of J_{5u} (as defined below) with sufficient accuracy.

Calculate the average of each set S_i, $Tavg_i$, and subtract it from all elements of that set, to create a set $S0_i$ = {$t_i(1)$ - $Tavg_i$, $t_i(2)$ - $Tavg_i$, ...}.

Combine the sets $S0_i$, i=1 to 12, to create an estimated probability distribution $f_J(t)$.

J_{5u} is defined as the time interval that includes all but 10^{-5} of $f_J(t)$, from the 0.0005th to the 99.9995th percentile of $f_J(t)$.

J_{RMS} is defined as the standard deviation of $f_J(t)$.

26.3.1.7.2 Even-Odd Jitter (EOJ)

For one of the 12 specific transitions in QPRBS13-CEI in Table 26-7, or QPRBS9-CEI in Table 26-8:

a) Trigger once in 3 repeats of the QPRBS13-CEI or QPRBS9-CEI test pattern.

Obtain the mean time (T3) for this transition in the first QPRBS13-CEI or QPRBS9-CEI.

Obtain the mean time (T4) for the same transition in the second QPRBS13-CEI or QPRBS9-CEI.

b) The difference between the two means (T4 – T3), is the estimated period of the repeating pattern.

For each of the 12 specific transitions in QPRBS13-CEI in Table 26-7, or in QPRBS9-CEI in Table 26-8.

1) Trigger once in 2 repeats of the QPRBS13-CEI or QPRBS9-CEI test pattern.

Obtain the mean time (T1) for the specific transition in the first QPRBS13-CEI or QPRBS9-CEI.

Obtain the mean time (T2) for the same transition in the second QPRBS13-CEI or QPRBS9-CEI.

2) Calculate EOJ for this transition as |(T2 – T1) – (T4 – T3)|.

EOJ is the maximum of the 12 measurements.

NOTE: Both of (T2 - T1) and (T4 - T3) are about 8191 UI for QPRBS13-CEI, or 511 UI for QPRBS9-CEI, which is much larger than the EOJ value. Hence, each of T1 through T4 should have high precision.

26.3.2 Receiver Characteristics

A compliant receiver shall autonomously operate at the specified BER with the worst case combination of a compliant transmitter and a compliant channel. The receiver also shall not cause error propagation that violates the error burst length requirement as defined in Section 26.2.2. Further receiver electrical requirements at compliance point R (see Figure 26-1) are specified in Table 26-9, with the receiver interference tolerance parameters specified in Table 26-10. Lanes not under test should be enabled and transmitting or receiving asynchronous or uncorrelated signals.

Table 26-9. Receiver Electrical Input Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	R_Baud		36		58	Gsym/s
Effective return loss (ERL)		See Section 26.3.1.3	9			dB
Differential to Common Mode Input Conversion	R_SCD11		Equation (26-6)			dB
Interference Tolerance		Table 26-10				
Jitter Tolerance		Table 26-11				

Table 26-10. Receiver interference tolerance parameters (Note 2)

Parameter	Test 1 values		Test 2 values		Units
	Min	Max	Min	Max	
Pre-FEC Bit Error Ratio (BER)		10^{-6}		10^{-6}	
COM, including effects of broadband noise		3		3	dB
Insertion loss at Nyquist, Note 1		10		20	dB
RSS_DFE4. Note 2	0.025	-	0.05	-	

NOTES:
1. Measured between TX and RX package balls (see Figure 26-1).
2. Definition can be found in Annex 93A of IEEE Std 802.3 [27]. See Section 26.3.2.4.

26.3.2.1 Input Baud Rate

All devices shall work within the range from 36 Gsym/s to 58 Gsym/s as specified for the device, with the baud rate tolerance as per Section 3.2.11. A CEI implementation complies to the specifications of this clause over the range of baud rates stated for the implementation within this range.

26.3.2.2 Reference Input Signals

The receiver shall accept differential input signal amplitudes produced by a compliant transmitter connected with the minimum attenuation specified in Figure 26-2 to the receiver. This may be larger than the 1200 mVppd maximum of the transmitter due to output/input impedances and reflections.

The minimum input amplitude is defined by the minimum transmitter amplitude, the actual receiver input impedance and the loss of the actual PCB. Note that the minimum transmitter amplitude is defined using a well controlled load impedance, however the real receiver is not, which can leave the receiver input signal smaller than expected.

26.3.2.3 Input Return Loss

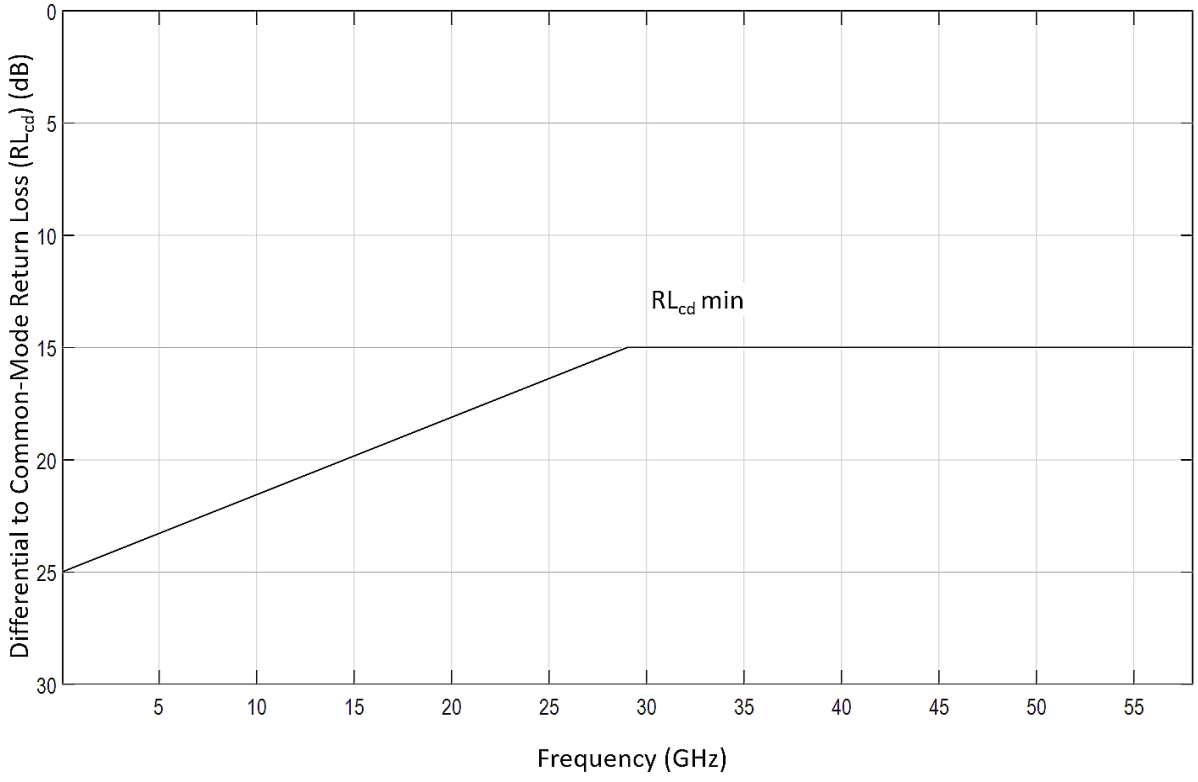
ERL of the receiver at compliance point R is computed using the procedure in 93A.5 [28] with the values in Table 26-5. Parameters that do not appear in Table 26-5 take values from Table 26-1. The value of T_{fx} is 0. N_{bx} is set to the value of N_b in Table 26-1.

Receiver ERL at compliance point R shall be greater than or equal to ERL value in Table 26-9.

The reference impedance for differential return loss measurements shall be 100 Ω. The differential to common-mode return loss, in dB, of the receiver shall meet Equation (26-6). The differential to common-mode return loss limit $RL_{cd}(f)$ is shown in Figure 26-5.

$$RL_{cd}(f) \geq RL_{cd}min(f) = \begin{pmatrix} 25 - 0.34485\left(\frac{f \times 58}{f_b}\right), & 0.05 \leq f \leq 0.5f_b \\ 15, & 0.5f_b < f \leq f_b \end{pmatrix}(dB) \quad (26\text{-}6)$$

Figure 26-5.Receiver differential to common-mode return loss limit for 58 Gsym/s.



26.3.2.4 Receiver Interference Tolerance

The receiver interference tolerance test is based on the test defined in Annex 120D.3.2.1 of IEEE Std 802.3 [27].

The receiver on each lane shall meet the pre-FEC BER requirement with channels matching the Channel Operating Margin (COM) and loss parameters for Test 1 and Test 2 in Table 26-10.

The test channel should be created using printed circuit boards with short interconnecting cables.

The following considerations apply to the interference tolerance test. The transmitter package is omitted in the COM calculation. The Test transmitter's measured SNDR should be used for SNR_{TX} in the COM calculation. The transmitter output levels are set such that R_{LM} is equal to 0.95. The test transmitter meets the specifications in Section 26.3.1. The test transmitter is constrained such that for any transmitter equalizer setting the differential peak-to-peak voltage is less than 800 mV, and the normalized amplitudes of the coefficients of the transmitter equalizer c(-3), c(-2), c(-1), c(0) and c(1) are between the minimum and maximum limits given in Table 26-6.

The lower frequency bound for the noise spectral density constraints, f_{NSD1}, is 1 GHz. The ERL of the test channel at TP5 (as defined in Annex 93A of IEEE Std 802.3 [27], IEEE Std 802.3cd [28] and IEEE Std 802.3ck [29]) shall meet the requirements in Section 26.3.2.3, and be 3 dB better. The test transmitter's jitter parameters J_{5u} and J_{RMS} are measured. A_{DD} and σ_{RJ} are calculated from the measured values of J_{5u} and J_{RMS} using Equation (26-7), and Equation (26-8), respectively and used for COM parameters. Other COM parameters are set according to the values in Table 26-1. The broadband noise is added and adjusted to achieve the COM value in Table 26-10. The test pattern to be used is QPRBS31-CEI defined in Appendix 16.C.3.2. A test system with a fourth-order Bessel-Thomson low-pass response with 43 GHz 3 dB bandwidth is to be used for measurement of the signal applied by the pattern generator and for measurements of the broadband noise.

$$A_{DD} = \left(\frac{J_{5u}}{2} + Q_{5d} \sqrt{(Q_{5d}^2 + 1) \times J_{RMS}{}^2 - \left(\frac{J_{5u}}{2} \right)^2} \right) / (Q_{5d}^2 + 1) \quad (26\text{-}7)$$

$$\sigma_{RJ} = \left(\frac{J_{5u}}{2} - A_{DD} \right) / (Q_{5d}) \quad (26\text{-}8)$$

where Q_{5d} = 4.2649.

NOTE 1—Q_{5d} is an approximated solution of $Q(Q_{5d}) = 1 \times 10^{-5}$. Q(x) is the Normal probability density function.

NOTE 2—Calculation of A_{DD} requires that the term in the square-root in Equation (26-7) be positive. If this does not hold, a different transmitter should be used in the test setup.

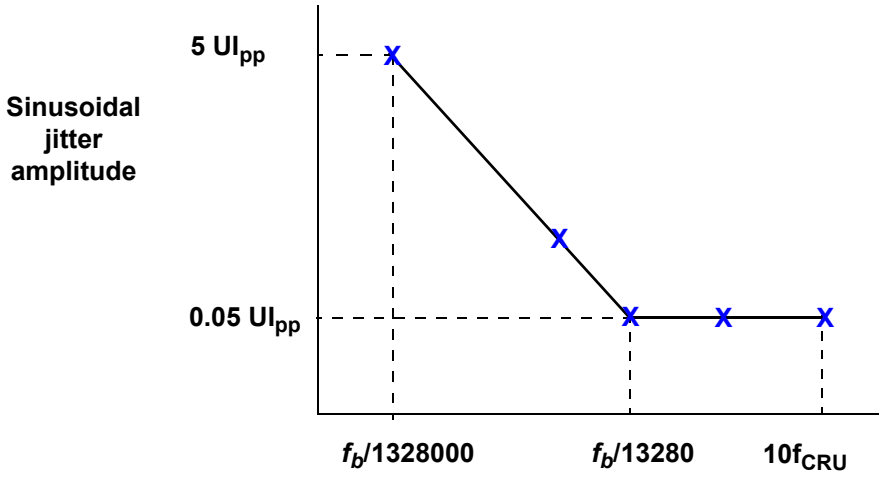
26.3.2.5 Receiver Jitter Tolerance

Receiver jitter tolerance shall meet the conditions and parameters defined in Table 26-11. This sinusoidal jitter is part of the jitter applied in the stressed input test. The sinusoidal jitter is calibrated at 10x the reference CRU's bandwidth and must be tested at $f_{CRU}/100$, $f_{CRU}/3$, f_{CRU}, $3f_{CRU}$, and $10f_{CRU}$, where f_{CRU} is the jitter corner frequency given by $f_b/13280$, with sinusoidal jitter of 5 UI, 0.15 UI, 0.05 UI, 0.05 UI, and 0.05 UI respectively. For this test the channel used is as for the receiver interference tolerance described in Section 26.3.2.4. Note that the values measured for J5u and JRMS include the effects of this added sinusoidal jitter. Noise is added to obtain a COM of 3 dB with these measured jitter values as for the interference tolerance test. The receiver bit error ratio (BER) shall meet the requirements of Section 26.2.2 for each pair of jitter frequency and peak-to-peak amplitude values listed above and shown in Figure 26-6.

Table 26-11. Receiver Jitter Tolerance Parameters

Frequency Range	Sinusoidal jitter, peak-to-peak (UI)
$f < f_b/1328000$	Not Specified
$f_b/1328000 < f \leq f_b/13280$	$5*f_b/(1328000*f)$
$f_b/13280 < f \leq 10f_{CRU}$	0.05

Figure 26-6. Receiver Jitter Tolerance Mask



26.3.2.6 Single Ended Input Voltage

The single ended voltage levels with respect to the receiver ground at the input of the receiver are dependent on the transmitter implementation and the inter-ground difference. The voltage levels at the input of an AC coupled receiver (if the effective AC

coupling is done within the receiver) or at the TX side of the external AC coupling cap (if AC coupling is done externally) will be between -0.35V and 1.95V with respect to local ground.

26.3.2.7 Input Lane-to-Lane Skew

Refer to Section 3.2.8.

27 CEI-112G-LR-PAM4 Long Reach Interface

This clause details the requirements for the CEI-112G-LR-PAM4 long reach high speed electrical interface between nominal baud rates of 36.0 Gsym/s and 58.0 Gsym/s using PAM4 coding. A compliant device shall meet all of the requirements listed below. The electrical interface is based on high speed, low voltage logic. Connections are point-to-point balanced differential pairs and signaling is unidirectional.

The electrical IA is based on loss and jitter budgets and defines the characteristics required to communicate between a CEI-112G-LR-PAM4 transmitter and a CEI-112G-LR-PAM4 receiver using copper signal traces on a printed circuit board. The use of cables to replace or partially replace the copper signal traces on the printed circuit board is acceptable and may extend the physical length of the connection. The characteristic impedance of the signal paths is nominally 100 Ω differential. The signal path or channel between a transmitter and a receiver shall meet the channel operating margin (COM), a method and a threshold quantity used for channel compliance.

CEI-112G-LR-PAM4 assumes using forward error correction (FEC) to achieve the bit error ratio (BER) target. The FEC guidances are described in Appendix 16.D.

Long reach CEI-112G-LR-PAM4 devices from different manufacturers shall be interoperable.

27.1 Requirements

1. Support serial baud rates (f_b) within the range from 36.0 Gsym/s to 58.0 Gsym/s as specified for the device using PAM4 coding. A CEI implementation complies to the specifications of this clause over the range of baud rates stated for the implementation within this range.
2. Capable of achieving a raw Bit Error Ratio (BER) of 10^{-4} or better per lane. FEC is assumed to be used in the system to achieve corrected BER of 10^{-15} or better per lane. The baud rate includes the overhead required for FEC. The definition of FEC is outside the scope of this IA (see Appendix 16.D).
3. Capable of driving up to 1000 mm of backplane and up to 2 connectors.
4. Shall support AC-coupled operation.
5. Shall allow multi-lanes (1 to n).
6. Shall support hot plug.

27.2 General Requirements

27.2.1 Data Patterns

See Appendix 16.C.5.

27.2.2 Bit Error Ratio

A raw Bit Error Ratio (BER) better than or equal to 10^{-4} is required on each lane. A compliant receiver, when receiving from a compliant transmitter over a compliant channel, shall deliver the specified raw BER to the subsequent FEC decoder. Error bursts with length more than 126 PAM4 symbols delivered to the PAM4 decoder shall occur with a probability of less than 1 in 10^{20} PAM4 symbols. To enable a more practical test, the error bursts with length more than 61 PAM4 symbols delivered to the PAM4 decoder should occur with a probability of less than 1 in 10^{12} PAM4 symbols.See Appendix 16.D.

27.2.3 Ground Differences

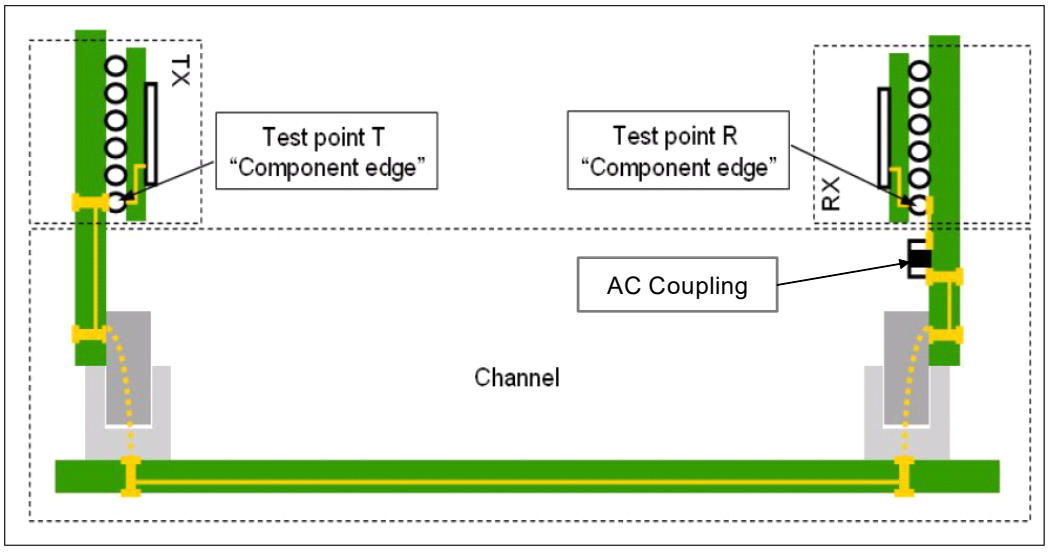
Please refer to Section 3.2.4.

27.2.4 Channel Compliance

A forward channel and associated dominant crosstalk channels are deemed compliant if the channel characteristics conform to the requirements defined in this section.

27.2.4.1 Reference Model

Figure 27-1.CEI-112G-LR-PAM4 Reference Model



Note: Test points differ from definitions in Section 1.8, as an AC-coupling capacitor, if physically located outside of the package, is part of the channel.

The channel is defined between test point T and test point R.

27.2.4.2 Channel Operating Margin

For an informative introduction into the Channel Operating Margin method, please refer to Appendix 25.D. The Channel Operating Margin (COM) of the channel is computed using the procedure in Annex 93A of IEEE Std 802.3 [27] as modified by IEEE Std 802.3ck [29], with the Test 1 and Test 2 values in Table 27-1. Test 1 and Test 2 differ in the value of the device package model transmission line length z_p. An informative package model overview can be found in Appendix 25.F. For engineered links, the length and electrical properties of the package for Test 2 can be modified based on the actual package.

Table 27-1. COM Parameter Values

Parameter	Symbol	Value	Units
Signaling rate	f_b	36.0 - 58.0	Gsym/s
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package (PKG) model Single-ended device capacitance Single-device series inductance Single-ended capacitance at the device-to-pkg IF Transmission line length, Test 1 Transmission line length, Tx Test 2 Transmission line length, Rx Test 2 Transmission line 2 length Single-ended PKG capacitance at pkg-to-board IF Transmission line characteristic impedance Transmission line 2 characteristic impedance	 C_d L_s C_b z_p z_p z_p z_{p2} C_p Z_c Z_{c2}	 120 120 30 12 31 29 1.8 87 87.5 92.5	 fF pH fF mm mm mm mm fF Ω Ω
Transmission line parameter Transmission line parameter Transmission line parameter Transmission line parameter	γ_0 τ a_1 a_2	0 6.141×10^{-3} 9.909×10^{-4} 2.772×10^{-4}	1/mm ns/mm $ns^{1/2}/mm$ ns/mm
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	50	Ω
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.50	—
Transmitter equalizer, 3rd pre-cursor coefficient Minimum value Maximum value Step size	$c(-3)$	 -0.06 0 0.02	 — — —

Table 27-1. COM Parameter Values

Transmitter equalizer, 2nd pre-cursor coefficient Minimum value Maximum value Step size	$c(-2)$	 0 0.12 0.02	 — — —
Transmitter equalizer, 1st pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.34 0 0.02	 — — —
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.2 0 0.02	 — — —
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –20 -2 1	 dB dB dB
Continuous time filter, DC gain2 Minimum value Maximum value Step size	g_{DC2}	 –6 0 1	 dB dB dB
Continuous time filter, scaled zero frequency	f_z	f_b /2.5	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	f_b /2.5 f_b	GHz GHz
Continuous time filter, low frequency pole/scaled zero	f_{LF}	f_b /80	GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.413 0.413 0.608	 V V V
Number of signal levels	L	4	—
Level separation mismatch ratio	R_{LM}	0.95	—
Transmitter signal-to-noise ratio	SNR_{TX}	33	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	12	UI
Normalized DFE coefficient maximum limit for n = 1 to N_b	$b_{max}(1)$ $b_{max}(2\text{-}3)$ $b_{max}(4\text{-}N_b)$	0.85 0.3 0.2	— — —
Normalized DFE coefficient minimum limit for n = 1 to N_b	$b_{min}(1)$ $b_{min}(2)$ $b_{min}(3\text{-}N_b)$	0.3 0.05 -0.03	— — —
Number of DFE floating tap groups	N_{bg}	3	—

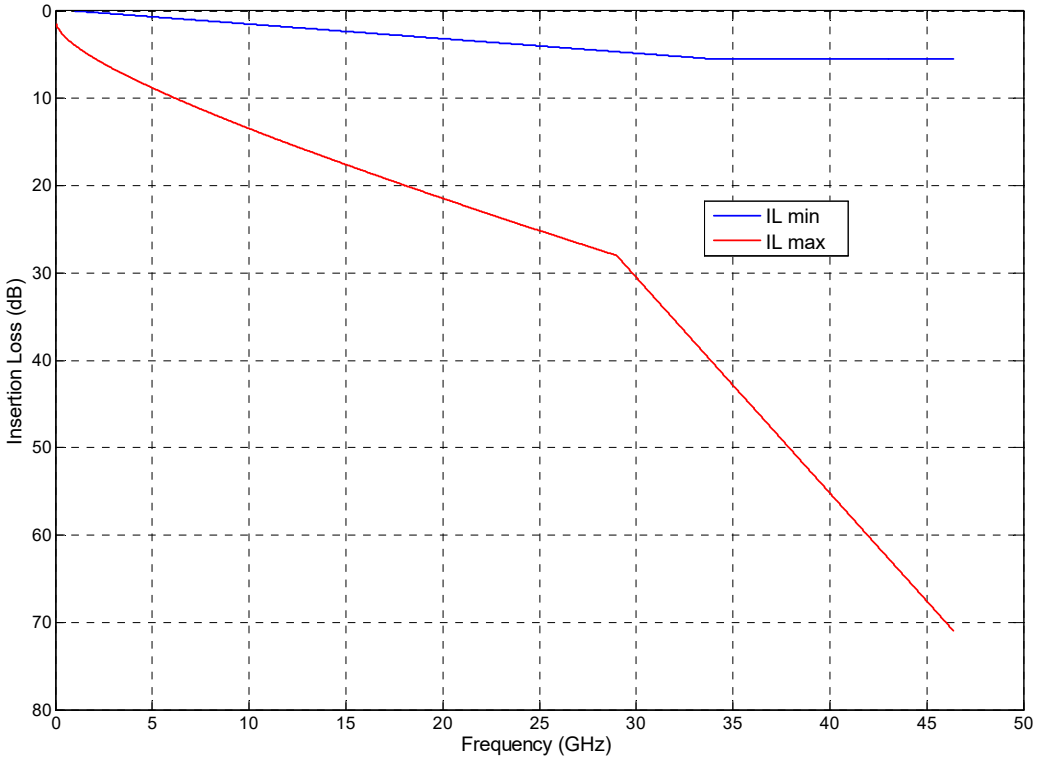
Table 27-1. COM Parameter Values

Number of DFE floating taps per group	N_{bf}	3	—
DFE maximum span including floating taps	N_f	40	UI
Normalized DFE coefficient magnitude limit for floating taps	B_{maxf}	0.05	—
DFE floating tap tail root-sum-of-squares limit	$\sigma tmax$	0.02	—
DFE floating tap tail starting position	Nts	25	UI
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.02	UI
One-sided noise spectral density	η_0	8.2×10^{-9}	V^2/GHz
Target detector error ratio	DER_0	10^{-4}	—
Channel operating margin, min	*COM*	3.0	dB

Using Tr = 0.3984 UI, in Equation (93A–46) [27], COM shall be greater than or equal to 3.0 dB for each test. This minimum value allocates margin for practical limitations on the receiver implementation, and the largest step size allowed for transmitter equalizer coefficients.

27.2.4.3 Informative Channel Insertion Loss

Figure 27-2.Channel Insertion Loss Limit for 58.0 Gsym/s



$$IL_{max} = \begin{bmatrix} 0.998 + 2.397\sqrt{\frac{f \times 58}{f_b}} + 0.486\frac{f \times 58}{f_b}, & f_{min} \le f \le f_b/2 \\ -43.63 + 2.47\frac{f \times 58}{f_b}, & f_b/2 < f \le 0.8 f_b \end{bmatrix} \quad (27\text{-}1)$$

$$IL_{min} = \begin{bmatrix} 0, & f_{min} \le f \le 1GHz \\ \frac{1}{6}(f-1), & 1GHz < f \le 34GHz \\ 5.5, & 34GHz < f \le 0.8 f_b \end{bmatrix} \quad (27\text{-}2)$$

Channel insertion loss is an informative recommendation.

The channel must comply with the normative specification in Section 27.2.4.2.

27.2.4.4 Channel Effective Return Loss (ERL)

The background of ERL is described in the informative Appendix 25.E. ERLs of the channel (between test points T and R) are computed at test point T and at test point R using the procedure in 93A.5 [27] with the values in Table 27-2. Parameters that do not appear in Table 27-2 take values from Table 27-1. The value of T_{fx} is 0. N_{bx} is set to the value of $N_b+N_{bg}*N_{bf}$ in Table 27-1.

Channel ERLs shall be greater than or equal to 9.5 dB.

Table 27-2. Channel ERL Parameter Values

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	0.531	UI
Incremental available signal loss factor	β_x	0	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.618	-
Length of the reflection signal	N	3500	UI

27.2.4.5 Channel AC-coupling

The transmitter shall be AC-coupled to the receiver. The impact of an AC-coupling capacitor implemented in the channel between the package balls of the transmitter and receiver (i.e., between compliance points T and R) is accounted for within the channel specifications. Common-mode specifications are defined as if the AC-coupling capacitor is implemented in the channel between compliance points T and R. Should the capacitor not be implemented between compliance point T and compliance point R, it is the responsibility of implementers to consider any necessary modifications to common-mode and channel specifications required for interoperability as well as any impact on the verification of transmitter and receiver compliance. In particular the common-mode specifications for the transmitter in Table 27-3 may not be appropriate.

The low-frequency 3 dB cutoff of the AC-coupling shall be less than 100 kHz.

27.3 Electrical Characteristics

The electrical signaling is based on high speed low voltage logic with a nominal differential impedance of 100 Ω.

27.3.1 Transmitter Characteristics

The transmitter electrical requirements at compliance point T (see Figure 27-1) are specified in Table 27-3, and the jitter requirements are specified in Table 27-4.

Table 27-3. Transmitter Electrical Output Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	T_Baud		36		58	Gsym/s
Output Differential Voltage	T_Vdiff	. See Note 1, 3			1200	mVppd
DC Common mode Voltage	T_Vcm	See Note 3.	0		1.9	V
Output AC Common Mode Voltage	T_VcmAC	See Note 2, 3.			30	mVrms
Single-ended Transmitter Output Voltage	T_Vse	See Note 1, 3.	-0.3		1.9	V
Effective return loss (ERL)		See Section 27.3.1.3	10			dB
Common Mode Output Return Loss	T_SCC22	Equation (27-3)				dB
Level Separation Mismatch Ratio	T_RLM	See Note 1, 3, 4. 5	0.95			-
Steady-state Voltage	T_Vf		0.4		0.6	V
Linear Fit Pulse Peak	T_Pk		0.67 × T_Vf			V
Signal-to-Noise-and-Distortion-Ratio	T_SNDR		32.5			dB

NOTES:
1. Signals are specified as measured through a fourth-order Bessel-Thomson low-pass response with 43 GHz 3 dB bandwidth
2. Sampling oscilloscopes will not be able to pattern lock and may substitute 40GHz bandwidth limit with compensation for the reduced bandwidth
3. Measured as described in Section 27.3.1.2. T_Vdiff min is set by the steady-state voltage T_Vf min.
4. Measured as described in Section 27.3.1.6
5. T_RLM is defined in Appendix 16.C.4.3.

Table 27-4. Transmitter Output Jitter Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Uncorrelated Jitter (time interval from 0.05% to 99.95% of the probability distribution)	T_J_{3u}	See Note 1			0.106	UI
Uncorrelated jitter RMS (standard deviation of the probability distribution)	T_J_{RMS}				0.023	UIrms
Even-Odd Jitter	T_EOJ				0.025	UIpp

NOTES:
1. Measured as described in Section 27.3.1.7.

27.3.1.1 Transmitter Baud Rate

All devices shall work within the range from 36 Gsym/s to 58 Gsym/s as specified for the device, with the baud rate tolerance as per Section 3.2.11. A CEI implementation complies to the specifications of this clause over the range of baud rates stated for the implementation within this range.

27.3.1.2 Transmitter Amplitude and Swing

The differential output voltage T_Vdiff is defined to be True minus Complement. The common-mode output voltage T_Vcm is defined to be one half of the sum of True and Complement. These definitions are illustrated in Section 1.6.1.

For a QPRBS13-CEI test pattern (Appendix 16.C.3.1), the peak-to-peak value of the differential output voltage (T_Vdiff) shall be less than or equal to the limit given in Table 27-3 regardless of the transmit equalizer setting.

The DC common-mode output voltage (T_Vcm) shall be within the limits in Table 27-3 with respect to local ground.

The AC common-mode output voltage (T_VcmAC) shall be less than or equal to the limit given in Table 27-3 with respect to local ground. Common-mode output voltage requirements shall be met regardless of the transmit equalizer setting.

The single-ended transmitter output voltage (T_Vse) shall be within the limits in Table 27-3 with respect to local ground.

The transmitter shall be capable of providing a differential steady state output amplitude (2xT_V_f) between 800 and 1200 mVppd with transmit emphasis disabled.

Transmitter differential output amplitude shall additionally adhere to the requirements in Section 27.3.1.6.

Power-down behavior is beyond the scope of CEI IA.

27.3.1.3 Transmitter Return Loss

ERL of the transmitter at compliance point T is computed using the procedure in 93A.5 [27] with the values in Table 27-5. Parameters that do not appear in Table 27-5 take values from Table 27-1. The value of T_{fx} is 0. N_{bx} is set to the value of $N_b+N_{bg}*N_{bf}$ in Table 27-1.

Table 27-5. Transmitter and Receiver ERL Parameter Values

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	0.531	UI
Incremental available signal loss factor	β_x	0	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.618	-
Length of the reflection signal	N	200	UI

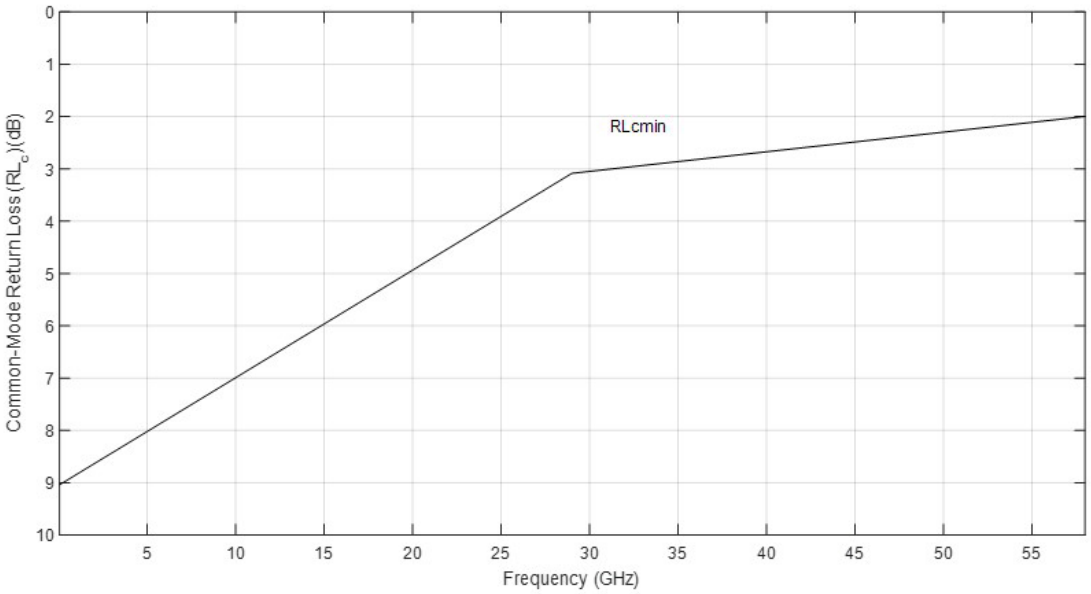
Transmitter ERL at T shall be greater than or equal to 10 dB.

This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements shall be 100 Ω.

The common-mode output return loss, in dB, of the transmitter shall meet Equation (27-3), where f is the frequency in GHz. The common-mode return loss limit $RL_C(f)$ is shown in Figure 27-3. This output impedance requirement applies to all valid output levels. The reference impedance for common-mode return loss measurements shall be 25 Ω.

$$RL_C(f) \geq RL_c min(f)) = \begin{pmatrix} 9.05 - 0.2056\left(\frac{f \times 58}{f_b}\right), & 0.05 \leq f \leq 0.5 f_b \\ 4.175 - 0.0375\left(\frac{f \times 58}{f_b}\right), & 0.5 f_b < f \leq f_b \end{pmatrix} \quad (dB) \qquad (27\text{-}3)$$

Figure 27-3.Transmitter common mode return loss limit for 58 Gsym/s



27.3.1.4 Transmitter Lane-to-Lane Skew

Please refer to Section 3.2.7.

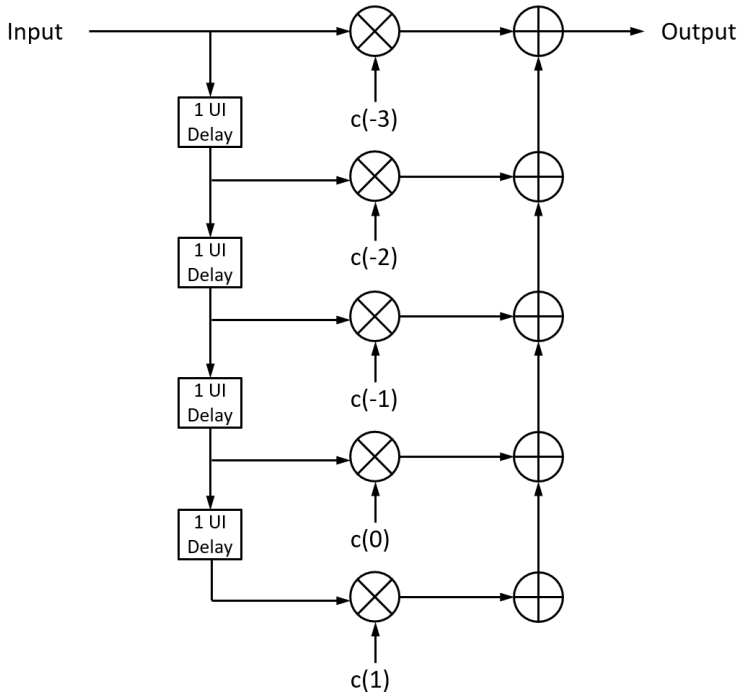
27.3.1.5 Transmitter Short Circuit Current

Please refer to Section 3.2.9.

27.3.1.6 Transmitter output waveform requirements

The transmitter function includes programmable equalization to compensate for the frequency-dependent loss of the channel and facilitate data recovery at the receiver. The functional model for the transmit equalizer is the five tap transversal filter shown in Figure 27-4.

Figure 27-4.Transmit equalizer functional model



Link budgets in this document assume optimized TX FIR equalization that is part of the system management function. The specific implementation is outside the scope of this document.

27.3.1.6.1 Linear fit to the measured waveform

The following test procedure defines linear fit pulse response, linear fit error e(k) (see Section 11.3.1.6.4), and normalized transmitter coefficient values.

For each configuration of the transmit equalizer, capture at least one complete cycle of the QPRBS13-CEI test pattern (Appendix 16.C.3.1) at the TX package ball (see Figure 27-1).

Compute the linear fit pulse response p(k) from the captured waveform per Section 11.3.1.6.2 using Np = 29 and Dp = 4. For aligned symbol values x(n) use -1, -ES1, ES2, and 1 to represent symbol values of -1, -1/3, 1/3, and 1, respectively, and where ES1 and ES2 are the effective symbol levels determined in Appendix 16.C.4.3.

Define r(k) to be the linear fit pulse response when transmit equalizer coefficients have been set to the “preset” values (see Section 11.3.1.6.1).

For each configuration of the transmit equalizer, compute the normalized transmit equalizer coefficients, c(i), according to Section 11.3.1.6.2 - Section 11.3.1.6.5.

27.3.1.6.2 Steady-state voltage and linear fit pulse peak

The linear fit pulse, p(k), is determined according to the linear fit procedure in Section 11.3.1.6.2 - Section 11.3.1.6.5, as modified by Section 27.3.1.6.1. The steady-state voltage T_Vf is defined to be the sum of the linear fit pulse p(k) divided by M, as shown in Equation (11-12). However, Np=20 for this calculation.

The steady-state voltage, T_Vf, shall satisfy the requirements in Table 27-3.

The linear fit pulse peak, T_Pk, is the highest value of p(k). It shall satisfy the requirement in Table 27-3.

27.3.1.6.3 Transmitter equalizer coefficients

Table 27-6. Coefficient Range and Step Size

Coefficients	Normalized Amplitude		Normalized Step Size (%)
	Min (%)	Max (%)	
c(-3)	-6	0	0.5 to 2.5
c(-2)	0	12	0.5 to 2.5
c(-1)	-34	0	0.5 to 2.5
c(1)	-20	0	0.5 to 2.5
c(0)	50	100	0.5 to 2.5

The normalized amplitudes of the coefficients of the transmitter equalizer (computed per Section 27.3.1.6.1) shall meet the requirements in Table 27-6. "min" is defined as the minimum normalized amplitude of the coefficient that must be supplied by the transmitter to be compliant. "max" is defined as the maximum normalized amplitude of the coefficient that must be supplied by the transmitter to be compliant.

The amplitude of a coefficient can be computed by multiplying its normalized amplitude by T_Vf, which is defined in Section 27.3.1.6.2.

The peak-to-peak output voltage is approximated by

$$(|c(-3)|+ |c(-2)| + |c(-1)| + |c(0)| + |c(1)|) * 2 * T_Vf \quad (27\text{-}4)$$

and should not exceed the limit for T_Vdiff given in Table 27-3.

27.3.1.6.4 Transmitter Output Noise and Distortion

Signal-to-noise-and-distortion ratio (SNDR) is measured at the transmitter output using the following method, with the transmitter on the lane under test transmitting QPRBS13-CEI and transmitters on lanes not under test enabled and transmitting QPRBS31-CEI test pattern as defined in Appendix 16.C.3.2, or a valid CEI signal, or transmitting the same pattern with a slightly different Baud rate on each lane so that lane to lane signals are asynchronous. These transmitters shall have identical transmit equalizer settings to the transmitter under test.

Compute the linear fit to the captured waveform and the linear fit pulse response, p(k), and error, e(k), according to Section 27.3.1.6.1. Denote the standard deviation of e(k) as σ_e.

With the QPRBS13-CEI pattern and the same configuration of the transmit equalizer, measure the RMS deviation from the mean voltage at a fixed point in a run of at least 6 consecutive identical PAM4 symbols. The RMS deviation is measured for a run of each of the four PAM4 symbol levels.The average of the four measurements is denoted as σ_n.

SNDR is defined by Equation (27-5) where p_{max} is the maximum value of p(k).

$$SNDR = 10\log_{10}\left(\frac{p_{max}^2}{\sigma_e^2 + \sigma_n^2}\right)(dB) \quad (27\text{-}5)$$

SNDR shall be greater than 32.5 dB for any allowable transmit equalizer setting.

27.3.1.7 Transmitter output jitter

Jitter measurements in this sub-clause are performed with transmitters on physical lanes not under test enabled and transmitting QPRBS31-CEI test pattern as defined in Appendix 16.C.3.2, or a valid CEI signal, or transmitting the same pattern with a slightly different Baud rate on each lane so that lane to lane signals are asynchronous. These transmitters shall have identical transmit equalizer settings to the transmitter under test.

J_{3u}, J_{RMS}, and EOJ are defined by measurements of 12 specific transitions in a QPRBS13-CEI pattern in order to exclude short-term correlated jitter. The 12 transitions represent all possible combinations of four identical symbols followed by two different identical symbols as shown in Table 27-7. The sequences are located by the symbol indices given in the table where symbols 1 to 7 are the run of seven +1s.

Alternatively, EOJ can be defined by measurements of 12 specific transitions in a QPRBS9-CEI pattern (see Appendix 25.G) in order to exclude short-term correlated jitter. The 12 transitions represent all possible combinations of two to five identical symbols followed by two different identical symbols as shown in Table 27-8. The sequences are located by the symbol indices given in the table where symbols 1 to 5 are the run of five +1s.

The threshold used to define each transition is given in Table 27-7 and Table 27-8 where V_{-1}, $V_{-1/3}$, $V_{1/3}$, and V_1 are as defined in Appendix 16.C.4.3.

The jitter is measured with a clock from a clock recovery unit (CRU) (i.e., a first order golden PLL, with corner frequency at f_b/13280, and a 20 dB/decade slope, see Section 1.6) as the trigger or reference clock.

Table 27-7. QPRBS13-CEI Pattern Symbols Used for Jitter Measurement

Label	Description	Gray Coded PAM4 Symbols	Index of First Symbol	Index Transition Begins	Index Transition Ends	Index of Last Symbol	Threshold Level
REF	Reference for symbol index	3333333	1	--	--	7	--
R03	0 to 3 rise	10000 330	1830	1834	1835	1837	$(V_{-1}+V_1)/2$
F30	3 to 0 fall	23333 001	1269	1273	1274	1276	
R12	1 to 2 rise	0111111 2222221	3638	3644	3645	3651	$(V_{-1/3}+V_{1/3})/2$
F21	2 to 1 fall	022222 113	1198	1203	1204	1206	
R01	0 to 1 rise	100000 113	6835	6840	6841	6843	$(V_{-1}+V_{-1/3})/2$
F10	1 to 0 fall	21111 003	2992	2996	2997	2999	
R23	2 to 3 rise	32222 330	6824	6828	6829	6831	$(V_{1/3}+V_1)/2$
F32	3 to 2 fall	033333 2222223	7734	7739	7740	7746	
R02	0 to 2 rise	10000 223	3266	3270	3271	3273	$(V_{-1}+V_{1/3})/2$
F20	2 to 0 fall	122222 0000002	7282	7287	7288	7294	
R13	1 to 3 rise	011111 331	133	138	139	141	$(V_{-1/3}+V_1)/2$
F31	3 to 1 fall	23333 112	7905	7909	7910	7912	

Table 27-8. QPRBS9-CEI Pattern Symbols Used for Jitter/EOJ Measurement

Label	Description	Gray Coded PAM4 Symbols	Index of First Symbol	Index Transition Begins	Index Transition Ends	Index of Last Symbol	Threshold Level
REF	Reference for symbol index	33333	1	--	--	5	--
R03	0 to 3 rise	1000 331	260	263	264	266	$(V_{-1}+V_1)/2$
F30	3 to 0 fall	233333 001	511	5	6	8	
R12	1 to 2 rise	311 2221	464	466	467	470	$(V_{-1/3}+V_{1/3})/2$
F21	2 to 1 fall	122 11110	254	256	257	261	
R01	0 to 1 rise	200 113	503	505	506	508	$(V_{-1}+V_{-1/3})/2$
F10	1 to 0 fall	21111 0003	256	260	261	264	
R23	2 to 3 rise	3222 330	210	213	214	216	$(V_{1/3}+V_1)/2$
F32	3 to 2 fall	133 223	507	509	510	1	
R02	0 to 2 rise	200 22223	63	65	66	70	$(V_{-1}+V_{1/3})/2$
F20	2 to 0 fall	12222 001	321	325	326	328	
R13	1 to 3 rise	0111 331	166	169	170	172	$(V_{-1/3}+V_1)/2$
F31	3 to 1 fall	033 1112	263	265	266	269	

It is acceptable to meet the EOJ requirement with either QPRBS13 or QPRBS9 test pattern.

27.3.1.7.1 J_{3u} and J_{RMS} Jitter

For each transition i, 1 ..i ..12, of the transitions specified in Table 27-7, obtain a set S_i = {$t_i(1)$, $t_i(2)$, ...} of transition times modulo the period of the pattern. The 12 sets should be of equal size and the size of all sets should be chosen to enable calculation of J_{3u} (as defined below) with sufficient accuracy.

Calculate the average of each set S_i, $Tavg_i$, and subtract it from all elements of that set, to create a set $S0_i$ = {$t_i(1)$ - $Tavg_i$, $t_i(2)$ - $Tavg_i$, ...}.

Combine the sets $S0_i$, i=1 to 12, to create an estimated probability distribution $f_J(t)$.

J_{3u} is defined as the time interval that includes all but 10^{-3} of $f_J(t)$, from the 0.05th to the 99.95th percentile of $f_J(t)$.

J_{RMS} is defined as the standard deviation of $f_J(t)$.

27.3.1.7.2 Even-Odd Jitter (EOJ)

For one of the 12 specific transitions in QPRBS13-CEI in Table 27-7, or QPRBS9-CEI in Table 27-8:

a) Trigger once in 3 repeats of the QPRBS13-CEI or QPRBS9-CEI test pattern.

Obtain the mean time (T3) for this transition in the first QPRBS13-CEI or QPRBS9-CEI.

Obtain the mean time (T4) for the same transition in the second QPRBS13-CEI or QPRBS9-CEI.

b) The difference between the two means (T4 – T3), is the estimated period of the repeating pattern.

For each of the 12 specific transitions in QPRBS13-CEI in Table 27-7, or in QPRBS9-CEI in Table 27-8:

1) Trigger once in 2 repeats of the QPRBS13-CEI or QPRBS9-CEI test pattern.

Obtain the mean time (T1) for the specific transition in the first QPRBS13-CEI or QPRBS9-CEI.

Obtain the mean time (T2) for the same transition in the second QPRBS13-CEI or QPRBS9-CEI.

2) Calculate EOJ for this transition as |(T2 – T1) – (T4 – T3)|.

EOJ is the maximum of the 12 measurements.

NOTE: Both of (T2 - T1) and (T4 - T3) are about 8191 UI for QPRBS13-CEI, or 511 UI for QPRBS9-CEI, which is much larger than the EOJ value. Hence, each of T1 through T4 should have high precision.

27.3.2 Receiver Characteristics

A compliant receiver shall autonomously operate at the specified BER with the worst case combination of a compliant transmitter and a compliant channel. The receiver also shall not cause error propagation that violates the error burst length requirement as defined in Section 27.2.2. Further receiver electrical requirements at compliance point R (see Figure 27-1) are specified in Table 27-9, with the receiver interference tolerance parameters specified in Table 27-10. Lanes not under test should be enabled and transmitting or receiving asynchronous or uncorrelated signals.

Table 27-9. Receiver Electrical Input Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	R_Baud		36		58	Gsym/s
Effective return loss (ERL)		See Section 27.3.1.3	10			dB
Differential to Common Mode Input Conversion	R_SCD11		Equation (27-6)			dB
Interference Tolerance		Table 27-10				
Jitter Tolerance		Table 27-11				

Table 27-10. Receiver interference tolerance parameters (Note 2)

Parameter	Test 1 values		Test 2 values		Units
	Min	Max	Min	Max	
Pre-FEC Bit Error Ratio (BER)		10^{-4}		10^{-4}	
COM, including effects of broadband noise		3		3	dB
Insertion loss at Nyquist, Note 1		14		28	dB
RSS_DFE4. Note 2	0.05	-	0.05	-	

NOTES:
1. Measured between TX and RX package balls (see Figure 27-1).
2. Definition can be found in Annex 93A of IEEE Std 802.3 [27]. See Section 27.3.2.4.

27.3.2.1 Input Baud Rate

All devices shall work within the range from 36 Gsym/s to 58 Gsym/s as specified for the device, with the baud rate tolerance as per Section 3.2.11. A CEI implementation complies to the specifications of this clause over the range of baud rates stated for the implementation within this range.

27.3.2.2 Reference Input Signals

The receiver shall accept differential input signal amplitudes produced by a compliant transmitter connected with the minimum attenuation specified in Figure 27-2 to the receiver. This may be larger than the 1200 mVppd maximum of the transmitter due to output/input impedances and reflections.

The minimum input amplitude is defined by the minimum transmitter amplitude, the actual receiver input impedance and the loss of the actual PCB. Note that the minimum transmitter amplitude is defined using a well controlled load impedance, however the real receiver is not, which can leave the receiver input signal smaller than expected.

27.3.2.3 Input Return Loss

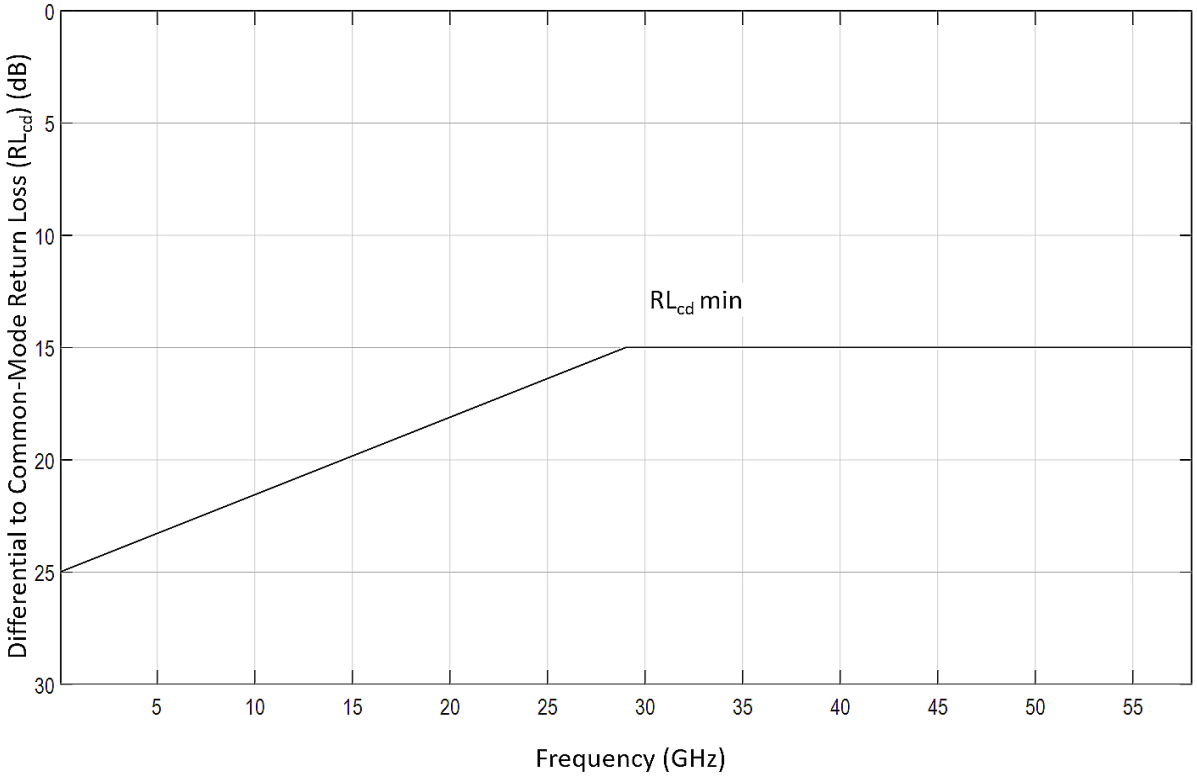
ERL of the receiver at compliance point R is computed using the procedure in 93A.5 [27] with the values in Table 27-5. Parameters that do not appear in Table 27-5 take values from Table 27-1. The value of T_{fx} is 0. N_{bx} is set to the value of Nb+Nbg*Nbf in Table 27-1.

The specification for the maximum value of the receiver ERL at compliance point R is the same as the specification for the maximum value of the transmitter at compliance point T.

The reference impedance for differential return loss measurements shall be 100 Ω. The differential to common-mode return loss, in dB, of the receiver shall meet Equation (27-6). The differential to common-mode return loss limit $RL_{cd}(f)$ is shown in Figure 27-5.

$$RL_{cd}(f) \geq RL_{cd}min(f) = \begin{pmatrix} 25 - 0.34485\left(\frac{f \times 58}{f_b}\right), & 0.05 \leq f \leq 0.5f_b \\ 15, & 0.5f_b < f \leq f_b \end{pmatrix} (dB) \quad (27\text{-}6)$$

Figure 27-5.Receiver differential to common-mode return loss limit for 58 Gsym/s



27.3.2.4 Receiver Interference Tolerance

The receiver interference tolerance test is based on the test defined in Annex 120D.3.2.1 of IEEE Std 802.3 [27].

The receiver on each lane shall meet the pre-FEC BER requirement with channels matching the Channel Operating Margin (COM) and loss parameters for Test 1 and Test 2 in Table 27-10.

The test channel should be created using printed circuit boards with short interconnecting cables.

The following considerations apply to the interference tolerance test. The transmitter package is omitted in the COM calculation. The Test transmitter's measured SNDR should be used for SNR_{TX} in the COM calculation. The transmitter output levels are set such that R_{LM} is equal to 0.95. The test transmitter meets the specifications in Section 27.3.1. The test transmitter is constrained such that for any transmitter equalizer setting

the differential peak-to-peak voltage is less than 800 mV, and the normalized amplitudes of the coefficients of the transmitter equalizer c(-3), c(-2), c(-1), c(0) and c(1) are between the minimum and maximum limits given in Table 27-6.

The lower frequency bound for the noise spectral density constraints, f_{NSD1}, is 1 GHz. The ERL of the test channel at TP5 (as defined in Annex 93A of IEEE Std 802.3 [27], IEEE Std 802.3cd [28], IEEE Std 802.3ck [29]) shall be 3dB better than the requirement in Section 27.3.2.3. The test transmitter's jitter parameters J_{3u} and J_{RMS} are measured. A_{DD} and σ_{RJ} are calculated from the measured values of J_{3u} and J_{RMS} using Equation (27-7), and Equation (27-8), respectively and used for COM parameters. Other COM parameters are set according to the values in Table 27-1. The broadband noise is added and adjusted to achieve the COM value in Table 27-10. The test pattern to be used is QPRBS31-CEI defined in Appendix 16.C.3.2. A test system with a fourth-order Bessel-Thomson low-pass response with 43 GHz 3 dB bandwidth is to be used for measurement of the signal applied by the pattern generator and for measurements of the broadband noise.

$$A_{DD} = \left(\frac{J_{3u}}{2} + Q_{3d} \sqrt{(Q_{3d}^2 + 1) \times {J_{RMS}}^2 - \left(\frac{J_{3u}}{2} \right)^2} \right) / (Q_{3d}^2 + 1) \quad (27\text{-}7)$$

$$\sigma_{RJ} = \left(\frac{J_{3u}}{2} - A_{DD} \right) / Q_{3d} \quad (27\text{-}8)$$

where Q_{3d} = 3.0902.

NOTE 1—Q_{3d} is an approximated solution of $Q(Q_{3d}) = 1 \times 10^{-3}$. Q(x) is the complement of the standard Normal cumulative distribution function (CDF).

NOTE 2—Calculation of A_{DD} requires that the term in the square-root in Equation (27-7) be positive. If this does not hold, a different transmitter should be used in the test setup.

27.3.2.5 Receiver Jitter Tolerance

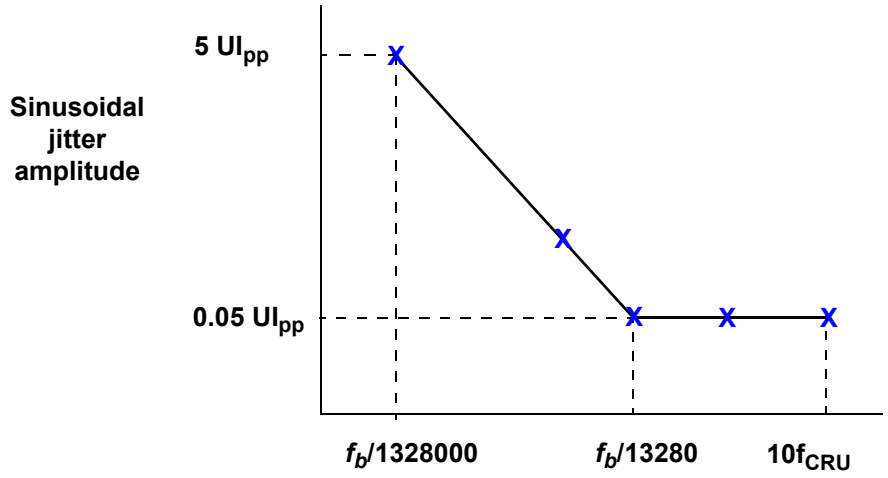
Receiver jitter tolerance shall meet the conditions and parameters defined in Table 27-11. This sinusoidal jitter is part of the jitter applied in the stressed input test.

The sinusoidal jitter is calibrated at 10x the reference CRU's bandwidth and must be tested at $f_{CRU}/100$, $f_{CRU}/3$, f_{CRU}, $3f_{CRU}$, and $10f_{CRU}$, where f_{CRU} is the jitter corner frequency given by $f_b/13280$, with sinusoidal jitter of 5 UI, 0.15 UI, 0.05 UI, 0.05 UI, and 0.05 UI respectively. For this test the channel used is as for the receiver interference tolerance described in Section 27.3.2.4. Note that the values measured for J3u and JRMS include the effects of this added sinusoidal jitter. Noise is added to obtain a COM of 3 dB with these measured jitter values as for the interference tolerance test. The receiver bit error ratio (BER) shall meet the requirements of Section 27.2.2 for each pair of jitter frequency and peak-to-peak amplitude values listed above and shown in Figure 27-6.

Table 27-11. Receiver Jitter Tolerance Parameters

Frequency Range	Sinusoidal jitter, peak-to-peak (UI)
f < f_b/1328000	Not Specified
f_b/1328000 < f ≤ f_b/13280	5*f_b/(1328000*f)
f_b/13280 < f ≤ 10f_{CRU}	0.05

Figure 27-6. Receiver Jitter Tolerance Mask



27.3.2.6 Single Ended Input Voltage

The single ended voltage levels with respect to the receiver ground at the input of the receiver are dependent on the transmitter implementation and the inter-ground difference. The voltage levels at the input of an AC coupled receiver (if the effective AC coupling is done within the receiver) or at the TX side of the external AC coupling cap (if AC coupling is done externally) will be between -0.35V and 1.95V with respect to local ground.

27.3.2.7 Input Lane-to-Lane Skew

Refer to Section 3.2.8.

28 CEI-112G-XSR+-PAM4 Extended Extra Short Reach Interface

This clause details the requirements for the CEI-112G-XSR+-PAM4 extended extra short reach high-speed electrical interface with nominal baud rates between 36 Gsym/s and 58 Gsym/s using PAM4 modulation. A compliant device shall meet all of the requirements listed in Section 28.1. The electrical interface is based on high-speed, low-voltage logic. Connections are point-to-point balanced differential pairs and signaling is unidirectional.

This electrical IA is based on loss and jitter budgets and defines the characteristics required to communicate between a CEI-112G-XSR+-PAM4 transmitter and a CEI-112G-XSR+-PAM4 receiver using copper signal traces on a substrate or printed circuit board (PCB). The characteristic impedance of the signal traces is nominally 92.5 Ω differential. However, the reference impedance of the channel S-parameters is 100 Ω.

28.1 Requirements

1. Support serial baud rates (f_b) within the range from 36 Gsym/s to 58 Gsym/s, as specified for the device, using PAM4 coding. A CEI implementation complies to the specifications of this clause for the stated baud rate for the implementation.
2. Capable of achieving a raw BER of 10^{-6} or better per lane. FEC is assumed to be used in the system to achieve corrected BER of 10^{-15} or better per lane. The baud rate includes the overhead required for FEC. The definition of FEC is outside the scope of this IA.
3. Capable of driving a channel with insertion loss up to 13 dB. The channel may include an ASIC package, an interconnect medium, a module socket, and a module package. The interconnect medium may include any combination of assembly substrate, PCB, or advanced cabling.
4. Shall support DC-coupled operation. AC-coupling can be supported by capacitors implemented on die.
5. Shall allow multiple-lane (1 to n) interfaces.
6. CEI-112G-XSR+-PAM4 devices from different manufacturers shall be interoperable.
7. This clause assumes recovered clock, not forwarded clock.

28.2 General Requirements

28.2.1 Data Patterns

See Appendix 16.C.5.

28.2.2 Bit Error Ratio

A raw BER of 10^{-6} or better is required on each lane.

A compliant receiver, when receiving from a compliant transmitter over a compliant channel, shall deliver the specified raw BER to the subsequent FEC decoder. Error bursts with length more than 7 PAM4 symbols delivered to the PAM4 decoder shall occur with a probability of less than 1 in 10^{20} PAM4 symbols. To enable a more practical test, error bursts with length more than 3 PAM4 symbols delivered to the PAM4 decoder should occur with a probability of less than 1 in 10^{12} PAM4 symbols.

28.2.3 Ground Differences

The ground difference between the driver and receiver shall be within the range ±50 mV.

28.2.4 Reference Models and Compliance Points

Compliance points are defined at the die-channel interface. The reference model and compliance points for the die-to-die channel are defined in 28.2.4.1. The compliance points for the die transmitter and receiver are defined in 28.2.4.2.

28.2.4.1 Reference Model and Compliance Points for the Die-to-Die Channel

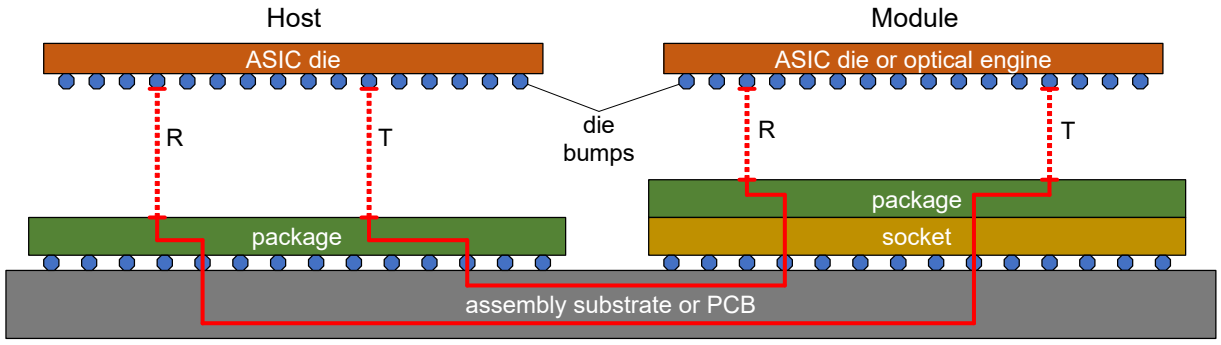
Reference models and compliance points used to specify a CEI-112G-XSR+-PAM4 implementation of the die-to-die channel are provided in this section. A reference model for the channel is provided in Figure 28-1. The channel includes a host ASIC package substrate, an assembly substrate or PCB, a module socket, and a module package substrate. The module socket is optional.

The channel is defined between test point T and test point R. The die bumps at T and R are not part of the channel.

The reference models provided for CEI-112G-XSR-PAM4 in Section 24.2.4.1 are also relevant to CEI-112G-XSR+-PAM4.

Channel characteristics are specified in Section 28.3.

Figure 28-1. Reference Model for Channel with socket



28.2.4.2 Compliance points for ASIC die or optical engine transmitter and receiver

Reference models and compliance points used to specify a CEI-112G-XSR+-PAM4 implementation of the die transmitter and receiver are provided in this section.

The transmitter and receiver on the host ASIC die, module ASIC die, or module optical engine are specified at test point T and test point R, respectively, as shown in Figure 28-1.

Die transmitter and receiver electrical characteristics are specified in Section 28.4.

28.3 Die-to-die channel characteristics

A forward channel and associated dominant crosstalk channels are deemed compliant if the channel characteristics conform to the requirements defined in this section.

28.3.1 Channel Operating Margin

For an informative introduction into the Channel Operating Margin method, please refer to Appendix 25.D.

The COM of the channel is computed using the procedure in Annex 93A of IEEE Std 802.3 [30] as amended by IEEE Std 802.3ck [31], the parameters listed in Table 28-1, and T_r = 0.3984 UI for $H_t(f)$ in Equation (93A–19).

COM shall be greater than or equal to 3 dB for each test. This minimum value allocates margin for practical limitations on the receiver implementation and the largest step size allowed for transmitter equalizer coefficients.

Table 28-1. COM Parameter Values

Parameter	Symbol	Value	Units
Signaling rate	f_b	36 to 58	Gsym/s
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Single-ended device series inductance Single-ended bump capacitance	 C_d L_s C_b	 100 120 30	 fF pH fF
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	45	Ω
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, second pre-cursor coefficient Minimum value Maximum value Step size	$c(-2)$	 –0.04 0.04 0.02	 — — —
Transmitter equalizer, first pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.18 0 0.02	 — — —
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.55	—
Transmitter equalizer, first post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.18 0 0.02	 — — —
Transmitter equalizer, second post-cursor coefficient Minimum value Maximum value Step size	$c(2)$	 –0.10 0.04 0.02	 — — —
Transmitter equalizer, third post-cursor coefficient Minimum value Maximum value Step size	$c(3)$	 –0.06 0.04 0.02	 — — —
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –10 0 1	 dB dB dB
Continuous time filter, DC gain 2 Minimum value Maximum value Step size	g_{DC2}	 –2 0 1	 dB dB dB
Continuous time filter, scaled zero frequency	f_z	f_b / 2.5	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	f_b / 2.5 f_b	GHz GHz
Continuous time filter, low frequency pole/zero	f_{LF}	f_b / 80	GHz

Table 28-1. COM Parameter Values

Parameter	Symbol	Value	Units
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.4 0.4 0.5	 V V V
Number of signal levels	L	4	—
Level separation mismatch ratio	R_{LM}	0.95	—
Transmitter signal-to-noise ratio	SNR_{TX}	32.5	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	0	UI
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.02	UI
One-sided noise spectral density	η_0	4.1×10^{-8}	V^2/GHz
Target detector error ratio	DER_0	10^{-6}	—

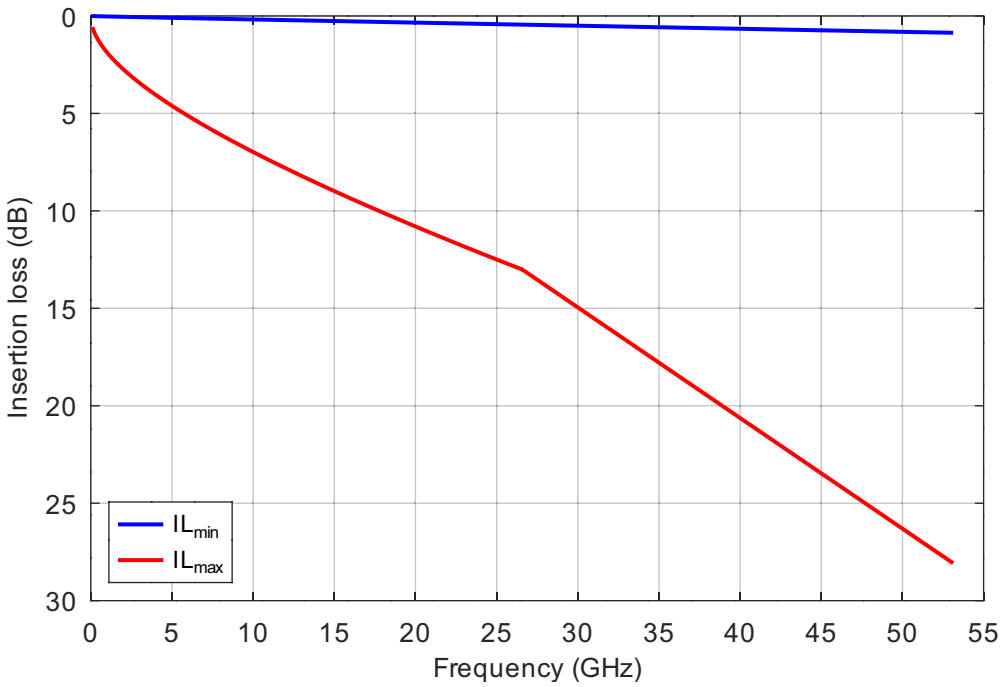
28.3.2 Informative Channel Insertion Loss

The recommended insertion loss limits are given by Equation (28-1) and Equation (28-2), respectively. Recommended insertion loss limits for a baud rate of 53.125 Gsym/s are illustrated in Figure 28-2.

$$IL_{max}(f) = \begin{bmatrix} 0.013 + 12.376\sqrt{\frac{f}{f_b}} + 8.4825\frac{f}{f_b} & f_{min} \le f < \frac{f_b}{2} \\ -2.08 + 30.16\frac{f}{f_b} & \frac{f_b}{2} \le f < f_b \end{bmatrix} \quad (28\text{-}1)$$

$$IL_{min}(f) = \left[0.009\sqrt{f} + 0.015f \quad f_{min} \le f < f_b\right] \quad (28\text{-}2)$$

Figure 28-2. Channel Insertion Loss Limits for 53.125 Gsym/s



28.3.3 Channel Effective Return Loss (ERL)

The background of ERL is described in the informative Appendix 25.E.

The channel ERL is computed at test point T and at test point R using the procedure in 93A.5 in Annex 93A of IEEE Std 802.3 [30] as amended by IEEE Std 802.3ck [31] with the values in Table 28-2. Parameters that do not appear in Table 28-2 take values from Table 28-1.

Channel ERL at test points T and R shall be greater than or equal to 5.6 dB.

Table 28-2. Channel ERL Parameter Values

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	0.531	UI
Incremental available signal loss factor	β_x	0	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.618	—
Length of the reflection signal	N	400	UI
Equalizer length associated with reflection signal	N_{bx}	0	—
Time-gated propagation delay	T_{fx}	0	ns
Tukey window flag	tw	1	—

28.3.4 Channel DC-coupling

Channel DC-coupling is defined in Section 24.2.4.6.

28.4 Electrical Characteristics

The electrical signaling is based on high-speed low-voltage logic with a nominal differential impedance of 100 Ω.

28.4.1 Transmitter Characteristics

Characteristics for the die transmitter is specified at compliance point T (see Section 28.2.4.2).

The transmitter electrical requirements are specified in Table 28-3 and the transmitter jitter requirements are specified in Table 28-4.

Table 28-3. Transmitter Electrical Output Specification

Characteristic	Symbol	Condition	MIN.	MAX.	UNIT
Baud Rate	T_Baud		36	58	Gsym/s
Output Differential Voltage	T_Vdiff	See Note 1, 2.		1000	mVppd
Output AC Common-Mode Voltage	T_VcmAC	See Note 1, 2.		15	mVrms
Single-ended Transmitter Output Voltage	T_Vse	See Note 1, 2.	0.1	1.2	V
Effective return loss (ERL)	T_ERL	See Section 28.4.1.3	11		dB
Common-Mode Output Return Loss	T_SCC22	200 MHz to $f_b/2$		-6	dB
Level Separation Mismatch Ratio	T_RLM	See notes 1, 3	0.95		—
Steady-state Voltage	T_Vf	See notes 1, 4	0.4	0.5	V
Linear Fit Pulse Peak	T_Pk	See notes 1, 4	0.85×T_Vf		V
Signal-to-Noise-and-Distortion-Ratio	T_SNDR	See notes 1, 4	32.5		dB

NOTES:
1. Signals are specified as measured through a fourth-order Bessel-Thomson low-pass response with 43 GHz 3 dB bandwidth. Sampling oscilloscopes will not be able to pattern lock and may substitute the 40 GHz bandwidth limit with compensation for the reduced bandwidth.
2. Measured as described in Section 28.4.1.2. T_Vdiff min is set by the steady-state voltage T_Vf min.
3. T_RLM is defined in Appendix 16.C.4.3.
4. Measured as described in Section 28.4.1.6.

Table 28-4. Transmitter Output Jitter Specification

Characteristic	Symbol	Condition	MIN.	MAX.	UNIT
Uncorrelated Jitter (time interval from 0.0005% to 99.9995% of the probability distribution)	T_J_{5u}	See Note 1		0.128	UI
Uncorrelated jitter RMS (standard deviation of the probability distribution)	T_J_{RMS}			0.0224	UIrms
Even-Odd Jitter	T_EOJ			0.025	UIpp

NOTES:
1. Measured as described in Section 28.4.1.7.

28.4.1.1 Transmitter Baud Rate

Transmitter baud rate is defined in Section 24.3.1.1.

28.4.1.2 Transmitter Amplitude and Swing

The differential output voltage T_Vdiff is defined to be True minus Complement. The common-mode output voltage T_Vcm is defined to be one half of the sum of True and Complement. These definitions are illustrated in Section 1.6.1.

For a QPRBS13-CEI test pattern (Appendix 16.C.3.1), the peak-to-peak value of the differential output voltage (T_Vdiff) shall be less than or equal to the limit given in Table 28-3 regardless of the transmit equalizer setting.

The AC common-mode output voltage (T_VcmAC) shall be less than or equal to the limit given in Table 28-3 with respect to local ground. Common-mode output voltage requirements shall be met for any valid transmit equalizer setting (see Section 28.4.1.6.3).

The single-ended transmitter output voltage (T_Vse) shall be within the limits in Table 28-3 with respect to local ground.

The transmitter shall be capable of providing a differential steady-state output amplitude (2xT_V_f) over the range of T_Vf given in Table 28-3 with transmit emphasis disabled.

Transmitter differential output amplitude shall additionally adhere to the requirements in Section 28.4.1.6.

Power-down behavior is beyond the scope of CEI IA.

28.4.1.3 Transmitter Return Loss

ERL of the transmitter at compliance point T is computed using the procedure in 93A.5 of IEEE Std 802.3 [30] as amended by IEEE Std 802.3ck [31] with the values in Table 28-5. Parameters that do not appear in Table 28-5 take values from Table 28-1.

Transmitter ERL at T shall be greater than or equal to the limit given in Table 28-3.

This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements shall be 100 Ω.

Table 28-5. Transmitter and Receiver ERL Parameter Values

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	0.531	UI
Incremental available signal loss factor	β_x	0	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.618	-
Length of the reflection signal	N	100	UI
Equalizer length associated with reflection signal	N_{bx}	0	—
Time-gated propagation delay	T_{fx}	0	ns
Tukey window flag	tw	1	—

28.4.1.4 Transmitter Lane-to-Lane Skew

Refer to Section 3.2.7.

28.4.1.5 Transmitter Short Circuit Current

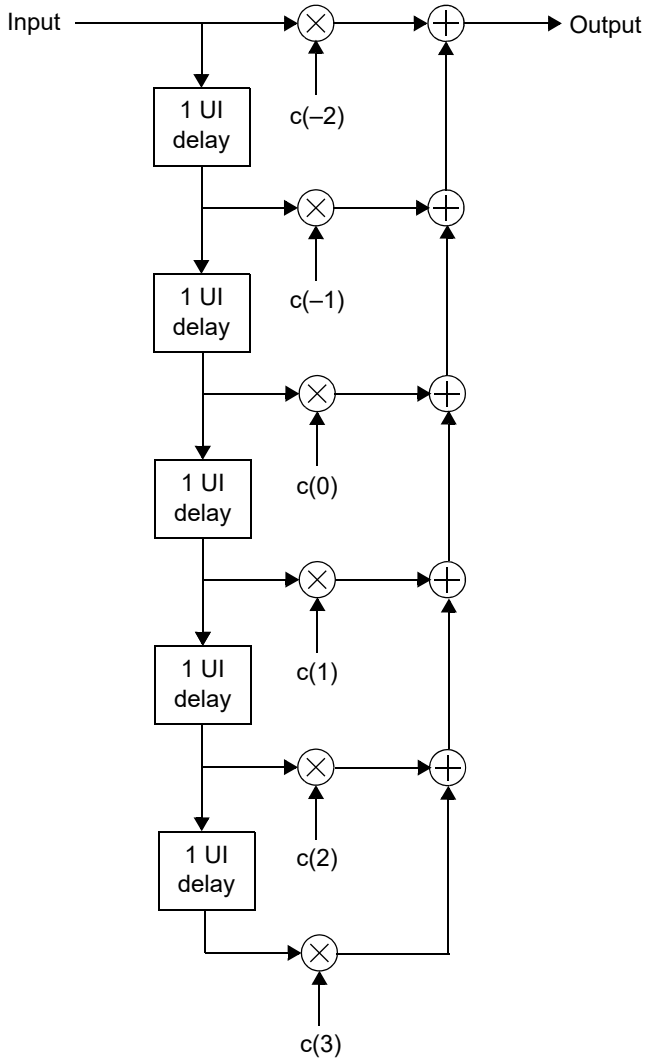
Refer to Section 3.2.9.

28.4.1.6 Transmitter output waveform requirements

The transmitter function includes programmable equalization to compensate for the frequency-dependent loss of the channel and facilitate data recovery at the receiver. The functional model for the transmit equalizer is the six-tap transversal filter shown in Figure 28-3.

Link budgets in this document assume optimized TX FIR equalization. The specific implementation is outside the scope of this document.

Figure 28-3. Transmit equalizer functional model



28.4.1.6.1 Linear fit to the measured waveform

Linear fit to the measured waveform is defined in Section 24.3.1.6.1.

28.4.1.6.2 Steady-state voltage and linear fit pulse peak

Steady-state voltage and linear fit pulse peak are defined in Section 24.3.1.6.2.

The steady-state voltage, T_Vf, shall satisfy the requirements in Table 28-3.

The linear fit pulse peak, T_Pk, shall satisfy the requirement in Table 28-3.

28.4.1.6.3 Transmitter equalizer coefficients

The normalized amplitudes of the coefficients of the transmitter equalizer (computed per Section 28.4.1.6.1) shall meet the requirements in Table 28-6. "min" is defined as the minimum normalized amplitude of the coefficient that must be supplied by the transmitter to be compliant. "max" is defined as the maximum normalized amplitude of the coefficient that must be supplied by the transmitter to be compliant.

The amplitude of a coefficient can be computed by multiplying its normalized amplitude by T_Vf, which is defined in Section 28.4.1.6.2.

The peak-to-peak output voltage is approximated by Equation (28-3) and should not exceed the limit for T_Vdiff given in Table 28-3.

$$2T_v_f \sum_{i=-2}^{3} |c(i)| \tag{28-3}$$

Table 28-6. Coefficient Range and Step Size

Coefficients	Normalized Amplitude		Normalized Step Size (%)
	Min (%)	Max (%)	
c(-2)	–4	4	0.2 to 2.5
c(-1)	–18	0	0.2 to 2.5
c(0)	40	100	0.2 to 2.5
c(1)	–18	0	0.2 to 2.5
c(2)	–10	4	0.2 to 2.5
c(3)	–6	4	0.2 to 2.5

28.4.1.6.4 Transmitter Output Noise and Distortion

Signal-to-noise-and-distortion ratio (SNDR) is defined in Section 24.3.1.6.4.

T_SNDR shall be greater than the limit given in Table 28-3 for any allowable transmit equalizer setting.

28.4.1.7 Transmitter output jitter

Transmitter output jitter is defined in Section 24.3.1.7, except that J_{8u} is replaced with J_{5u}. J_{5u} is defined as the time interval that includes all but 10^{-5} of $f_J(t)$, from the 0.0005th to the 99.9995th percentile of $f_J(t)$.

28.4.2 Receiver Characteristics

Characteristics for the die receiver is specified at compliance point R (see Section 28.2.4.2).

A compliant receiver shall autonomously operate at the specified BER with the worst case combination of a compliant transmitter and a compliant channel. The receiver also shall not cause error propagation that violates the error burst length requirement as defined in Section 28.2.2. Further receiver electrical requirements at compliance point R (see Section 28.2.4.2) are specified in Table 28-7. Lanes not under test should be enabled and transmitting or receiving asynchronous or uncorrelated signals.

Table 28-7. Receiver Electrical Input Specification

Characteristic	Symbol	Condition	MIN.	MAX.	UNIT
Baud Rate	R_Baud		36	58	Gsym/s
Effective return loss (ERL)	R_ERL	See Section 28.4.1.3	11		dB
Common-Mode Input Return Loss	R_SCC11	0.2-10 GHz		-6	dB
		10 GHz–f_b		-4	dB
Interference Tolerance		Table 28-8			
Jitter Tolerance		Table 24-12			

Table 28-8. Receiver Interference Tolerance Parameters (Note 1)

Parameter	Test 1 values	Test 2 values	Units
Pre-FEC bit error ratio (BER) (max)	10^{-6}	10^{-6}	
COM, including effects of broadband noise (max)	3	3	dB
Insertion loss at Nyquist, Note 2	2	13	dB

NOTES:
1. Definition can be found in Annex 93A of IEEE Std 802.3 [30] as amended by IEEE Std 802.3ck [31]. See Section 28.4.2.4.
2. Measured between TX and RX bumps (see Section 28.2.4.2).

28.4.2.1 Input Baud Rate

Refer to Section 24.3.2.1.

28.4.2.2 Reference Input Signals

The receiver shall accept differential voltage (Vdiff) produced by any compliant transmitter (see Section 28.4.1) connected to the receiver through any compliant channel (see Section 28.3.2). Note that the differential voltage at the receiver input may be affected by the impedances of the transmitter and receiver, and reflections.

The minimum input amplitude is defined by the minimum transmitter amplitude, the actual receiver input impedance, and the loss of the actual package trace. Note that the minimum transmitter amplitude is defined using a well controlled load impedance, however the real receiver is not, which can leave the receiver input signal smaller than expected.

28.4.2.3 Receiver Input Return Loss

ERL of the receiver is computed using the procedure in 93A.5 of IEEE Std 802.3 [30] as amended by IEEE Std 802.3ck [31] with the values in Table 28-5. Parameters that do not appear in Table 28-5 take values from Table 28-1.

Receiver ERL at R shall be greater than or equal to the limit given in Table 28-7.

The reference impedance for differential return loss measurements shall be 100 Ω.

28.4.2.4 Receiver Interference Tolerance

The receiver interference tolerance test is based on the test defined in subclause 120D.3.2.1 of IEEE Std 802.3 [30].

The receiver on each lane shall meet the pre-FEC BER requirement with channels matching the COM and loss parameters for Test 1 and Test 2 in Table 28-8.

The test channel should be created using a multiple-chip module (MCM) or PCB with short interconnecting cables.

The following considerations apply to the interference tolerance test. The transmitter package is omitted in the COM calculation. The test transmitter's measured SNDR should be used for SNR_{TX} in the COM calculation. The transmitter output levels are set such that R_{LM} is equal to 0.95. The test transmitter meets the specifications in Section 28.4.1. The test transmitter is constrained such that for any transmitter equalizer setting the differential peak-to-peak voltage is less than 800 mV, and the normalized amplitudes of the coefficients of the transmitter equalizer c(–2) to c(3) are between the minimum and maximum limits given in Table 28-6.

The lower frequency bound for the noise spectral density constraints, f_{NSD1}, is 1 GHz. The ERL of the test channel (as defined in Annex 93A of IEEE Std 802.3 [30] as amended by IEEE Std 802.3ck [31] shall meet the requirements in Section 28.3.3, and be 3 dB better. The test transmitter jitter parameters J_{5u} and J_{RMS} are measured. A_{DD} and σ_{RJ} are calculated from the measured values of J_{5u} and J_{RMS} using Equation (28-4) and Equation (28-5), respectively, and used for COM parameters. Other COM parameters are set according to the values in Table 28-1. The broadband noise is added and adjusted to achieve the COM value in Table 28-8. The test pattern to be used is QPRBS31-CEI defined in Appendix 16.C.3.2. A test system with a fourth-order Bessel-Thomson low-pass response with 43 GHz 3 dB bandwidth is to be used for measurement of the signal applied by the pattern generator and for measurements of the broadband noise.

$$A_{DD} = \left(\frac{J_{5u}}{2} + Q_{5d}\sqrt{(Q_{5d}^2+1)\times J_{RMS}{}^2 - \left(\frac{J_{5u}}{2}\right)^2}\right)/(Q_{5d}^2+1) \quad (28\text{-}4)$$

$$\sigma_{RJ} = \left(\frac{J_{5u}}{2} - A_{DD}\right)/Q_{5d} \quad (28\text{-}5)$$

where Q_{5d} = 4.2649

NOTE 1—Q_{5d} is an approximated solution of $Q(Q_5) = 1 \times 10^{-5}$.

NOTE 2—The calculation of ADD may, under certain conditions, pose a negative discriminant. If this condition occurs, the recommended solution is to increase sinusoidal jitter or bounded uncorrelated jitter such that the discriminant is positive.

28.4.2.5 Receiver Jitter Tolerance

Receiver jitter tolerance shall meet the conditions and parameters defined in Table 24-12 and shown in Figure 24-5.

This sinusoidal jitter is part of the jitter applied in the stressed input test. The sinusoidal jitter is calibrated at 10x the reference CRU bandwidth and must be tested at each frequency and sinusoidal jitter pair in Table 28-9, where f_{CRU} is the jitter corner frequency given by $f_b/13280$. For this test the channel used is as for the receiver interference tolerance described in Section 28.4.2.4. Note that the values measured for J_{5u} and JRMS include the effects of this added sinusoidal jitter. Noise is added to obtain a COM of 3 dB with these measured jitter values as for the interference tolerance test. The receiver BER shall meet the requirements of Section 28.2.2 for each pair of jitter frequency and peak-to-peak amplitude values.

Table 28-9. Sinusoidal Jitter

Jitter Frequency	Jitter Amplitude (UI)
$f_{CRU}/100$	5
$f_{CRU}/3$	0.15
f_{CR}	0.05
$3f_{CRU}$	0.05
$10f_{CRU}$	0.05

28.4.2.6 Single Ended Input Voltage

Refer to Section 24.3.2.6.

28.4.2.7 Input Lane-to-Lane Skew

Refer to Section 24.3.2.7.

29 CEI-112G-LINEAR-PAM4 Interface

This clause details the requirements for the CEI-112G-LINEAR-PAM4 high speed chip-to-module, chip to near-package module or chip to co-packaged module electrical interface with nominal baud rates of 36 Gsym/s to 56 Gsym/s. A compliant host or module shall meet all of the relevant requirements listed below. The electrical interface is based on high speed, analog electrical signaling, and connections are point-to-point balanced differential pairs.

This clause defines the linear electrical characteristics required to connect a host and optical PMD using copper signal traces on a printed circuit board or cables, a mated connector pair and copper signal traces inside an optical module. These specifications are normative at the test points shown in Figure 25-1 and Figure 29-1. A 'length' is effectively defined in terms of its attenuation and phase response rather than its physical length.

Hosts and modules compliant to CEI-112G-LINEAR-PAM4 from different manufacturers shall be inter-operable.

29.1 Requirements

The objectives and requirements for the CEI-112G-LINEAR-PAM4 implementation agreement are given by the project definition as follows:

- Support baud rates (f_b) within the range from 36.0 Gsym/s to 56.0 Gsym/s as specified for the device using PAM4 coding. A CEI implementation complies to the specifications of this clause over the range of baud rates stated for the implementation within this range.
- Capable of driving up to a minimum of 100 mm of host PCB trace plus one connector and a minimum of 20 mm of module PCB trace. The use of cables to replace or partially replace the copper signal traces on the printed circuit board is acceptable and may extend the physical length of the connection.
- Capable of achieving an end-to-end raw Bit Error Ratio (BER) of 2.0×10^{-4} or better per lane. FEC is assumed to be used to achieve a corrected BER of 10^{-15} or better per lane. The baud rate includes the overhead required for FEC. The definition of FEC is outside the scope of this IA (see Appendix 16.D).
- Shall support AC-coupled operation.
- Shall allow multi-lanes (1 to n).
- Shall support hot plug.

29.2 General CEI Requirements

29.2.1 Data Patterns

See Appendix 16.C.5

29.2.2 Transmitter equalizer function

Host FIR (or equivalent) may be needed to meet TP1a eye requirements (see Figure 29-1).

29.2.3 Bit Error Ratio

In the transmit direction a host outputs a compliant electrical signal, and a compliant module, when receiving the compliant electrical signal, transmits a compliant optical output signal on the medium. In the receive direction, a compliant module, when receiving a compliant optical input, delivers a compliant electrical output signal to the host. A compliant host, when receiving a compliant electrical signal from a compliant module, delivers the specified raw BER to the subsequent FEC decoder. Error bursts with length more than 130 PAM4 symbols delivered to the PAM4 decoder shall occur with a probability of less than 1 in 10^{20} PAM4 symbols. To enable a more practical test, error bursts with length more than 66 PAM4 symbols delivered to the PAM4 decoder should occur with a probability of less than 1 in 10^{12} PAM4 symbols. Optical compliance is typically set by another specification and error performance may also be set by another specification. Unless otherwise specified, a raw Bit Error Ratio (BER) better than or equal to 2.0×10^{-4} may be required provided that the error statistics are sufficiently random to meet the system requirements. The interface BER is the average of the BER across a group of lanes that share a FEC decoder. The impairments of both the optical and electrical interfaces cause errors at the host receiver. See also Appendix 16.D.

29.2.4 Ground Differences

The maximum ground difference between the host and module shall be ±50 mV. The common mode voltage limits are set taking this difference into account.

29.3 Electrical Characteristics

Hosts and modules shall meet the specifications defined in Table 29-1, Table 29-2, Table 29-3, Table 29-4, Table 29-5 and Table 29-6 as applicable. The direction of a signal (host-to-module or module-to-host) determines which table is applicable.

AC coupling is required in the module for both Tx and Rx.

29.3.1 End-to-end linear channel description

The linear interface has normative test points to ensure interoperability between host, module and optical fiber. Figure 29-1 shows the linear end-to-end connection between host A Tx and host B Rx (n lanes in one direction). The end-to-end linear channel contains the host re-timers, the host electrical channels, the optical modules and the optical interconnect. Figure 29-2 shows the end-to-end connections between CEI-112G-LINEAR-PAM4 host A and another host B with linear or retimed transmitter and linear or retimed receiver (one lane in each direction).

Requirements at the TP1, TP1a, TP4 and TP4a test points are defined in this clause. These test points are shown in Figure 25-1 and Figure 29-1. The TP2 and TP3 test points are not defined in this specification. They are defined in the appropriate optical specification such as IEEE Std 802.3db-2022 [30] Clause 167 for MMF optical, or IEEE Std 802.3-2022 [27] Clauses 124, 140, 151 or 168 for SMF optical specifications. Links with different optical specifications and symbol rates can follow a similar methodology. The relevant optical specifications at TP2 shall be met with any electrical input that is compliant to this specification at TP1a. The electrical specifications at TP4 shall be met with any optical input that is compliant to the relevant optical specification at TP3.

Figure 29-1. End-to-end linear channel

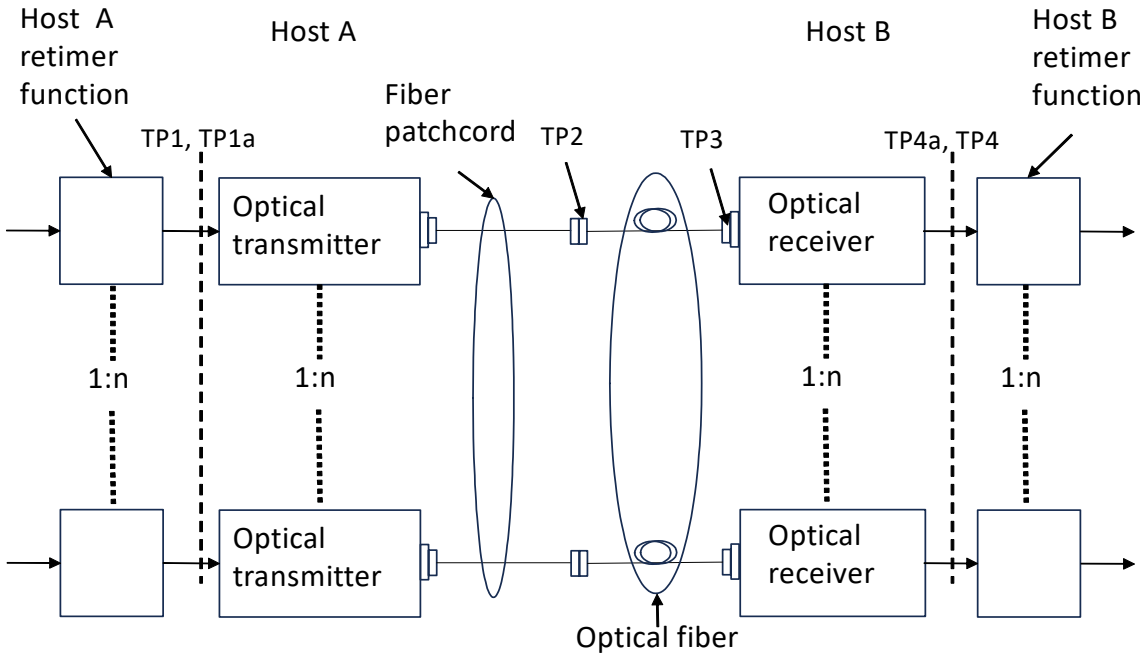
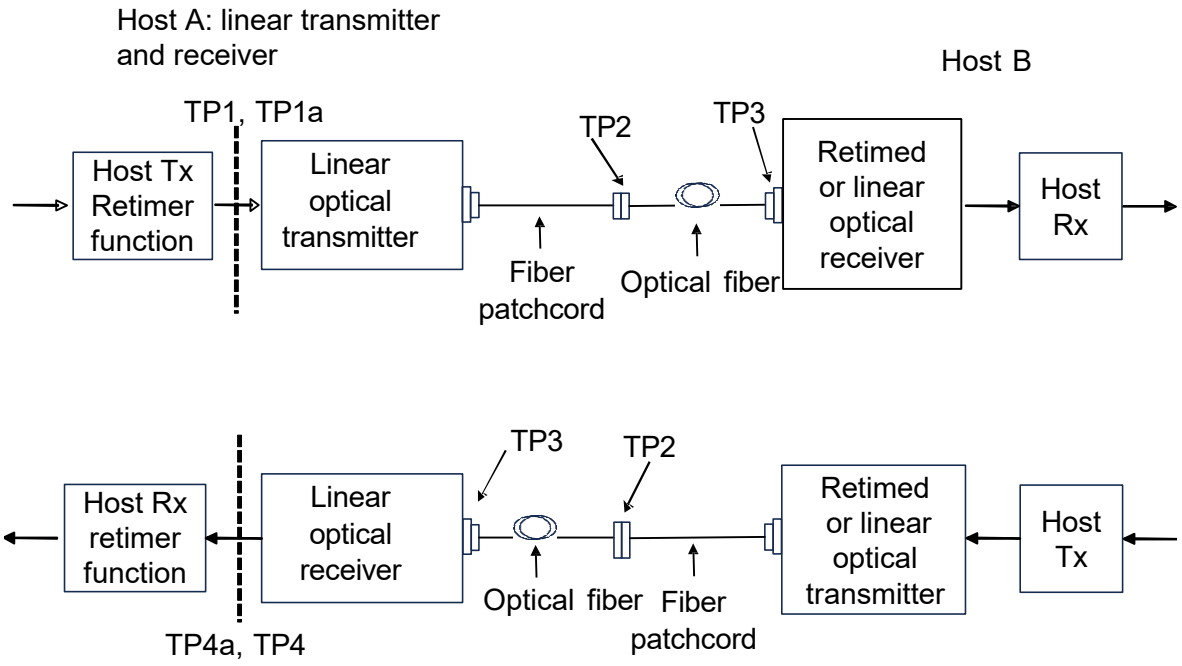


Figure 29-2. Link with linear and retimed modules (one of n lanes)



29.3.2 Compliance Point Specifications

See Section 25.3.1 for TP1, TP1a, TP4 and TP4a. Also see Section 29.3.1 which describes TP2 and TP3.

29.3.3 Host-to-Module Electrical Specifications

Each host-to-module lane shall meet the specifications of Table 29-1 and Table 29-2. Definitions and methodologies can be found in Sections 29.3.5 to 29.4.2. The module defaults to approximate a CTLE with parameters g_{DC} and g_{DC2} within the range shown in Table 29-8 for TP1a. A setting suitable for a low-loss host is recommended. The module's g_{DC} and g_{DC2} equivalents are made available to the host through the management interface. TP1a is assumed to comply with the J3u03 specification in IEEE Std 802.3ck Clause 162 Table 162-11.

The host uses the management interface to provide the module with the g_{DC} and g_{DC2} values that were used in the reference CTLE when the host passed the TP1a specifications in Section 29.4.1.1. After the module receives this information and is receiving a compliant input signal at TP1 it shall meet the optical specifications at TP2.

Table 29-1. Host-to-Module Electrical Specifications at TP1a (host output)

Parameter	Min.	Max.	Unit	Conditions
Differential Voltage pk-pk	-	525	mV	See Section 29.3.5, Note 1
VMA	200	450	mV	See Section 29.3.6
Low-Frequency Peak-to-Peak AC Common-Mode Voltage (VCM_{LF})	-	30	mV	See Section 29.3.7
Full-Band Peak-to-Peak AC Common-Mode Voltage (VCM_{FB})	-	80	mV	See Section 29.3.7
Common Mode Voltage	-300	2800	mV	See Table 1-2 and Section 1.6.1
Differential Termination Resistance Mismatch	-	10	%	At 1 MHz. See Section 29.3.8
Common Mode to Differential Mode Conversion (SDC22)	-	Equation 29-2	dB	See Note 2
Common Mode Return Loss (SCC22)	-	-2 -1.6 - 0.1*f -8.5 + 0.13*f	dB dB dB	0.25 ≤ f ≤ 4 GHz 4 < f ≤ 30 GHz 30 < f ≤ min(0.8*f_b, 43 GHz) See Note 2
Effective Return Loss (ERL)	8.5	-	dB	See Note 2
Transition Time	10	-	ps	See 16.C.4.1 except use a Bessel-Thomson filter bandwidth of 42 GHz
EECQ	-	3	dB	See Note 3, Section 29.3.12 and Section 29.4.1.1.1
C_{eeq_db}	-0.5	0.5	dB	Using EECQ method
Overshoot/undershoot	-	25	%	See Note 4

NOTES:
1. The differential voltage measured using a QPRBS13-CEI pattern will be less than the in-service differential voltage due to host loss and length of the QPRBS13-CEI pattern.
2. S-parameter specifications are based on a differential reference impedance of 100 Ω and a common mode reference impedance of 25 Ω
3. Open eye is generated through the use of a reference Continuous Time Linear Equalizer (CTLE) and FFE applicable to all three PAM4 eyes (see 29.4.1.5)
4. See IEEE Std 802.3db-2022 [30] subclause 167.8.8

Table 29-2. Host-to-Module Electrical Specifications (module input)

Parameter	Test Point	Min.	Max.	Unit	Conditions
Overload Differential Voltage pk-pk	TP1a	550	-	mV	See Section 29.4.2
Common Mode Voltage (Vcm)	TP1	-350	2850	mV	See Note 1
Differential Termination Resistance Mismatch	TP1	-	10	%	At 1 MHz. See Section 29.3.8
Differential Mode to Common Mode Conversion (SCD11)	TP1	-	Equation 29-1	dB	See Note 2
Effective Return Loss (ERL)	TP1	10	-	dB	See Section 29.3.9
Stressed Input Test	TP1a	See Section 29.4.1.4			

NOTES:
1. Vcm is defined in Table 1-2 General Definitions of Section 1.6
2. S-parameter specifications are based on a differential reference impedance of 100 Ω and a common mode reference impedance of 25 Ω

Table 29-3. Crosstalk parameters for host output test and module stressed input test calibration at TP4

Parameter	Target value	Unit	Conditions
Crosstalk Amplitude Differential Voltage pk-pk	700	mV	
Crosstalk Slew Time (between -210 mV and +210 mV)	10	ps	See Note 1

NOTES:
1. See 16.C.4.1 Transition Time and Slew Time except use a Bessel-Thomson filter bandwidth of 42 GHz

29.3.4 Module-to-Host Electrical Specifications

Each module-to-host lane shall meet the specifications of Table 29-4 and Table 29-5. Definitions and methodologies can be found in Sections 29.3.5 to 29.4.2.

Table 29-4. Module-to-Host Electrical Specifications at TP4 (module output)

Parameter	Min.	Max.	Unit	Conditions
Differential Voltage, pk-pk	300 300	620 720	mV mV	Initial value See Note 1
VMA	250	500	mV	See Section 29.3.6
DC Common Mode Voltage Tolerance (Vcm)	-350	2850	mV	See Note 2
Low-Frequency Peak-to-Peak AC Common-Mode Voltage (VCM_{LF})	-	30	mV	See Section 29.3.7
Full-Band Peak-to-Peak AC Common-Mode Voltage (VCM_{FB})	-	80	mV	See Section 29.3.7
Differential Termination Resistance Mismatch	-	10	%	At 1 MHz. See Section 29.3.8
Common Mode to Differential Mode Conversion (SDC22)	-	Equation 29-2	dB	See Note 3
Effective Return Loss (ERL)	10	-	dB	See Section 29.3.9
Common Mode Return Loss (SCC22)	-	-2	dB	From 250 MHz to min(0.8*f_b, 43 GHz) See Note 3
$EECQ_{SMF}$		8	dB	See Section 29.4.1.2
$EECQ_{MMF}$		10	dB	See Section 29.4.1.2

NOTES:
1. Host can request a change in amplitude after initialization. Module shall provide an output in this range.
2. Vcm is generated by the host. Specification includes effects of ground offset voltage.
3. S-parameter specifications are based on a differential reference impedance of 100 Ω and a common mode reference impedance of 25 Ω

Table 29-5. Module-to-Host Electrical Specifications (host input)

Parameter	Test Point	Min.	Max.	Unit	Conditions
Overload Differential Voltage pk-pk	TP4	720	-	mV	See Section 29.4.2
Differential Termination Resistance Mismatch	TP4a	-	10	%	At 1 MHz. See Section 13.3.6
Effective Return Loss (ERL)	TP4a	8.5	-	dB	See Section 29.3.9
Differential Mode to Common Mode Conversion (SCD11)	TP4a	-	Equation 29-1	dB	See Section 29.3.10
Stressed Input Test	TP4	See			
Common Mode Voltage (Vcm)	TP4a	-300	2800	mV	See Note 1, Note 2

NOTES:
1. Vcm is defined in Table 1-2 General Definitions of Section 1.6
2. Referred to host ground. Common mode voltage is generated by host

Table 29-6. Crosstalk parameters for module output test and host stressed input test calibration at TP1a

Parameter	Target value	Unit	Conditions
Crosstalk Amplitude differential voltage pk-pk	525	mV	
Crosstalk Slew Time (between -160 mV and +160 mV)	15	ps	See Note 1

NOTES:
1. See 16.C.4.1 Transition Time and Slew Time except use a Bessel-Thomson filter bandwidth of 42 GHz.

29.3.5 Output Differential Voltage, peak-peak

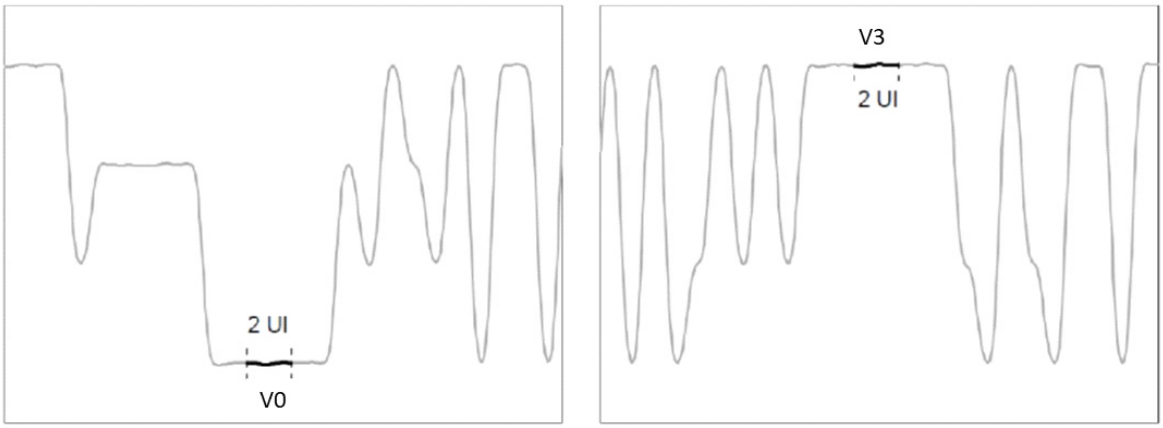
The differential voltage, peak-peak, (see Section 1.6.1 for definition of differential voltage peak-peak) shall meet the specifications given in Table 29-1 or Table 29-4 for the respective communication direction. Host Tx FIRs (or equivalent) may be needed to meet TP1a eye requirements for high loss channels. AC coupling is required in the module for both Tx and Rx. The waveform is observed through a fourth-order Bessel-Thomson response with a 3-dB bandwidth of 42 GHz using a QPRBS13-CEI pattern for TP1a (see Appendix 16.C.3.1) and the SSPRQ pattern for TP4 (see IEEE Std 802.3-2022 [27] subclause 120.5.11.2.3).

29.3.6 Voltage Modulation Amplitude (VMA)

VMA is the difference between the average voltage V3, measured over the central 2 UI of a run of 7 threes, and the average voltage V0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 29-3.

The waveform is observed through the appropriate compliance board and a fourth-order Bessel-Thomson response with a 3 dB bandwidth of 42 GHz. For TP1a the QPRBS13-CEI test pattern (specified in Appendix 16.C.3.1) is transmitted repetitively by the lane under test and the oscilloscope is set up to capture the complete pattern. For TP1a measurements the waveform is observed through the appropriate compliance board and the reference receiver as defined in Section 29.4.1.1. For TP4 the VMA is measured at the output of the CTLE in the reference Rx as defined in Section 29.4.1.2.1 using the SSPRQ test pattern.

Figure 29-3. Measurement of VMA voltage levels for EECQ



29.3.7 AC Common Mode Noise

Low-frequency and full-band peak-to-peak AC common mode voltages are defined by IEEE Std 802.3ck-2022 [29] subclause 120G.5.1.

29.3.8 Differential Termination Resistance Mismatch

See Section 13.3.6.

29.3.9 Effective Return Loss

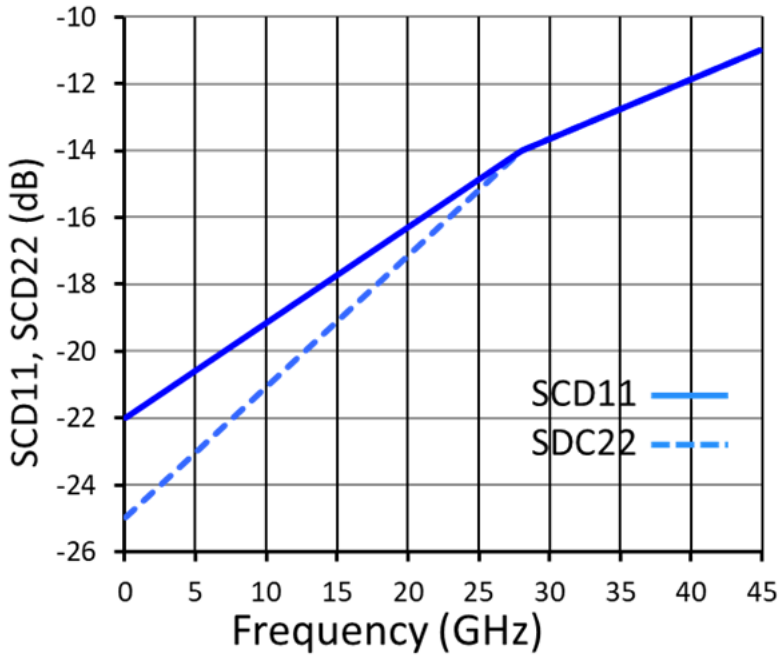
ERL is defined by Section 25.3.7 with the exception that for TP1/TP1a the value of Nbx is 2. For TP4 and TP4a the value of Nbx is 18, the DER0 is 10^{-4} and the reference to 95A.5 is changed to 93A.5.

29.3.10 Common to differential mode and differential to common mode conversion

The common mode to differential mode and differential mode to common mode conversion specifications are intended to limit the amount of unwanted signal energy that is allowed to be generated due to conversion of common mode voltage to differential mode voltage or vice versa. When measured at the respective input or

output test point, common mode to differential mode or differential mode to common mode conversion shall not exceed the limits given in Equation 29-1 and Equation 29-2 (illustrated in Figure 29-4 for f_b=56 GHz). The common mode to differential mode conversion specification for the host and module outputs is more stringent than for the inputs to take into account the lack of a common mode input return loss specification.

Figure 29-4. SCD11 for module input (TP1) and host input (TP4a), and SDC22 for module output (TP4) and host output (TP1a) (for f_b=56 GHz)



$$\begin{aligned} &\text{SCD11} \le -22+16*(\tilde{f}/f_b)\ \text{dB} && 0.05\ \text{GHz} \le f \le f_b/2 \\ &\text{SCD11} \le -19+10*(f/f_b)\ \text{dB} && f_b/2 < f \le 0.8*f_b \end{aligned} \quad (29\text{-}1)$$

$$\begin{aligned} &\text{SDC22} \le -25+22*(f/f_b)\ \text{dB} && 0.05\ \text{GHz} \le f \le f_b/2 \\ &\text{SDC22} \le -19+10*(f/f_b)\ \text{dB} && f_b/2 < f \le 0.8*f_b \end{aligned} \quad (29\text{-}2)$$

29.3.11 Common Mode Return Loss

The common mode output return loss specification is intended to limit the amount of common mode energy that can be reflected by the host and module outputs. This has an effect on EMI radiation and differential mode signals generated via common mode to differential mode conversion.

29.3.12 Electrical Eye Closure PAM4 (EECQ)

The EECQ algorithm calculates the degradation (noise, ISI) that a receiver can add to a transmitter signal.

The test method for measuring host output EECQ is based on the method for measuring TDECQ as defined by IEEE Std 802.3-2022 [27] subclause 140.7.5. This method is based on histograms measured at certain points within the eye diagram (as illustrated in Figure 29-7). See Section 29.4.1.1.1 for details on the EECQ measurement methods.

EECQ is defined by the method defined for TDECQ in IEEE Std 802.3-2022 [27] subclause 140.7.5. with the following exceptions:

1) VMA_{eecq} is used in place of OMA_{outer}. VMA_{eecq} is measured at the output of the reference equalizer (see Figure 29-6 and Figure 29-8). For TP1a, VMA = VMA_{eecq}

2) The reference equalizer in IEEE Std 802.3-2022 [27] subclause 121.8.5.4 is replaced with the reference equalizer in Section 29.4.1.1.1.

3) σ_G is added at the output of the Reference Rx (see Figure 29-6 and Figure 29-8).

4) Use SER = 4e-4 corresponding to a BER of 2e-4.

5) Crosstalk sources use a QPRBS13-CEI test pattern as defined in Appendix 16.C.3.1, or a QPRBS31-CEI test pattern as defined in Appendix 16.C.3.2, or a valid CEI signal.

6) The following equation is used for EECQ in place of TDECQ (Equation 121-12):

$$EECQ = 20\log_{10}(VMA_{eecq}/(6Q_tR)) \quad (29\text{-}3)$$

Where Q_t is 3.463 consistent with the BER of this specification.

7) The C_{eeq} limits constrain the tap weights for EECQ. The definition and equations for C_{eeq} can be found in IEEE Std 802.3-2022 [27] subclause 121.8.5.3 and Section 29.3.13.

29.3.13 Electrical Eye Closure PAM4 (C_{eeq})

C_{eeq} is a coefficient which accounts for the reference equalizer noise enhancement. The C_{eeq} limit constrains the tap weights for EECQ. The CTLE settings in the reference receiver may be adjusted (see Table 29-12) to bring C_{eeq} within the allowed range. Within the context of EECQ, C_{eeq} can be expressed in decibels as:

$$C_{eeq_db} = 20\log_{10}(C_{eeq}) \quad (29\text{-}4)$$

C_{eeq} is derived from the FFE tap weights of the reference equalizer and is measured after the CTLE in the reference Rx. C_{eeq} is defined identically to C_{eq} as defined in IEEE Std 802.3-2022 [27] subclause 121.8.5.3. See Section 29.4.1.1.1 for details on the C_{eeq} measurement methods.

29.3.14 Overshoot/Undershoot

Overshoot/Undershoot is measured after the fourth-order Bessel-Thomson filter (with a 3 dB bandwidth of 42 GHz) and after the CTLE for TP1a, before the CTLE for TP4. (See Figure 29-6 and Figure 29-8)

29.4 Host and Module testing

Host and module testing are performed at the appropriate test points shown in Figure 25-1 using the specified compliance test fixtures defined in Section 25.3.1. Module input stressed signals emulate the worst case host output signal at TP1a. Host input stressed signals emulate the worst case module optical input signal with additional impairments added for module O/E conversion.

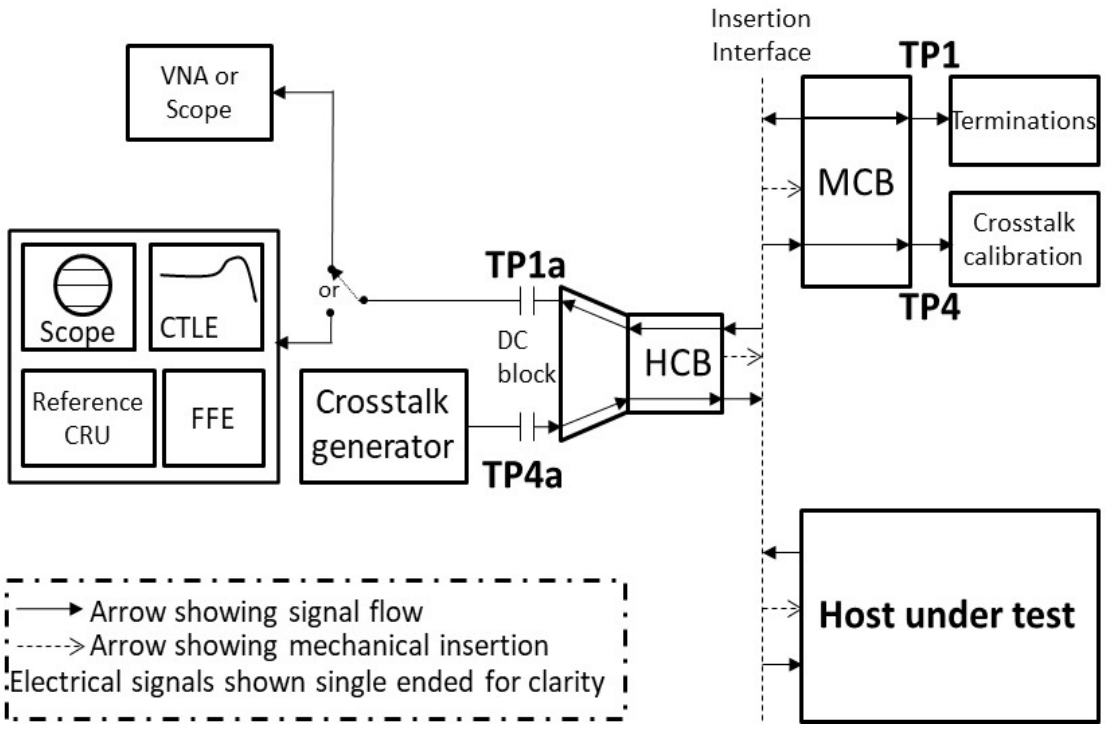
29.4.1 Host and module output and input tests

The parameters specified in Table 29-1 (host output) and Table 29-4 (module output) are verified using the test setup shown in Figure 29-5 (host output) and Figure 29-9 (module output). Compliance to the input specifications defined in Table 29-5 (host input) and Table 29-2 (module input) is verified using the test setup shown in Figure 29-10 (host input) and Figure 29-11 (module input).

29.4.1.1 Host output testing

The host output specifications are measured at TP1a of Figure 29-1 using a Host Compliance Board as defined in Section 25.3.1. The test setup is shown in Figure 29-5.

Figure 29-5. Host output test setup



29.4.1.1.1 Host output test method

The signal at TP1a may appear as a closed eye, therefore a reference receiver is used to equalize the host output signal and open the eye for EECQ measurements (see Section 29.3.12). The signals at the appropriate points in the reference receiver (see Figure 29-6) shall meet the specifications listed in Section 29.3.3 for host to module.

The waveform at TP1a is observed through a reference receiver consisting of a fourth order Bessel-Thomson filter with a bandwidth of 42 GHz concatenated with a continuous time linear equalizer (CTLE) followed by a 5-tap FFE. The tap weights of the 5-tap FFE are constrained per Table 29-7. The filters may be implemented in software. The measured signal is not averaged. The CTLE is defined in Section 29.4.1.5.

Figure 29-6. Host output (TP1a) reference receiver and measurement points

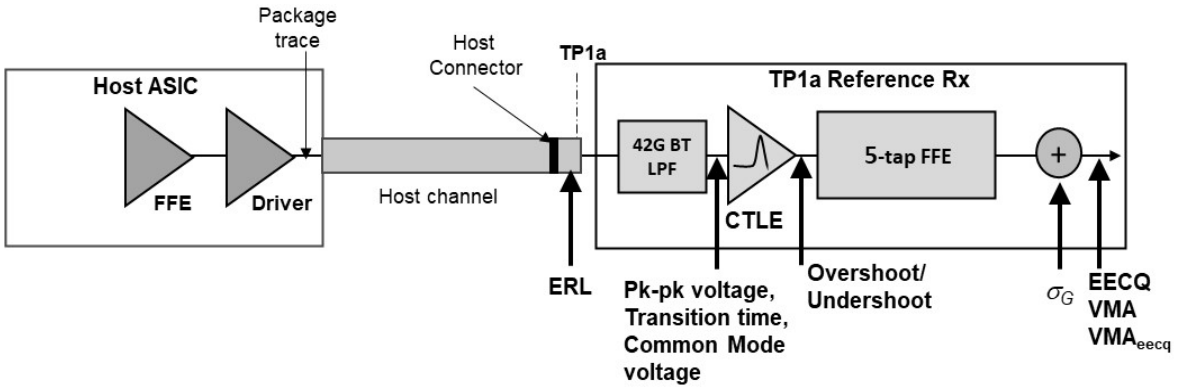


Table 29-7. Host output 5-tap Reference FFE Characteristics

Parameter	Min Value	Max Value
Pre-cursor	Not allowed	Not allowed
Tap 1 (main)	0.9	-
Tap 2 (post)	-0.07	0.07
Tap 3 to 5 (post)	-0.05	0.05
Note: Sum of the equalizer tap coefficients is equal to 1		

All co-propagating and counter-propagating lanes are active as crosstalk sources, using a QPRBS13-CEI test pattern as defined in Appendix 16.C.3.1, or a QPRBS31-CEI test pattern as defined in Appendix 16.C.3.2, or a valid CEI signal. If the QPRBS13-CEI is used for the co-propagating lanes they should be asynchronous to the lane under test or sufficiently delayed to remove correlation from the lane under test. If the QPRBS13-CEI or QPRBS31-CEI patterns are used, any pairs of aggressor lanes should also be asynchronous to each other or sufficiently delayed. Amplitude and Transition Times for counter-propagating lanes are defined in Table 29-3. The lanes under test are asynchronous to the lanes in the opposing direction within the limits for the protocol in use.

The QPRBS13-CEI test pattern (specified in Appendix 16.C.3.1) is transmitted repetitively by the lane under test and the oscilloscope is set up to capture the complete pattern for EECQ analysis as described in Section 29.3.12. The clock recovery unit (CRU) has a corner frequency of fb/13280 MHz and a slope of 20 dB/decade. The CRU can be implemented in hardware or software depending on oscilloscope technology. The time position of the pair of histograms in Figure 29-7 is defined as the one that minimizes EECQ. The three threshold levels Vth1 Vth2 and Vth3 may be adjusted

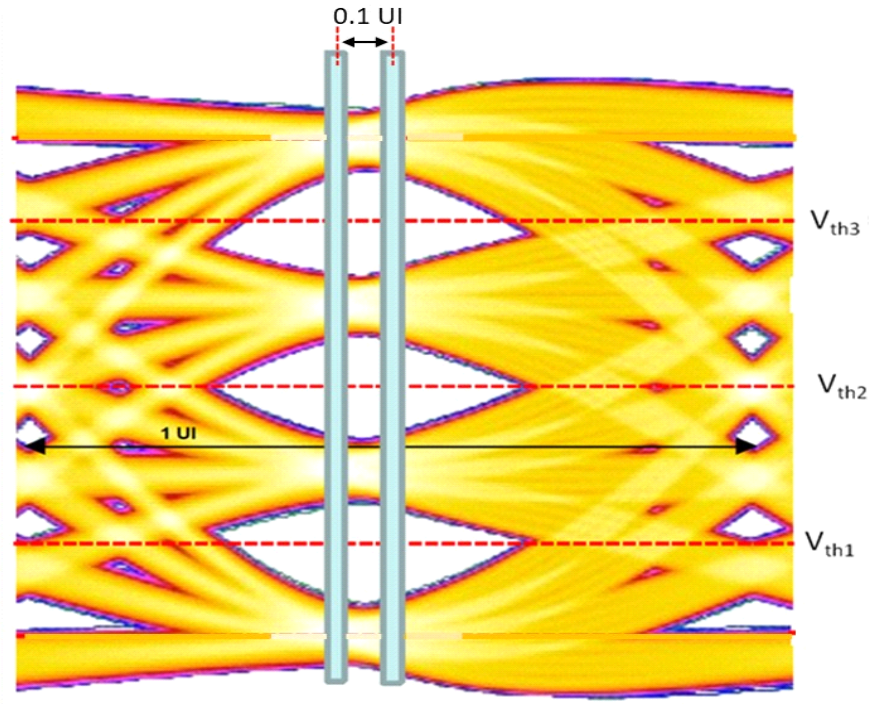
within limits as described for Pth1, Pth2, and Pth3 in IEEE Std 802.3-2022 [27] subclause 121.8.5.3.

Recommended g_{DC} and g_{DC2} setting vs channel IL are shown in Table 29-8.

Table 29-8. Recommended g_{DC} and g_{DC2} settings vs. Channel Insertion Loss (IL)

Ch IL (Note 1)	g_{DC}	g_{DC2}	Units
1.5	0	0.5	dB
2	0	0.5	dB
3	0	0.5	dB
4	0	1	dB
5	0.5	1	dB
6	1	1.5	dB
7	2	1.5	dB
8	2.5	1.5	dB
9	3.5	1.5	dB
10	4	2	dB
11	4.5	2	dB
12	5	2	dB
13	6	2	dB
Note 1: Channel IL measured from host ASIC package ball to TP1a			
Note 2: Table is based on 4 dB package loss, consideration should be given for actual package loss			

Figure 29-7. TP1a and TP4 EECQ measurement



29.4.1.2 Module output test (TP3 to TP4)

The module output EECQ is tested at TP4 of Figure 25-1 using a Module Compliance Board as defined in Section 25.3.1. The test setup is shown in Figure 29-9.

29.4.1.2.1 Module output test method

1) An optical stressed receiver conformance test signal with the specified pattern (typically SSPRQ) is applied to the optical input of the module.

2) Capture the differential signal at TP4 with a scope triggered with a clock from a reference clock recovery unit (CRU) with a first order transfer function with a 3 dB tracking bandwidth of f_b/13280 Hz.

3) The signal measured at TP4 is convolved with a channel that represents the additional loss present in a maximum loss channel including 1.5 dB package loss.

The signal at TP4 may appear as a closed eye, therefore a reference receiver with a Continuous Time Linear Equalizer (CTLE) (see Section 29.4.1.5), a 22-tap FFE and a 1-tap DFE is used to equalize the module output signal and open the eye for EECQ measurements. The measured signal after the reference receiver shall meet the EECQ and VMA specifications listed in Section 29.3.4 for module to host.

The waveform at TP4 is observed through an emulated channel (see Table 29-11) and a reference receiver (see Figure 29-8). The reference receiver consists of a fourth order Bessel-Thomson filter with a bandwidth of 42 GHz concatenated with a continuous time linear equalizer (CTLE) followed by a 22-tap FFE and a 1-tap DFE (see Figure 29-8). The constraints on the DFE values are shown in Table 29-9. The constraints on the 22-tap FFE are shown in Table 29-10. The filters may be implemented in software. The signal is not averaged. The CTLE is defined in Section 29.4.1.5. The time position of the pair of histograms in Figure 29-7 is defined as the one that minimizes EECQ. The three threshold levels Vth1 Vth2 and Vth3 may be adjusted within limits as described for Pth1, Pth2, and Pth3 in IEEE Std 802.3-2022 [27] subclause 167.8.6.

Figure 29-8. Module output (TP4) reference Rx and measurement points

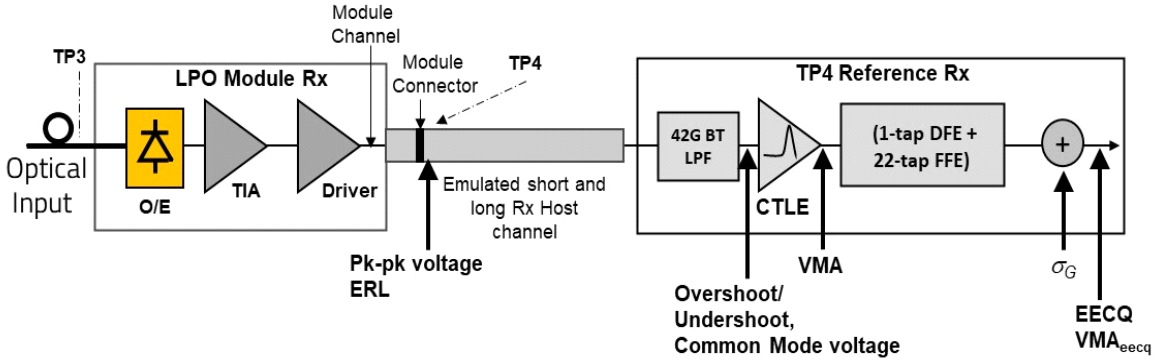


Table 29-9. Module output 1-tap Reference DFE Characteristics

Parameter	Min Value	Max Value
Range of b1 tap without pre-coding	0	0.4
Range of b1 tap with pre-coding	0	0.85
Note: Availability of pre-coding is dependent on the protocol and implementation		

Table 29-10. Module output 22-tap Reference FFE Characteristics

Tap Position	Min Value	Max Value
-1, -2, -3 (Pre-cursor)	-	-
0 (main)	0.3	-
1,2,3,4 (post)	-	-
5 (post)	-0.3	0.3
6 (post)	-0.2	0.2
7 (post)	-0.1	0.1
8-18 (post)	-0.07	0.07
Note: The main tap is the one with the largest tap weight. The sum of the FFE tap coefficients is equal to 1.		

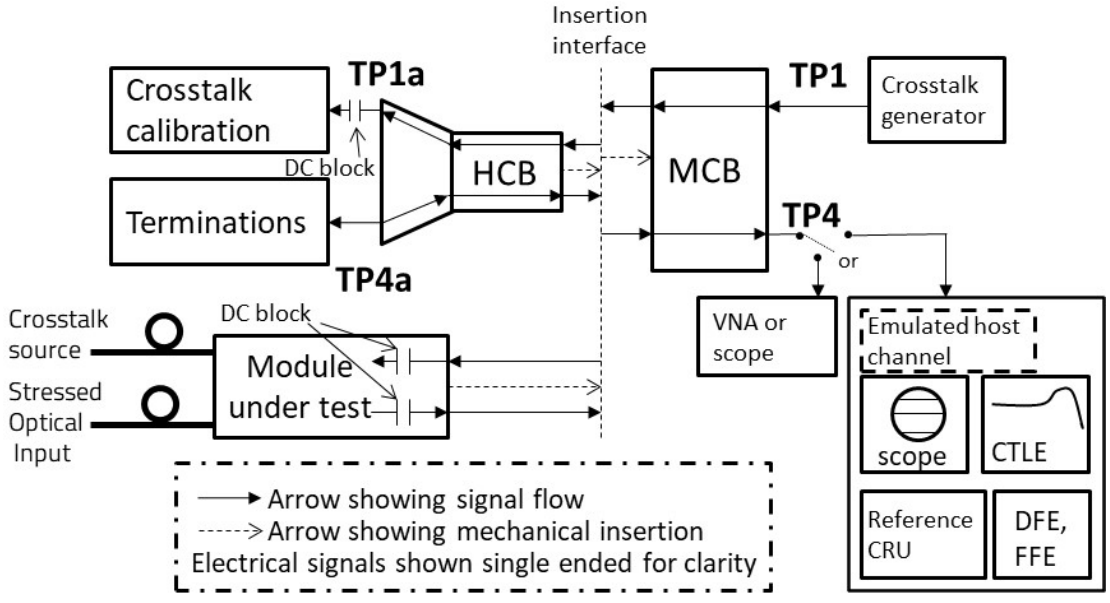
All co-propagating and counter-propagating lanes are active as crosstalk sources, using a QPRBS13-CEI test pattern as defined in Appendix 16.C.3.1, or a QPRBS31-CEI test pattern as defined in Appendix 16.C.3.2, or a valid CEI signal. If the QPRBS13-CEI is used for the co-propagating lanes they should be asynchronous to the lane under test or sufficiently delayed to remove correlation from the lane under test. If the QPRBS13-CEI or QPRBS31-CEI patterns are used, any pairs of aggressor lanes should also be asynchronous to each other or sufficiently delayed. Amplitude and Transition Times for counter-propagating lanes are defined in Table 29-6. The lanes under test are asynchronous to the lanes in the opposing direction within the limits for the protocol in use.

The test method for measuring module output electrical EECQ is illustrated in Figure 29-9 and described in Section 29.3.12. The host channel emulation is defined in IEEE Std 802.3ck-2022 [29] subclause 162.11.7.1.1 with trace loss from Table 29-11.

Table 29-11. Emulated Host Channels

Host Channel Type	Channel Insertion Loss (dB)	z_p (mm)
near-end	0	0
far-end	8.9	106.5 x 56/f_b

Figure 29-9. Module output test setup



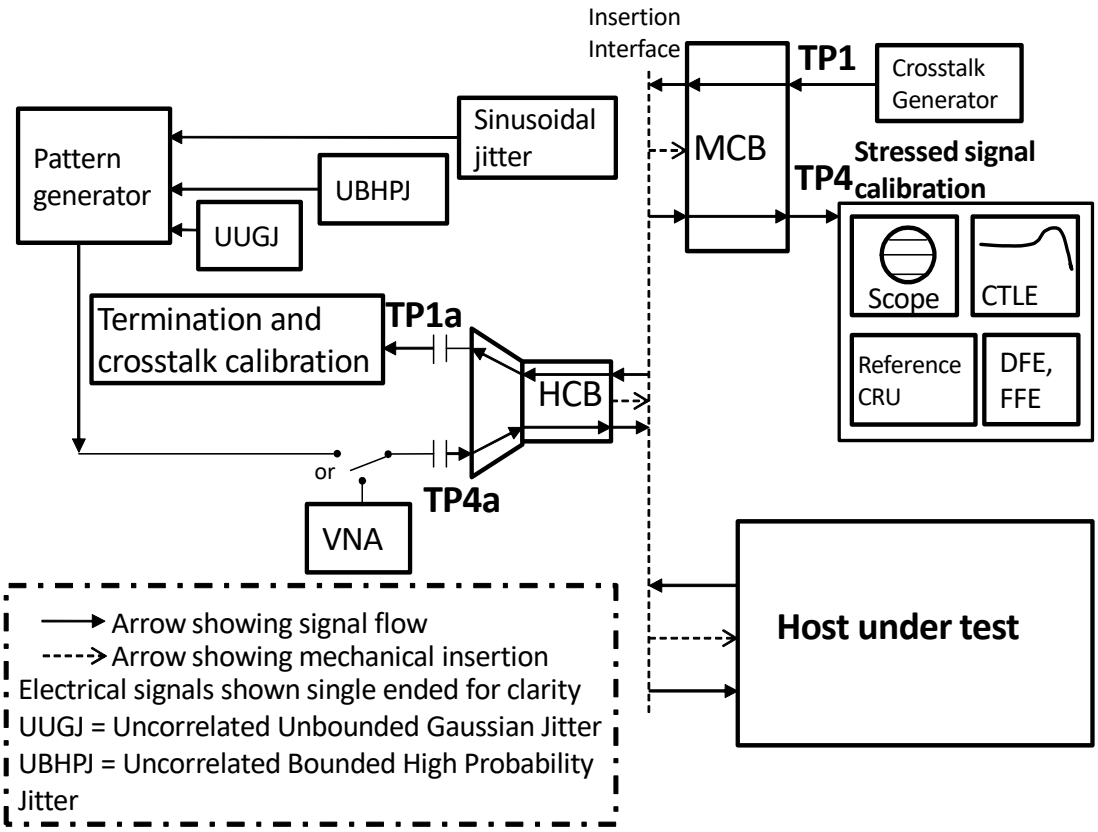
A compliant module delivers a signal according to Table 29-4 while receiving any compliant optical signal at TP3 with both the near end and far end emulated channels.

29.4.1.3 Host (TP4a) stressed input test

The ability of the host input to tolerate the parameters specified in Table 29-4 is defined by a stressed input test. The test signal is applied at TP4a of Figure 25-1 and calibrated at TP4, using a Host Compliance Board and Module Compliance Board specified in Section 25.3.1. The test setup is shown in Figure 29-10. The UBHPJ block including sinusoidal jitter is used to create non-compensable DJ. Add sinusoidal jitter as defined in Table 25-9.

A compliant host delivers an interface BER as specified in Section 29.2.3 while receiving the stressed input signal at TP4a/TP4.

Figure 29-10. Host input test setup



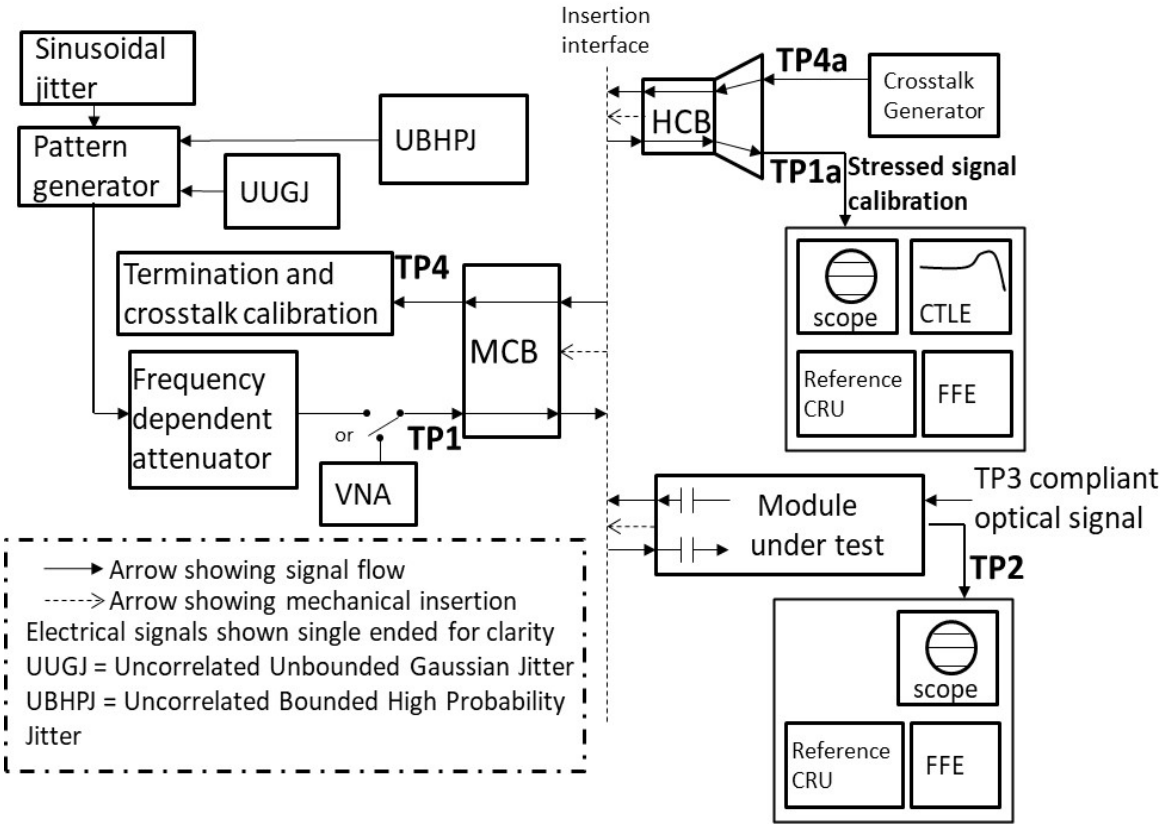
29.4.1.4 Module (TP1) stressed input test

The ability of the module input to tolerate the parameters specified in Table 29-1 is defined by a stressed input test. The test signal is applied at TP1 of Figure 25-1, and calibrated at TP1a using a Host Compliance Board and Module Compliance Board specified in Section 25.3.1. The test setup is shown in Figure 29-11. The module stressed input test represents the worst case high loss host. Modules are also expected to comply with the appropriate optical specifications when presented with lower loss channels that require different equalization settings as long as the signal

complies with the specifications in Table 29-1 and the module is provided the recommended CTLE settings for the lower loss channels. Equalization requirements for TP1a are described in Section 29.4.1.1.1.

A compliant module satisfies the appropriate optical specifications at TP2 while receiving the stressed input signal at TP1/TP1a when provided with the g_{DC} and g_{DC2} values used by the test equipment in the signal calibration to minimize the EECQ of that stressed input signal.

Figure 29-11. Module input test setup



29.4.1.4.1 Host (TP4a) and Module (TP1) stressed input test method

The reference CRU and reference receiver as defined in Section 29.4.1.2 are used to calibrate the stressed input test signal at TP4a (per Table 29-4). The reference CRU and reference receiver as defined in Section 29.4.1.1.1 are used to calibrate the stressed input test signal at TP1 (per Table 29-1). The TP1 stressed input test is calibrated using a QPRBS-13-CEI pattern. The TP4 stressed input test is calibrated using the SSPRQ pattern. The pattern is changed if necessary to the appropriate pattern when testing TP2 (typically SSPRQ). The pattern is changed to a scrambled idle pattern for the TP4a stressed input test.

The crosstalk source is asynchronous to the main pattern generator. The amplitude and rise/fall time of the crosstalk source are given in Table 29-3 and Table 29-6. The crosstalk signal is calibrated at TP4a or TP1 using a QPRBS13-CEI pattern, then the pattern on the lane under test is changed to the appropriate pattern for the spec item concerned. For multi-lane implementations additional lanes shall be active with either uncorrelated QPRBS31-CEI or QPRBS13-CEI patterns, scrambled idle pattern or valid CEI signals, using the above calibration methods.

29.4.1.4.1.1 Host input test signal calibration

The host input is tested at TP4a using a Host Compliance Board as defined in Section 25.4.1. The host input test setup is shown in Figure 29-10.

UBHPJ, UUGJ and SJ according to Table 25-9 are added to a clean test pattern until the jitter (except for EOJ) at the output of the pattern generator approximates the informative transmit recommendations given in Appendix 25.C.

With the crosstalk generator calibrated to meet the specifications in Table 29-6, the EECQ at TP4 is measured using the methodology and reference receiver defined in Section 29.4.1.2 with the receiver equalizer settings optimized to achieve minimum EECQ.

The UUGJ and pattern generator amplitude are adjusted to give values for EECQ and VMA equal to the maximum EECQ and minimum VMA specified in Table 29-4 measured using the reference receiver defined in Section 29.4.1.2.

29.4.1.4.1.2 Module input test signal calibration

The module input is tested at TP1 of Figure 25-1 using a Module Compliance Board as defined in Section 25.3.1. The module input test setup is shown in Figure 29-11. Pattern generator FIR settings, g_{DC} and g_{DC2} should be adjusted to minimize EECQ. Pattern generator amplitude is adjusted for VMA from Table 29-12. UBHPJ and UUGJ are adjusted for maximum EECQ in Table 29-1. Iterate as necessary.

The frequency-dependent attenuator is intended to represent the host channel and package. For the low loss channel the frequency dependent attenuator is omitted. For the high loss channel the target insertion loss is 15.2 dB at 26.56 GHz from the output of the pattern generator to TP1a. The frequency-dependent attenuator may be implemented with PCB traces. The target insertion loss is 15.2 dB at 26.56 GHz for the high loss channel and 4.0 dB at 26.56 GHz for the low loss channel. The target insertion loss represents the insertion loss from Table 29-12 with an additional 2.2 dB for the high loss channel, which provides some allowance for the difference between the effective insertion loss of the pattern generator output and the worst-case host transmitter package loss.

The complete path from the output of the pattern generator to TP1a should also meet the return loss specifications given for the mated HCB and MCB (see Section 29.5 and Section 25.4.1.2.2). The crosstalk generator is calibrated to meet the specifications in Table 29-3. The EECQ at TP1a is measured using the reference receiver and the methodology defined in Section 29.4.1.1. The UUGJ and pattern generator amplitude are adjusted to give values for EECQ equal to the maximum EECQ specified for the host output in Table 29-1, and VMA specified in Table 29-3 measured using the reference receiver defined in Section 29.4.1.1.

29.4.1.5 TP1a and TP4 CTLE used in Reference receiver

A CTLE is used in the reference receivers for both TP1a and TP4. The CTLE is defined by Equation 29-5.

$$H_{ctf}(f) = \frac{\left(1 + j10^{\frac{g_{DC}}{20}} \times \frac{f}{f_z}\right)\left(1 + j10^{\frac{g_{DC2}}{20}} \times \frac{f}{f_{LF}}\right)}{\left(1 + j\frac{f}{f_{p1}}\right)\left(1 + j\frac{f}{f_{p2}}\right)\left(1 + j\frac{f}{f_{LF}}\right)} \quad (29\text{-}5)$$

where:

g_{DC} and g_{DC2} are the CTLE relative gain parameters,

f_{p1}, f_{p2} are the frequencies of the CTLE poles,

f_z along with g_{DC} determine the high frequency zero,

f_{LF} along with g_{DC2} determine the low frequency zero of the CTLE.

The values of f_{p1}, f_{p2}, f_z, f_{LF} are given by Equation 29-6. Figure 29-12 shows the CTLE response of the reference CTLE with 0 dB of low frequency gain for a baud rate of 50 GBd with g_{DC} = 0 dB to 6 dB in 1 dB steps. Figure 29-13 shows the frequency response of the reference CTLE used for module and host output testing for a baud rate of 50 GBd with values for g_{DC} = 6 dB, g_{DC2} = 0 dB to 2.0 dB in 0.5 dB steps. The CTLE peaking value is the approximate difference between the low-frequency response (1 MHz) and the maximum high-frequency response in dB. The allowed ranges of g_{DC} and g_{DC2} are provided in Table 29-12.

Table 29-12. CTLE Gain Range

g_{DC2}			g_{DC}			Location
min	max	step size	min.	max.	step size	
0	2	0.5 dB	0	6	1.0 dB	TP1a, TP4

$f_{p1} = f_b / 1.8839$ $f_z = f_b / 2.862$

$f_{p2} = f_b$ $f_{LF} = f_b / 40$ (29-6)

Figure 29-12. Host and module output reference CTLE transfer function for 0 to 6 dB of high frequency gain and 0 dB of low frequency gain at 50 Gsym/s

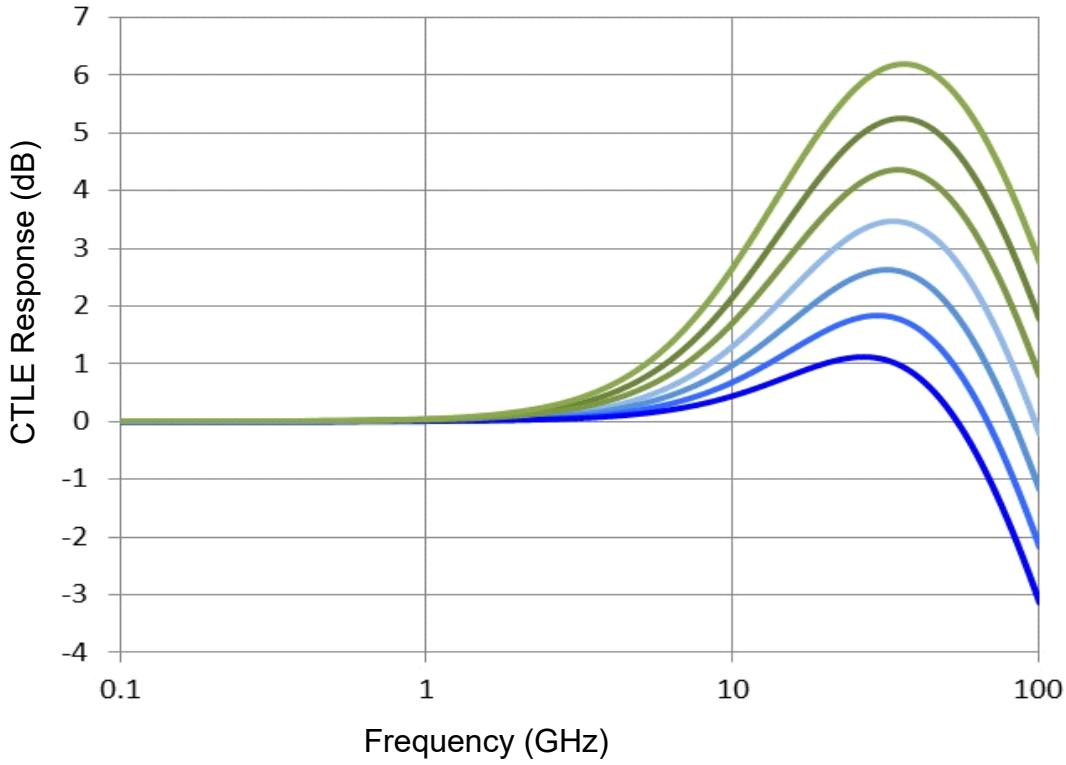
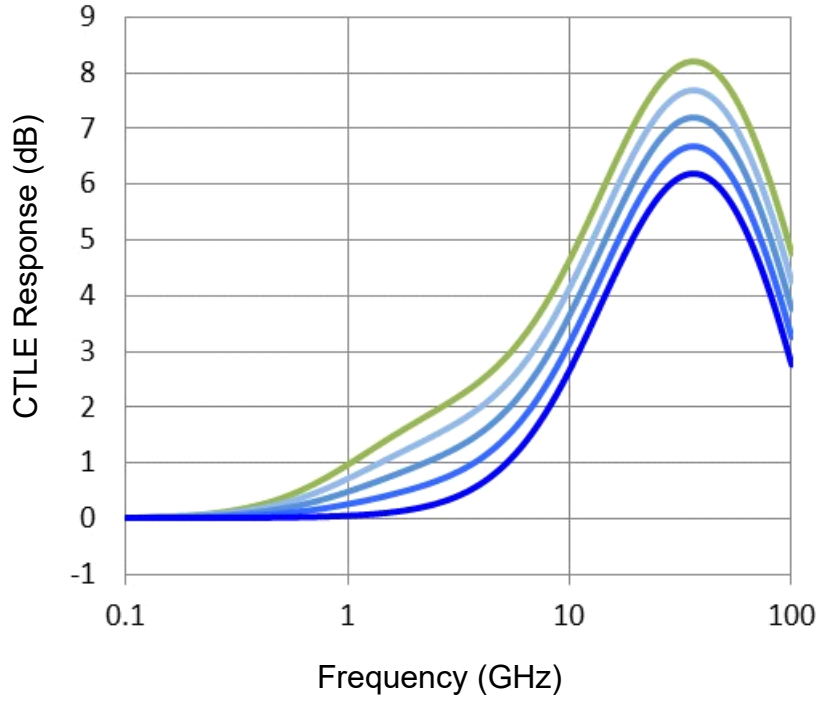


Figure 29-13. Host and module output reference CTLE transfer function for 6 dB of high frequency gain and 0 dB to 2.0 dB of low frequency gain at 50 Gsym/s



29.4.2 Input Overload Voltage Tolerance

The input voltage tolerance tests the acceptance of differential input peak-peak amplitudes produced by the extremes of operation from the host output (for host-to-module communication) or module output (for module-to-host communication).

The maximum voltage at an IC input can be larger than the maximum at the compliance point due to output/input impedances and reflections.

The input overload voltage tolerance specification is to be met for any valid CEI pattern. The differential voltage specified in Table 29-1 is somewhat smaller than the module input voltage tolerance due to the QPRBS13-CEI's pattern length accompanied with high host loss.

29.5 Compliance Boards

Use of compliance boards for testing is assumed for the parameters defined in Table 29-1 through Table 29-6. Figure 25-1 shows the test setup for making S-parameter measurements of the mated compliance boards. The compliance boards and measurement points are as specified in Section 25.4.

29.A Appendix - Recommended Electrical Channel

This appendix contains recommended electrical channels as described in Section 29.1. Note that in practice the host channel is not measurable as appropriate test points are not accessible.

The first recommended channel includes a host that consists of a majority of PCB trace with an expected host trace reach of up to at least 100 mm. The channel consists of host PCB trace, module PCB trace, vias, AC coupling capacitor and one connector, not in this order. The recommended PCB trace differential impedance is 90 ± 9 Ω. This full channel model is shown in Figure 29-14 below for Linear Pluggable Optical module (LPO) and Figure 29-15 for linear Near-Package Optics (NPO).

Figure 29-14. CEI-112G-LINEAR-PAM4 PCB – Pluggable Module Channel Reference Model

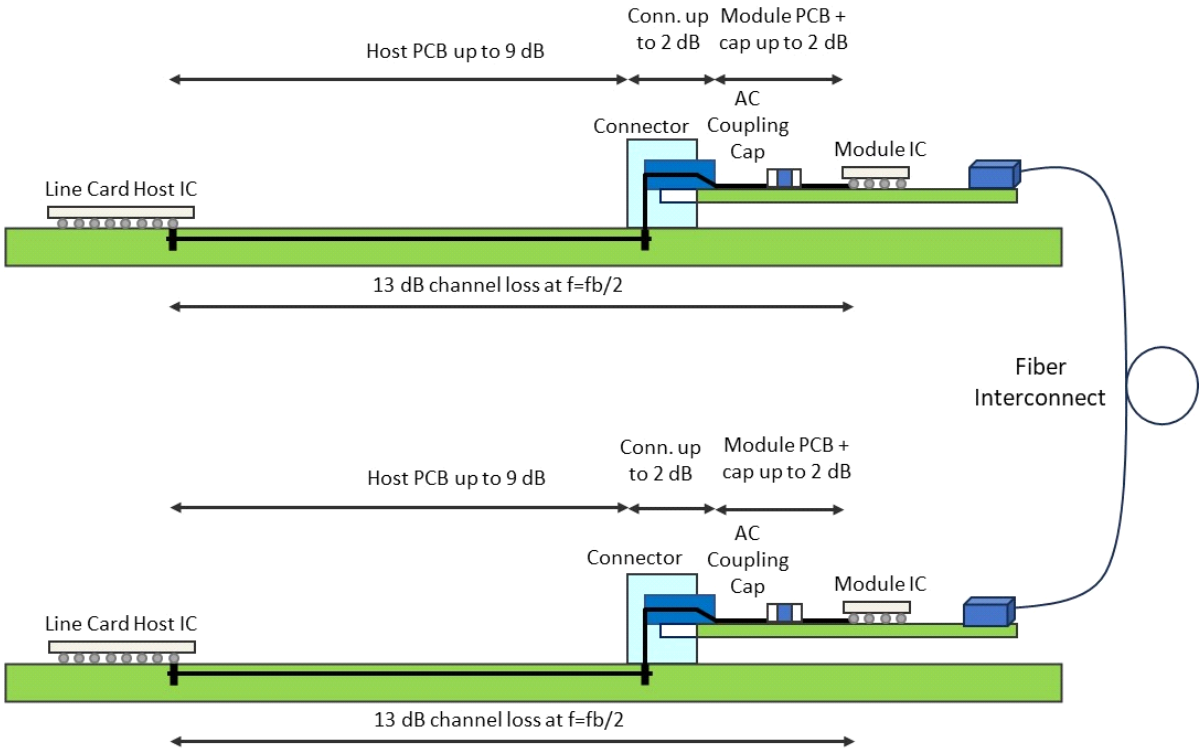
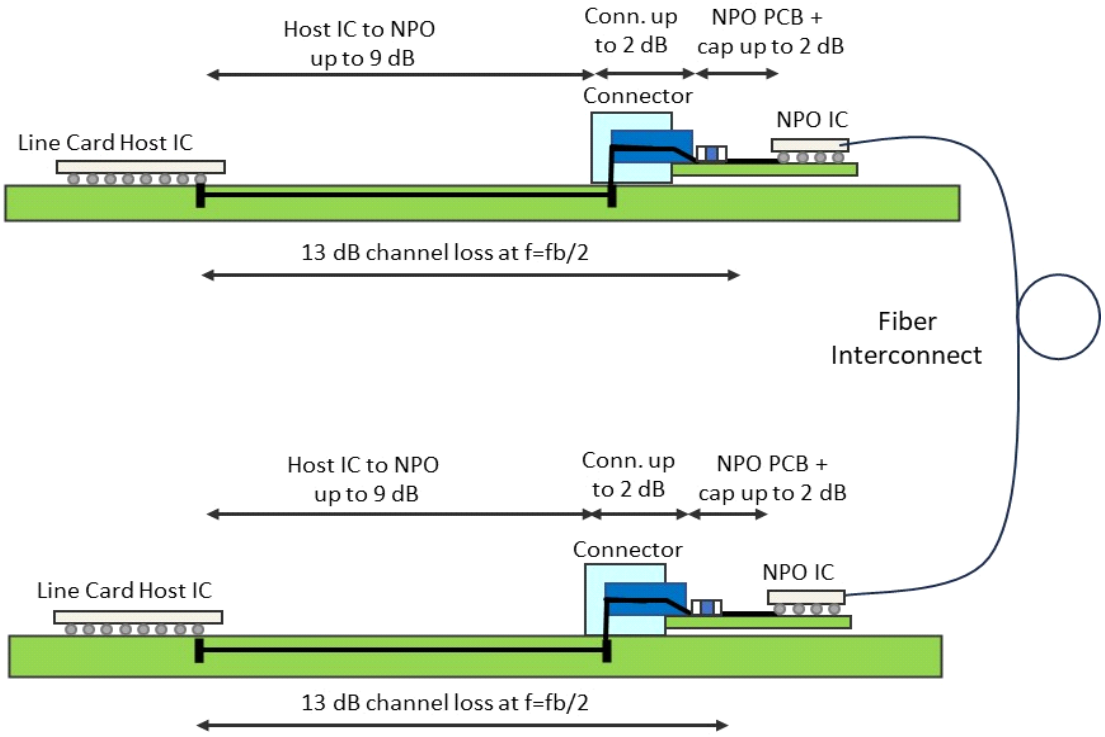


Figure 29-15. CEI-112G-LINEAR-PAM4 PCB – Near-Package Optics Channel Reference Model



The second recommended channel includes an extended reach host that consists of a majority of cable routing with an expected host cable reach of up to at least 350 mm. The channel consists of host PCB trace, module PCB trace, vias, AC coupling, two connectors and copper cable, not in this order. Note: The additional cable connector is considered part of the host channel budget. This full channel model is shown in Figure 29-16 below for Linear Pluggable Optical module (LPO) and Figure 29-17 for linear Near-Package Optics (NPO).

Figure 29-16. CEI-112G-LINEAR-PAM4 Cabled–Pluggable Module Channel Reference Model

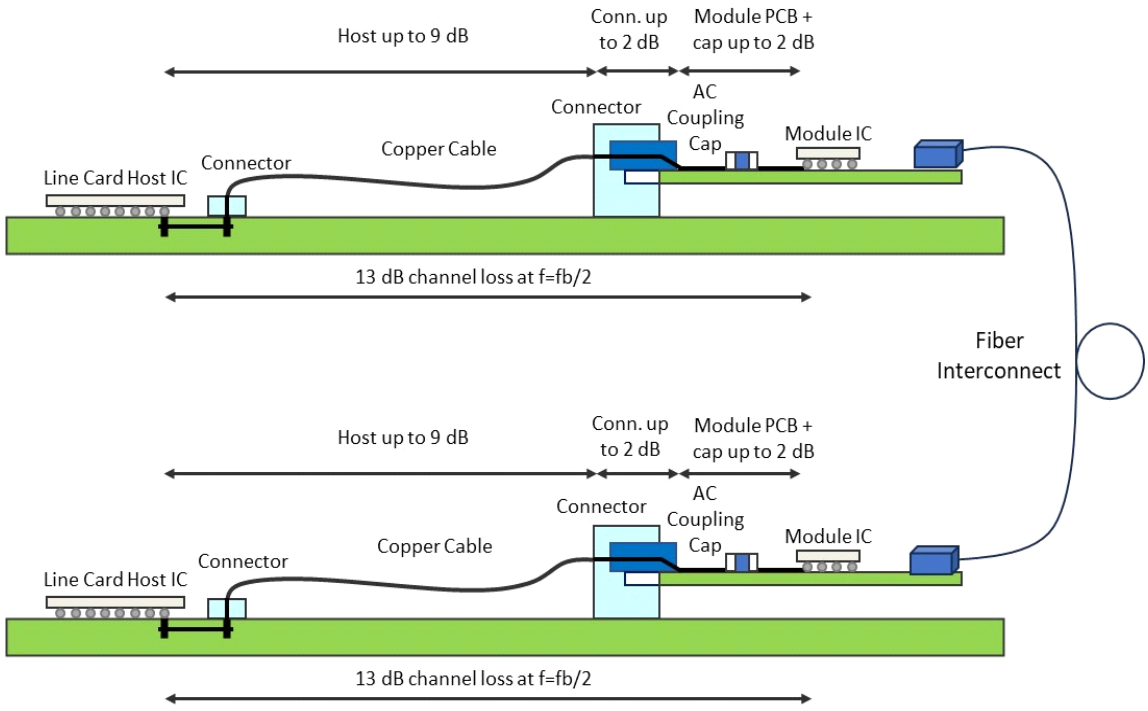
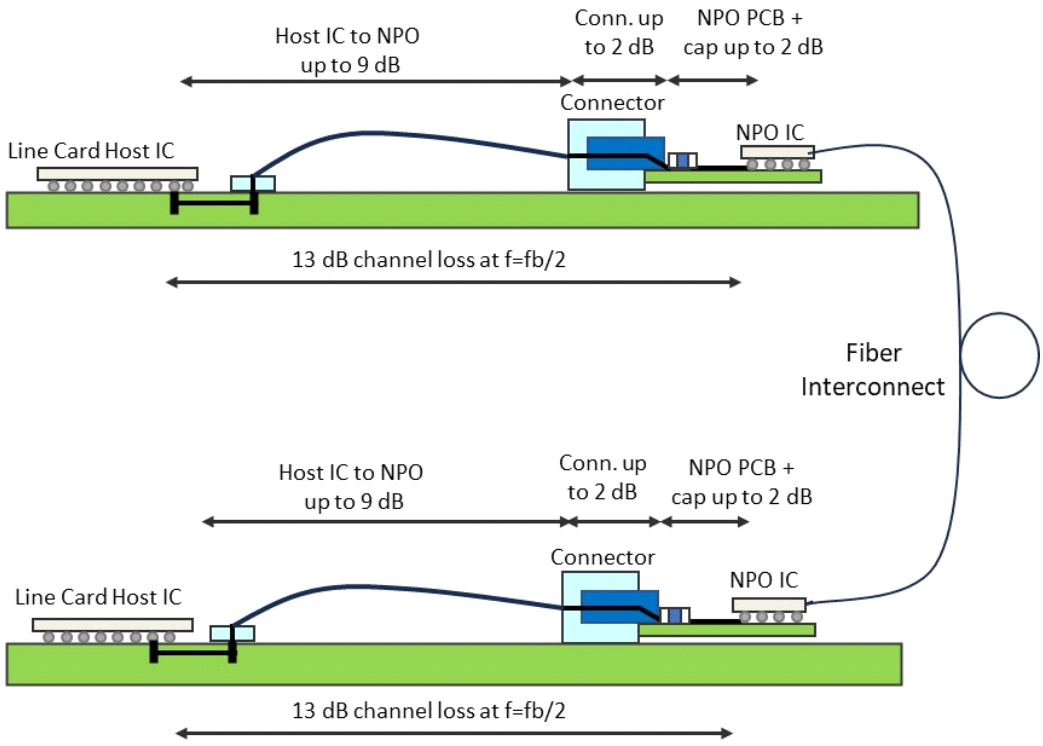
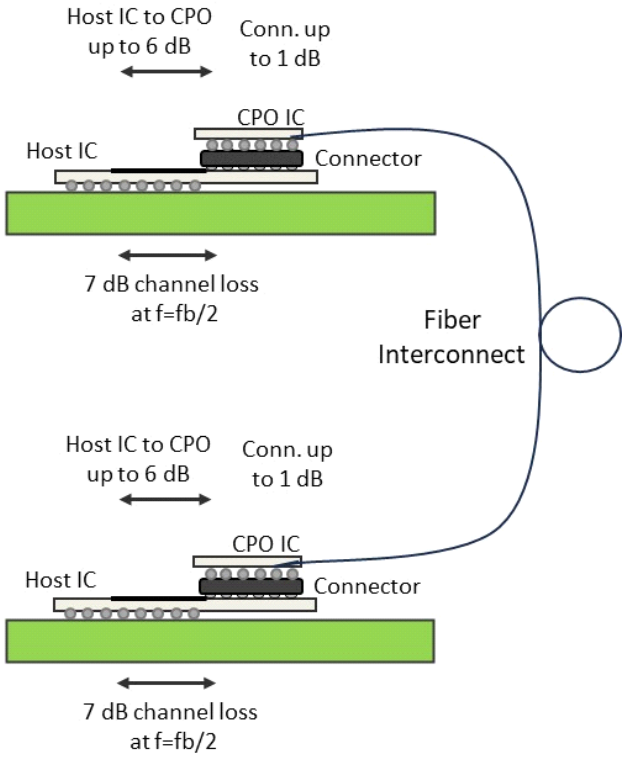


Figure 29-17. CEI-112G-LINEAR-PAM4 Cabled – Near-Package Optics Channel Reference Model



The third recommended channel includes a Co-Packaged Optics (CPO) host that consists of a optical IC mounted directly on a host IC package. The channel consists of package trace, module PCB trace and one connector, not in this order. This full channel model is shown in Figure 29-18 below for Co-Packaged Optical module (CPO). Note that the CPO reference model is not AC coupled.

Figure 29-18. CEI-112G-LINEAR-PAM4 Co-Packaged Optics Channel Reference Model



The expected reach is greatly influenced by the attenuation of the interconnect media used on the host. To illustrate this, Table 29-13 contains a comparison of several material class categories and the expected reach if the host consisted only of this media and no other interconnect pieces.

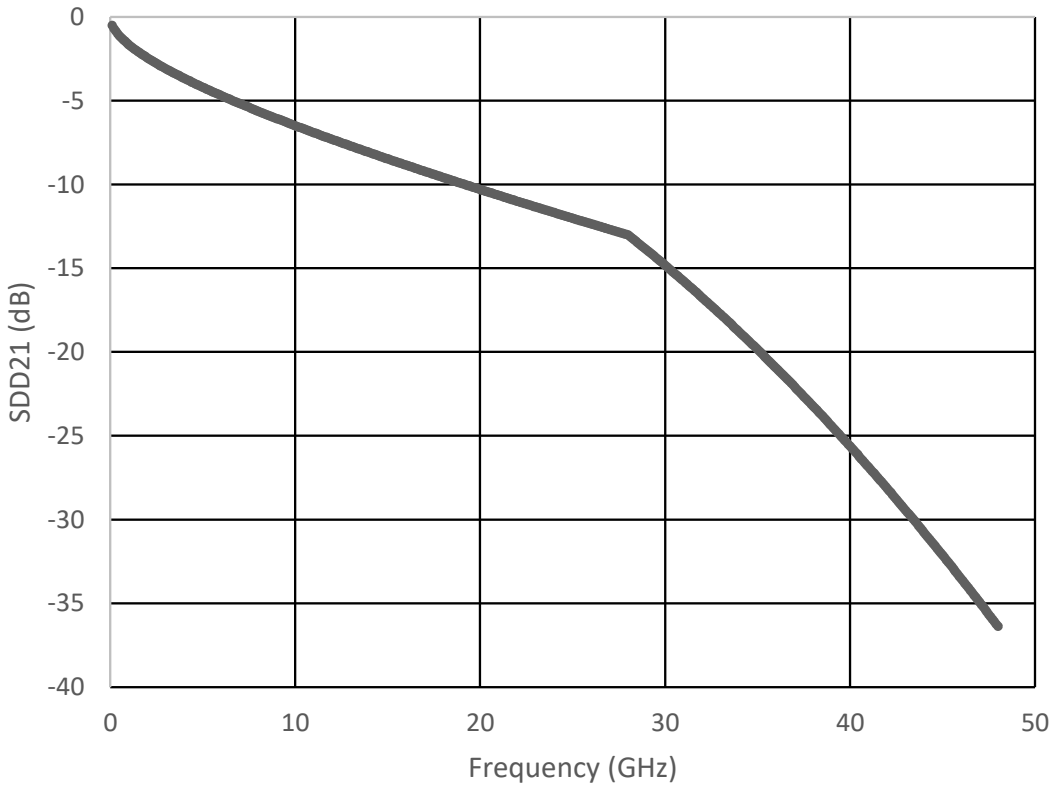
Table 29-13. Expected Reach of Different Material Classes

Material Class	Attenuation per mm (dB/mm)	Reach at 7 dB (mm)
Medium Loss PCB	0.1	70
Low Loss PCB	0.08	88
Ultra Low Loss PCB	0.05	140
TwinAx Cable	0.02	350

29.A.1 Insertion Loss

Host insertion loss and module insertion loss are recommended limits only. Achieving these recommended limits does not signify compliance nor guarantee successful communication between two devices. Equation (illustrated in Figure 29-19) represents the highest recommended insertion loss (see SDD21) between the package balls in the host and module. The equations for the channel are scaled from the recommended host insertion loss channel in the CEI-112G-VSR specification.

Figure 29-19. Recommended minimum SDD21 of the channel (for f_b= 56 GHz)



$$SDD21 = -0.01 - 10.75\sqrt{\frac{f}{f_b}} - 10.78\frac{f}{f_b} \qquad for\ f \le \frac{f_b}{2}$$

$$SDD21 = (-9.7)\left(\frac{f}{f_b}\right) - 32.6\left(\frac{f}{f_b}\right)^2 \qquad for\ \frac{f_b}{2} < f \le 0.85 f_b$$

In addition it is recommended that the Linear channel have an FOM_{ILD} less than or equal to 0.25 dB (see Section 20.2.7.4) and an ERL (Effective Return Loss) greater than or equal to 10 dB when using Nbx=2 for the Transmit direction and Nbx=18 for the Receive direction. (see Section 29.3.9)