Implementation Agreement for a 3.2Tb/s Co-Packaged (CPO) Module

OIF-Co-Packaging-3.2T-Module-01.0

March 29, 2023

Implementation Agreement created and approved

OIF

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TITLE: **Implementation Agreement for a 3.2Tb/s Co-Packaged (CPO) Module**

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ABSTRACT: This Implementation Agreement specifies key aspects and electro-optical-mechanical details of a 3.2Tb/s Co-Packaged Module encompassing optical and copper cable attach formats.

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OIF-Co-Packaging-3.2T-Module-01.0	March 29, 2023	Initial document release

1. Introduction

1.1. Scope

This document defines the technical specifications for a 3.2 Tb/s Co-packaged Optical (CPO) transceiver module, including mechanically compatible Copper Cable Attach modules, see Figure 1. These devices will serve as building blocks to enable lower power solutions for 51.2Tb/s switches, with 16 modules arranged in close proximity to the switch ASIC. Variants of the CPO modules are defined in this document, supporting 8 x 400GBASE-DR4 (with 32 Tx/Rx fiber pairs), 8 x 400GBASE-FR4 (with 8 Tx/Rx fiber pairs) and Copper Cable Attach modules (32 differential pair Tx/Rx electrical lanes). Full optical specification references are included in Section 4 “Optical Characteristics”.

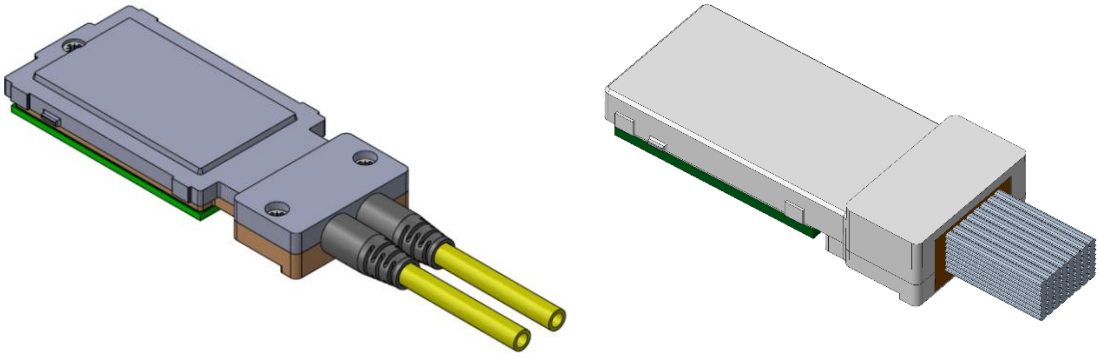

Figure 1 3.2T transceiver modules: Optical (L), and Copper Cable Attach (R)

1.2. Introduction

The 3.2 Tb/s transceiver is a building block for a 51.2 Tb/s switch assembly. The block diagram for the overall system is shown in Figure 2, with an example attachment model shown in Figure 3. The optical module provides conversion from short-reach electrical interfaces to optical I/O for the switch ASIC and the Copper Cable Attach (CCA) module supplies an electrical breakout from switch to front panel modules.

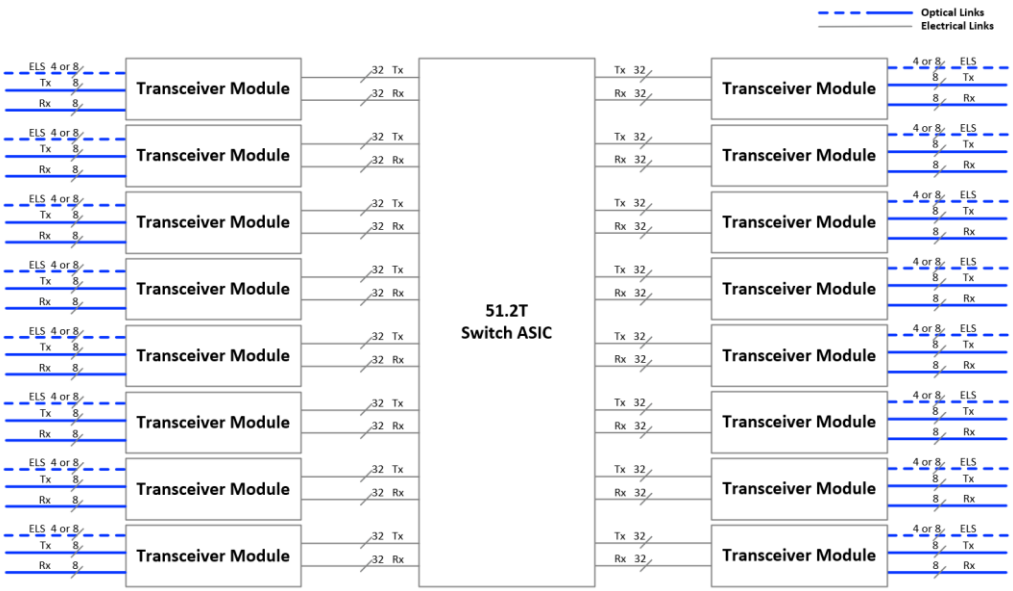

Figure 2 High-level system block diagram (Optical)

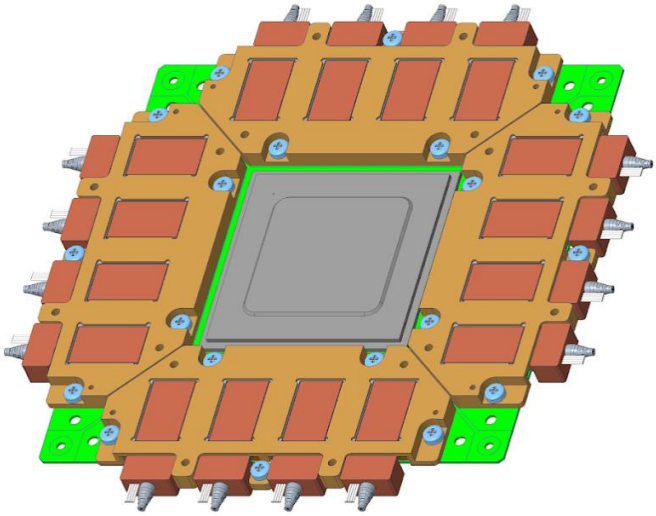

Figure 3 Example attachment system (51.2T)

Functional blocks for the optical transceiver module are shown in Figure 4. The module includes a digital signal processor (DSP), modulator driver and TIA functions in the optical transmitter and receiver. For the 400GBASE-FR4 variant, the module includes optical multiplexer (MUX) and de-multiplexer (DEMUX). The module variants defined include an internal laser option, with the laser diode integrated into the module, and external laser option with the laser being fed as an input to the module, the

primary use case of the external laser source (ELS) option is with the External Laser Small Formfactor Pluggable (ELSFP) module.

The configuration shown in Figure 4 is logical; implementations may arrange the DSP and transmit/receive lanes as appropriate, provided they support the inputs and outputs for the module, including optical, high-speed, DC, control, clock, etc. Given the high-density, integration of multiple functions and multiple 400G domains will likely be required.

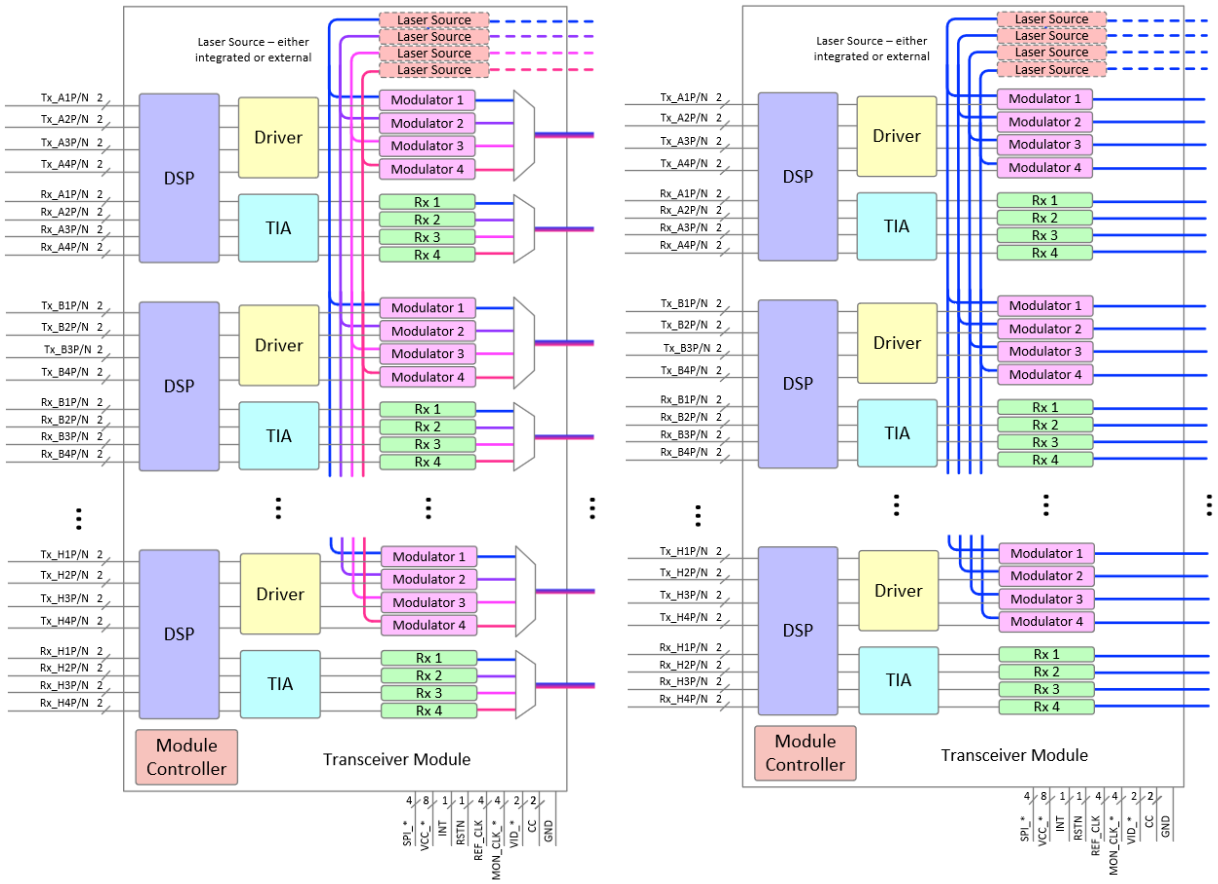

Figure 4 Functional block diagrams for variants 8×400GBASE-FR4 (L), and 8×400GBASE-DR4 (R)

The line side of the optical transceiver transmits and receives 8×400GBASE-FR4 or 8×400GBASE-DR4. The transceiver electrical interface facing the switch IC transmits and receives 32×106.25Gb/s electrical signals compliant to CEI-112G-XSR as a minimum.

The 400GBASE-FR4 variant also supports 200GBASE-FR4 operation for backward compatibility. When configured for 200G, the line side of the transceiver transmits and receives 8×200GBASE-FR4. The transceiver electrical interface facing the switch IC transmits and receives 32×53.125Gb/s PAM4 electrical signals. In this case, the CEI-112-XSR interface should operate in a 53.125Gb/s PAM4 mode.

Module Type	Host Side (Electrical)	Line Side	Internal/External Laser source
CPO3T2-400GDR4-IL	32 x 112G XSR	Optical 8 x 400G-DR4	Internal
CPO3T2-400GFR4-IL	32 x 112G XSR	Optical 8 x 400G-FR4 (incl. 8 x 200G-FR4)	Internal
CPO3T2-400GDR4-EL8PMF	32 x 112G XSR	Optical 8 x 400G-DR4	External, 8 PM fibers
CPO3T2-400GFR4-EL8PMF	32 x 112G XSR	Optical 8 x 400G-FR4 (incl. 8 x 200G-FR4)	External, 8 PM fibers
CPO3T2-400GDR4-EL4PMF	32 x 112G XSR	Optical 8 x 400G-DR4	External, 4 PM fibers
CPO3T2-400GFR4-EL4PMF	32 x 112G XSR	Optical 8 x 400G-FR4 (incl. 8 x 200G-FR4)	External, 4 PM fibers
CCA3T2-DAC			N/A

Table 1 3.2T Module Types Definition Table

The module will be mounted on a Co-Packaged Assembly Substrate, which provides high-speed data path to the Switch ASIC. Figure 5 shows two implementation options for the channel. In diagram (a) the ASIC package and module sit on the Co-Packaged Assembly Substrate (also referred to as Interposer technology). In (b) the ASIC die sits directly on the Co-Packaged Assembly Substrate. In both cases, the channel is defined as between the "die bumps" of the electrical circuits, as per CEI-112G-XSR-PAM4 definitions. This IA requires support of XSR interfaces. Modules may also optionally support XSR+ interfaces.

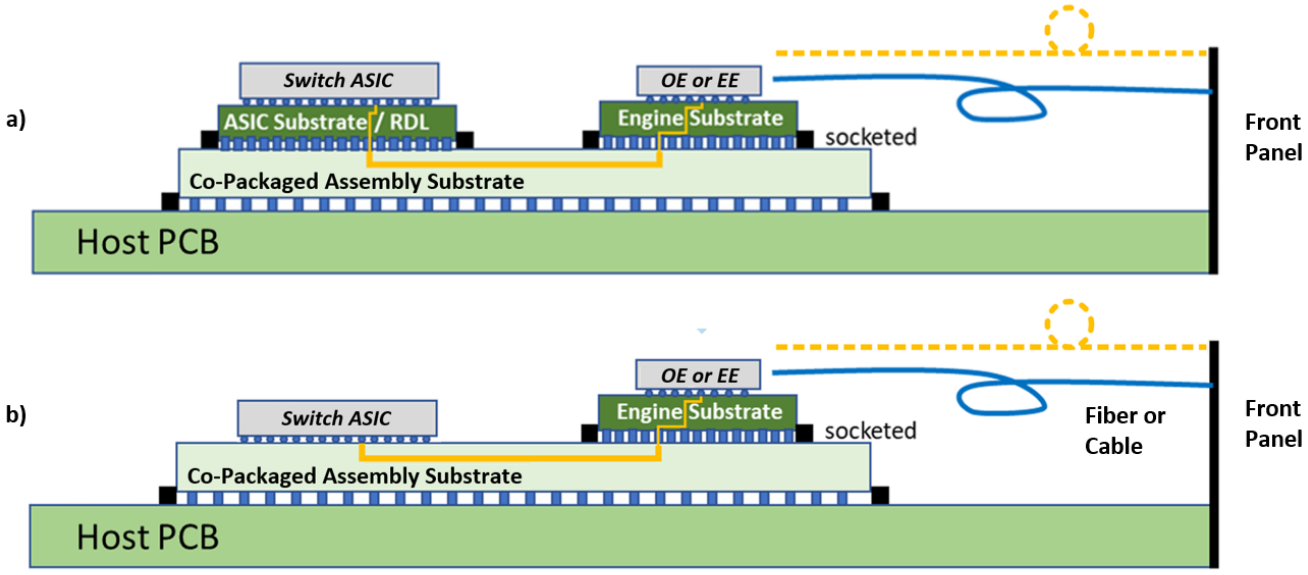

Figure 5 Typical electrical channel implementation options: a) with ASIC package/substrate; b) without ASIC package/substrate

The transceiver shall have adequate margin to operate under the switch ASIC FEC BER threshold under specified conditions and over life. The architecture anticipates that the electrical signal gets retimed on both sides of the link, but FEC is only applied at the host (switch IC), as shown in Figure 6, following the IEEE 802.3 AUI definition.

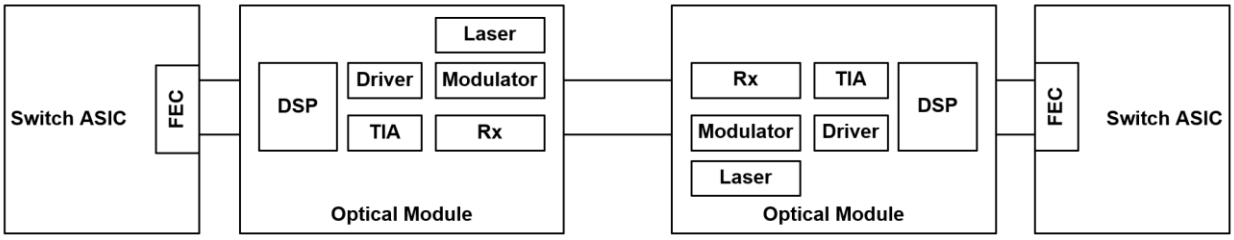

Figure 6 Arrangement of FEC correction

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Storage temperature	T_st	-40	85	°C	
Relative humidity, storage and transportation	RH	5	95	%	Note1
ESD, low speed pins (<5Gbps)	ESD_HBM_low_speed		1000	V	Human body model
ESD, high speed pins (>5Gbps)	ESD_HBM_high_speed		500	V	Human body model
ESD, low speed pins (<5Gbps)	ESD_CDM_low_speed		250	V	Charged device model
ESD, low speed pins (>5Gbps)	ESD_CDM_high_speed		125	V	Charged device model
Power supplies	VCC_3P3	-0.5	4.6	V	
	VCC_2P6	-0.5	3.6	V	
	VCC_1P8	-0.5	2.5	V	
	VCC_1P2	-0.5	1.8	V	JESD8-12A.01
	VCC_0P9	-0.5	1.2	V	
	VCC_0P7A, VCC_0P7B	-0.5	1.0	V	
	VCC_12	-0.5	16.8	V	
SPI pins	SPI_CLK, SPI_CSO, SPI_MOSI, SPI_MISO	-0.5	1.8	V	JESD8-12A.01
Low speed control	INTN, RSTN	-0.5	1.8	V	JESD8-12A.01
Reference Clock	REFCLK_1P/N, REFCLK_2P/N				
Vendor ID	VID_0, VID_1	-0.5	1.8	V	JESD8-12A.01
Connectivity Check	CC	TBD	TBD	V	
ELS input: optical power per fiber, 1:4	ELS_P_4		24	dBm	
ELS input: optical power per fiber, 1:8	ELS_P_8		24	dBm	

Note:

1. The environment in which the module is operated must be controlled to prevent condensation. Compliance with ambient temperature and humidity limits defined in GR-63 is required.

Table 2 Absolute Maximum Ratings

3. Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Note
Signaling rate, each lane, 200GBASE-FR4 mode			26.5625		GBaud	+/-100ppm
Signaling rate, each lane, 400G modes			53.125		GBaud	+/-100ppm
Modulation format			PAM4			
Module power supply noise tolerance, peak to peak	PSNR			2	%	Between 10Hz-10MHz
Operating case temperature, with integrated laser	Tcase_int	15		70	°C	Note 1
Operating case temperature, without integrated laser	Tcase_ext	15		85	°C	Note 1
Power consumption, with integrated laser	P			56	W	Tc = Max, End of Life
Power consumption, without integrated laser	P			48	W	Tc = Max, End of Life
Low Power Mode				2	W	per 2x400G. Note 3
Relative humidity	RH	5		90	%	Note 2
Expected component lifetime	T_{OP}	TBD			Years	

Note:
1. Tcase to be measured in the middle of the top surface of the heat spreader. Module shall support loopback operation at TBD case temp for 12 hours. System integrator responsible for system level thermal solution.
2. Non-condensing. Transceiver shall also support up to 95% RH for up to 500hrs over life of component.
3. Low Power mode is enabled through CMIS control with a 2x400G granularity

Table 3 Module Operating Conditions

Rail Type	Supply Rail	Vmin (V)	Vnom (V)	Vmax (V)	DC tol.	Max Current (A)
Adjustable (host controlled)	VCC_3P3	2.81	3.30	3.80	+/-3%	5.1
	VCC_2P6	2.20	2.60	3.00	+/-3%	3.6
	VCC_1P8	1.44	1.80	2.16	+/-3%	6.4
	VCC_0P9	0.77	0.90	1.04	+/-3%	28.0
	VCC_0P7A	0.60	0.70	0.81	+/-3%	18.0
	VCC_0P7B	0.60	0.70	0.81	+/-3%	21.0
	VCC_12	10.20	12.00	13.80	+/-5%	0.5
Fixed	VCC_1P2	-	1.20	-	-	2.0

Table 4 Power Supply Operating Specifications

Table 4 defines the operating ranges of the power supplies to the module. The supplies of 12V, 3.3V, 2.6V, 1.8V, 0.9V and two sets of 0.7V are variable within an approximate range of +/- 15% to 20% (as listed) and controlled by the host system. The 1.2V, being the communications supply, is of a fixed

nominal value within standard JEDEC range (+/- 8%). The DC tolerance column defines the accuracy of the set voltage vs its target.

3.1. Power Supply Sequencing

For module activation, the power supplies should be fully turned on in sequence, as shown in Figure 7. Each supply shall be ramped to its target value and held before the next supply begins its ramp. Min/max ramp times are specified in Table 5.

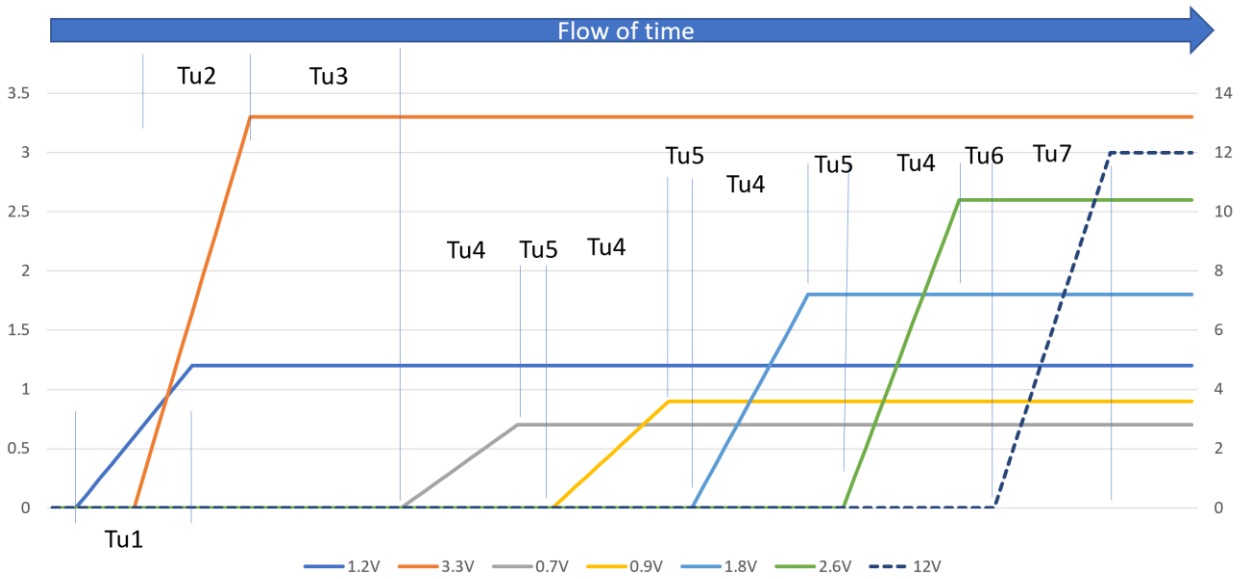

Figure 7 Module Activation Supply Sequencing

Measurement	Symbol	Min	Max	Units
1.2V Ramp Duration	Tu1	0.5	10	mS
3.3V Ramp Duration	Tu2	0.5	10	mS
Delay between 1.2V/3.3V, 0.7V	Tu3	0.5	-	mS
0.7V, 0.9V, 1.8V, 2.6V Ramp Duration	Tu4	0.5	10	mS
Delay between 0.7V, 0.9V, 1.8V, 2.6V	Tu5	0.5	-	mS
Delay between 2.6V, 12V	Tu6	0.5	-	mS
12V Ramp Duration	Tu7	0.5	10	mS

Table 5 Module Activation Supply Timing

For module deactivation, the reverse of the activation sequence should be followed, except the minimum time between deactivations is 0mS. Sequencing and Timing are shown in Figure 8.

If any power rail is dropped, then all rails should drop and they activation sequence started again to enable the module.

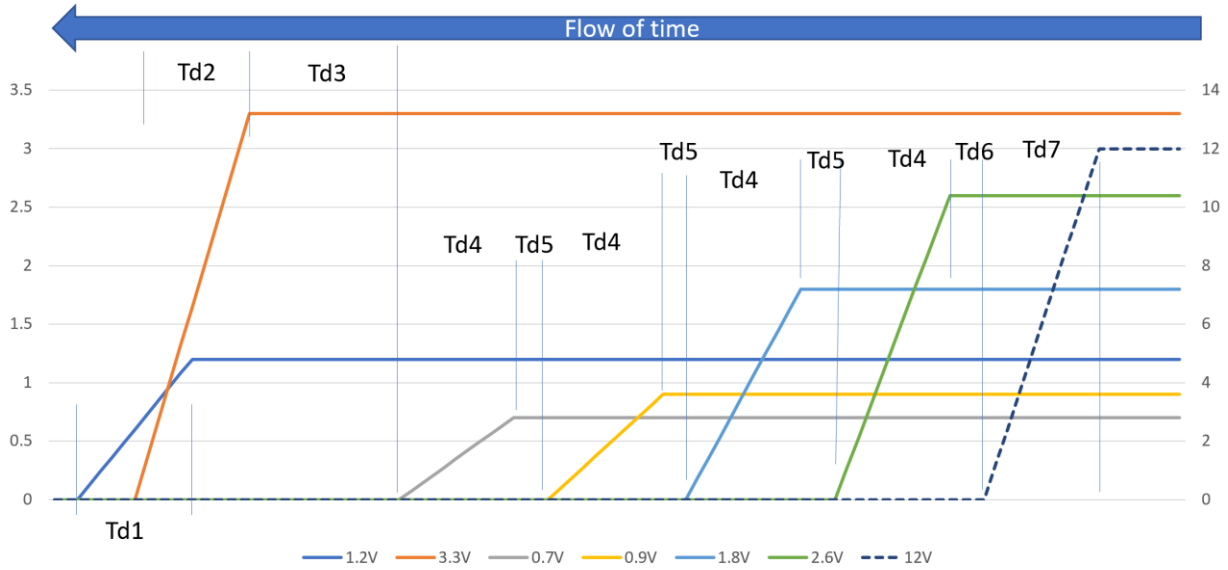

Figure 8 Module Deactivation Supply Sequencing

Measurement	Symbol	Min	Max	Units
1.2V Ramp Duration	Td1	0	10	mS
3.3V Ramp Duration	Td2	0	10	mS
Delay between 0.7, 1.2V/3.3V	Td3	0	10	mS
2.6V, 1.8V, 0.9V, 0.7V Ramp Duration	Td4	0	10	mS
Delay between 2.6V, 1.8V, 0.9V, 0.7V	Td5	0	10	mS
Delay between 12V, 2.6V	Td6	0	10	mS
12V Ramp Duration	Td7	0	10	mS

Table 6 Module Deactivation Supply Timing

3.2. Low Power Mode or Power Shutdown

In some applications, not all of the optical ports will be used. Ideally, these unused lanes can be shut down such that they consume no (power shutdown) or little (low-power-mode) power. Within the optical module, the ability to select shutdown/low-power-mode on a per port basis is preferred, but not required. The minimum granularity required for shutdown/low-power-mode is two 400G-FR4 interfaces. Max power consumption in low-power-mode is provided in Table 3.

4. Optical Characteristics

The optical specifications in general follow IEEE 802.3 and Open Compute Project as detailed below, unless this document specifies otherwise.

4.1. Optical Transmitter and Receiver Characteristics for 200GBASE-FR4 Mode

Optical module shall comply with requirements defined in IEEE 802.3 specification, section 122.7.1, and Open Compute Project: 200G-FR4 OCP Optical Transceiver Specification Rev 0.3.

4.2. Optical Transmitter and Receiver Characteristics for 400GBASE-DR4 Mode

Optical module shall comply with requirements defined in IEEE 802.3 specification, sections 124.7.1 and 124.7.2.

4.3. Optical Transmitter and Receiver Characteristics for 400GBASE-FR4 Mode

Optical module shall comply with requirements defined in IEEE 802.3cu specification, sections 151.7.1 and 151.7.2, and Open Compute Project: 400G-FR4 QSFP-DD OCP Optical Transceiver Specification Rev 0.1.

4.4. External Light Source

For CPO designs which use an external light source, the following specifications apply. The light needs to be coupled into a PM fiber, which in turn is coupled to the CPO. Loss budget and tolerance likely need careful attention to enable appropriate output power. The light source will provide a small control range as a means to tune the modulated output power, which allows the module to ensure compliance of its optical Tx output.

This implementation agreement does not restrict the implementation or form factor of the ELS, provided it complies with the specifications herein.

4.5. Test points for ELS and Optical Module (OE)

The test source for module compliance tests is calibrated at TP_{L3} (see Figure 9), which is defined as the output of a 2 to 5m patch cord. The optical output of the module is tested with a 2 to 5m patch cord.

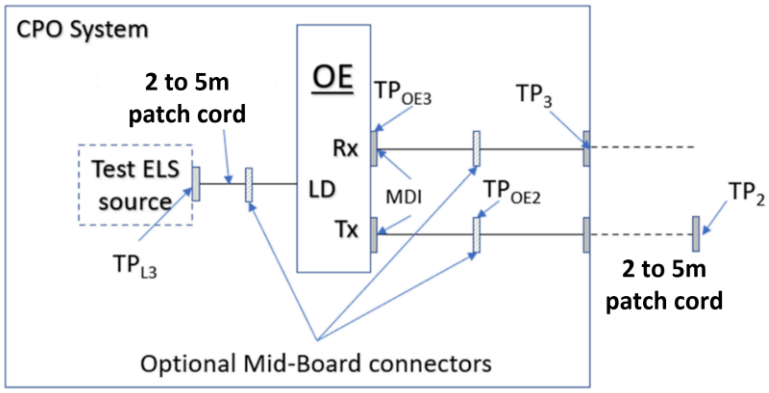

Figure 9 Optical test points for the 3.2T Module

4.6. External Light Source Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Note/Ref
FR4 Center Wavelength 1	FR-WL1	1264.5	1271	1277.5	nm	
FR4 Center Wavelength 2	FR-WL2	1284.5	1291	1297.5	nm	
FR4 Center Wavelength 3	FR-WL3	1304.5	1311	1317.5	nm	
FR4 Center Wavelength 4	FR-WL4	1324.5	1331	1337.5	nm	
DR4 Center Wavelength	DR-WL	1304.5	1311	1317.5	nm	
Optical power capability per fiber (EL8PMF)	P_{EL8PMF}	18.5			dBm	
Minimum set point of operating power per fiber (EL8PMF)	P_MIN_{EL8PMF}			15	dBm	Note 1
Optical power capability per fiber (EL4PMF)	P_{EL4PMF}	22			dBm	
Minimum set point of operating power per fiber (EL4PMF)	P_MIN_{EL4PMF}			18	dBm	Note 1
Optical power control granularity	P_C_{ELS}		1		dB	Note 1
Laser RIN	RINc	-141.5			dB/Hz	Note 2
Laser SMSR	SMSR	30			dB	
Laser linewidth	$\Delta\nu$	-	-	2	MHz	Notes 2,3
Polarization Extinction Ratio	r_{ex}	10			dB	
Output reflectance	Rx_Ref			-26	dB	
Optical return loss tolerance	ORLT			*TBD*	dB	was 17.1

Reflection Specifications	Symbol	Max	Unit	Reference
Optical return loss tolerance (System TP2)	Rtol_TX	17.1	dB	400GBASE-FR4 802.3cu-2021
		15.5	dB	100GBASE-DR 802.3cd-2018
Transmitter reflectance (System TP2)	Ref_TX	-26	dB	400GBASE-FR4 & 100GBASE-DR
Receiver reflectance (System TP3)	Ref_RX	-26	dB	400GBASE-FR4 & 100GBASE-DR
OE Optical return loss tolerance (OE TP_{OE3})	Rtol_TX_OE	17.1	dB	400GBASE-FR4 802.3cu-2021
		15.5	dB	100GBASE-DR 802.3cd-2018
OE Transmitter reflectance (OE TP_{OE2})	Ref_TX_OE	-26	dB	
OE Receiver reflectance (OE TP_{OE3})	Ref_RX_OE	-26	dB	
OE Laser input reflectance (OE TP_{L3})	Ref_Lin_OE	-28.2	dB	Placeholder for both DR and FR Assumes OE Tx is not the dominant source of reflection from the laser through the link
ELS Optical return loss tolerance: maximum of 3 connectors	Rtol_ELS	28.2	dB	oif2021.237.01, for both DR and FR, assumes 8 lasers per 3.2T

between ELS and OE (each with ORL of 45dB) (ELS TP_{L2})				
ELS Reflectance (ELS TP_{L2})	Ref_ELS	-26	dB	Matches IEEE Tx reflectance

Notes:

1. Optical power can be requested from the ELS at the specified output power granularity
2. At maximum optical return loss
3. The linewidth is defined as the -3dB full width of a self-heterodyne (3.5µs delay) measurement. Typically, one arm of the interferometer is shifted in frequency (OIF-ITLA-MSA-01.3). It is the Lorentzian component of the optical noise spectrum and is related to the white phase noise component of the optical field.

Table 7 External Light Source Specifications (at TP_{L3})

5. Electrical Specification

5.1. Electrical Connector

Electrical I/O connects from the assembly substrate into the module substrate via LGA pads. There are two different pad pitch areas: 0.9 mm x 0.6 mm for the RF region and 0.6 mm x 0.6 mm for the DC/low-speed region. The electrical pinout is shown in Figure 10 with the pinout details shown in Table 8.

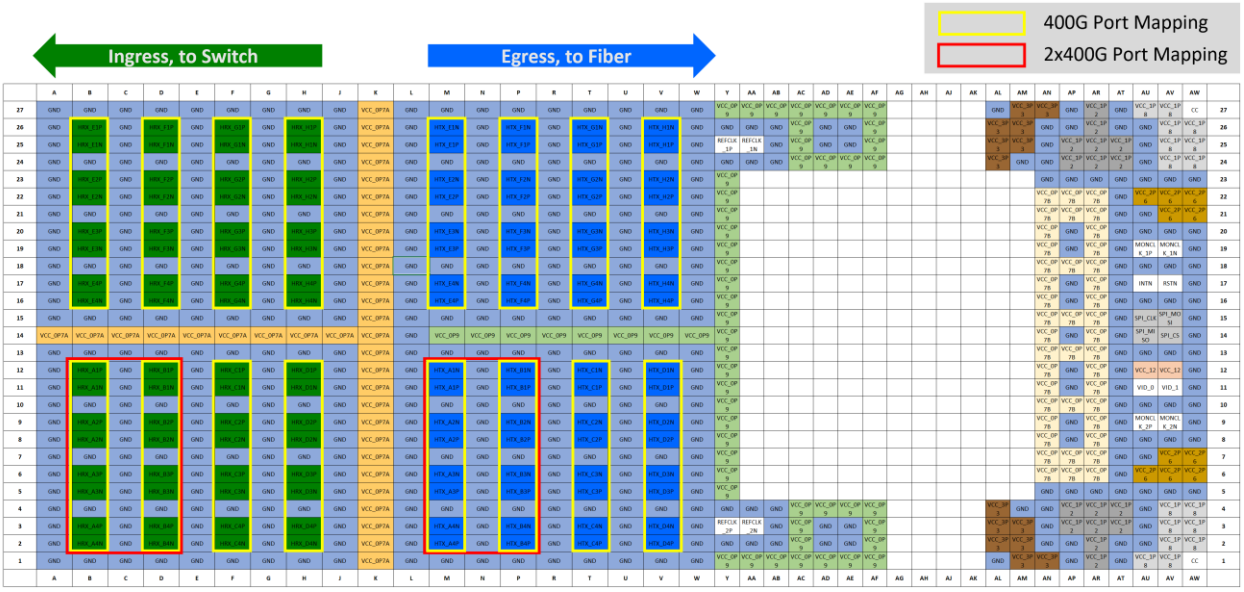

Figure 10 Electrical pins of 3.2 Tbs/s transceiver module (Top View)

Signal Group	LGA Net Name	Type	Count	Description
Host Side Interface				
Electrical Data Outputs	HRX_A[1:4][PN]	Output	8	Differential pair for RX data to HOST A – Lane 1 to 4
	HRX_B[1:4][PN]	Output	8	Differential pair for RX data to HOST B – Lane 1 to 4
	HRX_C[1:4][PN]	Output	8	Differential pair for RX data to HOST C – Lane 1 to 4
	HRX_D[1:4][PN]	Output	8	Differential pair for RX data to HOST D – Lane 1 to 4
	HRX_E[1:4][PN]	Output	8	Differential pair for RX data to HOST E – Lane 1 to 4
	HRX_F[1:4][PN]	Output	8	Differential pair for RX data to HOST F – Lane 1 to 4
	HRX_G[1:4][PN]	Output	8	Differential pair for RX data to HOST G – Lane 1 to 4
	HRX_H[1:4][PN]	Output	8	Differential pair for RX data to HOST H – Lane 1 to 4
Electrical Data Inputs	HTX_A[1:4][PN]	Input	8	Differential pair for TX data from HOST A – Lane 1 to 4
	HTX_B[1:4][PN]	Input	8	Differential pair for TX data from HOST B – Lane 1 to 4
	HTX_C[1:4][PN]	Input	8	Differential pair for TX data from HOST C – Lane 1 to 4
	HTX_D[1:4][PN]	Input	8	Differential pair for TX data from HOST D – Lane 1 to 4

	HTX_E[1:4][PN]	Input	8	Differential pair for TX data from HOST E – Lane 1 to 4
	HTX_F[1:4][PN]	Input	8	Differential pair for TX data from HOST F – Lane 1 to 4
	HTX_G[1:4][PN]	Input	8	Differential pair for TX data from HOST G – Lane 1 to 4
	HTX_H[1:4][PN]	Input	8	Differential pair for TX data from HOST H – Lane 1 to 4
Management Interface				
SPI	SPI_CLK	Input	1	SPI Serial clock
	SPI_CS	Input	1	SPI Chip Select. Additional chip select might be considered to support different implementations.
	SPI_MOSI	Input	1	SPI Master data output
	SPI_MISO	Output	1	SPI Master data input
Interrupt	INTN	Output	1	Interrupt output, Active low
Low Speed	RSTN	Input	1	Master Reset (PowerOnReset), Active Low
Reference Clocks				
Refclks	REFCLK_1P	Input	1	Positive Terminal of Differential Reference Clock
	REFCLK_1N	Input	1	Negative Terminal of Differential Reference Clock
	REFCLK_2P	Input	1	Positive Terminal of Differential Reference Clock
	REFCLK_2N	Input	1	Negative Terminal of Differential Reference Clock
Lineside Monitor Clocks				
	MONCLK_1P	Output	1	Positive Terminal of Monitoring Clock Output
	MONCLK_1N	Output	1	Negative Terminal of Monitoring Clock Output
	MONCLK_2P	Output	1	Positive Terminal of Monitoring Clock Output
	MONCLK_2N	Output	1	Negative Terminal of Monitoring Clock Output
Miscellaneous				
Vendor ID pins	VID_0, VID_1	Output	2	Vendor ID PIN, GND or float per agreement may be used for initial power up identification (optional)
Connectivity Check	CC	Inout	2	Optional Connectivity Check pins (if not used, No-connect)
Power Supplies				
Supplies	VCC_3P3	PWR	-	Variable power supply, controlled by host
	VCC_2P6	PWR	-	Variable power supply, controlled by host
	VCC_1P8	PWR	-	Variable power supply, controlled by host
	VCC_1P2	PWR	-	Fixed value power supply (for comms.)
	VCC_0P9	PWR	-	Variable power supply, controlled by host
	VCC_0P7A	PWR	-	Variable power supply, controlled by host
	VCC_0P7B	PWR	-	Variable power supply, controlled by host
	VCC_12	PWR	-	Variable power supply, controlled by host
	GND	GND	-	Ground

Table 8 Electrical Pin Definitions

5.2. Low Speed PIN Electrical Specification

The low-speed signal electrical specification is shown in Table 9. The 1.2V supply follows JEDEC standard JESD8-12A.01, normal range option. ModSelL pin will not be required as it will be included in the SPI bus (SPI chip select or SPI_CS). INTN and RSTN pins are required. VID_0 and VID_1 are optional. For further details on the SPI interface including timing and waveforms, see Section 7.2 SPI Interface Timing.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{cc}	IO Supply Voltage		1.1	1.2	1.3	V
V_{IL}	Input Low Voltage		-0.3		0.35 x V_{CC_1p2}	V
V_{IH}	Input High Voltage		0.65 x V_{CC_1P2}		V_{CC_1P2} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA			0.25 x V_{CC_1p2}	V
V_{OH}	Output High Voltage	I_{OH} = -2mA	0.75 x V_{CC_1P2}			V

Table 9 Low Speed Electrical Specification

5.3. High Speed PIN Electrical Specification

The egress (Tx) high speed electrical interface from the switch ASIC shall be AC-coupled inside the module; the ingress (Rx) will be AC coupled on the switch ASIC. The module's high speed electrical interface shall be compliant to CEI-112G-XSR-PAM4.

Rx electrical output squelch upon receiver loss of signal (Rx LOS) or loss of lock (Rx LOL) is required. During normal operation, when Rx LOS or Rx LOL occurs on any optical channel, module firmware (FW) shall check the squelch setting of all Rx and squelch the lanes that have Rx squelch enabled and shall do nothing for the lanes that have Rx squelch disabled. For any lane that is in the Rx squelch state, the output impedance levels are maintained while the differential voltage amplitude shall be less than the values defined in Table 10.

Tx optical output squelch is required. During normal operation, when the peak-to-peak electrical amplitude on any of the Tx input lanes from the switch ASIC is less than the input voltage level defined in Table 10, a Tx LOS will be triggered on that lane. Module FW shall check all the Tx and squelch the optical output of the channels that have Tx squelch enabled and shall do nothing for the channels that have Tx squelch disabled. For any channel in the Tx squelch state, the output optical power (AOP specifically) shall be turned off. The squelch selection (P_{AVG} or P_{OMA}) is defined by CMIS register control and the methodology is defined by the respective optical standard.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Differential peak-to-peak output voltage, at squelch				50	mV	
Differential peak-to-peak input voltage to trigger squelch				100	mV	

Table 10 Electrical Squelch Specification

5.4. Reference Clock Specification

Parameter	Conditions	Min	Typ	Max	Unit
Frequency[1]		---	156.25	---	MHz
Frequency Tolerance		---	---	100	ppm
Differential Swing	Peak-to-Peak	800	---	1600	mV
Single-ended Swing	Peak-to-Peak	400	---	800	mV
Duty Cycle		40	---	60	%
Rise Time	20% to 80%	---	---	400	ps
Fall Time	80% to 20%	---	---	400	ps
AC Coupling1		---	100	---	nF
RMS Jitter	12 kHz – 1 MHz			120	fs
	1 MHz – 20 MHz			150	fs
	12 kHz – 20 MHz			220	fs
Note: 1. The 156.25 MHz and 100 nF are the only values supported					

Table 11 Reference Clock Specification

5.5. Connectivity Check (CC) Pin Specification

The connectivity check (CC) pins will be used to detect that a module has been properly seated. The two pins should have a < 2 ohm trace connecting them. System integrators should have a pull-up on one pin and a pull-down on the other pin. By observing the CC pin with the pull-down, the system integrator can determine if the module is seated. Figure 11 shows the schematic scheme for the module.

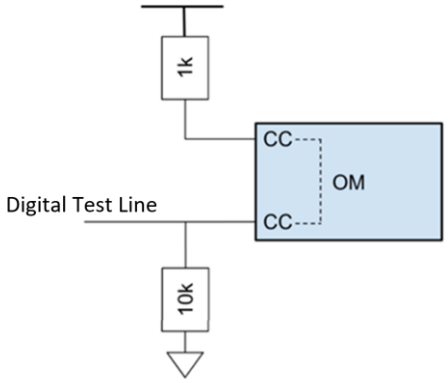

Figure 11 Connectivity Check (CC) pin schematic

6. Mechanical

The switch assembly consists of a high-density organic substrate, switch ASIC and modules. The modules may overhang the substrate arrayed around the perimeter (as shown in Figure 3), or may be embedded on the board. Optical fiber styles and strain relief on the figure are for illustration only, as these are not defined in the IA.

The mechanical drawing of the transceiver module is shown in Figure 12. All mechanical dimensions are shown in mm.

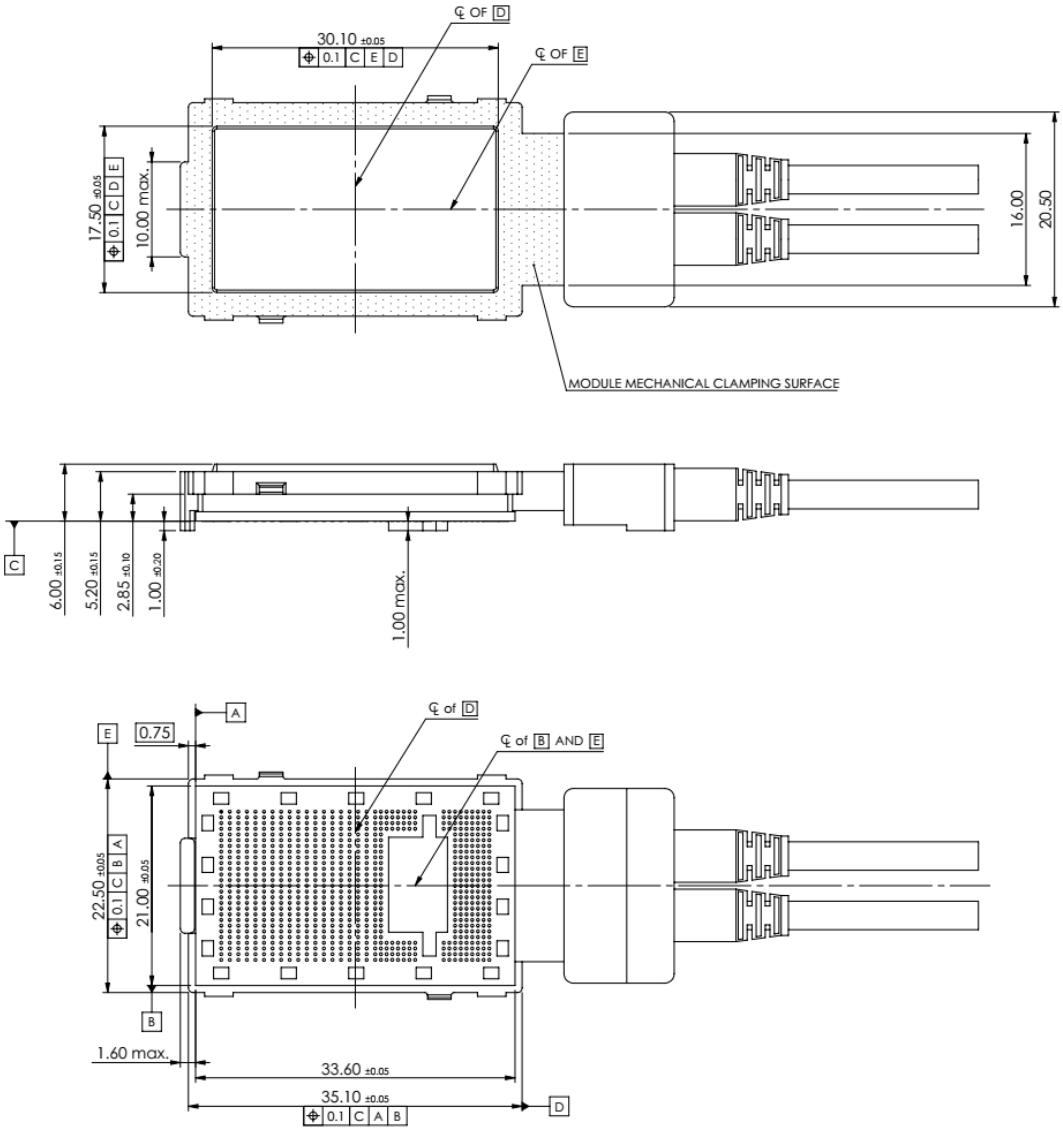

Figure 12 Module mechanical dimensions

The optical module is pigtailed with a minimum 5cm pigtail length. Optical connectors are not defined by the IA, options for implementation may be MPO style connectors to a bulk-head adaptor inside the switch system, or directly to the front-panel faceplate.

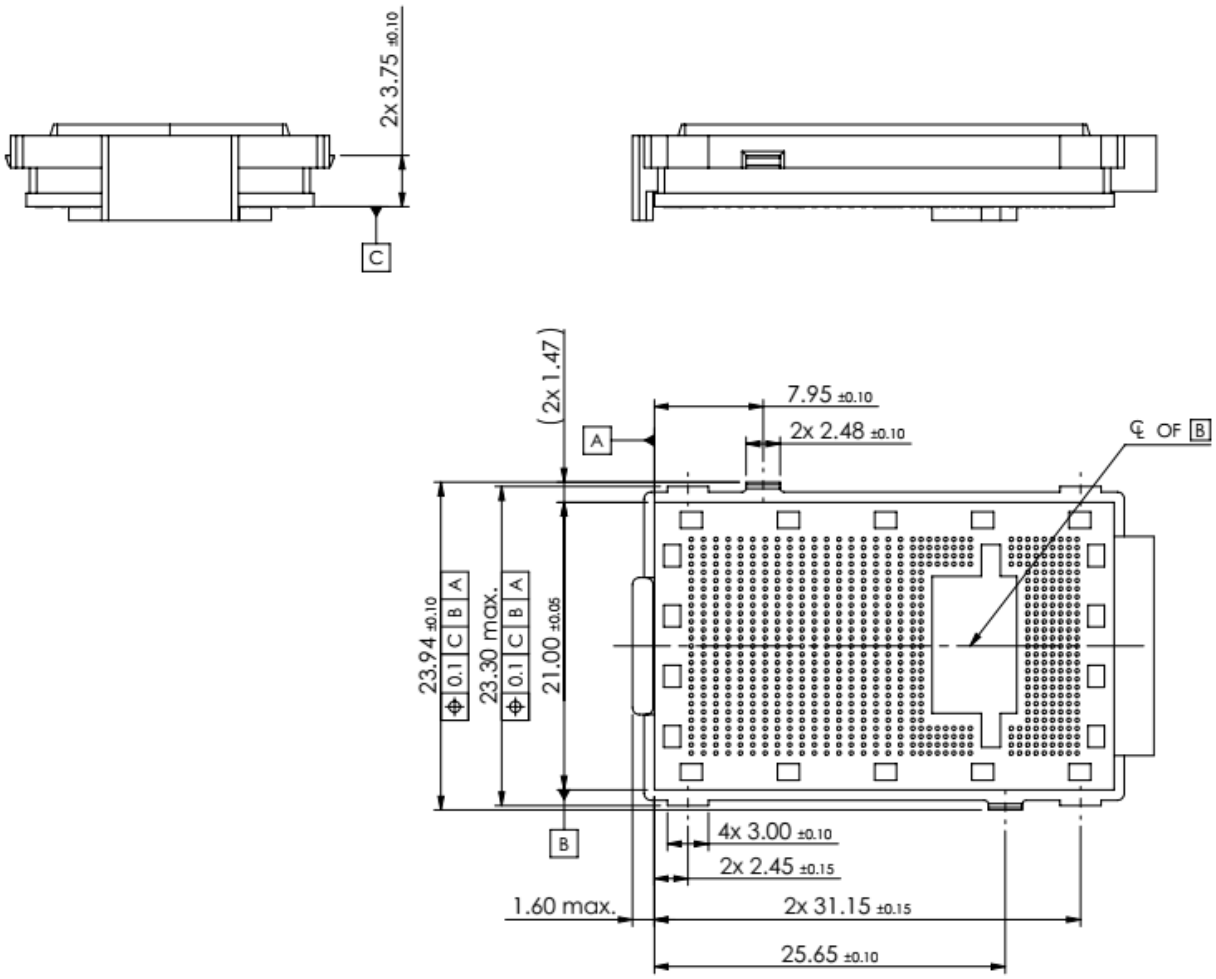

Figure 13 Optical module latch detail and tolerance

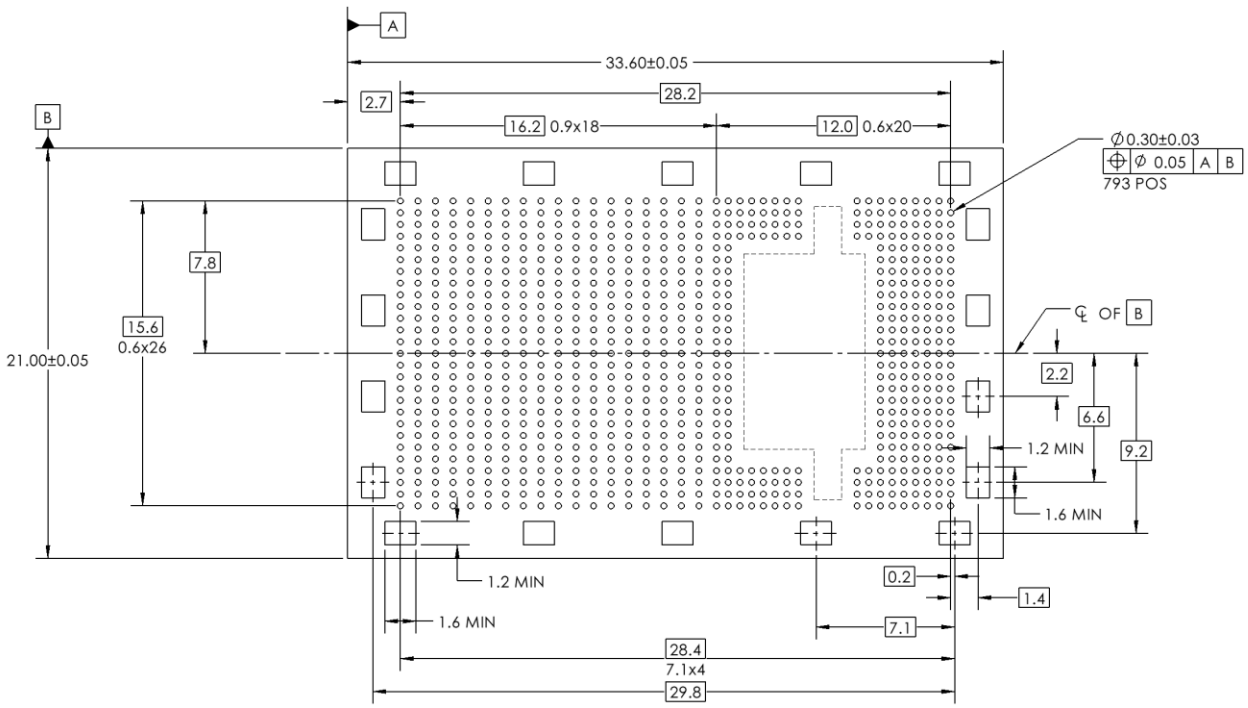

Figure 14 Module mechanical footprint (see notes below)

Notes for Figure 14: All pads in the footprint are Non Solder Mask Defined (NSMD) pads and the recommended soldermask must sit below the finished pads height. The recommended soldermask clearance is 2mils (0.05mm) for all pads. Plating of ENIG or ENEPIG is recommended.

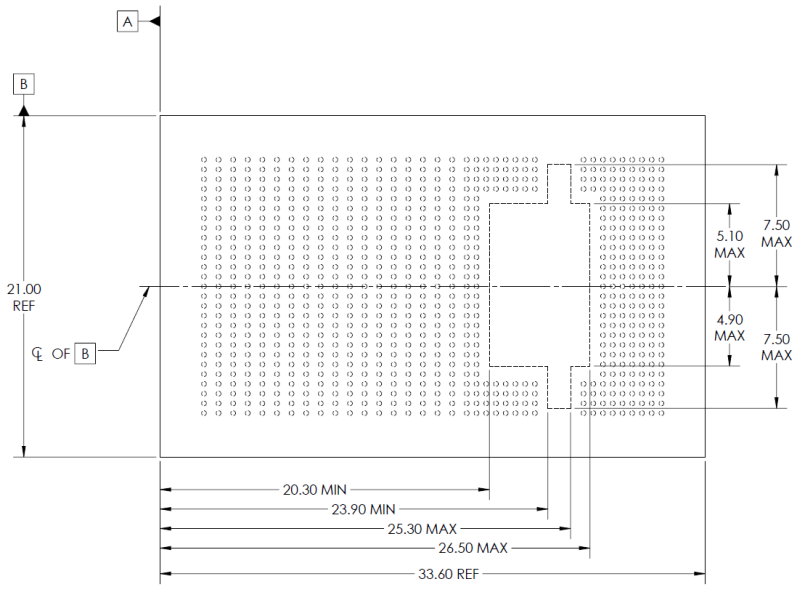

Figure 15 Pad area keep out dimensions for module

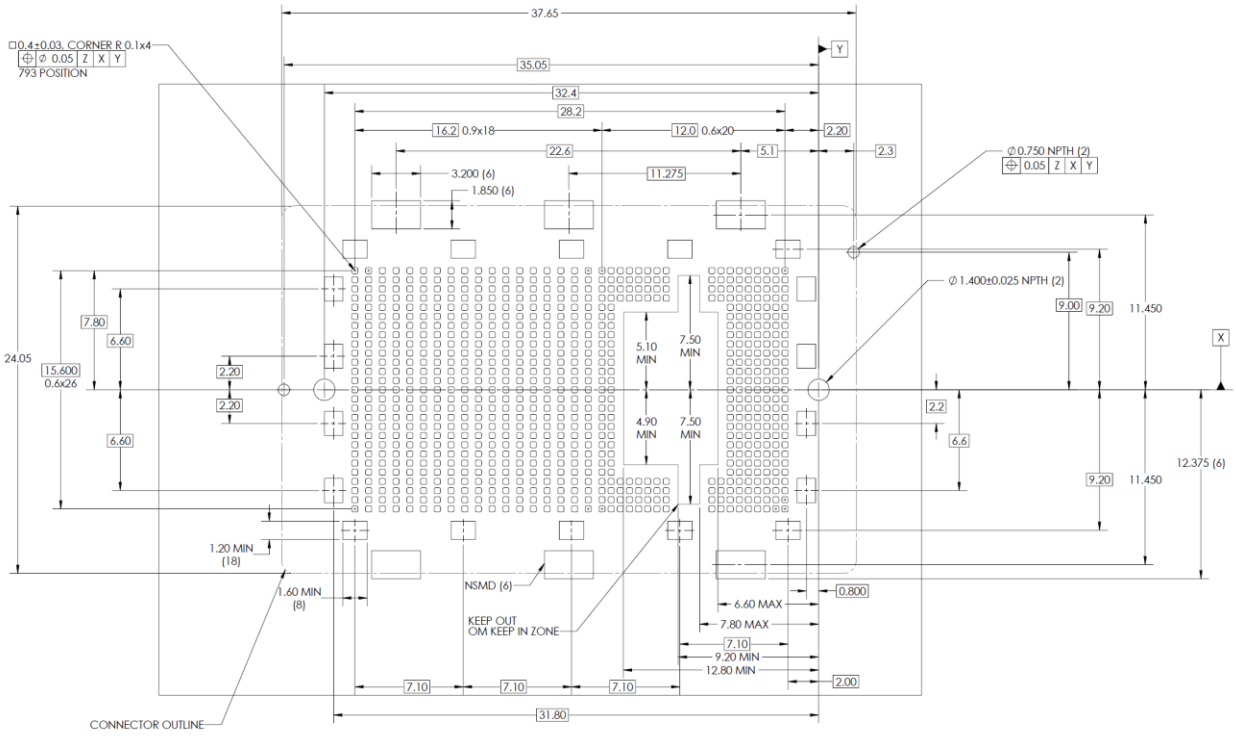

Figure 16 Substrate socket mechanical footprint (see notes below)

Notes for Figure 16: All pads in the footprint are Non-Solder Mask Defined (NSMD) pads and the recommended soldermask must sit below the finished pads height. The recommended soldermask clearance is 2mils (0.05mm) for all pads. Plating of ENIG or ENEPIG is recommended.

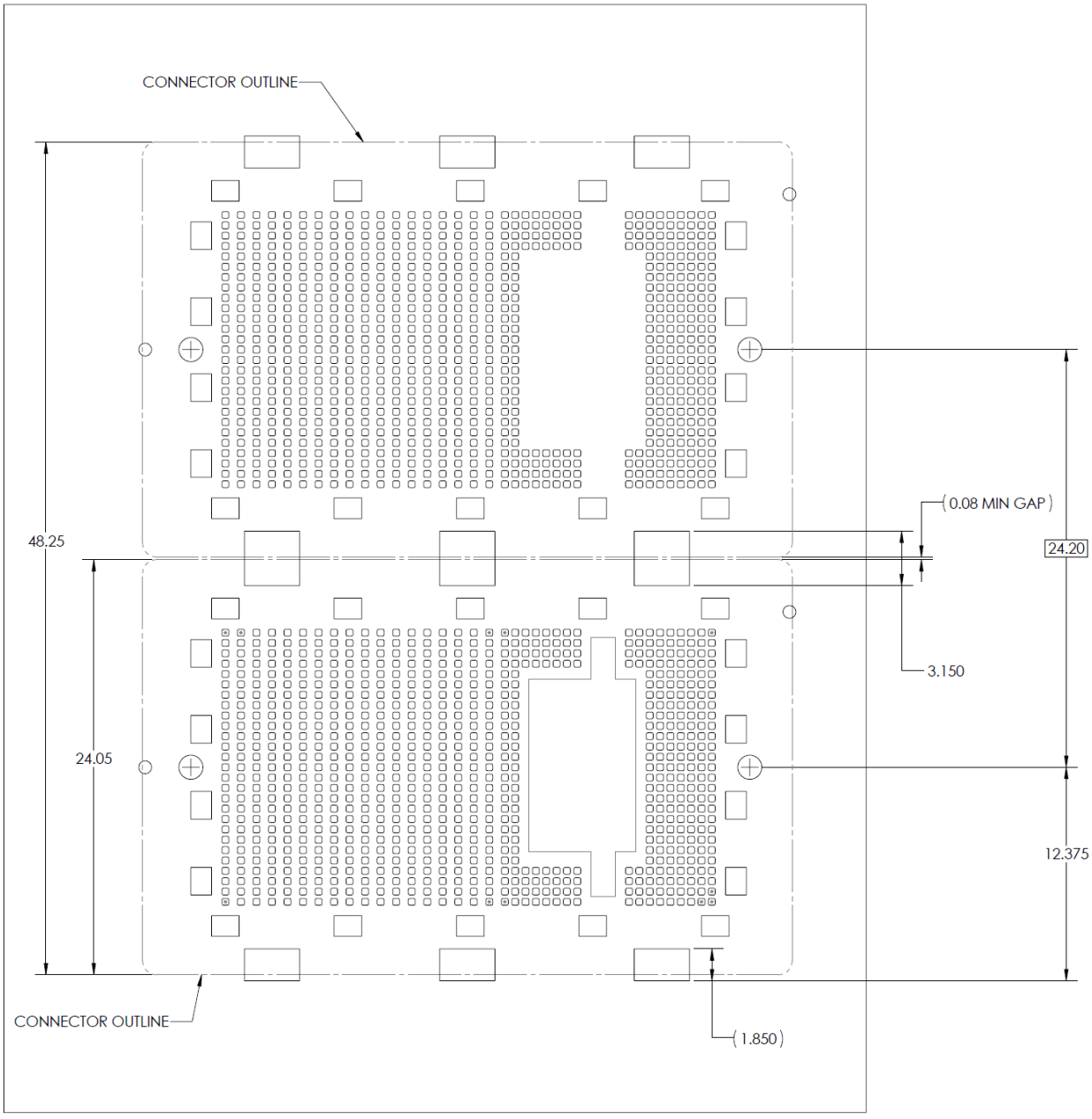

Figure 17 Abutment of Module Socket Footprints

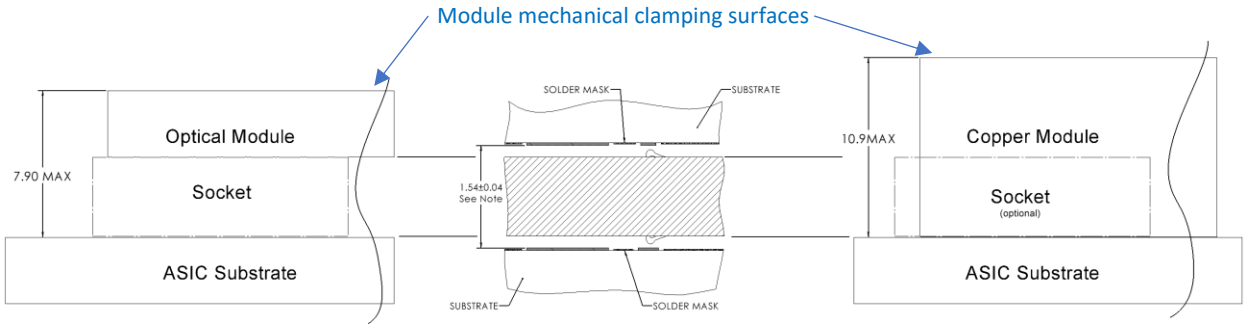

Figure 18 Socket Height and Tolerance (see notes below)

Notes for Figure 18: All pads in the footprint are Non Solder Mask Defined (NSMD) pads and the recommended soldermask must sit below the finished pads height. The recommended soldermask clearance is 2mils (0.05mm) for all pads. Plating of ENIG or ENEPIG is recommended.

The Socket Mated Seating Height (1.54mm +/- 0.04mm) is defined from the topmost (copper) surface of the ASIC Substrate to the bottommost (copper) surface of the Module Substrate in a compressed state.

6.1. Optical Connectors to External Laser Source

For optical module designs that rely on the External Laser Source (ELS), the CW light source will be coupled via four or eight polarization maintaining fibers assembled into a ribbon or fiber bundle. On the transceiver module, each CW source will be split and distributed to eight or four transmitters respectively. In the four fiber scenario, for example the laser source may have 9 dB of splitting loss and 3 dB of modulation loss, with the balance of the input power to output power allocated to excess loss due to coupling into and out of the transceiver module, and excess loss from splitters, waveguides, modulator, and mux.

6.2. Thermal Considerations

To interface with the cooling element, the optical modules will incorporate a heat spreader on the top surface. A Thermal Interface Material (TIM) will be used between the cooling element and the module's heat spreader. To maximize cooling efficiency and minimize module case temperature, the optical module's heat spreader flatness should be as uniform as possible across the CPO assembly.

For initial design guidance, the vendor should assume that all heat from the transceiver module will be removed through the heat spreader (all other surfaces, including the LGA pins, are adiabatic). The vendor can assume the switch heat sink will keep the heat spreader surface below the maximum specified case temperature shown in Table 3.

7. Management Interface, Control, and Status

7.1. Management Interface

The management interface for the optical module is the OIF Common Management Interface Specification (CMIS 5.3 or later), implemented with SPI signaling at 1.2V electrical levels at clock rates to 20MHz.

This module Implementation Agreement covers timing and voltage definitions for the communications, and the CMIS Implementation Agreement covers the protocols.

The SPI interface timing is shown in Table 12, with reference waveforms in Figure 19.

7.2. SPI Interface Timing

The SPI interface timing is shown in Table 12.

Symbol	Parameter	Condition	Min.	Max.	Unit
f_{SCK}	Clock Frequency		1	20	MHz
t_{DS}	Data set-up time		7	--	ns
t_{DH}	Data hold time		7	--	ns
$t_{V(Q)}$	Data output valid time	From clock falling edge	--	15	ns
t_{BB}	Back to back timing		5	--	us
t_{SS}	Slave select timing		50	1 UI	ns

Table 12 SPI Interface Timing

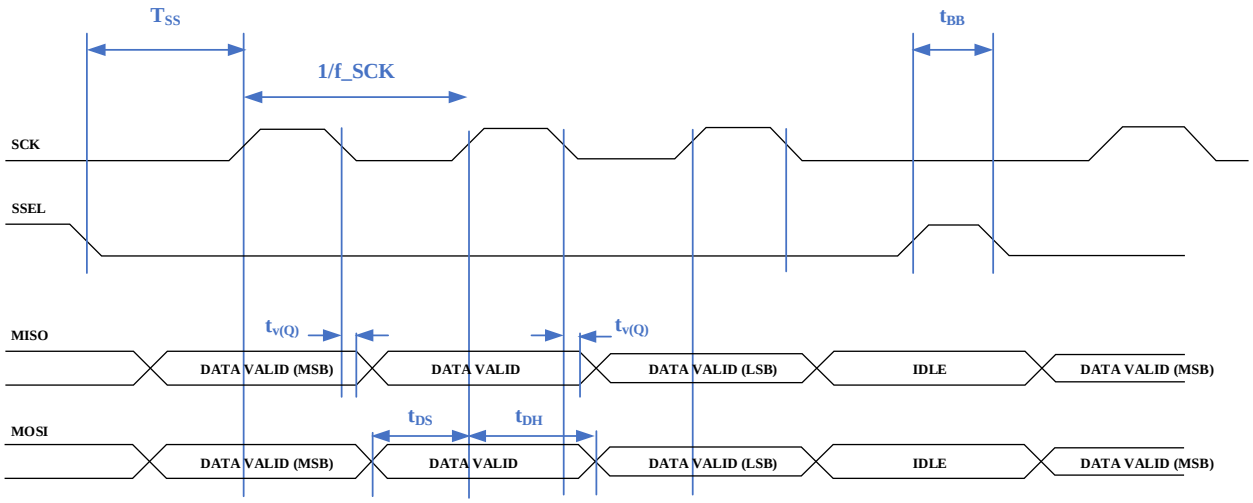

Figure 19 SPI Timing Diagram

7.3. Alarm and Warning Settings

Alarms and warnings are optional and to be set to the same level for all installed modules High/low levels are selected to be outside the specified operating range such that if triggered, action is required.

Parameter	High Alarm	Low Alarm	High Warning	Low Warning	Unit	Note
Case temperature	Tmax+10	Tmin-5	Tmax+10	Tmin-5	°C	
Voltage	Vmax+10%	Vmin-10%	Vmax+10%	Vmin-10%	V	
Tx output optical power, each lane	6.7	-7.2	6.7	-7.2	dBm	
Rx outer optical modulation amplitude, each lane	6.5	-40	6.5	-40	dBm	Note1
Tx laser bias current	Vendor specific	Vendor specific	Vendor specific	Vendor specific	mA	Note2

Note:
1. Rx LOS is used for low Rx signal strength indicator, therefore it is not expected that this low alarm/warning would trigger.
2. The alarms/warnings are to be defined by each vendor, but should follow the same principles shown above

Table 13 Alarm and Warning Settings

7.4. Timing Requirements for Control and Status

Table 14 shows timing requirements for control and status information of CPO module. It matches QSFP-DD specification with addition of following:

1. Serial bus hardware ready time
2. Monitor data ready time
3. Reset assert time
4. LPMode assert time
5. LPMode de-assert time
6. Application or rate select change time

Parameter	Symbol	Min	Typ	Max	Unit	Note
MgmtInit duration	t_init			2000	ms	
Reset init assert time	t_reset_init	10			us	
Serial bus hardware ready time	t_serial			2000	ms	Note1
Monitor data ready time	t_data			2000	ms	Note2
Reset assert time	t_reset			3000	ms	Note3
LPMode assert time	toff_LPMode			100	us	Note4
LPMode de-assert time	ton_LPMode			3000	ms	Note5
IntL assert time	ton_IntL			200	ms	

IntL de-assert time	toff_IntL			500	us	
Rx LOS assert time	ton_LOS			100	ms	
Tx fault assert time	ton_flag			200	ms	
Flag assert time	ton_flag			200	ms	
Mask assert time	ton_mask			100	ms	
Mask de-assert time	toff_mask			100	ms	
Application or rate select change time	t_ratesel			100	ms	
Module select wait time	ModSelL_WaitTime		N/A			
DataPathDeinit max duration	DataPathDeinit_MaxDuration		TBD			
DataPathInit max duration	DataPathInit_MaxDuration		TBD			
ModulePwrDn max duaration	ModulePwrDn_MaxDuration		TBD			
Rx squelch assert time	ton_Rxsq			100	ms	
Rx squelch de-assert time	toff_Rxsq			2000	ms	
Tx squelch assert time	ton_Txsq			400	ms	
Tx squelch de-assert time	toff_Txsq			2000	ms	
Tx disable assert time	ton_txdis			100	ms	
Tx disable de-asssert time	toff_txdis			400	ms	
Rx output disable assert time	ton_rxdis			100	ms	
Rx output disable de-assert time	toff_rxdis			100	ms	
Squelch disable assert time	ton_sqdis			100	ms	
Squelch disable de-assert time	toff_sqdis			100	ms	

Note:

1. Time from power on until the module responds to data transmission over the SPI bus.
2. Time from power on until DDM updates start and reflect accurate values.
3. Time from ResetL rising edge to module operational (if module has been previously configured into normal operational mode)
4. Time from LPMode rising edge to module achieves ModuleLowPwr state (maximum allowable time from CMIS)
5. Time from LPMode falling edge to module achieves ModuleReady state (maximum allowable time from CMIS)
6. Time from optical loss of signal to pin deassert.

Table 14 Timing Requirements for Control and Status

7.5. Digital Diagnostic Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Reported case temperature accuracy	Tcase_Err	-3		3	°C
Reported voltage accuracy	Vcc_Err	Vtyp-2%		Vtyp+2%	mV

Reported Tx output power accuracy	Pout_Err	-2		2	dB
Reported Rx input power accuracy	Pin_Err	-2		2	dB
Reported Tx bias current accuracy	Ibias_Err	-10		10	%

Table 15 Digital Diagnostic Specification

8. Environmental and Thermal

Parameter	Symbol	Min	Typical	Max	Unit	Note
Altitude, during operation, relative to sea level		-50		1800	m	
Altitude, storage, to sea level				5	km	
Altitude, transportation, to sea level				12	km	
Gaseous contamination						Note1
Assembly cycles		TBD				Note2
Optical assembly cycles		TBD				Note3

Note:
1. Conform to Severity Level G1 per ANSI/ISA 71.04-1985.
2. Number of cycles of mount/unmount from CPO substrate
3. Number of cycles of connect/disconnect of optical patch cables

Table 16 Environmental Regulation Requirement

1 References

1.1 Normative references

1.2 Informative references

The following documents are referenced in generating this specification:

- IEEE 802.3bs – Media Access Control Parameters, Physical Layers and Management Parameters for 200 Gb/s and 400 Gb/s Operation; this amendment to 802.3 was adopted December 2017
- IEEE 802.3cu D2.2– Media Access Control Parameters, Physical Layers and Management Parameters for 100 Gb/s and 400 Gb/s over SMF at 100 Gb/s per Wavelength.
- OIF-CEI-x.x (CEI-112G-XSR currently in draft)
- CMIS revision 5.0 – Common Management Interface Specification
- Open Compute Project: 200G-FR4 QSFP-DD OCP Optical Transceiver Specification Rev 0.2
- Open Compute Project: 400G-FR4 QSFP-DD OCP Optical Transceiver Specification Rev 0.1

2 Appendix A: Copper Cable Attach (CCA3T2) Implementation (Informative)

A CCA3T2-DAC switch implementation (as illustrated in the right image shown in Figure 1) uses low loss passive twin-ax cable in an electrical link between the CCA3T2 module and front-panel pluggable IO ports on the faceplate of the system, providing channel signal integrity improvement that enable the use of pluggable modules. For example, one CCA3T2 module could map to (4) OSFP ports as shown below in Figure 20. In this case interoperability is extended from the 3.2T Module footprint, to the front-panel. In the 51.2T attachment system example shown in Figure 3, this enables routing (16) CCA3T2 modules to (64) eight-lane IO ports (e.g. OSFP).

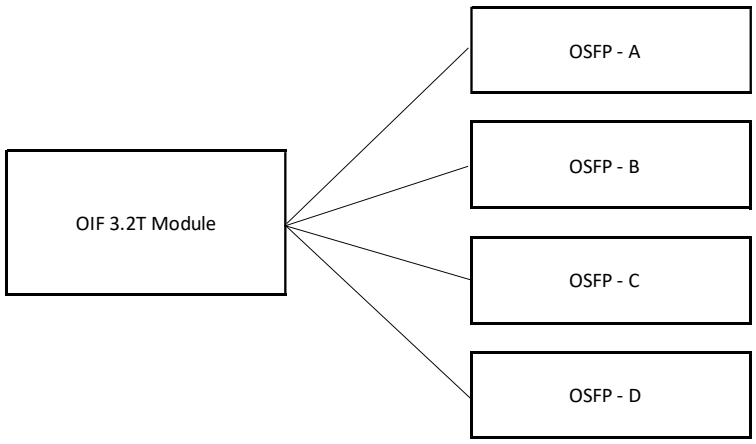

Figure 20 CCA3T2-DAC to (4) OSFP IO Ports Cable Routing Illustration

In this informative appendix a differential pair lane mapping is provided for each twin-ax cable between the 3.2T module footprint (as shown in Figure 10 and Table 8) and the (4) OSFP IO ports (per the OSFP port pin numbering). The signal definitions shown in Table 17 correspond to the 3.2T module footprint definitions shown in Figure 10.

OSFP - A				OSFP - B				OSFP - C				OSFP - D			
31	GND	GND	30	31	GND	GND	30	31	GND	GND	30	31	GND	GND	30
32	HRX_G1P	HRX_H1P	29	32	HRX_E1P	HRX_F1P	29	32	HRX_C1P	HRX_D1P	29	32	HRX_A1P	HRX_B1P	29
33	HRX_G1N	HRX_H1N	28	33	HRX_E1N	HRX_F1N	28	33	HRX_C1N	HRX_D1N	28	33	HRX_A1N	HRX_B1N	28
34	GND	GND	27	34	GND	GND	27	34	GND	GND	27	34	GND	GND	27
35	HRX_G2P	HRX_H2P	26	35	HRX_E2P	HRX_F2P	26	35	HRX_C2P	HRX_D2P	26	35	HRX_A2P	HRX_B2P	26
36	HRX_G2N	HRX_H2N	25	36	HRX_E2N	HRX_F2N	25	36	HRX_C2N	HRX_D2N	25	36	HRX_A2N	HRX_B2N	25
37	GND	GND	24	37	GND	GND	24	37	GND	GND	24	37	GND	GND	24
38	HRX_G3P	HRX_H3P	23	38	HRX_E3P	HRX_F3P	23	38	HRX_C3P	HRX_D3P	23	38	HRX_A3P	HRX_B3P	23
39	HRX_G3N	HRX_H3N	22	39	HRX_E3N	HRX_F3N	22	39	HRX_C3N	HRX_D3N	22	39	HRX_A3N	HRX_B3N	22
40	GND	GND	21	40	GND	GND	21	40	GND	GND	21	40	GND	GND	21
41	HRX_G4P	HRX_H4P	20	41	HRX_E4P	HRX_F4P	20	41	HRX_C4P	HRX_D4P	20	41	HRX_A4P	HRX_B4P	20
42	HRX_G4N	HRX_H4N	19	42	HRX_E4N	HRX_F4N	19	42	HRX_C4N	HRX_D4N	19	42	HRX_A4N	HRX_B4N	19
43	GND	GND	18	43	GND	GND	18	43	GND	GND	18	43	GND	GND	18
44			17	44			17	44			17	44			17
45			16	45			16	45			16	45			16
46			15	46			15	46			15	46			15
47			14	47			14	47			14	47			14
48	GND	GND	13	48	GND	GND	13	48	GND	GND	13	48	GND	GND	13
49	HTX_G1N	HTX_H1N	12	49	HTX_E1N	HTX_F1N	12	49	HTX_C1N	HTX_D1N	12	49	HTX_A1N	HTX_B1N	12
50	HTX_G1P	HTX_H1P	11	50	HTX_E1P	HTX_F1P	11	50	HTX_C1P	HTX_D1P	11	50	HTX_A1P	HTX_B1P	11
51	GND	GND	10	51	GND	GND	10	51	GND	GND	10	51	GND	GND	10
52	HTX_G2N	HTX_H2N	9	52	HTX_E2N	HTX_F2N	9	52	HTX_C2N	HTX_D2N	9	52	HTX_A2N	HTX_B2N	9
53	HTX_G2P	HTX_H2P	8	53	HTX_E2P	HTX_F2P	8	53	HTX_C2P	HTX_D2P	8	53	HTX_A2P	HTX_B2P	8
54	GND	GND	7	54	GND	GND	7	54	GND	GND	7	54	GND	GND	7
55	HTX_G3N	HTX_H3N	6	55	HTX_E3N	HTX_F3N	6	55	HTX_C3N	HTX_D3N	6	55	HTX_A3N	HTX_B3N	6
56	HTX_G3P	HTX_H3P	5	56	HTX_E3P	HTX_F3P	5	56	HTX_C3P	HTX_D3P	5	56	HTX_A3P	HTX_B3P	5
57	GND	GND	4	57	GND	GND	4	57	GND	GND	4	57	GND	GND	4
58	HTX_G4N	HTX_H4N	3	58	HTX_E4N	HTX_F4N	3	58	HTX_C4N	HTX_D4N	3	58	HTX_A4N	HTX_B4N	3
59	HTX_G4P	HTX_H4P	2	59	HTX_E4P	HTX_F4P	2	59	HTX_C4P	HTX_D4P	2	59	HTX_A4P	HTX_B4P	2
60	GND	GND	1	60	GND	GND	1	60	GND	GND	1	60	GND	GND	1

Table 17 Electrical Lane Mapping from the CCA3T2-DAC to (4) OSFP IO Ports

3 Appendix B: Glossary

The following terms are used in this document:

- 200GE – 200 Gigabit Ethernet
- 400GE – 400 Gigabit Ethernet
- 400GBASE-FR4 – 400GE optical standard utilizing 4 wavelengths on a 1310nm CWDM grid with each wavelength transmitting 106.25Gb/s using 53.13Gbaud PAM4 modulation
- 200GBASE-FR4 - 200GE optical standard utilizing 4 wavelengths on a 1310nm CWDM grid with each wavelength transmitting 53.13Gb/s using 26.56GBaud PAM4 modulation
- 400GBASE-DR4 - 400GE optical standard utilizing 4 optical lanes operating at 1310nm, with each lane transmitting 106.25Gb/s using 53.13Gbaud PAM4 modulation
- BER – Bit Error Rate
- CEI-112G-XSR/+ – Common Electrical Interface specification operating at a serial data rate of 112Gb/s over short reaches common in multi-chip modules
- CCA – Copper Cable Attach
- CMIS – Common Management Interface Specification
- CPO – Co-Packaged Optics
- DEMUX – De-multiplexer
- DSP – Digital Signal Processor

- EBO – Extended Beam Optical Connector
- ELS – External Laser Source
- ER – Extinction Ratio
- ESD – Electro-Static Discharge
- ILS – Integrated Light Source
- LD – Laser Diode used as a CW source for the co-packaged optical module
- MUX – Multiplexer
- NRZ – Non-Return-to-Zero
- OMA – Optical Modulation Amplitude
- PAM – Pulse Amplitude Modulation
- PAVG – Power Average (Optical)
- POMA – Power Optical Modulation Amplitude
- PMF – Polarization Maintaining Fiber
- QSFP56 – Quad Small Form-factor Pluggable (QSFP) operating at 4×56Gbps, used for 200GE
- QSFP-DD – Quad Small Form-factor Pluggable Double Density operating at 8×56Gbps, used for 400GE
- SECQ – Stressed Eye Closure Quaternary
- SiPho – Silicon Photonics
- SMSR – Side Mode Suppression Ratio
- SPI – Serial Peripheral Interface
- TDECQ – Transmitter and Dispersion Eye Closure Quaternary
- TIA – Trans-impedance Amplifier

4 Appendix B: Open Issues / current work items

5 Appendix C: List of companies belonging to OIF when document approved

Accton Technology Corporation	Lessengers Inc.
ADTRAN	Linktel Technologies Co., Ltd.
Advanced Fiber Resources (AFR)	Lumentum
Advanced Micro Devices, Inc.	Luxshare-ICT
AIO Core Co., Ltd	MACOM Technology Solutions
Alibaba	Marvell Semiconductor, Inc.
Alphawave Semi	Maxim Integrated Inc.
Amphenol Corp.	MaxLinear Inc.
Arista Networks	MediaTek
Astera Labs	Meta Platforms
Ayar Labs	Microchip Technology Incorporated
BitifEye Digital Test Solutions GmbH	Microsoft Corporation
BizLink Technology, Inc.	Mitsubishi Electric Corporation
Broadcom Inc.	Molex
Cadence Design Systems	Multilane Inc.
Casela Technologies USA	NEC Corporation
Celestica	Nokia
China Information Communication Technologies Group	NTT Corporation
China Telecom	Nubis Communications, Inc.
Ciena Corporation	NVIDIA Corporation
Cisco Systems	O-Net Communications (Shenzhen) Limited
Coherent	Open Silicon Inc.
ColorChip LTD	Optomind Inc.
Commscope Connectivity Belgium BVBA	Orange
Cornelis Networks, Inc.	PETRA
Corning	Precision Optical Transceivers, Inc.
Credo Semiconductor (HK) LTD	Quantifi Photonics USA Inc.
Dell, Inc.	Quintessent Inc.
DustPhotonics	Ragile Networks, Inc.
EFFECT Photonics B.V.	Rambus Inc.
Eoptolink Technology	Ranovus
Epson Electronics America, Inc.	Retym
Ericsson	Rosenberger Hochfrequenztechnik GmbH & Co. KG
EXFO	Samsung Electronics Co. Ltd.

Foxconn Interconnect Technology Ltd	Samtec Inc.
Fujikura	SCINTIL Photonics
Fujitsu	Semtech Canada Corporation
Furukawa Electric Co., Ltd.	Senko Advanced Components
Global Foundries	SeriaLink Systems Ltd.
Google	Sicoya GmbH
Hakusan Inc	Socionext Inc.
Hewlett Packard Enterprise (HPE)	Source Photonics, Inc.
Hisense Broadband Multimedia Technologies Co., LTD	Spirent Communications
Huawei Technologies Co., Ltd.	Sumitomo Electric Industries, Ltd.
IBM Corporation	Sumitomo Osaka Cement
Idea Sistemas Electronicos S.A.	Synopsys, Inc.
Infinera	TE Connectivity
InfiniLink	Tecdia Inc.
InnoLight Technology Limited	Tektronix
Integrated Device Technology	Telefonica S.A.
Intel	TELUS Communications, Inc.
Jabil Canada Corporation	US Conec
Juniper Networks	Viavi Solutions Deutschland GmbH
Kandou Bus	Wilder Technologies, LLC
KDDI Research, Inc.	Wistron Corporation
Keysight Technologies, Inc.	Yamaichi Electronics Ltd.
Kuaishou Technology	ZTE Corporation
KYOCERA Corporation	