Implementation Agreement for 112 Gb/s Retimed Transmitter Linear Receiver (*RTLR*)

OIF-EEI-112G-RTLR-01.0

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Draft Implementation Agreement

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Implementation Agreement for 112 Gb/s Retimed Transmitter Linear Receiver (RTLR)

Revision 01.0

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Abstract:

OIF EEI-112G-RTLR (*TRO*) offers both energy efficiency and support for the full Ethernet C2M 100 Gb/s or OIF CEI-112G-VSR-PAM4 16 dB (ball-ball) channel. OIF EEI-112G-RTLR (*TRO*) specifies a 112 Gb/s chip-to-module PAM4 electrical interface for use with a retimed optical transmitter and linear optical receiver for operation within the range from 36 to 56 GSym/s and for channel loss up to 16 dB loss at the Nyquist frequency including one connector. OIF EEI-112G-RTLR (*TRO*) specification is identical to OIF CEI-VSR-112G-PAM4 specifications for the egress (host to module) path. For the egress (host to module) path, where transmitter retiming provides a fully compliant optical output. On the ingress (module to host) path OIF EEI-112G-RTLR (*TRO*) avoids the need for a DSP/re-timer in the module and uses an enhanced version of OIF CEI-112G-LINEAR-PAM4 specifications by utilizing host ASIC DSP SerDes capability.

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Document Revision History

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Table 1: RTLR IA document revision history

Document	Date	Revision	Revisions/Comments
OIF 2024.281.00	June 16, 2024	0.1	Initial OIF EEI-112G-RTLR draft.
OIF 2024.281.01	July 17, 2024	0.2	2nd draft of OIF EEI-112G-RTLR.
OIF 2024.281.02	July 29, 2024	0.3	3rd draft incorporating minor editorial comments.
OIF 2024.281.03	August 13, 2024	0.4	4th draft incorporating minor editorial comments.
OIF 2024.281.04	October 14, 2024	0.5	5th draft incorporating EEI review informal comments.
OIF 2024.281.05	February 12, 2025	0.6	6th draft incorporating comments from the 1st straw ballot.
OIF 2024.281.06	May 20, 2025	0.7	7th draft incorporating comments from the 2nd straw ballot.
OIF 2024.281.07	August 13, 2025	0.8	8th draft incorporating comments from the 3rd straw ballot.
OIF 2024.281.07	October 1, 2025	01.0	Straw/principal ballots closed with no comments, draft forwarded for publication.

1 Introduction

1.1 Scope

This Implementation Agreement details the requirements for the OIF EEI-112G-RTLR (*TRO*) high-speed chip-to-module electrical interface with nominal baud rates within the range from 36 GSym/s to 56 GSym/s. A compliant host or module shall meet all of the relevant requirements listed below. The host-module "egress" electrical interface assumes a retimer and equalizer in the module and is identical to IEEE Std 802.3 Annex 120G [4] interfaces or can operate with the OIF CEI-112G-VSR-PAM4 [1] with the exception that the host PCB budget is limited to 11.9 dB. The module-host "ingress" electrical interface is based on differential high-speed analog electro-optical signaling similar to the OIF CEI-112G-LINEAR-PAM4 [2].

This implementation agreement combines Retimed Transmitter (RT) optics with Linear Receiver (LR) optics, both compliant to IEEE Std 802.3 (see 1.3 RTLR Compatible PMDs). The implementation agreement defines electro-optical characteristics to connect Linear Receiver (LR) PMD electrical signal from the module through the host connector and host channel.

The EEI-112G-RTLR is organized in five sections and two appendices. Section 2 contains general requirements including error ratios, and Section 3 contains electrical and optical specifications and recommendations for both transmit (egress) and receive (ingress) paths, with tables for module output and host input and definitions of electrical parameters. Section 4 addresses module output and host input testing. Section 5 provides references; Appendix A 6 is a glossary and Appendix B 7 is a list of OIF member companies.

1.2 Requirements

The objectives and requirements for the EEI-112G-RTLR (*TRO*) implementation agreement are as follows:

- Supports the Ethernet (53.125 GSym/s) baud rate (fb) with PAM4 signaling. This specification can be extended to support baud rates within the range from 36 Gsym/s to 56 Gsym/s with PAM4 signaling. The EEI-112G-RTLR (*TRO*) implementation complies with the specifications of this clause over the range of baud rates stated for the implementation within this range.
- Capable of driving up to a minimum of 200 mm of host PCB trace plus one connector and a minimum of 20 mm of module PCB trace. The use of cables to replace or partially replace the copper signal traces on the printed circuit board is acceptable and may extend the physical length of the channel.
- Capable of achieving an end to end (FEC transmit-FEC receive) raw Bit Error Ratio (BER) of 2.8×10^{-4} or better from FEC transmit to FEC receive, and for Ethernet, must meet Frame Loss Ratio (FLR) requirements in 2.3.1. FEC is assumed to be used to achieve a corrected BER of 10^{-13}. The baud rate includes the overhead required for FEC. The definition of FEC is outside the scope of this IA (see CEI Appendix 16.D).
- Egress path is compliant to OIF CEI-112G-VSR-PAM4 [1] or IEEE Std 802.3 Annex 120G [4].
- Capable of supporting optical PMD specifications at TP2 and TP3 compliant to one of the following: IEEE Std 802.3 100G PAM4 SMF, MMF PMD specifications [5], [6], [7], or [8].
- Shall support AC-coupled operation.

- Shall allow multi-lanes (1 to n).
- Shall support hot plug.

1.3 RTLR Compatible PMDs

RTLR specification support 802.3 multi-mode (MMF) PMDs, see 1.3.1, and single-mode (SMF) PMDs, see 1.3.2, that do not use precoding. RTLR is applicable to other PAM4 optical PMD specifications which may include precoding.

1.3.1 RTLR Supported MMF PMDs

The EEI-112G-RTLR supports the following MMF Ethernet PMDs:

- 100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, and 800GBASE-VR8 [8]
- 100GBASE-SR1, 200GBASE-SR2, 400GBASE-SR4, and 800GBASE-SR8 [8].

1.3.2 RTLR Supported SMF PMDs

The EEI-112G-RTLR supports the following SMF Ethernet PMDs:

- 400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2 [5]
- 100GBASE-DR and 100GBASE-FR1 [6]
- 400GBASE-FR4 [7].

1.4 RTLR Host Interface IDs

RTLR host electrical IDs are listed below:

- EEI-100G-RTLR-1-S (100 GbE 1-lane short mode)
- EEI-100G-RTLR-1-L (100 GbE 1-lane long mode)
- EEI-200G-RTLR-2-S (200 GbE 2-lanes short mode)
- EEI-200G-RTLR-2-L (200 GbE 2-lanes long mode)
- EEI-400G-RTLR-4-S (400 GbE 4-lanes short mode)
- EEI-400G-RTLR-4-L (400 GbE 4-lanes long mode)
- EEI-800G-RTLR-8-S (800 GbE 8-lanes short mode)
- EEI-800G-RTLR-8-L (800 GbE 8-lanes long mode)

RTLR host electrical interface IDs are specified by SFF-8024 Table 4-5, see [13].

2 General Requirements

2.1 Patterns

Patterns referenced in this IA are defined in OIF CEI 5.2 [14] Appendix 16.C.

2.2 Host Transmit Function (Egress)

Host transmit equalization function requirements are specified in OIF CEI-112G-VSR-PAM4 [1] or IEEE Std 802.3 Annex 120G [4].

2.2.1 Bit Error Ratio

In the egress direction the bit error rate requirements are identical to those of IEEE Std 802.3 Annex 120G [4] and operates with OIF CEI-112G-VSR-PAM4 [1].

2.3 Host Receive Function (Ingress)

Host receive equalization function requirements are specified in this IA.

2.3.1 Bit Error Rate and Frame Loss Ratio

In the ingress direction, a compliant module, when receiving a compliant optical input, delivers a compliant electrical output signal to the host. A compliant host, when receiving a compliant electrical signal from a compliant module, delivers the specified raw BER to the FEC decoder in its PCS, which makes corrections to achieve the specified frame loss ratio (FLR) for 64-octet frames with minimum interpacket gap, allowing for a transmitting host with two AUIs at maximum error ratio. For single-lane 100GBASE-R PHY types in IEEE Std 802.3, the specified FLR is 6.2×10^{-10}, and for multilane 100G/lane PMDs, it is 6.2×10^{-11}. The impairments of both the optical and electrical interfaces cause errors at the host receiver. The raw BER requirement in the ingress direction from TP2 to host SerDes receive is better than or equal to 2.5×10^{-4} for the Ethernet PMDs in section 1.3 provided the error statistics are sufficiently random[1]. For modules that have multiple lanes that share a FEC decoder this BER is the average of the BER of the lanes that share the decoder. To achieve the specified FLR, the codeword error ratio in the host PCS must be less than 1.7×10^{-12} for a single lane or 5.5×10^{-12} for multiple lanes, for a signal with no errors from any AUIs in the transmitting host, such as a test signal, but including any errors from any C2C AUI in the receiving host. This may be achieved by keeping the proportion of

[1] Additional BER allocations for AUIs in each host, each of 10^{-5}, allow for a chip to module AUI in the host in the Egress direction (see 2.2.1) and a chip-to-chip (C2C) AUI in each of Egress and Ingress. The total raw BER is less than or equal to the $2.8\text{x}10^{-4}$ requirement set in 1.2.

codewords with exactly 16 errors below 1.6×10^{-12} or 5×10^{-12} respectively. Extrapolation of the logarithm of the FEC histogram can be used with care to estimate this.

2.3.2 Ground Differences

The maximum ground difference between the host and module shall be in the range of ±50 mV. The common mode voltage limits are set taking this difference into account.

3 Electrical and Optical Specifications

RTLR modules are specified to interoperate with fully retimed modules as well as other RTLR modules.

3.1 RTLR Transmit and Receive Paths

Figure 1 illustrates 4 lanes RTLR transmit and receive functions with normative specifications at TP1, TP2, TP3, and TP4. Specifications at TP1 are identical to OIF CEI-112G-VSR-PAM4 [1] or IEEE Std Annex 120G [4]. TP2 and TP3 in this specification are identical to TP2 and TP3 in IEEE Std 802.3 100G PAM4 SMF or MMF PMD specifications of [5], [6], [7], or [8]. For SIGNAL_DETECT definition and SIGNAL_DETECT levels see relevant IEEE Std 802.3 PMD clauses. SIGNAL_DETECT “False” indicates insufficient optical signal. Any of the IEEE Std 802.3 SMF and MMF PMDs TP3 signals received by the EEI-112G-RTLR produce an analog signal at TP4. The analog electrical specifications at TP4 shall be met with any optical input that is compliant to the relevant optical specifications at TP3 including the specifications for stressed input sensitivity, input sensitivity, maximum OMA and maximum average power. These specifications are normative at the test points shown in Figure 1. Modules compliant to EEI-112G-RTLR from different manufacturers shall be interoperable. An RTLR module is compliant to one of the listed IEEE PMDs, see 1.3, or to another specification. RTLR modules, see Figure 2, are interoperable at the optical interface with retimed or linear implementations that meet the same TP2 and TP3 specifications, as defined in section 1.3. Links with different optical specifications and symbol rates can follow RTLR methodology from TP3 to TP4.

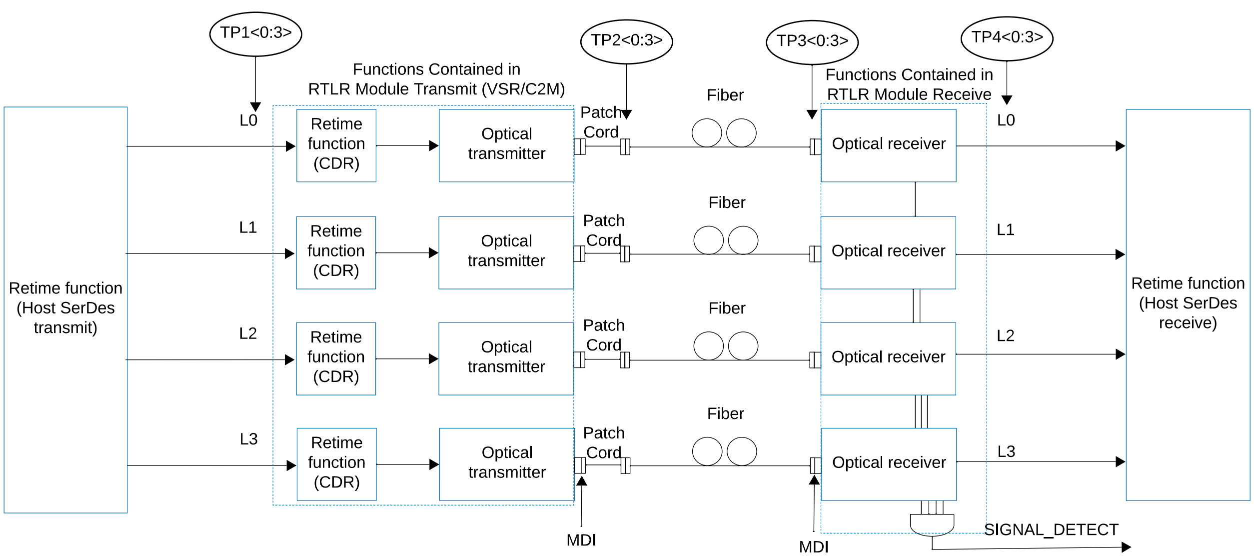

Figure 1: Block diagram illustration for 4-lane parallel RTLR transmit and receive paths

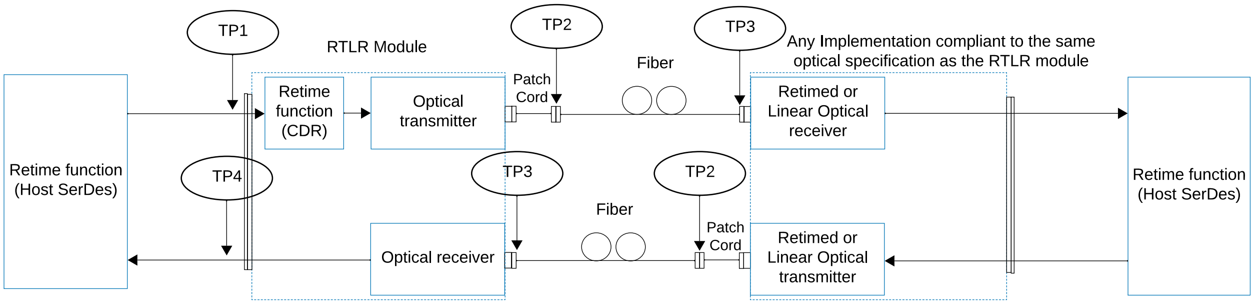

Figure 2: RTLR interoperable links shown for duplex 1-lane implementation

3.2 Compliance Point and Compliance Boards

The compliance points are described in Section 25.3.1 of the OIF CEI-112G-VSR-PAM4 [1] specification, and section 3.1, which provides an overview of link functionality and compliance test points.

The use of compliance boards for testing is assumed for the parameters defined in Table 2, Table 3, and Table 4. The compliance boards and measurement points are as specified in OIF CEI Section 25.4 [1].

3.3 RTLR Electrical Channel Characteristics

Electrical specifications at TP1a are provided in OIF CEI-112G-VSR-PAM4 [1] or IEEE Std 802.3 C2M [4], optical specifications at TP2 and TP3 can be provided by one of the following IEEE Std 802.3 [5], [6], [7], or [8]. The EEI-112G-RTLR reference loss budget is shown in Figure 3. It is identical to the loss budget in IEEE Std 802.3 C2M [4] and the total loss budget is the same as in OIF CEI-112G-VSR-PAM4 [1]. The RTLR ball-ball insertion loss is recommended to be less than 16 dB with 11.9 dB allocated to the host PCB/cable losses.

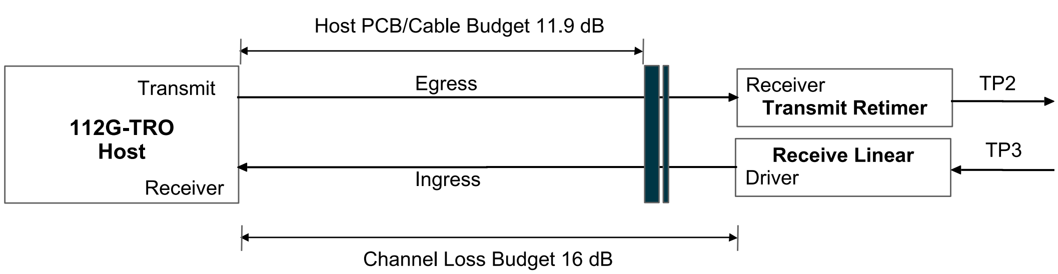

Figure 3: EEI-112G-RTLR insertion loss budget

3.4 Egress Electrical Characteristics

In the egress direction RTLR shall meet the specifications in the IEEE Std 802.3 C2M [4] or the OIF VSR [1], with the exception that the OIF VSR Host PCB loss is limited to 11.9 dB.

3.5 Ingress Module-to-Host Electrical Specifications

Hosts and modules shall meet the specifications defined in Table 2 and Table 3. Definitions and methodologies can be found in sections 3.6 and 4. A module shall meet specifications of Table 2 for all TP3 optical signals that are compliant to the relevant standard [5], [6], [7], [8]; see 1.3. It shall meet specifications at overload, stressed sensitivity level, and sensitivity at minimum TECQ. For all module output measurement unless otherwise specified use fourth-order Bessel-Thomson low-pass response with 42 GHz 3 dB bandwidth.

AC coupling is required in the module (see 3.5.2).

3.5.1 Module output modes

The RTLR module output shall support two modes: both Short and Long. For each output mode, the module shall meet the EECQ requirements of Table 2 for both near-end and far-end measurements, see Table 5.

The host selects which output mode the module is to use using the module's management interface. This is the same mechanism as the Ethernet C2M 100 Gb/s hosts use that is described in Annex 120G.3.2.1 [4].

3.5.2 Module output AC coupling requirements

The module outputs shall have AC-coupling within the module with the low frequency 3 dB cutoff of less than or equal to 100 kHz. For all module output measurement unless otherwise specified use fourth-order Bessel-Thomson low-pass response with 42 GHz 3 dB bandwidth.

Table 2: Module-to-host TP4 electrical specifications (module output)

Parameter	Min.	Max.	Unit	Conditions
Differential output voltage, pk-pk Short mode Long mode	 - -	 500 720	 mV mV	Host may request short or long modes, see 3.5.1
VMA Short mode Long mode	 200 350	 - -	 mV mV	See section 3.6.1 and 3.5.1
Common Mode Voltage (Vcm) tolerance	-350	2,850	mV	See Note 1
Peak to Peak AC Common Mode Voltage Low-frequency (Vcm_{LF})	-	32	mV	See 3.6.2
Peak to Peak AC Common Mode Voltage Full-band (Vcm_{FB})	-	80	mV	See 3.6.2
Differential Termination Resistance Mismatch	-	10	%	At 1 MHz, See OIF CEI 13.3.6
Common Mode to Differential Mode Conversion (SDC22)	-	See Equation 2	dB	See Note 2
Effective Return Loss (ERL)	10	-	dB	See Note 3
Common Mode Return Loss (SCC22)	-	-2 $-1.6 - 0.1*f$ $-8.5 + 0.13*f$	dB	$0.25 \le f < 4$ GHz $4 \le f < 30$ GHz $30 \le f \le \min(0.8*fb, 42\text{ GHz})$, See Note 2
EECQ (Short and Long Modes) MMF PMDs	-	9	dB	See Section 1.3.1, 4.1, 4.2, see also Note 4
EECQ (Short and Long Modes) SMF PMDs	-	8	dB	See Section 1.3.2, 4.1 and 4.2, see also Note 4

NOTES:
1. Vcm is generated by the host. Specification includes effects of ground offset voltage.
2. S-parameter specifications are based on a differential reference impedance of 100 Ω and a common mode reference impedance of 25 Ω.
3. See Section 3.6.4.
4. Reference equalizer for Short and Long Modes near-end eye measurement is 22 tap FFE and 1 tap DFE. Reference equalizer for Short and Long Modes far-end eye measurement is Continuous Time Linear Equalizer (CTLE), 22 tap FFE and 1 tap DFE, see 4.4.

Table 3: Module-to-host electrical specifications (host input)

Parameter	Test Point	Min	Max.	Unit	Conditions
Overload Differential Voltage pk-pk Short Mode Long Mode	TP4	 530 720	 - -	mV	See Section 4.5
Differential Termination Resistance Mismatch	TP4a	-	10	%	At 1 MHz, See CEI 13.3.6
Effective Return Loss (ERL)	TP4a	8.5	-	dB	See 3.6.4
Differential Mode to Common Mode Conversion (SCD11)	TP4a	See Equation 1		dB	
EECQ Stressed Input Test	TP4	-	9	dB	See 4.3.1 and note 1
DC Common Mode Voltage	TP4a	-300	2,800	mV	See note 1 and 2
NOTES: 1. Reference equalizer for EECQ stressed input calibration is 22 tap FFE and 1 tap DFE 2. Vcm is defined in Table 1-2 General Definitions of OIF CEI Section 1.6 3. Referred to host ground. Common mode voltage is generated by host					

Table 4: Crosstalk parameters for module output test and host stressed input test

Parameter calibrated at TP1a	Test Point	Unit	Conditions
Crosstalk Amplitude differential voltage pk-pk	860	mV	
Crosstalk Slew Time (between -270 mV and +270 mV)	15	ps	See Note 1
NOTES: 1. See OIF CEI 16.C.4.1 Transition Time and Slew Time except using a Bessel-Thomson filter bandwidth of 42 GHz.			

3.6 Parameter Definitions

3.6.1 Voltage Modulation Amplitude (VMA)

VMA is the difference between the average voltage V3, measured over the central 2 UI of a run of 7 threes, and the average voltage V0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 4. The waveform is observed through the appropriate compliance board and a fourth-order Bessel-Thomson response with a 3 dB bandwidth of 42 GHz, see Figure 8. The SSPRQ test pattern (specified in IEEE Std 802.3 subclause 120.5.11.2.3 [12]) is transmitted repetitively by the lane under test and the oscilloscope is set up to capture the complete pattern.

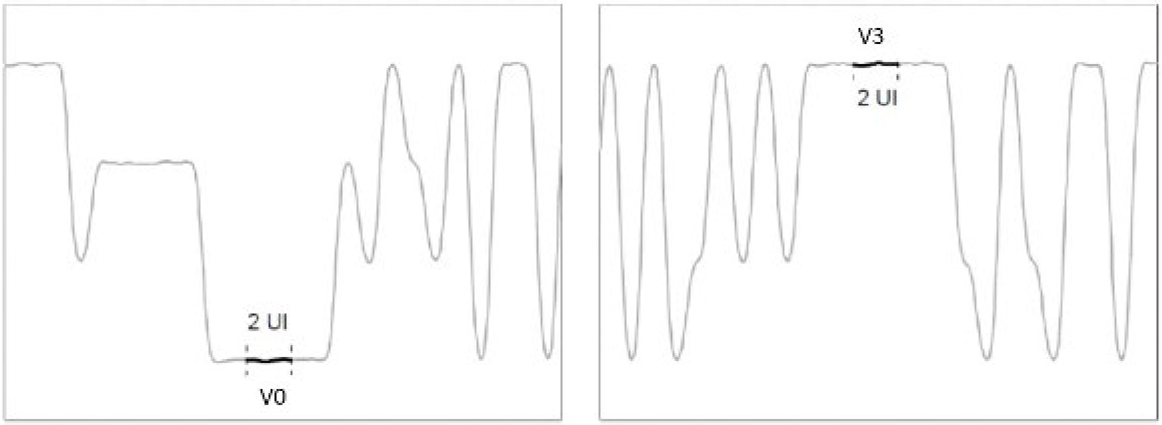

Figure 4: Measurement of VMA levels for EECQ

3.6.2 Common Mode Noise

See IEEE Std 802.3 CL 120G.5.1 [4].

3.6.3 Differential Termination Resistance Mismatch

See OIF CEI Section 13.3.6 [3].

3.6.4 Effective Return Loss

ERL at TP4 and TP4a are defined by OIF CEI Section 25.3.7 [1] with the exception that DER0 is 10^{-4} and equalizer Nbx is 18.

3.6.5 Common to differential mode and differential to common mode conversion

The differential mode to common mode conversion SCD11 and the common mode to differential mode conversion SDC22 specifications are intended to limit the amount of unwanted signal energy that is allowed to be generated due to conversion of common mode voltage to differential mode voltage or vice versa. When measured at the respective input or output test point, common mode to differential mode or differential mode to common mode conversion shall not exceed the limits given in Equation 1 and Equation 2 (illustrated in Figure 5 for f_b=53.125 GSym/s). The common mode to differential mode conversion specification for the module output is more stringent than for the host input to take into account the lack of a common mode input return loss specification. Figure 5 shows the limits of SCD11 for host input (TP4a) and SDC22 for module output (TP4) (for f_b=53.125 GSym/s).

$$SCD11 < -22 + 16 \times \left(\frac{f}{f_b}\right) \text{ dB} \qquad \text{for } 0.05 \le f \le \frac{f_b}{2}$$

$$SCD11 < -19 + 10 \times \left(\frac{f}{f_b}\right) \text{ dB} \qquad \text{for } \frac{f_b}{2} \le f < \left(0.8 \times \frac{f}{f_b}\right) \text{ GHz} \qquad \textbf{Equation 1}$$

$$SDC22 < -25 + 22 \times \left(\frac{f}{f_b}\right) \text{ dB} \qquad \text{for } 0.05 \le f \le \frac{f_b}{2}$$

$$SDC22 < -19 + 10 \times \left(\frac{f}{f_b}\right) \text{ dB} \qquad \text{for } \frac{f_b}{2} \le f < \left(0.8 \times \frac{f}{f_b}\right) \text{ GHz} \qquad \textbf{Equation 2}$$

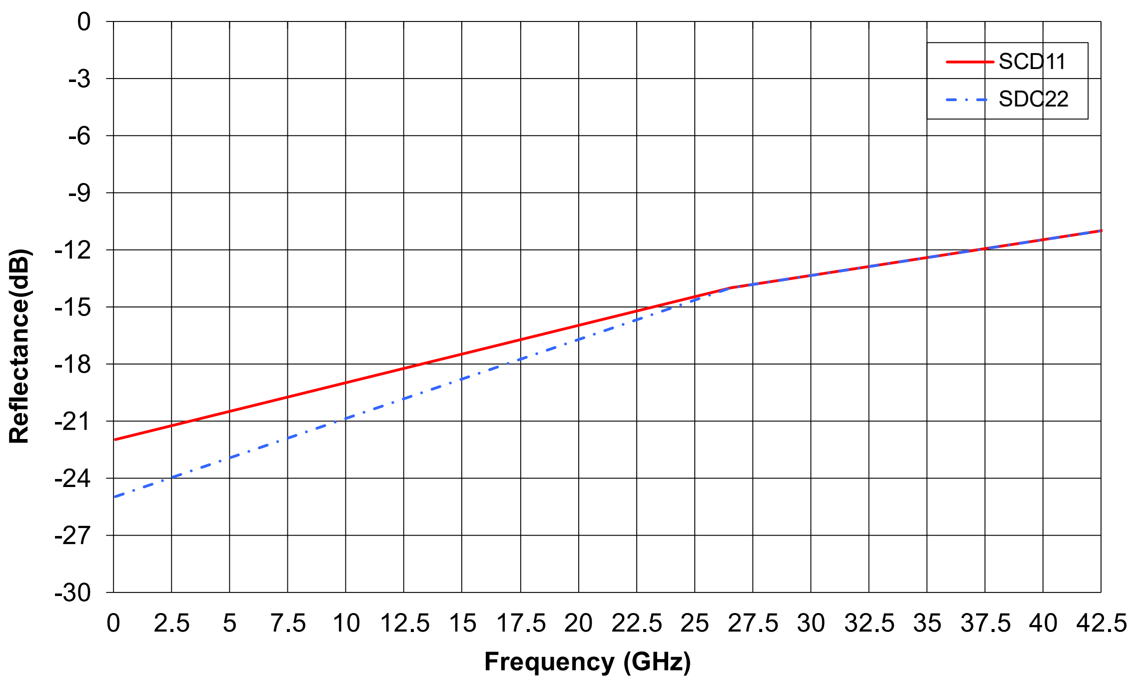

Figure 5: SCD11 for host input (TP4a) and SDC22 for module output (TP4) (for f_b=53.125 GSym/s)

3.6.6 Common Mode Output Return Loss

The common mode output return loss specification is intended to limit the amount of common mode energy that can be reflected by the host output. This has an effect on EMI radiation and differential mode signals generated via common mode to differential mode conversion.

3.6.7 Electrical Eye Closure PAM4 (EECQ)

EECQ is a type of penalty and is used to measure an electrical signal. It calculates the Gaussian noise that a receiver could add to a signal and measures the Vertical Eye Closure parameters. See Section 4.1 for details on the EECQ measurement methods.

4 Host and Module Testing

Host and module input and output signals are defined at the appropriate test points shown in CEI Figure 25-1 using the specified compliance test fixtures defined in OIF CEI 25.3.1 [1]. Host input stressed signals emulate the worst case module optical input signal with additional impairments added for module O/E conversion.

4.1 Module output tests

The module output test setup is shown in Figure 6 and the reference points are shown in Figure 8.

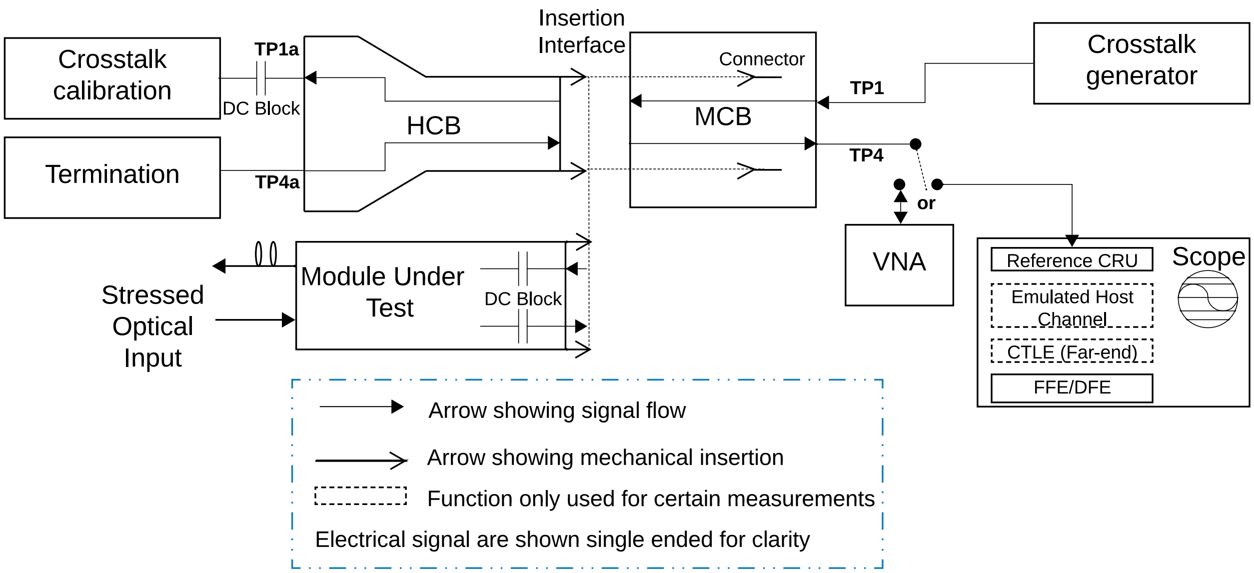

Figure 6: Module output test setup

The SSPRQ test pattern (specified in IEEE Std 802.3 [12]) is transmitted repetitively by the lane under test and the oscilloscope is set up to capture the complete pattern for EECQ analysis as described for TDECQ in IEEE Std 802.3 subclause 121.8.5 [11]. This pattern is also used for VMA and differential peak-to-peak voltage measurements at TP4. The lowest measured EECQ values are achieved with the equalizer optimization method described in 121.8.5 [11]. Alternative optimization methods such as minimum mean squared error (MMSE) may be used to determine equalizer tap weights to reduce test time and are expected to report equal or higher values of EECQ. These alternative methods should not be used for receiver sensitivity and stressed receiver sensitivity calibration.

The clock recovery unit (CRU) has a corner frequency of fb/13280 MHz and a slope of 20 dB/decade. The CRU can be implemented in hardware or software depending on oscilloscope technology. All co-propagating and counter-propagating lanes are active as crosstalk sources, using a QPRBS13-CEI test pattern as defined in CEI Appendix 16.C.3.1, or a QPRBS31-CEI test pattern as defined in OIF CEI Appendix 16.C.3.2 [14] or valid Ethernet signal. If the QPRBS13-CEI is used for the co-propagating lanes they should be asynchronous to the lane under test or sufficiently delayed to remove correlation from the lane under test. If the QPRBS13-CEI or QPRBS31-CEI patterns are used, any pairs of aggressor lanes should also be asynchronous to each other or sufficiently delayed. Amplitude and transition times for counter-propagating lanes are defined in Table 4. The lanes under test are asynchronous to the lanes in the opposing direction within the limits for the protocol in use.

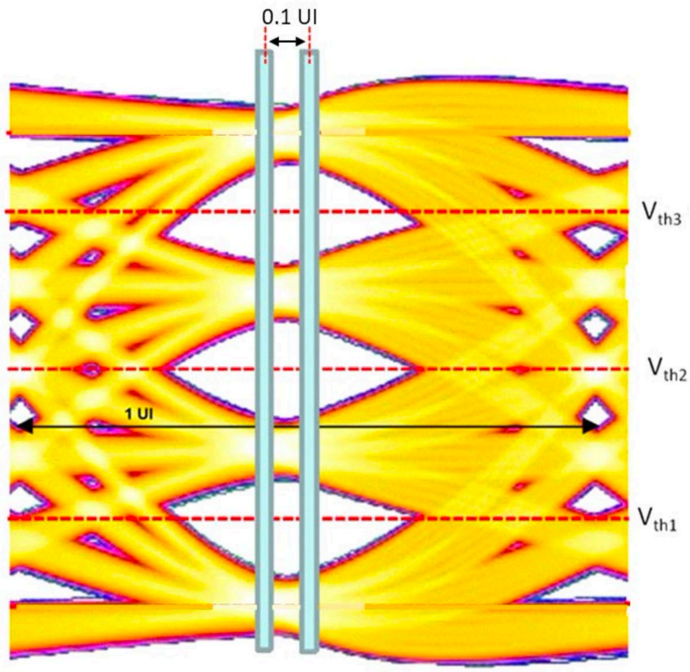

Figure 7: TP4 EECQ measurement

The signal at TP4 may appear as a closed eye, therefore a reference receiver is used to equalize the module output signal and open the eye for EECQ measurements. The reference receiver for the near-end measurement is a 1-tap DFE and 22-tap FFE and the reference receiver far-end also includes a Continuous Time Linear Equalizer (CTLE (see 4.4). The measured signal after the reference receiver shall meet the EECQ specification listed in Table 2 for module to host. The time position of the pair of histograms in Figure 7 for the module output (TP4) is the one that minimizes EECQ. The three threshold levels Vth1, Vth2, Vth3 may be adjusted within the limits as described for Pth1, Pth2, and Pth3 in IEEE Std 802.3 167.8.6 [8].

EECQ eye measurement method is illustrated in Figure 7 and the block diagram for measuring module output parameters including EECQ and VMA_{EECQ} is illustrated by Figure 8. EECQ test method is based on the method for measuring TDECQ as defined by IEEE Std 802.3 [9] with the following exceptions:

I. VMA_{EECQ} is used in place of OMA_{outer}. VMA_{EECQ} is measured at the output of the reference equalizer.
II. The reference equalizer in IEEE Std 802.3 [11] is replaced with the reference equalizer in Section 4.4.
III. Use SER = $5x10^{-4}$ corresponding to a BER of $2.5x10^{-4}$.
IV. σ_G is added at the output of the reference receiver, rather than before the FFE.

V. Crosstalk sources use a QPRBS13-CEI test pattern as defined in OIF Appendix 16.C.3.1, or a QPRBS31-CEI test pattern as defined in Appendix 16.C.3.2 or Ethernet signal.

VI. The following equation is used for EECQ in place of TDECQ [9] (Equation 121-12):

$$EECQ = 20 \times log10\left(\frac{VMA_{EECQ}}{6} \times \frac{1}{Q_t R}\right)$$ **Equation 3**

Where Q_t is 3.403 consistent with the BER and SER of this specification.

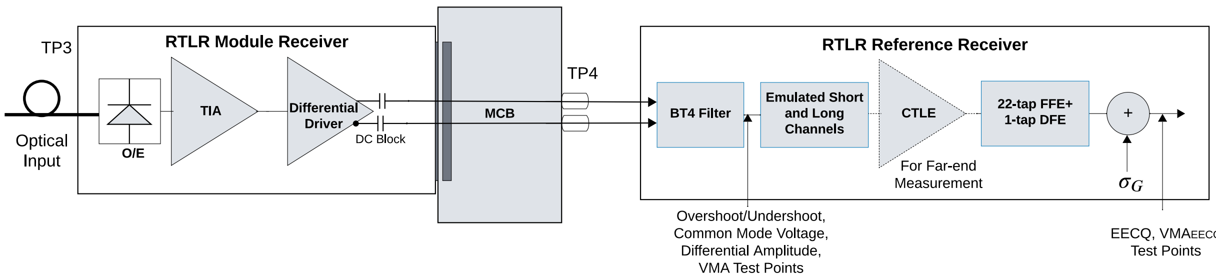

Figure 8: Module Output TP4 Measurements

4.2 Near-end and far-end eye measurement methodology

A calibrated optical stressed receiver input test signal with the specified test pattern (typically SSPRQ) is input to the module. The signal measured at TP4 is first convolved with the reference synthetic host channel defined in IEEE Std 802.3ck [10] with the exception that z_p for each test is provided in Table 5 and C0 and C1 are both zero.

Table 5: PCB length for module output measurements

Module output mode	Host channel type	PCB length, z_p (mm)
Short	near-end	0
Short	far-end	133
Long	near-end	80
Long	far-end	244.7

The loss of the emulated host channel for the Long far-end measurement is 11.9 dB at 53.125 GHz obtained with a z_p of 244.7 mm. Note that this does not include the MCB loss. The module output shall meet the EECQ specification with all the emulated channel conditions in Table 5.

A compliant module delivers a signal according to Table 2 while receiving any compliant optical signal at TP3.

4.3 Host input test

The ability of the host input to tolerate the parameters specified in Table 3 is tested using a stressed input test. There are two stressed signals, representing a worst compliant module in Short and Long output modes, see 3.5.1. The host chooses which of the two settings it is tested with. Each test signal is applied at TP4a of Figure 9 and calibrated at TP4, using the Host Compliance Board and the Module Compliance Board specified in OIF CEI 25.4 [1]. The test setup is shown in Figure 9. The UBHPJ block and sinusoidal jitter are used to create non-compensable DJ. The sinusoidal jitter is as defined in OIF CEI Table 25-9.

A compliant host delivers an interface BER as specified in Section 2.3.1 while receiving the stressed input signal at TP4a/TP4 with an EECQ value defined in Table 3. An Ethernet host complies to the frame loss ratio (FLR) specification in the applicable optical specification, see 1.3.

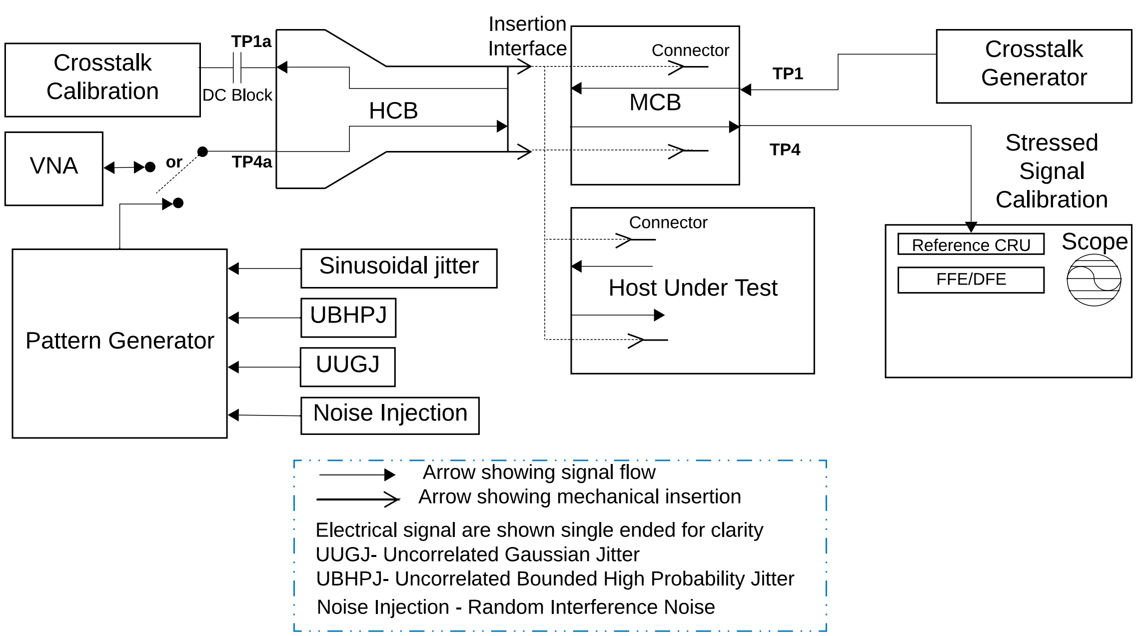

Figure 9: Host stressed input test setup

4.3.1 Host receive stressed input test method

The reference CRU and reference receiver as defined in Section 4.4 are used to calibrate the stressed input test signal at TP4a (per Table 3). The TP4a stressed input test is calibrated using a SSPRQ pattern. The pattern is changed to a scrambled idle pattern for the TP4a stressed input test. The crosstalk source is asynchronous to the main pattern generator. The amplitude and rise/fall time of the crosstalk source are given in Table 4. The Host under test sends out a QPRBS31-CEI or scrambled idle pattern or valid

Ethernet signal during the test. For multi-lane implementations additional lanes shall be active with either uncorrelated QPRBS31-CEI or QPRBS13-CEI patterns, scrambled idle pattern or valid Ethernet signal, with the same amplitude as the lane under test.

4.3.2 Host input test signal calibration

The host input is tested at TP4a using a Host Compliance Board as defined in OIF CEI Section 25.4.1 [1]. The host input test setup is shown in Figure 9. UBHPJ, UUGJ and SJ are added to a clean test pattern until the jitter (except for EOJ) at the output of the pattern generator approximates the informative transmit recommendations given in OIF CEI Appendix 25.C. With the crosstalk generator calibrated to meet the specifications in Table 4, the EECQ at TP4 is measured using the reference receiver defined in Section 4.4 with the optimal receiver equalizer settings and the methodology defined in Section 4.1. The UUGJ, Noise Injection, and pattern generator amplitude are adjusted to give the maximum EECQ defined in Table 3 and minimum VMA specified for the module output mode requested in Table 2, measured using the reference receiver defined in Section 4.4.

4.4 TP4 reference receiver

The signal at TP4 is observed through a reference receiver consisting of a 4th order Bessel-Thomson filter with a bandwidth of 42 GHz concatenated with a Continuous Time Linear Equalizer (CTLE) followed by a 22-tap FFE and 1-tap DFE. The CTLE is defined in Section 4.4.1. The sum of the reference receiver FFE tap coefficients is constrained to be equal to 1. Individual reference receiver FFE tap weights are constrained to the values given in Table 6. The constraints on the DFE values are given in Table 7. The Bessel-Thomson filter, CTLE, FFE, and DFE may be implemented in software, the signal is not averaged.

Table 6: 22-tap reference FFE tap weights

Parameter	Min Value	Max Value
Pre-cursor (-3) to (-1) [1]	Not constrained	Not constrained
Main (0)	0.75	NA
Post-cursor (1) to (4) [1]	Not constrained	Not constrained
Post-cursor (5) [2]	-0.3	0.3
Post-cursor (6) [2]	-0.2	0.2
Post-cursor (7) [2]	-0.1	0.1
Post-cursor (8) to (18)	-0.07	0.07

1. The weights for these taps are not limited in IEEE Std 802.3 clauses 121 [11], 124 [5], 140 [6], 151 [7] or 167 [8].
2. Tap weights based on IEEE Std 802.3 subclause 167 [8].

Table 7: 1-tap reference DFE tap weight

Parameter	Min Value	Max Value
Range of b1 tap without precoding [1]	0	0.4 [2]
Range of b1 tap with precoding	0	0.85 [3]

1. Ethernet PMDs [5], [6], [7], and [8] are specified without precoding.
2. To mitigate burst error generation without precoding b1 max limited to 0.4.
3. Optical specifications other than those in section 1.3 may use precoding in which case the DFE tap constraint is relaxed.

4.4.1 TP4 CTLE used in reference receiver

A CTLE is used in the TP4 reference receiver for module far-end testing. It is not used for the module near end testing and calibration of the stressed host input The CTLE is defined by Equation 4:

$$H_{CTLE}(f) = \frac{\left(10^{\frac{gDC}{20}} + j \times \frac{f}{f_z}\right)\left(10^{\frac{gDC2}{20}} + j \times \frac{f}{f_{LF}}\right)}{\left(1 + j \times \frac{f}{f_{LF}}\right)\left(1 + j \times \frac{f}{f_{p1}}\right)\left(1 + j \times \frac{f}{f_{P2}}\right)} \qquad \textbf{Equation 4}$$

Frequencies of poles and zeros scale with baud rate (f_b) and are listed below:

$$f_{p1} = f_b / 1.8839$$

$$f_{p2} = f_b$$

$$f_z = f_b / 2.862$$

$$f_{LF} = f_b / 40.$$

where: gDC+ gDC2 is the low-frequency gain, f_{p1}, f_{p2} are the frequencies of the CTLE poles f_z along with gDC determine the high frequency zero, f_{LF} along with gDC2 determine the low frequency zero of the CTLE.

The allowed values of high frequency gain gDC vary from 0 to -11 dB in 1 dB steps for the module far-end test.

The allowed values of low frequency gain gDC2 vary from 0 to -2.5 dB in 0.5 dB steps for the module far-end test. The CTLE is not used for the module near end test and calibration of the stressed host input test.

Figure 10 shows the CTLE response of the reference CTLE with 0 dB of low frequency gain for a baud rate of 53.125 GSym/s with gDC = -2 dB to -11 dB in 1 dB steps, gDC2 = 0 dB. Figure 11 shows the frequency response of the reference CTLE for a baud rate of 53.125 GSym/s with values for gDC = -6 dB, gDC2 = 0 dB to -2.0 dB in 0.5 dB steps. The CTLE peaking value is the approximate difference between the low-frequency response (1 MHz) and the maximum high-frequency response in dB.

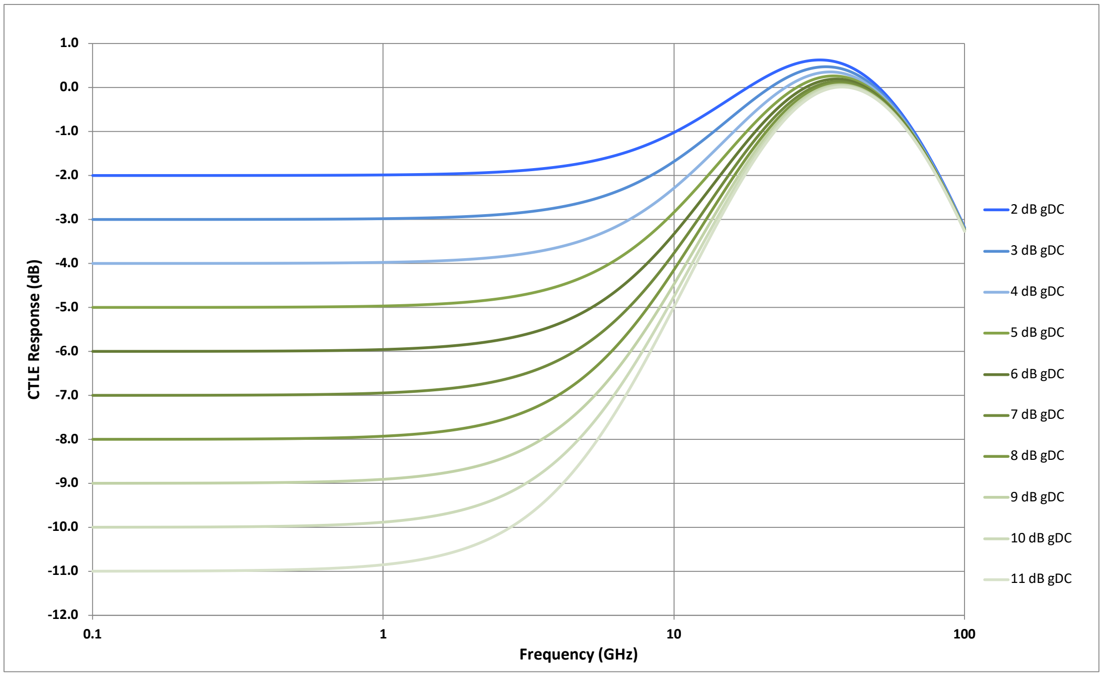

Figure 10: Module output reference CTLE response with gDC= [-2 to -11] dB

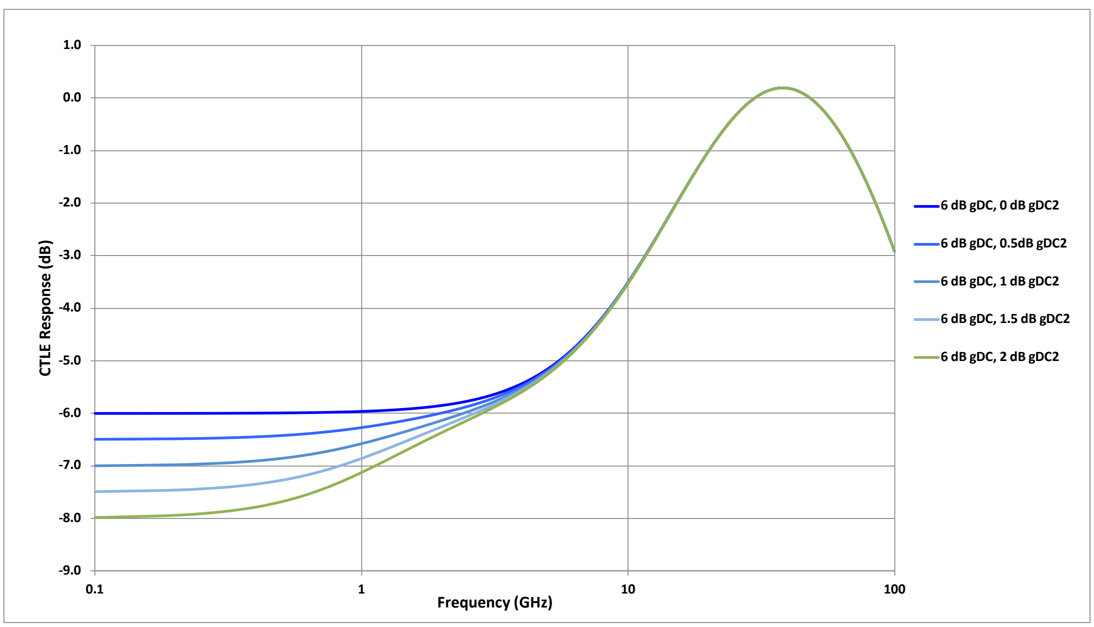

Figure 11: Module output reference CTLE response with gDC=-6 dB and gDC2=[0, -0.5, -1.5, -2.0] dB

4.5 Host receive overload voltage tolerance

The input voltage tolerance tests the acceptance of differential input peak-peak amplitude produced by the extremes of operation from the module output. The maximum voltage at a device input can be larger than the maximum at the compliance points due to output/input impedances and reflections. The input overload voltage tolerance specification is to be met for any valid Ethernet signal with the maximum peak-peak amplitude for the requested mode in Table 3. The peak-peak amplitude is measured with the SSPRQ pattern.

5 References

5.1 Normative references

[1] OIF CEI 5.2 clause 25 CEI-112G-VSR-PAM4 Very Short Reach Interface, https://www.oiforum.com/wp-content/uploads/OIF-CEI-05.2.pdf, January 2024
[2] OIF CEI-112G-LINEAR-PAM4 Interface
[3] OIF CEI 5.2 subclause 13.3.6 CEI-28G-VSR-PAM4 Very Short Reach Interface, https://www.oiforum.com/wp-content/uploads/OIF-CEI-05.2.pdf, January 2024
[4] IEEE Std 802.3ck-2022 as amended by IEEE Std 802.3df-2024 Annex 120G Chip-to-module Attachment Unit Interfaces 100GAUI-1 C2M, 200GAUI-2 C2M, 400GAUI-4 C2M, and 800GAUI-8 C2M
[5] IEEE Std 802.3-2022 as amended by IEEE Std 802.3df-2024 Clause 124 Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8 and 800GBASE-DR8-2
[6] IEEE Std 802.3-2022 Clause 140 Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-DR, and 100GBASE-FR1
[7] IEEE Std 802.3-2022 Clause 151 Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-FR4
[8] IEEE Std 802.3db-2022 as amended by IEEE Std 802.3df-2024 Clause 167 Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 100GBASE-SR1, 200GBASE-SR2, and 400GBASE-SR4, 800GBASE-VR8, and 800GBASE-SR8
[9] IEEE Std 802.3-2022 subclause 121.8.5, Transmitter and dispersion eye closure for PAM4 (TDECQ),
[10] IEEE Std 802.3ck-2022 subclause 162.11.7.1, Channel signal and crosstalk path calculations
[11] IEEE Std 802.3-2022 subclause 121.8.5.4, TDECQ reference equalizer
[12] IEEE Std 802.3-2022 subclause 120.5.11.2.3, SSPRQ test pattern.
[13] SNIA SFF-8024 SFF Module Management Reference Code Tables, Rev. 4.13, July 2025.

5.2 Informative references

The following interface standards and specifications are relevant to this specification.

[14] OIF-CEI-5.2 Appendix 16.C – General PAM4 Requirements, January 2024
[15] OIF-CEI-5.2 Appendix 16.D – FEC Guidance and Background Material, January 2024.

6 Appendix A: Glossary

The following terms are used in this document based on definitions from IEEE Std 802.3, OIF CEI, and Wikipedia:

Table 8: Glossary presents definitions for acronyms used in this IA

Term	Definition
AUI	Attachment Unit Interface (AUI) is a physical and logical interface originally defined in the IEEE Std 802.3 10BASE5 Ethernet and now being used for the C2M applications.
BER	Bit Error Ratio is the number of bit errors divided by the total number of transferred bits during a studied time interval.
C2M	Chip-to-module interface a type of Ethernet AUI interface similar to VSR.
CRU	Clock recovery unit, a component that recovers timing of a signal.
CEI	Common Electrical IO, an OIF Implementation Agreement containing clauses defining electrical interface specifications.
CTLE	Continuous Time Linear Equalizer.
DFE	Decision feedback equalizer. A DFE is a nonlinear equalizer that uses past symbol decisions to eliminate the ISI caused by previously detected symbols on the current symbol being detected.
EECQ	EECQ is an estimate of signal impairment, given a target SER. It is defined similarly to TECQ, but because of the nature of intensity detection an EECQ of X dB is equivalent to a TECQ of X/2 dB for the same reference equalizer.
Egress	Egress Is the direction from the host ASIC towards the optical medium.
FFE	Feed forward equalizer.
HCB	Host Compliance Board, a test board to measure the host output or inject signal into the host input.
Ingress	Ingress is the direction from the optical medium towards the host ASIC.
MCB	Module Compliance Board, a test board to measure the module output or inject signal into the module input.
MDI	A Medium Dependent Interface (MDI), the MDI is the interface “optical

	connector" between the PMD and the fiber optic cabling.
PAM	Pulse amplitude modulation, a form of signal modulation where the message information is encoded in the amplitude of a series of signal pulses. For optical links it refers to intensity modulation.
PAM4	Pulse amplitude modulation-4 is a two-bits modulation that takes two bits at a time and maps the signal amplitude to one of four possible levels.
PMD	IEEE Std 802.3 Physical Medium Dependent (PMD), is the portion of the Physical Layer between the PMA and the Medium Dependent Interface (MDI).
Retimer(CDR)	Clock and data recovery, a component that re-establishes the timing of a signal that may have been degraded due to impairments on a transmission line, the retimed signal is now able to continue further to its destination.
RTLR	Retimed Transmitter Linear Receiver
SER	PAM4 symbol error ratio.
SerDes	A Serializer/Deserializer is a pair of functional blocks or transceiver commonly used in high speed communications that converts parallel data to serial data and vice versa. The transmitter section is a parallel-to-serial converter, and the receiver section is a serial-to-parallel converter.
SIGNAL_DETECT	SIGNAL_DETECT is the global indicator of the presence of optical signal on all lanes, above the specified optical signal threshold level, see specific IEEE Std 802.3 PMD specifications.
TDECQ	Transmitter Dispersion Eye Closure Quaternary, TDECQ is a measure of each optical transmitter's vertical eye closure when transmitted through a worst case optical channel and equalized with the reference equalizer. TDECQ is an approximate method to calculate the penalty for a target SER.
TRO	Transmit Retimed Optics an alternate name used in industry for RTLR.
VMA	Voltage Modulation Amplitude is the low frequency signal amplitude.
VSR	An OIF Very Short Reach bi-directional specification similar to IEEE Std 802.3 C2M.

† Some definitions include content from IEEE Std 802.3 and www.wikipedia.com.

7 Appendix B: List of companies belonging to OIF when document is approved

1Finity
Accelight Technologies, Inc.
Accton Technology Corporation
Adtran Networks SE
Advanced Fiber Resources (AFR)
Advanced Micro Devices, Inc.
AIO Core
Alibaba
Alphawave Semi
Altera
Amphenol Corp.
Anritsu
Applied Optoelectronics, Inc.
Arista Networks
Astera Labs
Ayar Labs
BizLink Technology, Inc.
Broadcom Inc.
Cadence Design Systems
Casela Technologies USA
Celero Communications Inc.
Celestica
China Telecom
CICT
Ciena Corporation
CIG Photonics Japan Limited
Cisco Systems
Coherent
ColorChip
Cornelis Networks
Corning
Credo Semiconductor
Lightelligence
Lightmatter
Linktel Technologies
Lumentum
Lumilens
Lumiphase AG
LUXIC Technology
Luxshare Technologies
MACOM Technology Solutions
Marvell Semiconductor, Inc.
MaxLinear Inc.
MediaTek
Meta Platforms
Microchip Storage
Microsoft Corporation
Mitsubishi Electric
Molex
Multilane Inc.
NEC Corporation
Nokia
NTT Corporation
NVIDIA
O-Net Technologies
Omattrix Ltd Co
Optomind Inc.
Orange
PETRA
Photonicx AI
Point2 Technology
Precision Optical Technologies
Quantifi Photonics
Quintessent Inc.

Dai Nippon Printing
Dell
Dexerials Corporation
DustPhotonics
EFFECT Photonics
Eoptolink Technology
Epson Electronics America
Ericsson
EXFO
Femtum Inc.
Formerica Optoelectronics
Foxconn Interconnect Technology
Fujikura
Furukawa Electric
GlobalFoundries
Google
H3C Technologies
Hakusan Inc
Hewlett Packard Enterprise
HGGenuine Optics Tech Company
Huawei Technologies
InfiniLink US
Jabil
Kandou Bus
KDDI Research
Keysight Technologies
Kuaishou Technology
KYOCERA Corporation
Lessengers Inc.
Ligent, Inc.
Ranovus
Renesas Electronics
Retym
Rosenberger Hochfrequenztechnik
Ruijie Networks
Samtec Inc.
SCINTIL Photonics
Semtech Canada Corporation
Senko Advanced Components
SeriaLink Systems
Sicoya GmbH
Socionext
Source Photonics
Sumitomo Electric Industries, Ltd.
Sumitomo Osaka Cement
Suzhou TFC Optical Communication Co (TFC)
Synopsys, Inc.
TE Connectivity
Tektronix
Telefonica S.A.
TELUS Communications, Inc.
TeraHop
TeraSignal
Texas Instruments
US Conec
Viavi Solutions
Wilder Technologies
Xphor Ltd.
Yamaichi Electronics Ltd.
ZTE Corporation