OIF 448Gbps Signaling for AI Workshop
April 15-16, 2025

OIF High-Density Connector Project 448Gbps Considerations

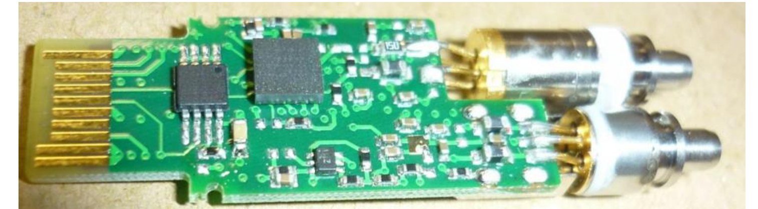
Matt Traverso

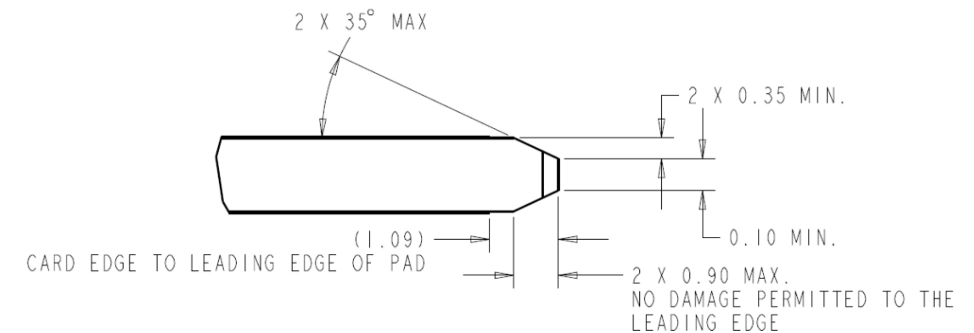
16 April 2025

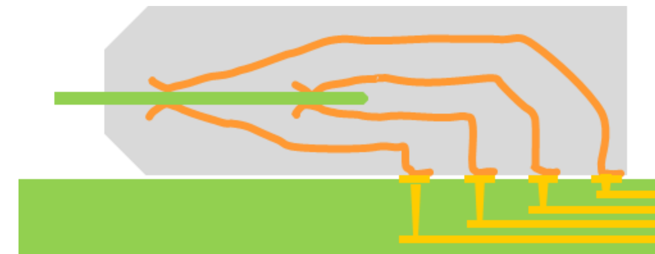
Current State of the Art: PCB Edge Connectivity

- Pluggable Optics since GBIC (1995) have leveraged PCB Edge connectivity
- PCB Edge connections mandate:
  - Limited number of contacts
  - Constrained thickness – PCB stackup!
  - Contact stubs due to mechanical insertion
  - Density and crosstalk tradeoff
  - Via transitions to PCB bottom

SFP PCBA







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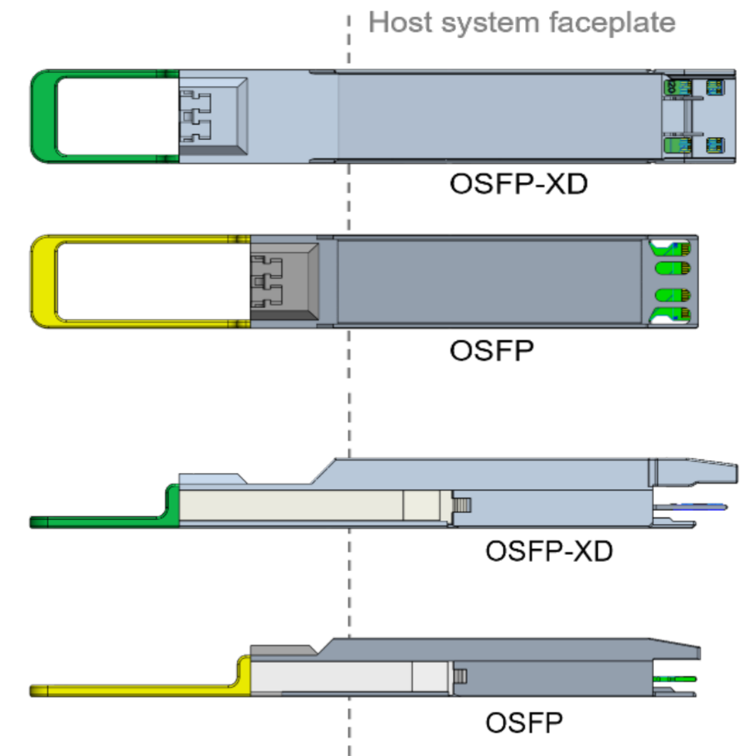
*Lane = TX Diff Pair + RX Diff Pair

Current State of the Art: (8-16 Lanes*)

- OSFP connector supports
  - 8 differential lanes at 224G-PAM4 signaling of transmit and receive for 1.6T
- OSFP developing support for
  - 8 differential lanes at 448G-PAM4 signaling of transmit and receive for 3.2T
  - Signal integrity challenges
- OSFP-XD targets support of
  - 16 differential lanes at 224G-PAM4 signaling of transmit and receive for 3.2T
  - Signal integrity / routing challenges



https://www.osfpmsa.org/assets/pdf/OSFP1600_and_OSFP-XD.pdf

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OIF | ACCELERATING MARKET ADOPTION OF OPTICAL NETWORKING TECHNOLOGIES

PROJECT HIGHLIGHTS 2025

150+ Member Companies → Identifies Industry Needs and Gaps → Publishes Implementation Agreements (specifications), Requirements and White Papers → Performs Interoperability Demonstrations

OIF High Density (HD) Connector Project

— launched at OIF Q1 2025 meeting as part of the Energy Efficient Interfaces track

OPTICAL

Multi-Vendor Interoperability in Client Form Factors

1600ZR+
- <1000km Multi-Span Coherent DWDM

1600ZR, 800ZR, 400ZR
- >80km Coherent DWDM

1600LR, 800LR
- <10km Coherent Point-to-Point

ENERGY EFFICIENT INTERFACES

Next Generation Low Latency Interfaces for AI/ML & Data Centers
- Compute Optics Interface (COI)
- RTLR (Retimed Tx, Linear Rx)
- External Laser Sources (ELSFP)
- Co-Packaged Modules (3.2T)
- CEI-Linear

PROTOCOL

FlexE
- More Efficient
- Agile Networking

OIF
- Member Driven Global Organization
- 25+ Years of Service
- 150+ Member Companies
- 80+ IAs (specifications)
- 65+ Interop Demos

MANAGEMENT

Common Management Interface Specification (CMIS)
- Single Solution Ranging From Copper to Coherent
- Simplified Bring up Between Host and Module
- Supports Standard and Custom Interfaces

ELECTRICAL

Common Electrical I/O (CEI)
- High-Speed Building Blocks
- 448G, 224G, 112G, 56G, 28G
- LR, MR, VSR, XSR+, XSR, MCM, Linear
- Protocol Agnostic Link Training

NETWORKING

Transport SDN APIs
- Automation, Programmability

Enhanced Network Operations
- Artificial Intelligence
- Digital Twin
- DC Storage and Optical Multi-Layer Coordination

FOR MORE INFORMATION, VISIT WWW.OIFORUM.COM/TECHNICAL-WORK/CURRENT-WORK/

OIF High Density (HD) Connector Project

- This project will write an informative requirements document for a High Density (HD) connector for optical interconnect applications, addressing today's limits.
- Possible schedule:
  - Q3'25: Draft complete & ready for Straw Ballot
  - Q4'25: Informative Requirements Document Approval
- If successful, a follow-on project may write a Specification(s)
- Requirements alternatives:
  - Any combination of front pluggable and NPO
  - Connector and mechanicals or connector only
  - One or multiple connector lane count

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Contributors to OIF HD Connector Project Start Proposal

- Andreas Bechtolsheim, Arista
- Vipul Bhatt, Coherent
- Katsumi Fukumitsu, Fujitsu
- Toshiyasu Ito, Yamaichi
- Kenneth Jackson, Sumitomo Electric
- Jeff Hutchins, Ranovus
- Ryu Kimbara, Hakusan
- Samuel Kocsis, Amphenol
- David Law, HPE
- Terry Little, FIT
- Jeff Maki, Juniper Networks
- Tom Mitcheltree, USConec
- David Piehler, Dell
- Anand Ramaswamy, Broadcom
- Tyler Royer, Senko
- Jignesh Shah, Samtec
- Mike Sluyski, Cisco
- Scott Sommers, Molex
- Craig Thompson, NVIDIA
- Davide Tonietto, Huawei
- Nathan Tracy, TE
- Matt Traverso, Marvell
- Ed Ulrichs, Intel
- Peter Winzer, Nubis
- Rangchen Yu, Terahop
- Leo Zhang, Luxshare

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High Density Connector: System Feature Examples

- Front accessibility/pluggability key requirement
  - Cabled host
  - Vertical line card architecture (VLC)
- Existing front pluggable form factor modularity benefits maintained
  - Testability, Replaceability, & Configurability
  - Existing business model: independent optics suppliers
- NPO for proximity to Switch ASIC or GPU for low electrical channel loss
- Cabled host support between NPO and front panel
- High yield, high reliability

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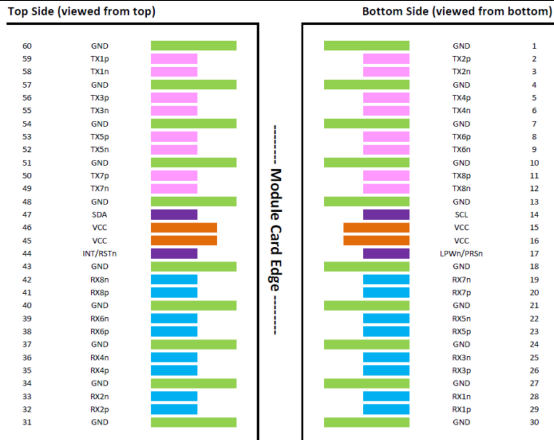
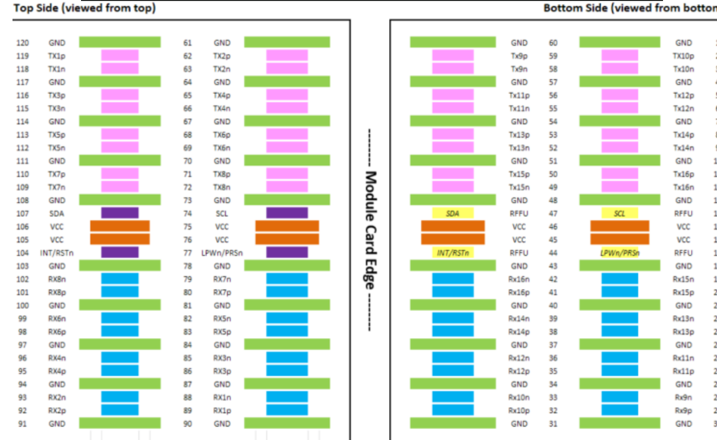
HD Connector Parameter Targets

OSFP 1.6T/3.2T
8 Lane support
single row (1D)



OSFP-XD 3.2T
16 Lane support
two row (1.5D)



New HD Connector Concept
High lane count support
many row/col (2D)

- BW: 12.8T / 25.6T
- Pitch: 0.5mm
- High lane count: 64 Tx/Rx signal pairs + 16 power & control
- Design I/O rate: 224G PAM4 / 448G PAM6 or PAM8 (TBD)

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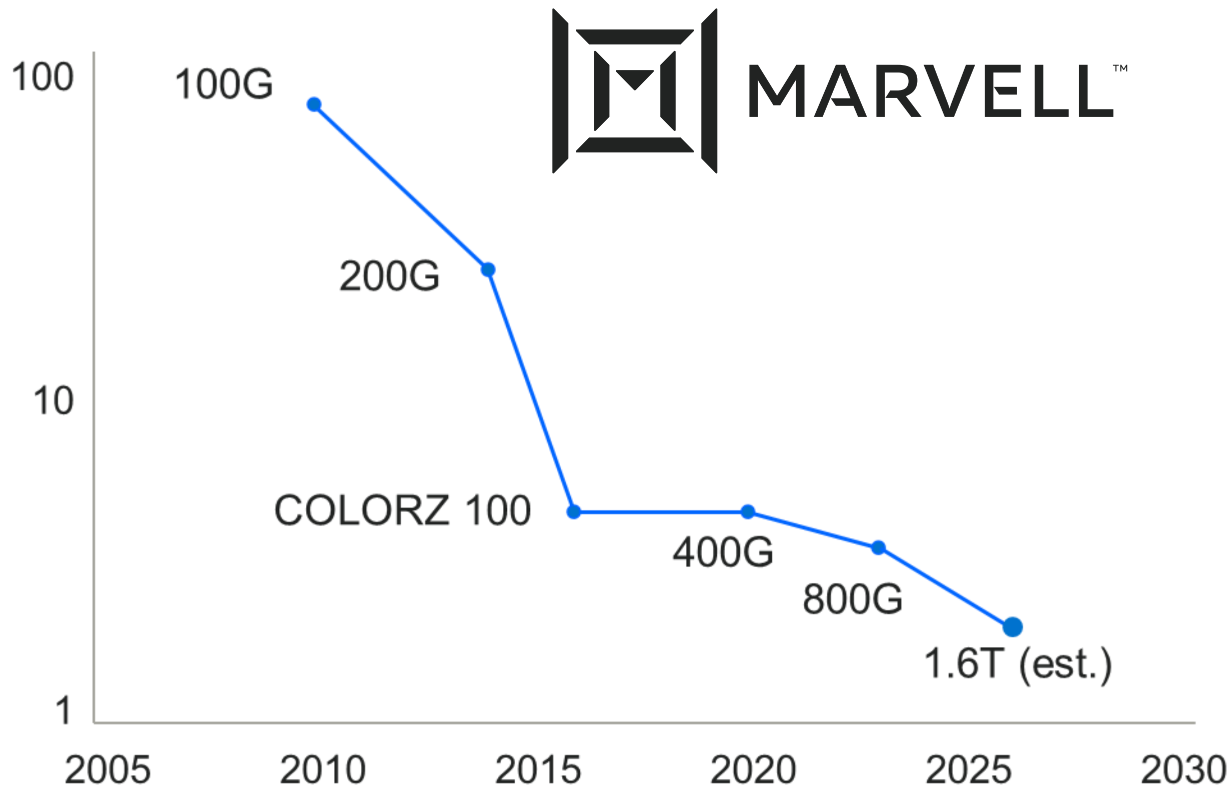
HD Connector Thermal & Size Considerations



- Each pluggable BW iteration has demonstrated efficiency gains
- However, 12.8T of BW at 5pJ/b is >60W
- Focus on enhanced cooling capacity
- Size – more consensus required, but targeting >3x density increase over OSFP variants

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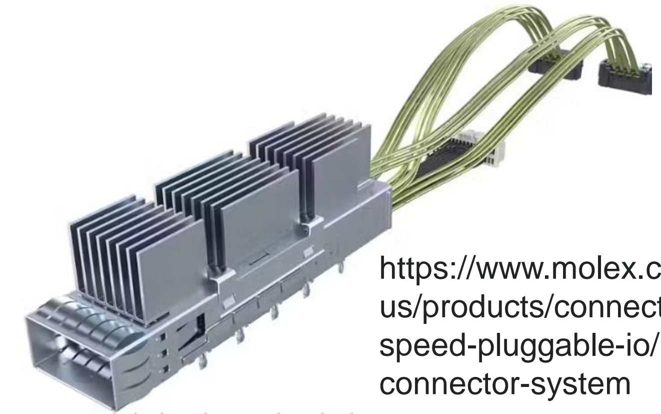
Cable connected Pluggable Cages

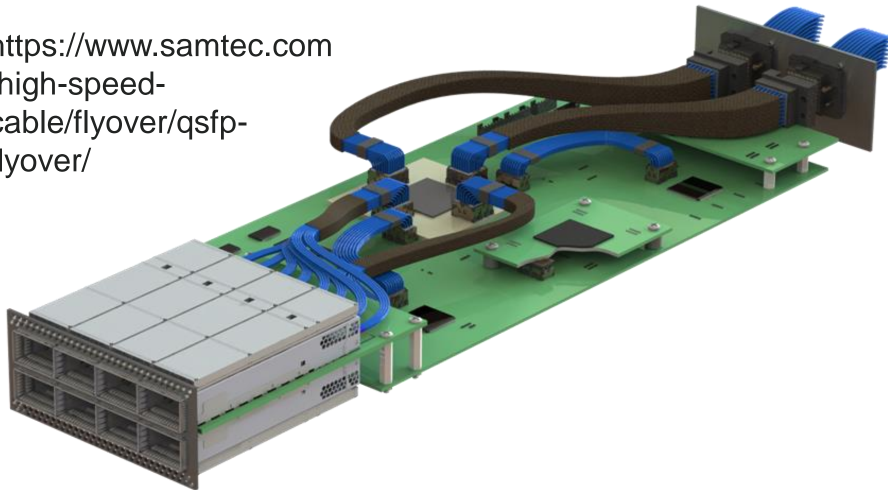
https://www.te.com/en/products/brands/adrenaline.html

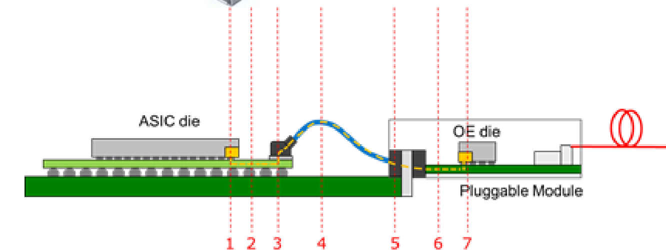
- Pluggable optics cages with cabled connectivity addresses
  - Lower channel insertion loss than PCB routing
  - Tighter tolerance to pluggable PCB edge connector



https://www.molex.com/en-us/products/connectors/high-speed-pluggable-io/bipass-i-o-connector-system

https://www.samtec.com/high-speed-cable/flyover/qsfp-flyover/





1. ASIC die escape
2. ASIC package fan-out
3. Package escape, on-package connectors
4. Fly-over cables
5. Module cage connectors
6. Module substrate fan-out
7. OE die escape

HUAWEI

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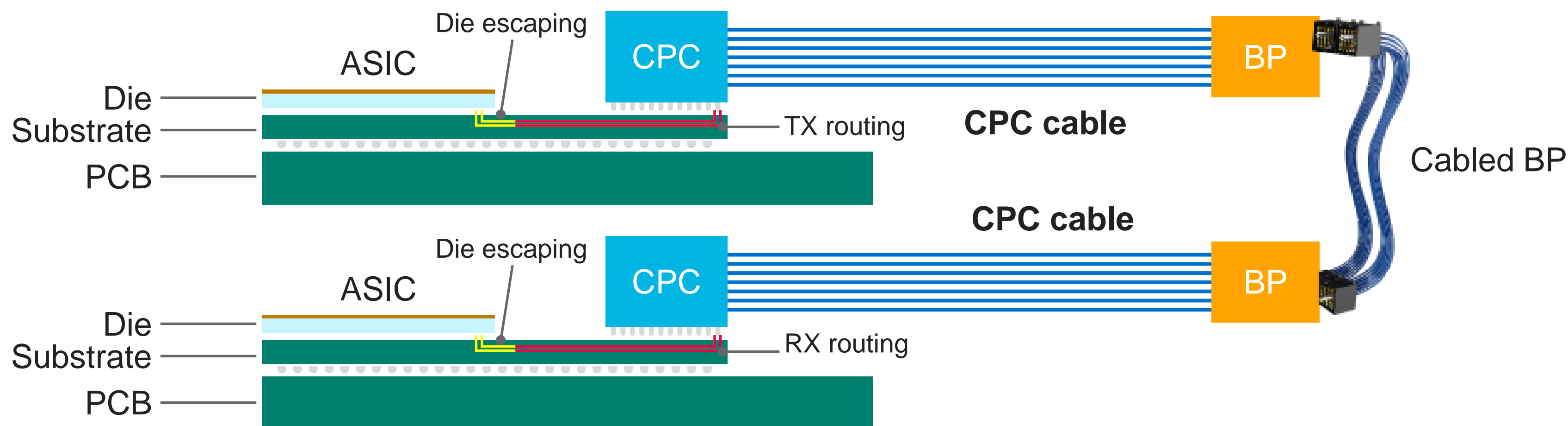
CPC (copper channel) for 448G scale-up connectivity



Modulation	Baud rate	Required SNR	Target reach	Insertion loss	Additional note
PAM4	212.5G	17.65 dB	>1m cabled backplane	>80 dB	Not feasible
PAM6	170G	21.2 dB	>1m cabled backplane	>50 dB	Optional FECi may be needed
PAM8	141.6G	23.7 dB	>1m cabled backplane	>40 dB	

448G copper interconnect: PAM4 is a non-starter

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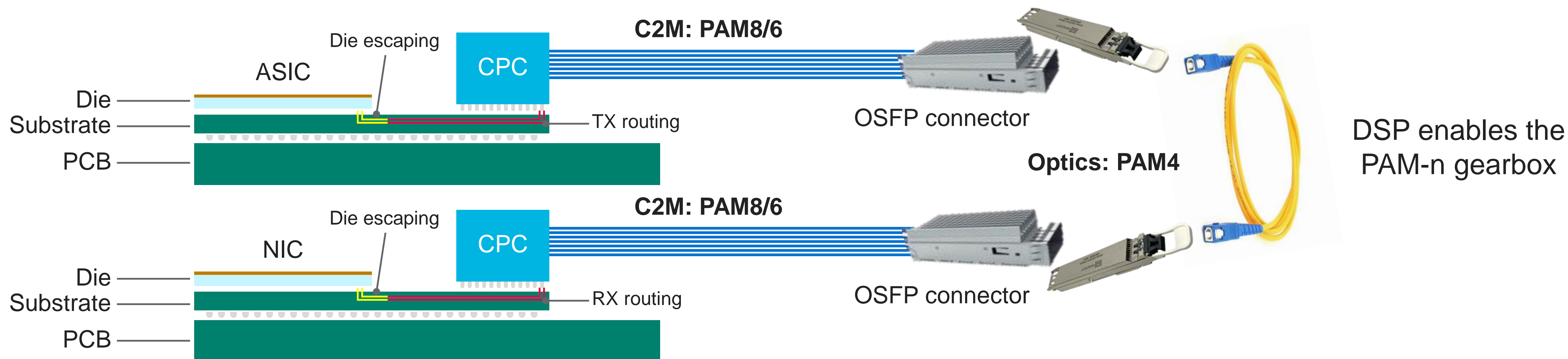
3.2T scale-out connectivity powered by DSP



448G	C2M	Optical	Notes
DSP	PAM8/6	PAM4	✓
LRO	PAM8/6	PAM4	✗
LPO	PAM8/6	PAM4	✗

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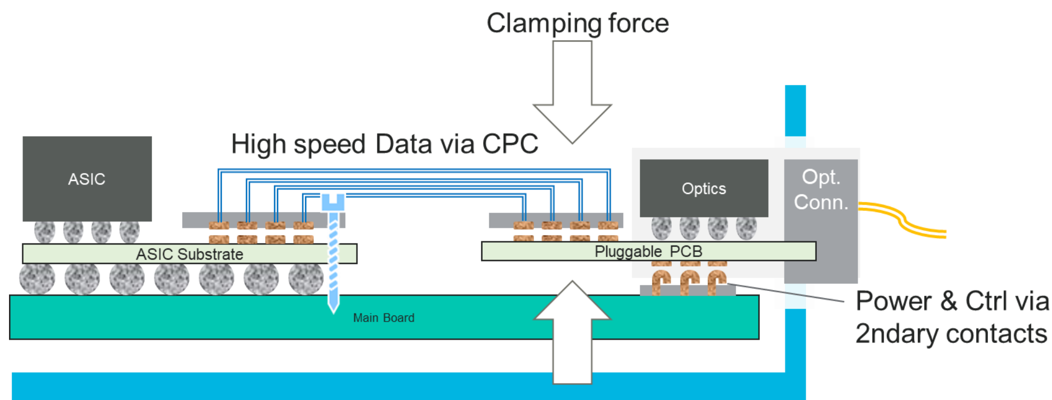
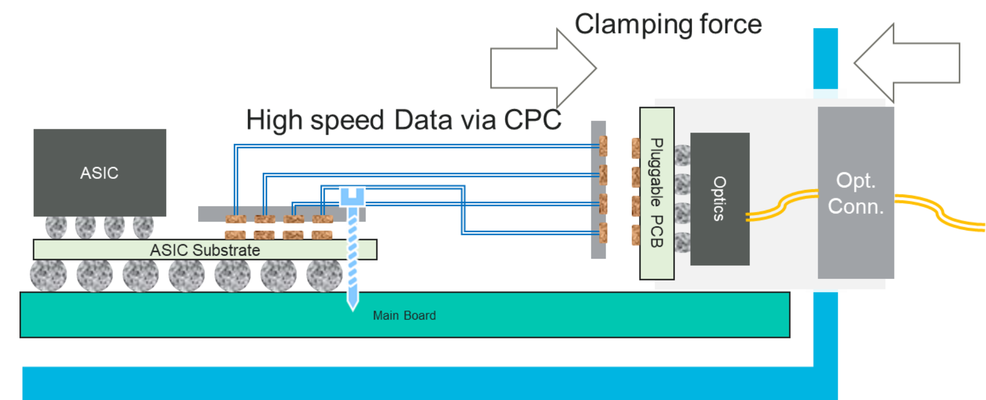
Example Geometry Highly Parallel Pluggable via CPC pluggability

- **Right Angle:** Enable 64 to 128 Diff Pairs via CPC
  - Secondary connector for Power & Ctrl Functions feasible
  - More conventional thermal path
  - Need sufficient height for vertical coupling turn to faceplate



- **Surface Normal:** Enable 64 to 128 Diff Pairs via CPC
  - Support for Power & Ctrl likely thru main connection
  - Likely needs right angle thermal path
  - Need sufficient width / height for edge coupling turn to faceplate



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HD Connector Concept Example

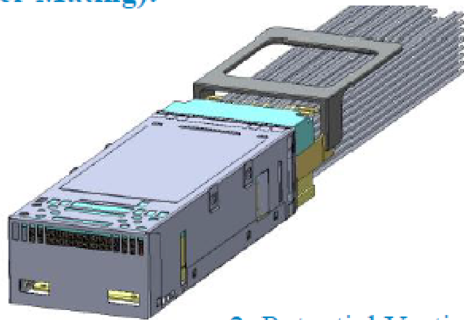
Envelope Size (After Mating):

L: 104.15mm

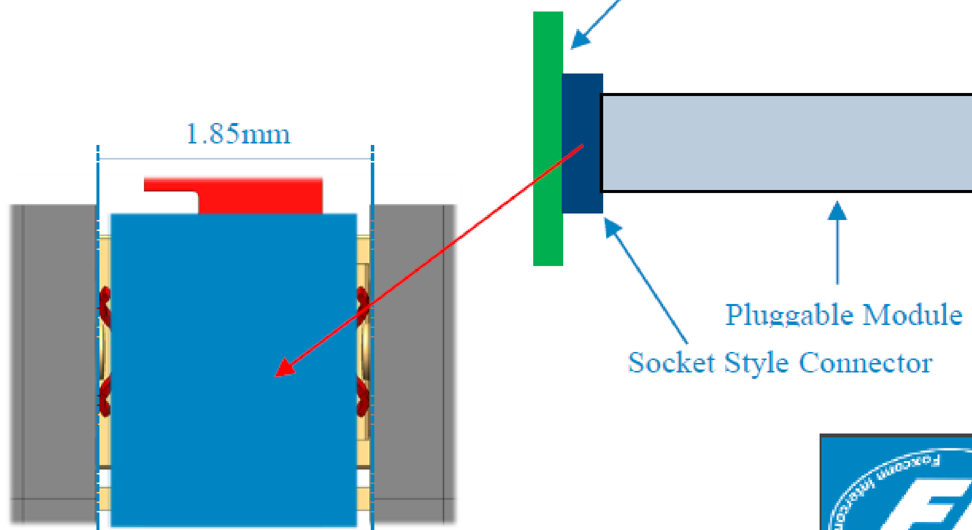
W: 37.08mm

H: 23.63mm

1. Optional RA Application



2. Potential Vertical Line Card Application

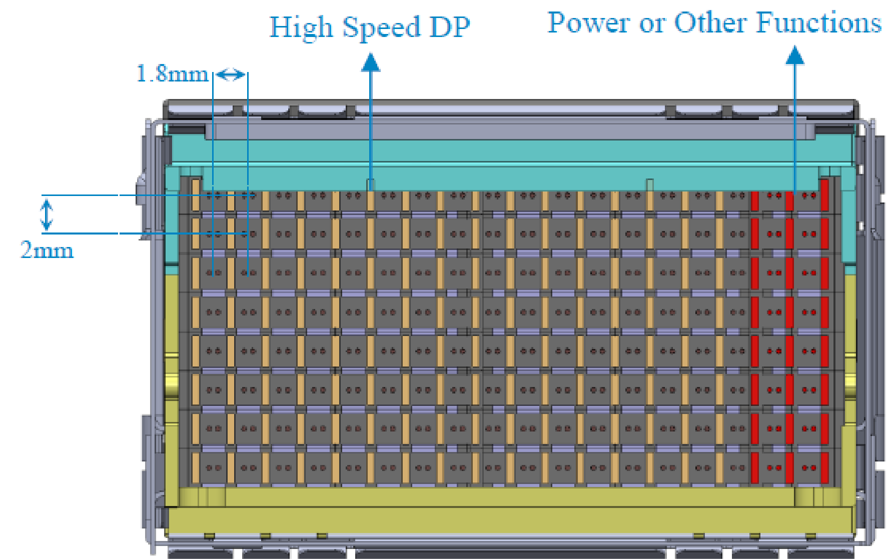


Mating Distance:

1.85mm mating distance between cable to cable.

Features:

- 144 differential pairs – 18 by 8 – 16 Power or Other functions (can be adjusted);
- Scalable to 448 Gbps application;
- Each differential pair fully shielded;
- Very short mating & trans;
- Pluggable transceiver with high signals density;
  Very short transceiving distance at mating area;
- Cable to Cable & Cable to Board available.



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HD Connector Project

- Opportunity to define next generation interconnect suitable for highly parallel connections
- Enable new and existing system topologies for AI applications
- High bandwidth density with support for high lane rate

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