Implementation Agreement for Integrated Coherent Transmit-Receive Optical Sub Assembly

OIF-IC-TROSA-01.0

August 20, 2019

Implementation Agreement created and approved
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ABSTRACT: This document details an Implementation Agreement for an Integrated Coherent Transmit-Receive Optical Sub Assembly (IC-TROSA) targeting modulation and data-rate agnostic coherent applications having nominal symbol rates up to 64Gbaud.

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Document Revision History

Document	Date	Revisions/Comments
OIF-IC-TROSA-01.0	August 20, 2019	Initial document release

1. Introduction

This document details an Implementation Agreement for an Integrated Coherent Transmit-Receive Optical Sub Assembly (IC-TROSA) targeting modulation and data-rate agnostic coherent applications having nominal symbol rates up to 64Gbaud. This IA aims to identify and specify the common features and properties of IC-TROSA to enable them to broadly meet the needs of current and future coherent systems.

The IC-TROSA Implementation Agreement defines the following: (1) Required functionality; (2) High speed electrical interfaces; (3) Low speed electrical interfaces; (4) Environmental and operating characteristics; (5) Electro-optical characteristics; (6) Mechanical requirements; (7) Management Interface. Additional informative electro-optical specifications are also included in Appendix B.

Two electro-mechanical form factors are defined within this IC-TROSA IA. Type-1 uses a surface mount (SMT) Ball Grid Array (BGA) configuration. The alternative electro-mechanical form factor Type-2 employs a mechanical enclosure utilizing separate flexible PCBs for low speed and RF I/O interfaces. Mechanical, electrical, and functional differences between the Type-1 and Type-2 form factors are highlighted where appropriate, otherwise common performance characteristics are required for the two form factors.

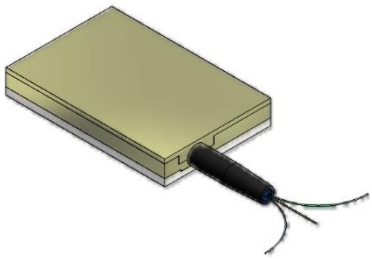


Figure 1-1: Type-1 IC-TROSA

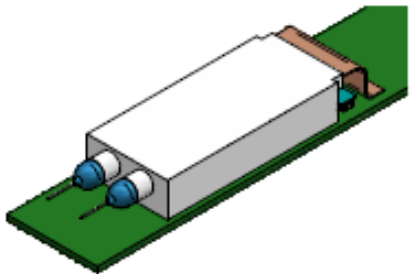


Figure 1-2: Type-2 IC-TROSA

The IA defines an IC-TROSA as a digitally controlled optical board mount module with integrated logic for purposes of optical configuration, stabilization, and monitoring. The IA further defines the management interface in terms of the communications hardware and management system software specifications. The IC-TROSA management interface specification is common to both Type-1 and Type-2 electro-mechanical form-factors with a few exceptions for laser control and some Alarm, Control, and I/Os as described within this IA.

The IA does not define the technologies used to implement the IA, nor the expected optical transmission performance of coherent systems using receivers conforming to the IA.

2. Functionality

2.1. Electro-Optic Architecture

The required electro-optic functional blocks, as well as some optional functions, needed to implement a coherent transmitter, receiver, and laser (Type-2 only) are shown in Figure 2-1. An IC-TROSA that meets the objectives of the IA contains the functionality shown within the dashed line boxes in Figure 2-1 and the Control & Monitoring functionality as shown in Figure 2-3 or Figure 2-4 unless otherwise noted as optional.

An IC-TROSA shall provide at a minimum the following electro-optic functionality:

A. A Receive (RX) signal input fiber that shall be Single Mode Fiber (SMF).

B. Type-1 Package shall have a Laser Input fiber, split internally between Modulator and Local Oscillator (LO) functions. The Laser Input fiber shall be Polarization Maintaining Single Mode Fiber (PM-SMF).

C. A Type-2 Package will not have a Laser Input fiber. The Laser function is integrated inside the Type-2 Package.

D. A Transmit (TX) signal output fiber that shall be Single Mode Fiber (SMF)

E. A polarization splitting element, separating the RX light into two orthogonal polarizations, with each polarization delivered to a 90 degree hybrid mixer.

F. A polarization maintaining power splitter or polarization splitting element, splitting the local oscillator input power equally and delivering it to the two 90 degree hybrid mixers.

G. Two (2) 90 degree hybrid mixers with differential optical outputs.

H. Eight (8) photo-detectors comprised of 4 sets of differential detectors.

I. Four (4) linear trans-impedance amplifiers providing differential RF output signals [RX-XI, RX-XQ, RX-YI, RX-YQ] from the receiver.

J. A polarization maintaining power splitter or polarization splitting element, splitting the Laser input power equally and delivering it to the two pair of nested Mach-Zehnder modulators.

K. Four (4) nested Mach-Zehnder modulators

L. Four (4) linear high bandwidth modulator driver amplifiers with differential input signals [TX-XI, TX-XQ, TX-YI, TX-YQ] to the transmitter.

M. An integrated control and Management Interface as described in Section 11.

N. An IC-TROSA *may* also contain the following optical functionality:

O. Optical power tap(s) and monitor photodiode(s) in the RX input path either before the polarization splitting element or in each path after the splitting element. This IA does not prohibit the use of additional taps and monitor photodiodes within the IC-TROSA for control, monitoring, or vendor specific functions.

P. A variable optical attenuator in the Signal input path either before the polarization splitting element or in each path after the splitting element.

Q. X (X-Pol) and Y (Y-Pol) indicate a pair of mutually orthogonal polarizations of any orientation, and I and Q are mutually orthogonal phase channels in each polarization. The IC-TROSA, therefore, has 4x polarization-phase differential RF input channels labeled as TX-XI, TX-XQ, TX-YI, TX-YQ for the transmitter and 4x polarization-phase differential RF output channels labeled as RX-XI, RX-XQ, RX-YI, RX-YQ from the receiver.

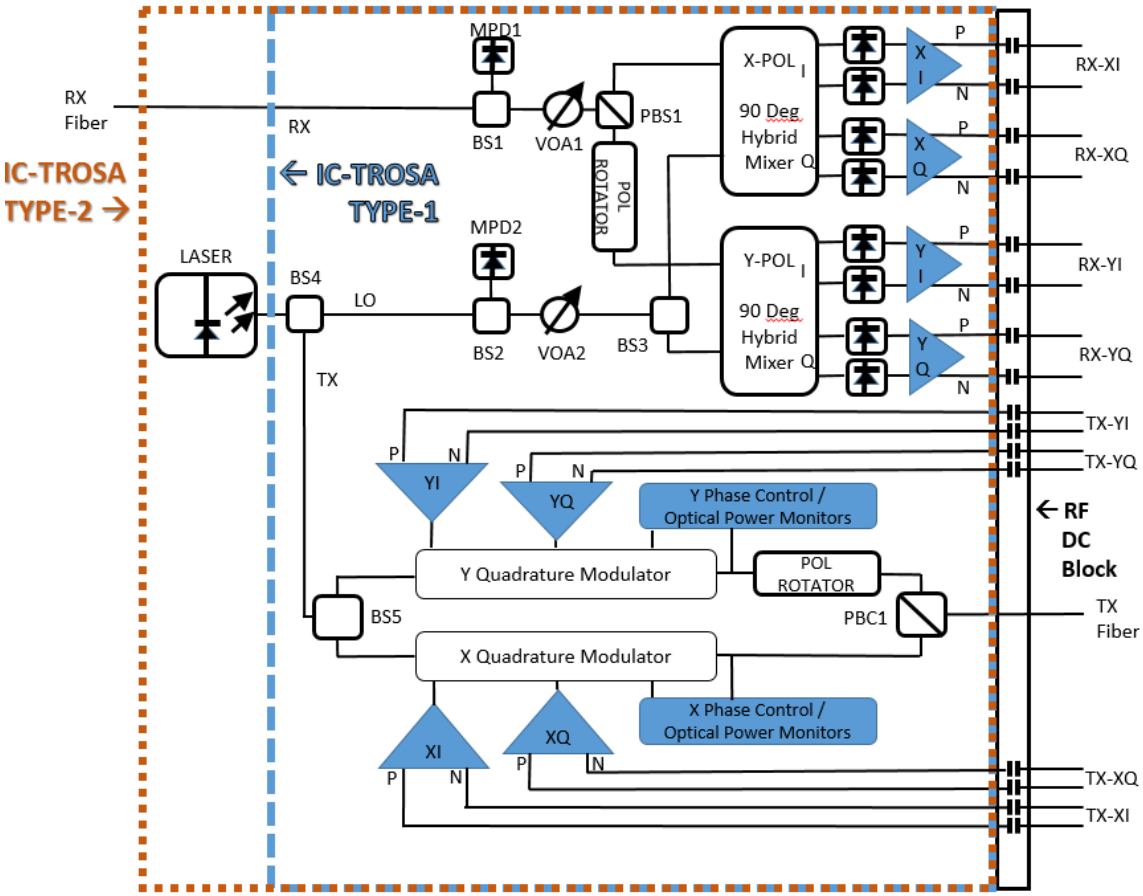


Figure 2-1: IC-TROSA Electro-Optic Functional Reference Diagram Including Optional Components

Notes:

1. DC blocking capacitors for high speed TX and RX data lines are optionally located inside or outside the package.
2. IC-TROSA Type-1 does not have an integrated Laser source.
3. VOAs and MPDs represent general power control functions with optional locations. Other VOA and MPD locations as well as additional VOAs and MPDs are acceptable.
4. The area enclosed by the long dashed lines indicate the Type-1 Package functionality.
5. The area enclosed by the short dashed lines indicate the Type-2 Package functionality.
6. The area enclosed by the solid lines indicate the DC blocking capacitors.
7. The SOAs in the TX path are optional.

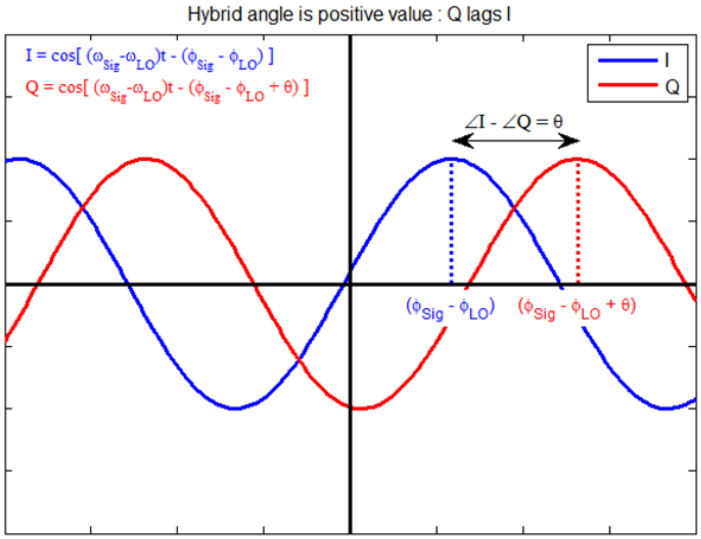


Figure 2-2: Coherent Detection I-Q Phase Relationship

The phase relationship between I and Q outputs is established by the heterodyne technique with the frequency of the Signal input to the receiver greater than the frequency of the LO input. Under this condition, when the I and Q output waveforms are observed in the time domain, the Q channel lags the I Channel by nominally +90 degrees, as shown in Figure 2-2.

Channel outputs 'p' and 'n' are the complementary outputs for each polarization-phase channel and are defined such that the output voltage for 'p' increases as the RX and Local Oscillator approach the in-phase condition to form constructive interference, and the output voltage for 'n' decreases under the same conditions.

The TIAs in the receiver function enable multiple signal monitors and control methods. The most notable TIA control selection is between automatic or manual gain control operating mode (AGC or MGC). TIAs can support: AGC only, MGC only, or both. All are valid implementations. The TIAs may also facilitate a bandwidth equalization function and provide various input signal strength and/or output level monitors (PI). In the AGC operating mode there is a RF output level adjust control (Output Adjust, OA) available and in the MGC operating mode an external signal (Gain Adjust, GA) is used to control the gain of each differential amplifier.

The IC-TROSA also comprises a modulation function employing a Polarization Multiplexed-Quadrature Modulator or PM-Q Modulator at the transmitter. Each quadrature modulator typically comprises of two inner nested Mach-Zehnder modulators with bias control, a 90º phase shifter in the outer modulator with phase control, and an output power monitoring output. Any implementation or technology choices may be used to realize this basic functionality. This modulator function also includes linear RF driver

amplifiers for each of the four modulator stages TX-XI, TX-XQ, TX-YI, TX-YQ as shown in Figure 2-1.

The optical power from a narrow line width laser source is divided into two parts with a beam splitter (BS) and each part is independently modulated by a quadrature modulator. The Y modulator output has its polarization rotated 90º by the polarization rotator creating a polarization state orthogonal to the X modulator. The resulting X and Y modulated signals are then combined with a polarization beam combiner and output through an optical output ("TX") fiber. The power in each of the two polarizations is independently monitored with photodiodes.

As indicated in Figure 2-1, the PM-Q Modulator function includes the following basic components:

a) One optical Laser Input fiber (internal laser in the case of Type-2 package)
b) One optical power splitter
c) Four linear modulator driver amplifiers
d) Two independent quadrature modulators
e) Two independent monitoring photodiodes
f) One polarization multiplexer including polarization rotator and combiner
g) One optical Transmit "TX" output

The following interfaces are specified for the PM-Q modulator function:

a) One optical Transmit fiber (TX)
b) Four high-speed data interfaces
c) Four modulator bias control interfaces
d) Two phase control interfaces
e) Two power monitoring interfaces

The two polarized signal components in the output are referred to as "X" and "Y", and the quadrature modulators that encode information onto the polarization components are correspondingly referred to as X and Y modulators. Each quadrature modulator is driven by an "I" and a "Q" data signal. The four high-speed data interfaces are referred to as TX-XI, TX-XQ, TX-YI and TX-YQ.

Each of the four data modulators needs to be biased with a suitable DC voltage. This IA specifies biasing as being an IC-TROSA internal design function supporting both single-ended as well as push-pull biasing. No external bias contacts are provided. The I and Q phase offset is controlled via vendor proprietary internal control algorithms executed and monitored by the IC-TROSA micro controller. External phase control pins are not provided. The phase offset between I and Q in X and Y arms is controlled by phase control interfaces *X* Phase and *Y* Phase respectively.

I and Q are established by the heterodyne technique, with the frequency of the RX input to the receiver greater than the frequency of the LO input. The I and Q channel outputs are measured in the time domain.

Under these conditions the RX Q channel phase lags by nominally +90 degrees the RX I channel phase, as shown in Figure 2-2.

2.2. Control and Monitoring Architecture

The control and monitoring functional blocks required to implement a Type-1 IC-TROSA are shown in Figure 2-3. The Type-2 configuration with integrated laser is shown in Figure 2-4. The primary interfaces are: power supplies, digital communications interface, dedicated alarm & control I/Os, high speed RF contacts for TX and RX I/Q data, and in case of Type-1 package an optical fiber interface to the laser. An IC-TROSA that meets the objectives of the IA contains the functionality shown within these two figures. The Type-2 IC-TROSA typically requires the use of one or more Thermo-Electric Coolers (TECs) inside the IC-TROSA package. In this case, the Type-2 requires one or more external TEC controller ICs located on the host PCB with several TEC power I/Os mating the TEC controller with the IC-TROSA. The IC-TROSA Alarm & Control I/Os provide a TEC_EN function which may be used by the IC-TROSA's micro controller to enable or disable the external TEC Controllers. The I/Os required for TEC control are listed and described in detail in the Low Speed Electrical I/O and the Dedicated Alarm & Control I/O sections of this document.

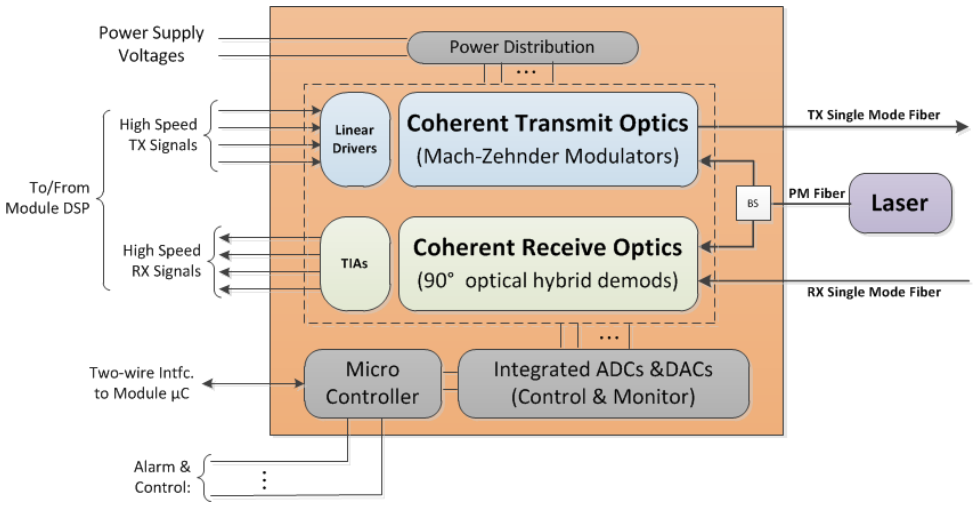


Figure 2-3: Type-1 Control & Monitoring Functional Diagram

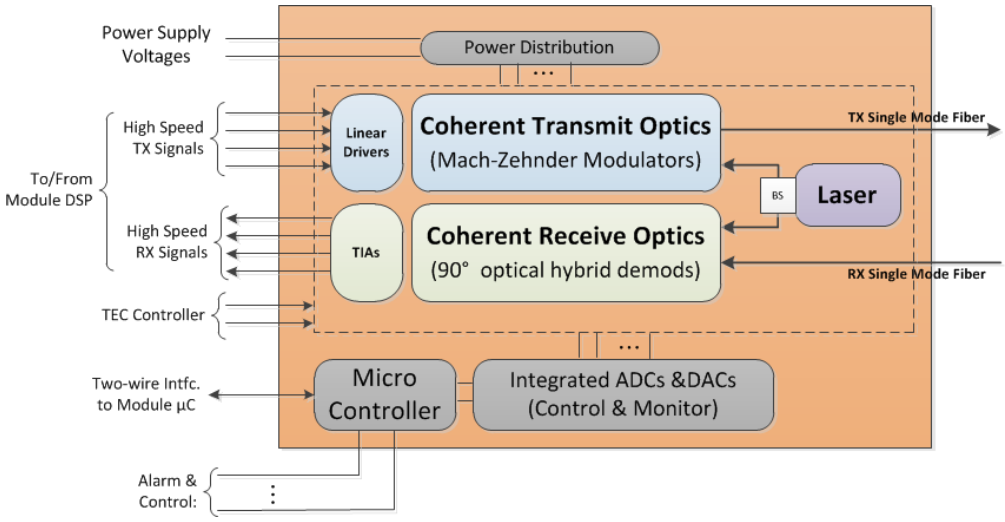


Figure 2-4: Type-2 Control & Monitoring Functional Diagram

3. Power Supply Architecture

3.1. Overview

Power supplies for the IC-TROSA are all located external to the IC-TROSA package and are described in

Table 3-1. Proper Initialization and Reset of an IC-TROSA requires the host board or module to have on/off control over all the IC-TROSA primary and secondary power supplies. By definition the IC-TROSA does not have the capability of enabling/disabling its own power supplies. Device initialization is described below.

The primary power supply (P0) is a nominal +3.3V DC supply. This primary supply is the first to be activated on the IC-TROSA for the purpose of initializing the IC-TROSA's internal micro controller, alarm and control logic, and management interface. IC-TROSA's highly integrated structure requires multiple vendor specific voltage levels. To achieve a multi-vendor implementation agreement, the IC-TROSA IA specifies a number of vendor defined power supplies. An implementation of IC-TROSA does not require the use of all these supplies. However, to ensure a host PCB is 100% compatible with all possible vendor implementations it may be required for the host PCB to have all supplies available. In addition to the single "Primary" power supply P0 the IC-TROSA requires multiple vendor defined "Secondary" power supplies (P1, P2, P3, P4, P5, and P6). Upon device start-up, the external host controller has the responsibility for querying the IC-TROSA, through the management interface, for the proper setting and sequencing of each secondary supply. The I/O mapping of all IC-TROSA power supplies are listed within the Low Speed Electrical Interface section of this document.

3.2. Primary Supply (P0)

The primary power supply P0 is a nominal +3.3V DC "Narrow Range" supply as defined by JEDEC specification JESD8C.01 revision September 2007. This supply is the first to be activated on the IC-TROSA for the purpose of initializing the IC-TROSA's internal logic controller and management interface into the Low Power Mode.

3.3. Secondary Supplies (P1, P2, P3, P4, P5, P6)

The several secondary supplies offer both positive and negative DC voltage ranges. The power supply turn-up sequencing is an important feature of the IC-TROSA to avoid potential damage to internal components. Vendor specific voltage level and sequencing information for the secondary supplies are contained within the C000h area of the management interface register map. Upon device start-up, after primary supply has been activated and stabilized, the host module micro controller has the responsibility of querying the IC-TROSA for secondary power supply information and applying to the IC-TROSA package the correct nominal voltage values and sequencing for each secondary supply. Therefore, vendors should avoid ganging the P0 primary supply contacts for high power functions such as TX and RX. Achieving low power mode requires secondary power supplies to be disabled without disabling P0 primary supply.

The “Voltage Range” in Table 3-1 are the specified ranges for the nominal voltages required to meet the intent of this IA. For Secondary supply specifications the IC-TROSA vendor shall provide the customer with a min, nominal, and max specification for each supply setting. A vendor seeking to be compliant with this IA is not required to use secondary supplies, but they are required to adhere to the allowable voltage ranges when they are utilized. Otherwise ganging of secondary supplies with other secondary supplies having same nominal voltage set points is allowed within this IA. However, to allow end users of an IC-TROSA to have a multi-vendor capability on the host design, the vendor should not require ganging of secondary power supplies on the host side. Secondary power supply ganging shall be achieved internal to the IC-TROSA.

Table 3-1: Power Supply Requirements

Package Style	Symbol	Vendor Specified Nominal Voltage Range	Voltage Range [1]		
			Min	Nom	Max
Type-1	P0+	+3.3 [2]	3.15	3.3	3.45
	P1+	0 to +12	VS	VS	VS
	P2-	0 to -12	VS	VS	VS
	P3+	0 to +12	VS	VS	VS
	P4-	0 to -12	VS	VS	VS
	P5+	0 to +12	VS	VS	VS
	P6+	0 to +12	VS	VS	VS
Type-2	P0+	+3.3	3.15	3.3	3.45
	P1+	0 to +12	VS	VS	VS
	P2-	0 to -12	VS	VS	VS
	P3+	0 to +12	VS	VS	VS
	P4-	0 to -12	VS	VS	VS
	P5+	0 to +18	VS	VS	VS
	P6+	0 to +12	VS	VS	VS

Notes:

1. VS = Vendor Specified voltage requirements
2. JEDEC “Narrow Range” specification JESD8C.01 revision September 2007

3.4. Low Power Mode

IC-TROSA Low Power Mode is specifically defined as having only the Primary 3.3V supply (P0) enabled. The host application shall determine if the IC-TROSA low power state is sufficiently low power by reading register “Maximum Power Consumption in Low Power Mode” 801Eh. “Low Power Mode” is the default steady state for IC-TROSA after the “Initialize” transient state. Refer to the IC-TROSA State Machine as shown in Figure 11-11. Should the Low Power Mode not provide sufficiently low power for the host application, the host may completely power down IC-TROSA by disabling all primary and secondary supplies according to the vendor specified power down sequence. For details on initiating Low Power Mode from a high power state refer to Section 11.7 and command sequencing in Figure 11-13.

4. High Speed Electrical Interface

4.1. Common Features

The basic structure of the high speed interface is the same for both IC-TROSA package styles. Only the package contact styles differ. The common features are shown in Table 4-1.

Table 4-1: High Speed Electrical Interface Common Features

Parameter	Value	Notes
Interface type	Differential	
Channel number	4 x TX 4 x RX	26 total RF I/Os including GNDs
Channel configuration	G-S-S-G	
RF Coupling	AC coupling	DC blocking capacitor locations are vendor specific and may be located internal or external to the IC-TROSA package.
Line impedance	100 Ohm Differential	Includes flex PCB for Type-2 packages
Channel pin-out	TX-XI TX-XQ TX-YI TX-YQ RX-XI RX-XQ RX-YI RX-YQ	
Differential pin-out	Signal Complimentary Signal	P N

4.2. Allowable RF Channel Mappings

IC-TROSA carries forward several optional RF channel mappings as defined in OIF-CFP2-ACO-01.0. All RF mappings shown in this IC-TROSA IA may be altered to adopt any of the allowable mappings in Figure 4-1.

Mapping	X:Y	I,Q	p/n	Notes
[0,x,x]	X:Y			Pol. ***cannot*** be interleaved
[1,x,x]	Y:X			
[x,0,x]		I,Q:I,Q		Same across Pol.
[x,1,x]		Q,I:Q,I		
[x,2,x]		I,Q:Q,I		Flip across Pol.
[x,3,x]		Q,I:I,Q		
[x,x,0]			p/n,p/n:p/n,p/n	Same across Pol. and I,Q
[x,x,1]			n/p,n/p:n/p,n/p	
[x,x,2]			p/n,p/n:n/p,n/p	Flip across Pol.
[x,x,3]			n/p,n/p:p/n,p/n	
[x,x,4]			p/n,n/p:p/n,n/p	Flip across I,Q
[x,x,5]			n/p,p/n:n/p,p/n	
[x,x,6]			p/n,n/p:n/p,p/n	Flip across Pol. and I,Q
[x,x,7]			n/p,p/n:p/n,n/p	

Figure 4-1: TX and RX RF Channel Mappings on the Electrical Interface

Note: For more detailed description of Channel Mapping table refer to OIF-CFP2-ACO-01.0.

4.3. High Speed Electrical Interface for Type-1 Form Factor

The high speed TX and RX electrical interfaces for a Type-1 IC-TROSA form-factor utilizes a 2D surface mount ball grid array in a G-S-S-G arrangement as shown in Figure 4-2. To reduce high speed channel skew between IC-TROSA and most common coherent DSP ball maps the TX and RX contacts are grouped in a single outer row. These high speed contacts are grouped by function and separated from the low speed contacts by a column of ground contacts to improve signal integrity. In order to keep IC-TROSA in the smallest possible form factor, the required RF DC decoupling capacitors for each of the high speed differential TX and RX data contacts are located outside the IC-TROSA on the host PCB for Type-1.

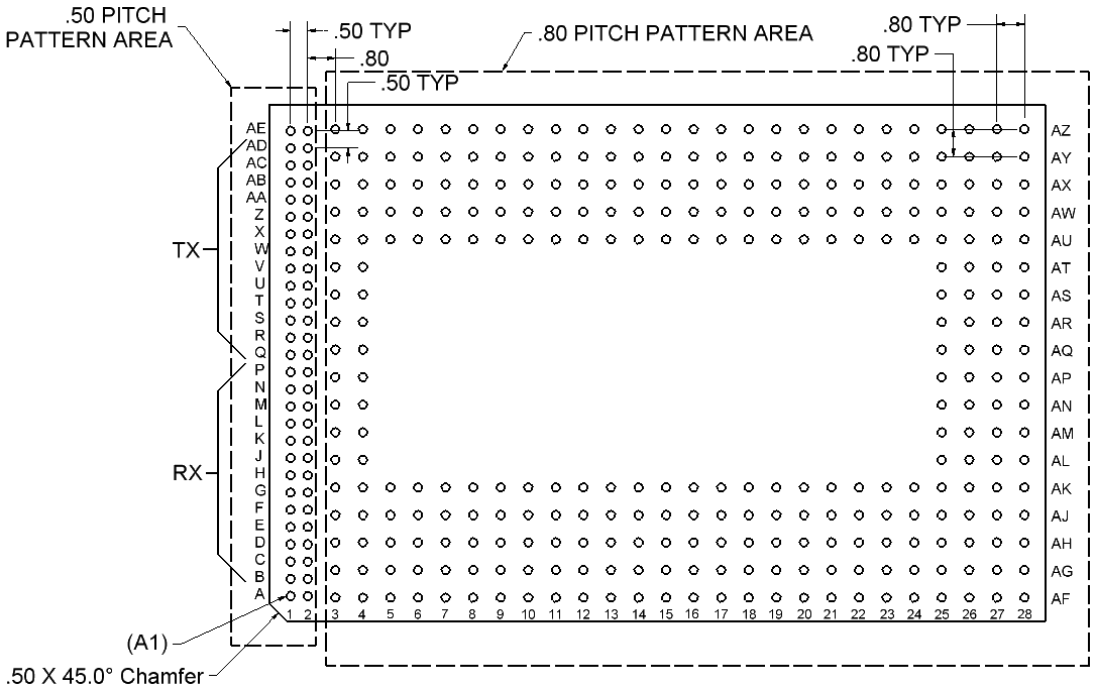


Figure 4-2: Type-1 Electrical Contact Map. Bottom View

Table 4-2: Type-1 High Speed Electrical I/O Functional Map

RX Contacts			TX Contacts			Isolation Grounds	
Ball	Function		Ball	Function		Ball	Function
A1	No Contact		Q1	GND		A2	No Contact
B1	GND		R1	TX-YQn		B2	GND
C1	RX-YQn		S1	TX-YQp		C2	GND
D1	RX-YQp		T1	GND		D2	GND
E1	GND		U1	TX-YIn		E2	GND
F1	RX-YIn		V1	TX-YIp		F2	GND
G1	RX-YIp		W1	GND		G2	GND
H1	GND		X1	TX-XQn		H2	GND
J1	RX-XQn		Z1	TX-XQp		J2	GND
K1	RX-XQp		AA1	GND		K2	GND
L1	GND		AB1	TX-XIn		L2	GND
M1	RX-XIn		AC1	TX-XIp		M2	GND
N1	RX-XIp		AD1	GND		N2	GND
P1	GND		AE1	No Contact		P2	GND
---	---		---	---		Q2	GND
---	---		---	---		R2	GND
---	---		---	---		S2	GND
---	---		---	---		T2	GND
---	---		---	---		U2	GND
---	---		---	---		V2	GND
---	---		---	---		W2	GND
---	---		---	---		X2	GND
---	---		---	---		Z2	GND
---	---		---	---		AA2	GND
---	---		---	---		AB2	GND
---	---		---	---		AC2	GND
---	---		---	---		AD2	GND
---	---		---	---		AE2	No Contact

4.4. High Speed Electrical Interface for Type-2 Mechanical Form Factor

The high speed electrical interface for the Type 2 form factor is realized using RF flexible PCB interfaces attached to the short side of the package body as shown in Figure 4-3 below. The opposite end of the RF flexible PCB interfaces are then used to connect the high speed signal lines to the host board. The flexible PCBs allow for a customized RF connection between a vendor-specific interface on the IC-TROSA package and a customer-specific interface on the host PCB.

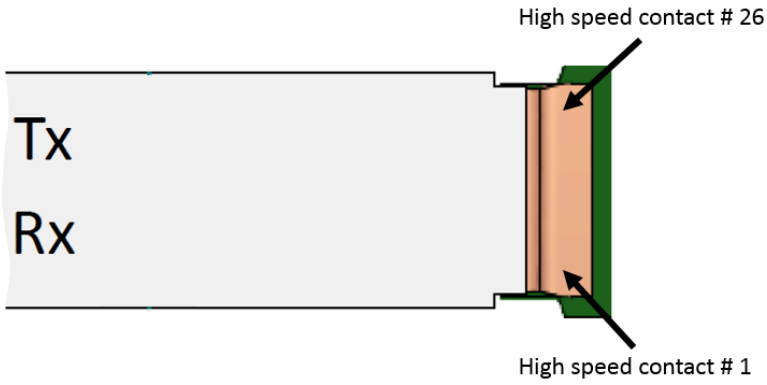


Figure 4-3: Type-2 High Speed Flex Interface Top View

Table 4-7: Type-2 High Speed Electrical I/O Map

RX Contacts			TX Contacts	
Contact #	Function		Contact#	Function
1	GND		14	GND
2	RX-YQn		15	TX-YQn
3	RX-YQp		16	TX-YQp
4	GND		17	GND
5	RX-YIn		18	TX-YIn
6	RX-YIp		19	TX-YIp
7	GND		20	GND
8	RX-XQn		21	TX-XQn
9	RX-XQp		22	TX-XQp
10	GND		23	GND
11	RX-XIn		24	TX-XIn
12	RX-XIp		25	TX-XIp
13	GND		26	GND

5. Dedicated Alarm & Control I/Os

5.1. Common Alarm & Control I/Os

A few dedicated hardware I/Os are allocated to critical functions and are applicable to both Type-1 and Type-2 packages. These critical functions require dedicated hardware I/O due to their reliance on fast response time or fail-safe requirements. Fail-safe are those I/Os which bypass the control firmware and directly initiate certain hardware functions. The Common Alarm & Control I/Os for both Type-1 and Type-2 IC-TROSA are shown in Table 5-1. Logic levels and timing requirements for two-wire interface lines TWI_SDA and TWI_SCL are specified in section 11 of this IA.

Table 5-1: Common Alarm & Control I/O Specification

Function	Type[1]	Description	Applicable IC-TROSA Form Factor	Assertive (Active) Level
TWI_SDA	Bi-directional	Two-wire Serial Data	Type 1 & 2	---
TWI_SCL	Bi-directional	Two-wire Serial Clock from bus Master	Type 1 & 2	---
TEC_EN	Output	Thermo-Electric Cooler Enable	Type-2	High
TECn_DMD (TEC_DEMAND)	Analog Output	Thermo-Electric Cooler current demand control signal	Type-2	Analog
RESET	Input	Reset controller	Type 1 & 2	Low
TX_DIS	Input	Transmit Disable	Type-1 & 2	Low
RX_LOS	Output	Receive Loss of Signal	Type 1 & 2	Low
INT_SRQ	Output	Interrupt/Service Request	Type 1 & 2	Low
MOD_SEL	Input	Module Select	Type 1 & 2	Low

Note:

1. Input/output designations are from IC-TROSA perspective.

5.2. Type-1 Alarm & Control I/O Configuration

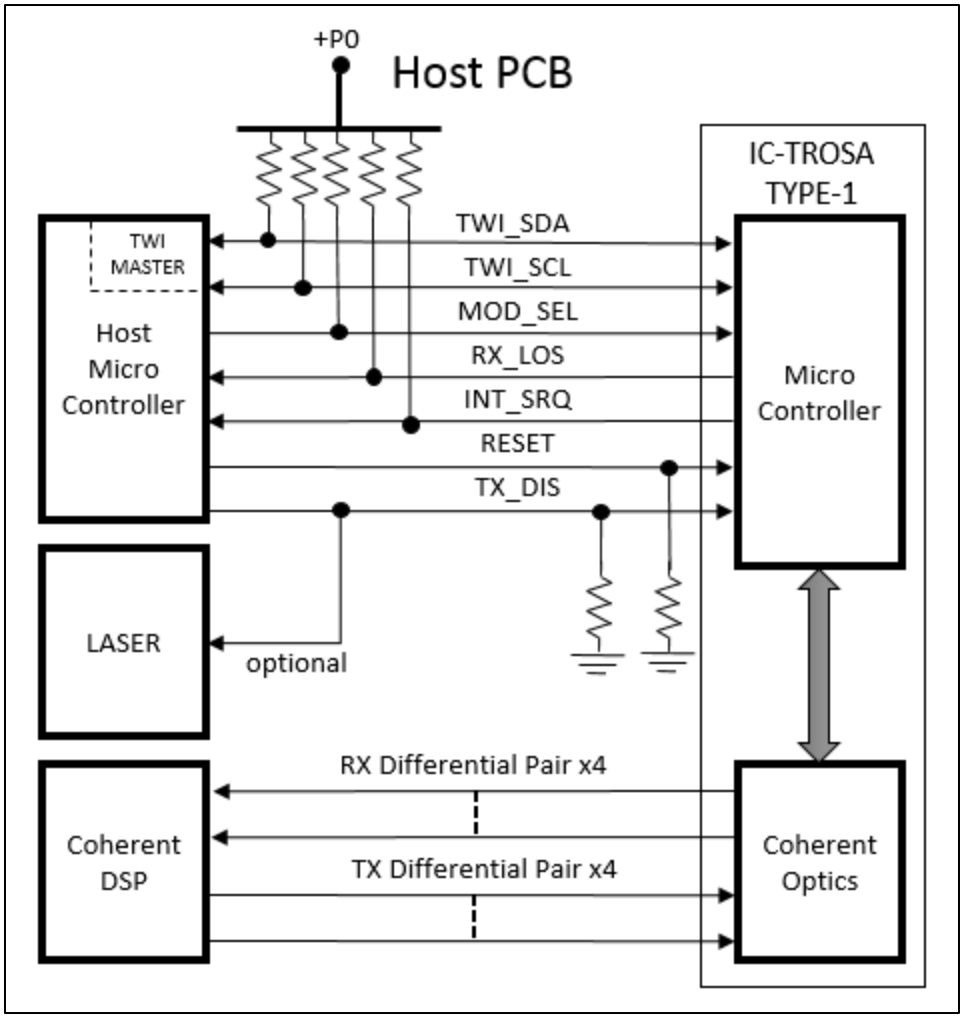


Figure 5-1: Type-1 Alarm & Control I/O Hardware Configuration

5.3. Type-2 Alarm & Control I/O Configuration

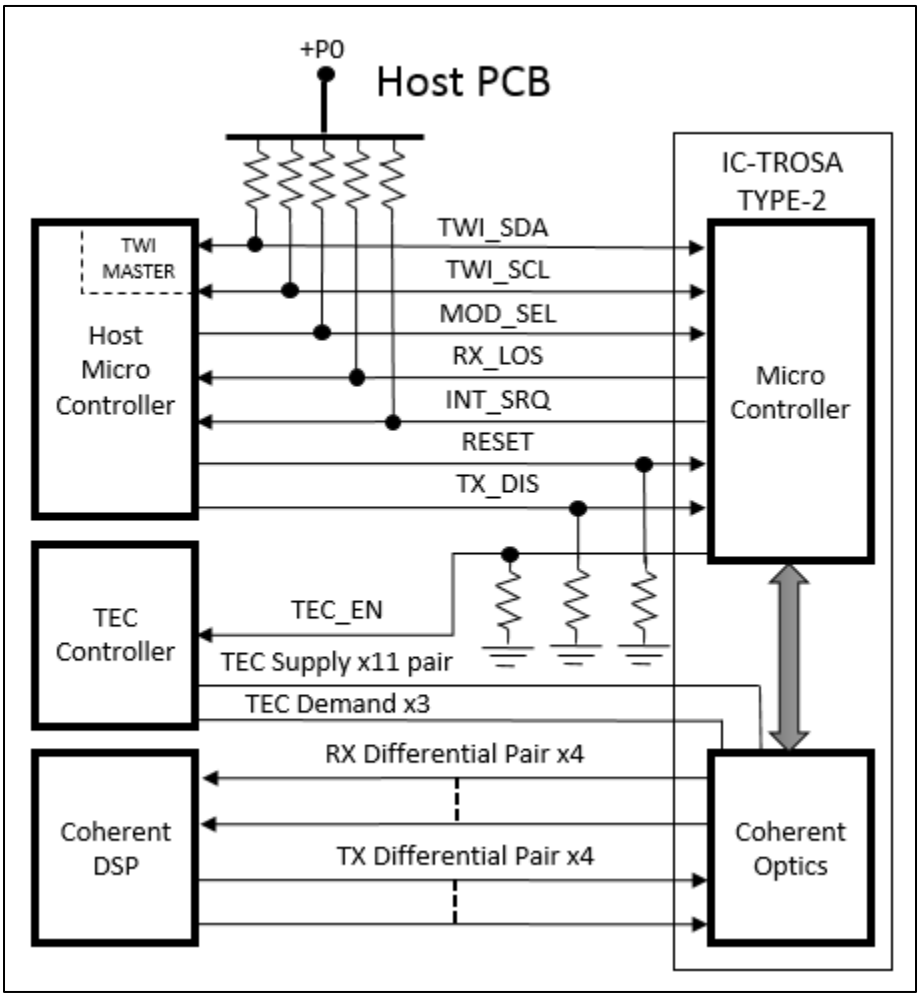


Figure 5-2: Type-2 Alarm & Control I/O Hardware Configuration

5.4. Alarm & Control Detailed Descriptions

5.4.1. TEC_EN (Thermo-Electric Cooler Enable)

TEC_EN is an active high output control signal used only for a Type-2 IC-TROSA. It functions as an enable/disable control signal to one or more thermo-electric cooler controllers located external to the IC-TROSA. A high level on the TEC_EN I/O will enable the TEC controller. A logical low on this I/O will disable the TEC controller and shut off all current to the IC-TROSA internal TECs. This control signal may be used to create a low power mode. The TEC_EN I/O has a pull-down resistor to electrical ground. Upon start-up and/or RESET conditions, and prior to the IC-TROSA internal controller being fully ready, the IC-TROSA TEC_EN I/O is held in a low state disabling all TEC controllers.

5.4.2. RESET

RESET is an active low input control to the IC_TROSA. It applies to both Type-1 and Type-2 package designs. The RESET I/O is used to reset the IC-TROSA internal logic controller and management interface. It is, in effect, a processor or controller reset only. RESET has a pull-down resistor to ground. Upon host module power-up, RESET effectively holds the IC-TROSA in RESET mode until the host controller sets RESET high enabling the IC-TROSA internal controller. After a RESET the IC-TROSA controller returns all IC-TROSA settings to the default state. Holding RESET low prevents the internal controller from performing its boot-up sequence. Reset events are recorded in "Initialize State Latch" B022h.0

5.4.3. TECn_DMD (Thermo-Electric Cooler Demand)

The TECn_DMD I/O is an output from the IC-TROSA. It is intended to drive a power amplifier which supplies current back to the TEC in a closed loop temperature control scheme. The loop function and loop bandwidth control is most likely provided by the microprocessor in the IC-TROSA in the form of a PID (Proportional-Integral-Derivative) controller. Up to n=three TECn DMD terminals are provided for IC-TROSA applications requiring multiple temperature controlled zones.

The TEC DMD output has a voltage range from 0V to 2.5V full scale. It is intended to drive a high impedance (>5k ohms) input so that no further circuits are required to interface it to the control input of the power amplifier. The maximum current drawn from the TEC demand pin should be <5mA end-of-life, over temperature (EOLOT). The TEC Demand output is configured such that 0V represents maximum cooling of the TEC top plate. Then 2.5V represents maximum heating. The balance point, no heating or cooling, is set at 1.25V mid-range. Using these voltages the circuits can be configured using readily available DAC and voltage reference circuits. The TEC DMD output signal should be monotonic with increasing input signal.

The TEC power amplifier is placed remotely to the IC-TROSA to avoid problems associated with noise in the case of a switching design or heatsinking in the case of a linear design. It should accept the TEC demand signal on a high impedance input pin and produce a proportional output suitable to drive the TEC. The TEC power amplifier may be a discrete circuit implementation or an integrated (e.g. components encapsulated in a sub-package) solution. In order to realize a practical circuit implementation the power amplifier may limit the maximum cool condition to a voltage slightly above 0V (example: 100mV) to avoid any problems associated with noise. TEC power amplifier may be a noise source for the lasers. At present the TEC power amplifier noise requirement is not specified and is vendor dependent and the host shall provide a variable power supply that is as clean as possible.

5.4.4. TX_DIS (Transmit Disable)

TX_DIS is an active low control I/O used to disable light transmission from the IC-TROSA TX port. TX_DIS has a pull-down resistor to ground. During IC-TROSA power-up and RESET this TX_DIS is held low effectively shutting down TX transmissions from the IC-TROSA TX port. TX_DIS is an input I/O on both Type-1 and Type-2 packages. For Type-1 IC-TROSA it is optional to have the IC-TROSA control optical output power to the IC-TROSA TX port. In this case, the TX_DIS line is not required to be tied to the Laser's TX_DIS input, but the host must power up IC-TROSA before power-up & power-down of the laser. For a Type-2 IC-TROSA containing an integrated Laser, this I/O is an active low input control I/O from the host controller. A low state on the TX_DIS line will disable transmissions through TX output port.

5.4.5. RX_LOS (Receive Loss of Signal)

RX_LOS is an active low output I/O on both Type-1 and Type-2 IC-TROSA. RX_LOS indicates a receiver loss of signal condition as defined by a user defined minimum receive power level stored in the management interface settings. RX_LOS is pulled high to P0 primary supply by a pull-up resistor. A low level on RX_LOS indicates the input receive signal is below the user defined threshold.

5.4.6. INT_SRQ (Interrupt / Service Request)

INT_SRQ is an active low output I/O for both Type-1 and Type-2 IC-TROSA. INT_SRQ is used by the IC-TROSA to indicate a fault or alarm condition to the host controller. A high level on INT_SRQ indicates no alarm or fault present. A low level indicates the presence of a fault or alarm condition requiring the host to query the IC-TROSA management interface alarm registers to determine the source(s) of the status request. INT_SRQ is pulled high by a pull-up resistor to P0 primary power supply.

5.4.7. MOD_SEL (Module Select)

MOD_SEL is an active low input control I/O to both Type-1 and Type-2 IC-TROSA. MOD_SEL serves as a module select control to be used in conjunction with the Two-wire interface. MOD_SEL allows multiple IC-TROSA modules to co-exist on a single two-wire interface bus under the control of a single host controller. MOD_SEL has a pull-up resistor to the P0 primary power supply disabling two-wire communication responses from IC-TROSA until its internal controller has indicated a "Ready" status by setting INT_SRQ low to indicate IC-TROSA has completed a power reset. With MOD_SEL held high the IC-TROSA shall not respond to or acknowledge any Two-wire communications from the host controller. Also, MOD_SEL shall not change during any Two-wire interface transaction.

5.4.8. Implementing Monitor Tick Source in IC-TROSA

IC-TROSA does not have a dedicated hardware I/O for capturing PM Tick Source (Performance Monitor Tick Source) signals as described in CFP MSA Hardware Specification Revision 1.4. However, IC-TROSA does support CFP-MSA-Management Interface Specification 2.6 r06a registers used for Tick Source

configuration, timing, and latching and in addition it provides an "External Soft PM Interval Sync" bit within register C02Eh bit 15 which can be asserted by the external application host controller through the IC-TROSA TWI. Additionally, a Vendor Specific hardware I/O may optionally be mapped to the "External Soft PM Interval Sync" bit in order to provide a PM Tick Source hardware input. This I/O mapping is an optional feature and the implementation is vendor specific. Mapping of Vendor Specific I/Os are located in the Vendor Specific area of the IC-TROSA register map.

5.5. Alarm & Control I/O Electrical Requirements

Table 5-2: Alarm & Control I/O Electrical Requirements

Function	Logic	Sym	Vmin[1]	Vmax[1]	Condition
TECn_DMD	Analog		0V	+2.5V	+1.25V is zero current demand reference voltage
TEC_EN	LVCMOS	VOL VOH VIL VIH	--- [2]P0min-0.2V -0.3V +2V	+0.2V --- +0.8V [2]P0max+0.3V	4.7k-10k Ω Pull-down to GND
RESET	LVCMOS				4.7k-10k Ω Pull-down to GND
TX_DIS	LVCMOS				4.7k-10k Ω Pull-down to GND
RX_LOS	LVCMOS				4.7k-10k Ω Pull-up to +P0
INT_SRQ	LVCMOS				4.7k-10k Ω Pull-up to +P0
MOD_SEL	LVCMOS				4.7k-10kΩ Pull-up to +P0

Notes:

1. +3.3V LVCMOS logic levels from JEDEC specification JESD8C.01 revision September 2007
2. P0 is a reference to the IC-TROSA P0+ Power Supply used for all logic functions and communications.

5.6. Alarm & Control I/O Timing Requirements

Table 5-3: Alarm & Control I/O Timing Requirements

Function	Symbol	Min	Max	Units	Conditions
TWI_SDA	See section 11 for TWI timing requirements				
TWI_SCL	See section 11 for TWI timing requirements				
TEC_EN Assert			100	ms	Time from TEC_EN control bit assert to TEC_EN pin asserted
TEC_EN De-assert			100	ms	Time from TEC_EN control bit de-assert to TEC_EN pin de-assert
RESET Assert			2.5	sec	Module Initialization time from RESET
RESET De-assert			---	---	Not specified
TX_DIS Assert			100	μs	Application specific
TX_DIS De-assert			20	ms	Time from Tx Disable pin De-asserted until IC-TROSA enters the Tx-Turn-on State
RX_LOS Assert			150	ms	Time from hardware RX_LOS pin asserted to RX_LOS Pin State asserted.
RX_LOS De-Assert			150	ms	Time from hardware RX_LOS pin de-asserted to RX_LOS Pin State de-asserted.
INT_SRQ Assert			150	ms	Time from any condition of FAWS alarm/status state to INT_SRQ asserted.
INT_SRQ De-assert			150	ms	Time from last FAWS condition cleared to INT_SRQ de-asserted.
MOD_SEL	See Table 11-2 for MOD_SEL timing requirements related to operation with TWI				

6. Low Speed Electrical Interface

6.1. Low Speed Electrical Interface for Type-1 Form Factor

The low speed electrical connections for the Type-1 form factor are located on the bottom side of the package and form part of the 2D array of contacts as already shown in Figure 4-2. Note that for solder reflow mounting method the unused contacts on the interface are required to be present. Removing unused contacts may cause an imbalance in the package during the mounting process resulting in poor contact or misalignment. When using the solderless mechanical mounting method it is recommended to remove all unnecessary and unused contacts between the Type-1 IC-TROSA and the electrical interposer as the required compression force is directly proportional to the number of contacts.

The electrical interface functionality is shown pictorially as a 2D ball map in Figure 6-1 and specified in Table 6-1.

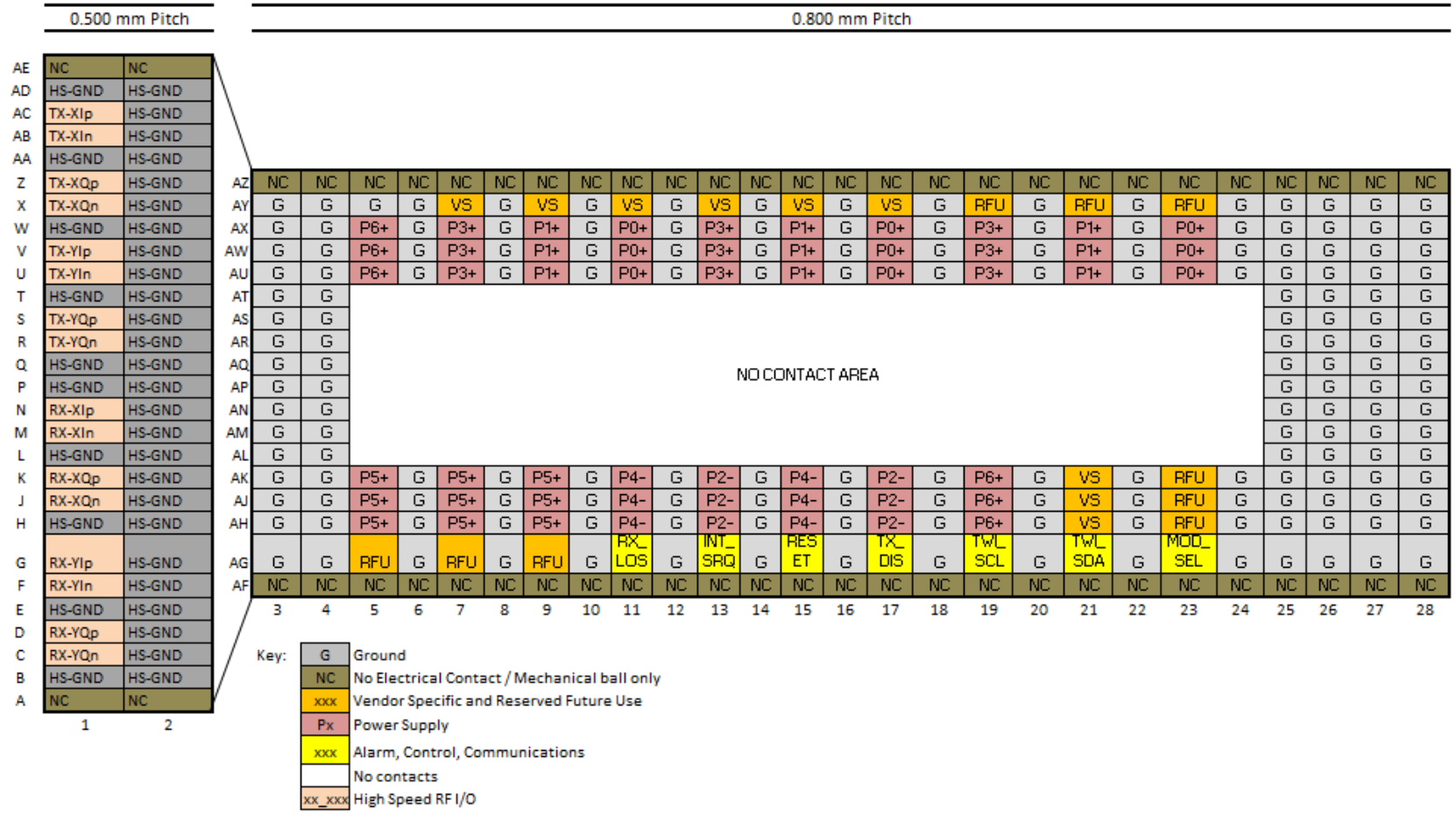


Figure 6-1: Type-1 I/O Contact Map (Package Bottom View)

Table 6-1: Type-1 Low Speed I/O Contact Map

Item #	Contact	Symbol	Description
1	AF3	NC	Mech. contact/ no connection
2	AG3	GND	Ground
3	AH3	GND	Ground
4	AJ3	GND	Ground
5	AK3	GND	Ground
6	AL3	GND	Ground
7	AM3	GND	Ground
8	AN3	GND	Ground
9	AP3	GND	Ground
10	AQ3	GND	Ground
11	AR3	GND	Ground
12	AS3	GND	Ground
13	AT3	GND	Ground
14	AU3	GND	Ground
15	AW3	GND	Ground
16	AX3	GND	Ground
17	AY3	GND	Ground
18	AZ3	NC	Mech. contact/ no connection
19	AF4	NC	Mech. contact/ no connection
20	AG4	GND	Ground
21	AH4	GND	Ground
22	AJ4	GND	Ground
23	AK4	GND	Ground
24	AL4	GND	Ground
25	AM4	GND	Ground
26	AN4	GND	Ground
27	AP4	GND	Ground
28	AQ4	GND	Ground
29	AR4	GND	Ground
30	AS4	GND	Ground
31	AT4	GND	Ground
32	AU4	GND	Ground
33	AW4	GND	Ground
34	AX4	GND	Ground
35	AY4	GND	Ground
36	AZ4	NC	Mech. contact/ no connection
37	AF5	NC	Mech. contact/ no connection
38	AG5	RFU	Reserved for future OIF use
39	AH5	P5+	P5 Power Supply
40	AJ5	P5+	P5 Power Supply
41	AK5	P5+	P5 Power Supply
42	AL5	---	No contact area
43	AM5	---	No contact area
44	AN5	---	No contact area
45	AP5	---	No contact area
46	AQ5	---	No contact area
47	AR5	---	No contact area
48	AS5	---	No contact area

Item #	Contact	Symbol	Description
49	AT5	---	No contact area
50	AU5	P6+	P6 Power Supply
51	AW5	P6+	P6 Power Supply
52	AX5	P6+	P6 Power Supply
53	AY5	GND	Ground
54	AZ5	NC	Mech. contact/ no connection
55	AF6	NC	Mech. contact/ no connection
56	AG6	GND	Ground
57	AH6	GND	Ground
58	AJ6	GND	Ground
59	AK6	GND	Ground
60	AL6	---	No contact area
61	AM6	---	No contact area
62	AN6	---	No contact area
63	AP6	---	No contact area
64	AQ6	---	No contact area
65	AR6	---	No contact area
66	AS6	---	No contact area
67	AT6	---	No contact area
68	AU6	GND	Ground
69	AW6	GND	Ground
70	AX6	GND	Ground
71	AY6	GND	Ground
72	AZ6	NC	Mech. contact/ no connection
73	AF7	NC	Mech. contact/ no connection
74	AG7	RFU	Reserved for future OIF use
75	AH7	P5+	P5 Power Supply
76	AJ7	P5+	P5 Power Supply
77	AK7	P5+	P5 Power Supply
78	AL7	---	No contact area
79	AM7	---	No contact area
80	AN7	---	No contact area
81	AP7	---	No contact area
82	AQ7	---	No contact area
83	AR7	---	No contact area
84	AS7	---	No contact area
85	AT7	---	No contact area
86	AU7	P3+	P3 Power Supply
87	AW7	P3+	P3 Power Supply
88	AX7	P3+	P3 Power Supply
89	AY7	VS	Vendor Specific
90	AZ7	NC	Mech. contact/ no connection
91	AF8	NC	Mech. contact/ no connection
92	AG8	GND	Ground
93	AH8	GND	Ground
94	AJ8	GND	Ground
95	AK8	GND	Ground
96	AL8	---	No contact area
97	AM8	---	No contact area
98	AN8	---	No contact area
99	AP8	---	No contact area

Item #	Contact	Symbol	Description
100	AQ8	---	No contact area
101	AR8	---	No contact area
102	AS8	---	No contact area
103	AT8	---	No contact area
104	AU8	GND	Ground
105	AW8	GND	Ground
106	AX8	GND	Ground
107	AY8	GND	Ground
108	AZ8	NC	Mech. contact/ no connection
109	AF9	NC	Mech. contact/ no connection
110	AG9	RFU	Reserved for future OIF use
111	AH9	P5+	P5 Power supply
112	AJ9	P5+	P5 Power supply
113	AK9	P5+	P5 Power supply
114	AL9	---	No contact area
115	AM9	---	No contact area
116	AN9	---	No contact area
117	AP9	---	No contact area
118	AQ9	---	No contact area
119	AR9	---	No contact area
120	AS9	---	No contact area
121	AT9	---	No contact area
122	AU9	P1+	P1 Power supply
123	AW9	P1+	P1 Power supply
124	AX9	P1+	P1 Power supply
125	AY9	VS	Vendor specific
126	AZ9	NC	Mech. contact/ no connection
127	AF10	NC	Mech. contact/ no connection
128	AG10	GND	Ground
129	AH10	GND	Ground
130	AJ10	GND	Ground
131	AK10	GND	Ground
132	AL10	---	No contact area
133	AM10	---	No contact area
134	AN10	---	No contact area
135	AP10	---	No contact area
136	AQ10	---	No contact area
137	AR10	---	No contact area
138	AS10	---	No contact area
139	AT10	---	No contact area
140	AU10	GND	Ground
141	AW10	GND	Ground
142	AX10	GND	Ground
143	AY10	GND	Ground
144	AZ10	NC	Mech. contact/ no connection
145	AF11	NC	Mech. contact/ no connection
146	AG11	RX_LOS	Receiver loss of signal
147	AH11	P4-	P4 Power supply
148	AJ11	P4-	P4 Power supply
149	AK11	P4-	P4 Power supply
150	AL11	---	No contact area

Item #	Contact	Symbol	Description
151	AM11	---	No contact area
152	AN11	---	No contact area
153	AP11	---	No contact area
154	AQ11	---	No contact area
155	AR11	---	No contact area
156	AS11	---	No contact area
157	AT11	---	No contact area
158	AU11	P0+	P0 Primary power supply
159	AW11	P0+	P0 Primary power supply
160	AX11	P0+	P0 Primary power supply
161	AY11	VS	Vendor specific
162	AZ11	NC	Mech. contact/ no connection
163	AF12	NC	Mech. contact/ no connection
164	AG12	GND	Ground
165	AH12	GND	Ground
166	AJ12	GND	Ground
167	AK12	GND	Ground
168	AL12	---	No contact area
169	AM12	---	No contact area
170	AN12	---	No contact area
171	AP12	---	No contact area
172	AQ12	---	No contact area
173	AR12	---	No contact area
174	AS12	---	No contact area
175	AT12	---	No contact area
176	AU12	GND	Ground
177	AW12	GND	Ground
178	AX12	GND	Ground
179	AY12	GND	Ground
180	AZ12	NC	Mech. contact/ no connection
181	AF13	NC	Mech. contact/ no connection
182	AG13	INT_SRQ	Interrupt / Status request
183	AH13	P2-	P2 Power supply
184	AJ13	P2-	P2 Power supply
185	AK13	P2-	P2 Power supply
186	AL13	---	No contact area
187	AM13	---	No contact area
188	AN13	---	No contact area
189	AP13	---	No contact area
190	AQ13	---	No contact area
191	AR13	---	No contact area
192	AS13	---	No contact area
193	AT13	---	No contact area
194	AU13	P3+	P3 Power supply
195	AW13	P3+	P3 Power supply
196	AX13	P3+	P3 Power supply
197	AY13	VS	Vendor specific
198	AZ13	NC	Mech. contact/ no connection
199	AF14	NC	Mech. contact/ no connection
200	AG14	GND	Ground
201	AH14	GND	Ground

Item #	Contact	Symbol	Description
202	AJ14	GND	Ground
203	AK14	GND	Ground
204	AL14	---	No contact area
205	AM14	---	No contact area
206	AN14	---	No contact area
207	AP14	---	No contact area
208	AQ14	---	No contact area
209	AR14	---	No contact area
210	AS14	---	No contact area
211	AT14	---	No contact area
212	AU14	GND	Ground
213	AW14	GND	Ground
214	AX14	GND	Ground
215	AY14	GND	Ground
216	AZ14	NC	Mech. contact/ no connection
217	AF15	NC	Mech. contact/ no connection
218	AG15	RESET	RESET
219	AH15	P4-	P4 Power supply
220	AJ15	P4-	P4 Power supply
221	AK15	P4-	P4 Power supply
222	AL15	---	No contact area
223	AM15	---	No contact area
224	AN15	---	No contact area
225	AP15	---	No contact area
226	AQ15	---	No contact area
227	AR15	---	No contact area
228	AS15	---	No contact area
229	AT15	---	No contact area
230	AU15	P1+	P1 Power supply
231	AW15	P1+	P1 Power supply
232	AX15	P1+	P1 Power supply
233	AY15	VS	Vendor specific
234	AZ15	NC	Mech. contact/ no connection
235	AF16	NC	Mech. contact/ no connection
236	AG16	GND	Ground
237	AH16	GND	Ground
238	AJ16	GND	Ground
239	AK16	GND	Ground
240	AL16	---	No contact area
241	AM16	---	No contact area
242	AN16	---	No contact area
243	AP16	---	No contact area
244	AQ16	---	No contact area
245	AR16	---	No contact area
246	AS16	---	No contact area
247	AT16	---	No contact area
248	AU16	GND	Ground
249	AW16	GND	Ground
250	AX16	GND	Ground
251	AY16	GND	Ground
252	AZ16	NC	Mech. contact/ no connection

Item #	Contact	Symbol	Description
253	AF17	NC	Mech. contact/ no connection
254	AG17	TX_DIS	Transmit Disable
255	AH17	P2-	P2 Power supply
256	AJ17	P2-	P2 Power supply
257	AK17	P2-	P2 Power supply
258	AL17	---	No contact area
259	AM17	---	No contact area
260	AN17	---	No contact area
261	AP17	---	No contact area
262	AQ17	---	No contact area
263	AR17	---	No contact area
264	AS17	---	No contact area
265	AT17	---	No contact area
266	AU17	P0+	P0 Power supply
267	AW17	P0+	P0 Power supply
268	AX17	P0+	P0 Power supply
269	AY17	VS	Vendor specific
270	AZ17	NC	Mech. contact/ no connection
271	AF18	NC	Mech. contact/ no connection
272	AG18	GND	Ground
273	AH18	GND	Ground
274	AJ18	GND	Ground
275	AK18	GND	Ground
276	AL18	---	No contact area
277	AM18	---	No contact area
278	AN18	---	No contact area
279	AP18	---	No contact area
280	AQ18	---	No contact area
281	AR18	---	No contact area
282	AS18	---	No contact area
283	AT18	---	No contact area
284	AU18	GND	Ground
285	AW18	GND	Ground
286	AX18	GND	Ground
287	AY18	GND	Ground
288	AZ18	NC	Mech. contact/ no connection
289	AF19	NC	Mech. contact/ no connection
290	AG19	TWI_SCL	Two-Wire Interface – Serial Clock
291	AH19	P6+	P6 Power Supply
292	AJ19	P6+	P6 Power Supply
293	AK19	P6+	P6 Power Supply
294	AL19	---	No contact area
295	AM19	---	No contact area
296	AN19	---	No contact area
297	AP19	---	No contact area
298	AQ19	---	No contact area
299	AR19	---	No contact area
300	AS19	---	No contact area
301	AT19	---	No contact area
302	AU19	P3+	P3 Power supply
303	AW19	P3+	P3 Power supply

Item #	Contact	Symbol	Description
304	AX19	P3+	P3 Power supply
305	AY19	RFU	Reserved for future OIF use
306	AZ19	NC	Mech. contact/ no connection
307	AF20	NC	Mech. contact/ no connection
308	AG20	GND	Ground
309	AH20	GND	Ground
400	AJ20	GND	Ground
401	AK20	GND	Ground
402	AL20	---	No contact area
403	AM20	---	No contact area
404	AN20	---	No contact area
405	AP20	---	No contact area
406	AQ20	---	No contact area
407	AR20	---	No contact area
408	AS20	---	No contact area
409	AT20	---	No contact area
410	AU20	GND	Ground
411	AW20	GND	Ground
12	AX20	GND	Ground
413	AY20	GND	Ground
414	AZ20	NC	Mech. contact/ no connection
415	AF21	NC	Mech. contact/ no connection
416	AG21	TWI_SDA	Two-Wire Interface – Serial Data
417	AH21	VS	Vendor Specific
418	AJ21	VS	Vendor Specific
419	AK21	VS	Vendor Specific
420	AL21	---	No contact area
421	AM21	---	No contact area
422	AN21	---	No contact area
423	AP21	---	No contact area
424	AQ21	---	No contact area
425	AR21	---	No contact area
426	AS21	---	No contact area
427	AT21	---	No contact area
428	AU21	P1+	P1 Power supply
429	AW21	P1+	P1 Power supply
430	AX21	P1+	P1 Power supply
431	AY21	RFU	Reserved for future OIF use
432	AZ21	NC	Mech. contact/ no connection
433	AF22	NC	Mech. contact/ no connection
434	AG22	GND	Ground
435	AH22	GND	Ground
436	AJ22	GND	Ground
437	AK22	GND	Ground
438	AL22	---	No contact area
439	AM22	---	No contact area
440	AN22	---	No contact area
441	AP22	---	No contact area
442	AQ22	---	No contact area
443	AR22	---	No contact area
444	AS22	---	No contact area

Item #	Contact	Symbol	Description
445	AT22	---	No contact area
446	AU22	GND	Ground
447	AW22	GND	Ground
448	AX22	GND	Ground
449	AY22	GND	Ground
450	AZ22	NC	Mech. contact/ no connection
451	AF23	NC	Mech. contact/ no connection
452	AG23	MOD_SEL	Module Select
453	AH23	RFU	Reserved for future OIF use
454	AJ23	RFU	Reserved for future OIF use
455	AK23	RFU	Reserved for future OIF use
456	AL23	---	No contact area
457	AM23	---	No contact area
458	AN23	---	No contact area
459	AP23	---	No contact area
460	AQ23	---	No contact area
461	AR23	---	No contact area
462	AS23	---	No contact area
463	AT23	---	No contact area
464	AU23	P0+	P0 Power supply
465	AW23	P0+	P0 Power supply
466	AX23	P0+	P0 Power supply
467	AY23	RFU	Reserved for future OIF use
468	AZ23	NC	Mech. contact/ no connection
469	AF24	NC	Mech. contact/ no connection
470	AG24	GND	Ground
471	AH24	GND	Ground
472	AJ24	GND	Ground
473	AK24	GND	Ground
474	AL24	---	No contact area
475	AM24	---	No contact area
476	AN24	---	No contact area
477	AP24	---	No contact area
478	AQ24	---	No contact area
479	AR24	---	No contact area
480	AS24	---	No contact area
481	AT24	---	No contact area
482	AU24	GND	Ground
483	AW24	GND	Ground
484	AX24	GND	Ground
485	AY24	GND	Ground
486	AZ24	NC	Mech. contact/ no connection
487	AF25	NC	Mech. contact/ no connection
488	AG25	GND	Ground
489	AH25	GND	Ground
490	AJ25	GND	Ground
491	AK25	GND	Ground
492	AL25	GND	Ground
493	AM25	GND	Ground
494	AN25	GND	Ground
495	AP25	GND	Ground

Item #	Contact	Symbol	Description
496	AQ25	GND	Ground
497	AR25	GND	Ground
498	AS25	GND	Ground
499	AT25	GND	Ground
500	AU25	GND	Ground
501	AW25	GND	Ground
502	AX25	GND	Ground
503	AY25	GND	Ground
504	AZ25	NC	Mech. contact/ no connection
505	AF26	NC	Mech. contact/ no connection
506	AG26	GND	Ground
507	AH26	GND	Ground
508	AJ26	GND	Ground
509	AK26	GND	Ground
510	AL26	GND	Ground
511	AM26	GND	Ground
512	AN26	GND	Ground
513	AP26	GND	Ground
514	AQ26	GND	Ground
515	AR26	GND	Ground
516	AS26	GND	Ground
517	AT26	GND	Ground
518	AU26	GND	Ground
519	AW26	GND	Ground
520	AX26	GND	Ground
521	AY26	GND	Ground
522	AZ26	NC	Mech. contact/ no connection
523	AF27	NC	Mech. contact/ no connection
524	AG27	GND	Ground
525	AH27	GND	Ground
526	AJ27	GND	Ground
527	AK27	GND	Ground
528	AL27	GND	Ground
529	AM27	GND	Ground
520	AN27	GND	Ground
531	AP27	GND	Ground
532	AQ27	GND	Ground
533	AR27	GND	Ground
534	AS27	GND	Ground
535	AT27	GND	Ground
536	AU27	GND	Ground
537	AW27	GND	Ground
538	AX27	GND	Ground
539	AY27	GND	Ground
540	AZ27	NC	Mech. contact/ no connection
541	AF28	NC	Mech. contact/ no connection
542	AG28	GND	Ground
543	AH28	GND	Ground
544	AJ28	GND	Ground
545	AK28	GND	Ground
546	AL28	GND	Ground

Item #	Contact	Symbol	Description
547	AM28	GND	Ground
548	AN28	GND	Ground
549	AP28	GND	Ground
550	AQ28	GND	Ground
551	AR28	GND	Ground
552	AS28	GND	Ground
553	AT28	GND	Ground
554	AU28	GND	Ground
555	AW28	GND	Ground
556	AX28	GND	Ground
557	AY28	GND	Ground
558	AZ28	NC	Mech. contact/ no connection

6.2. Low Speed Electrical Interface for Type-2

The low speed interface for the Type-2 form factor is provided by a 60 contact flexible PCB connected to the package body. The flex-to-package interface is vendor-specific and must be contained within the Type-2 package LxWxH maximum dimensions. The 60 low speed contacts are terminated at the host PCB by a two-piece SMT connector as defined in Figure 6-2. Dimensional details are provided for this SlimStack™ family of connectors by Molex as shown in Figure 6-2 and detailed in Table 6-2. The mounting location of the low speed connector on the host PCB and its position relative to the Type-2 package body is not defined by this Implementation Agreement. The use of flex cables for the low speed I/Os allows for various mounting configurations to the host board. The preferred location is determined by the customer and the flex cable length and routing must be agreed between the customer and the IC-TROSA vendor.

Some applications, for example, integration of a Type-2 IC-TROSA into a QSFP-DD module, may require a lower profile and reduced pin count low speed connector such as Molex part number 505070-5420.

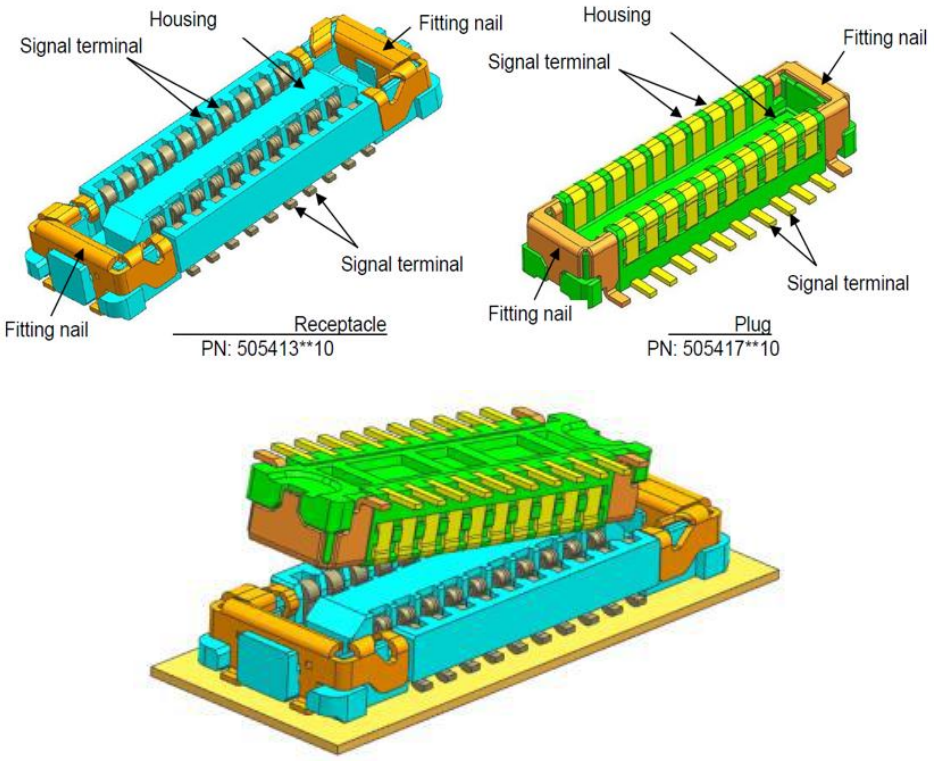


Figure 6-2: Type-2 Low Speed SMT Connector

Note:

1. The Receptacle is mounted on the host PCB and the Plug is mounted on the IC-TROSA flex cable.
2. 20-pin connector is shown as example. Specified connector version is 60 pin. Connector drawings provided by Molex.

Table 6-2: Type-2 Low Speed Connector Specifications

Parameter	Specification	Comments
Vendor	Molex	
Vendor Part	5054176010 (Plug) 5054136010 (Receptacle)	Part numbers for 60 pin mated pair
Description	SlimStack™ 0.35mm pitch board-to-board connector	
Circuits	60	Additionally 2 x “nail” high current end-point contacts for common ground usage
Circuit Rows	2	
Current per contact	0.3 Amp max	
Voltage per contact	50 V AC (RMS)/DC	
Contact pitch	0.35 mm	
Connector Orientation	Vertical	
Mated height	1.00 mm	
Width	2.00 mm	
Length	11.81 mm	Mated, not including flex cable thickness

6.3. Low Speed Connector Pin Sequence

The low speed flex cable may have vendor specific attach points on the IC-TROSA package, however, the host end of the flex cable shall always have the same I/O connectivity as shown in Table 6-3 and the connectivity order as shown in Figure 6-3. Odd numbered pins 1 through 59 are located on the inner portion of the low speed flex cable closest to the IC-TROSA body, and even numbered pins 2 through 60 are located on the outer edge of the low speed flex circuit further from the IC-TROSA body. Neither the orientation relative to the IC-TROSA body, nor the location of low speed connector is defined by this IA. Additionally, the connector may be mounted on either the top side of the host PCB, or on the bottom side. Pin numbers for the flex circuit are same for

either mounting option. However, the connector pin designations will be reversed for bottom side mounting.

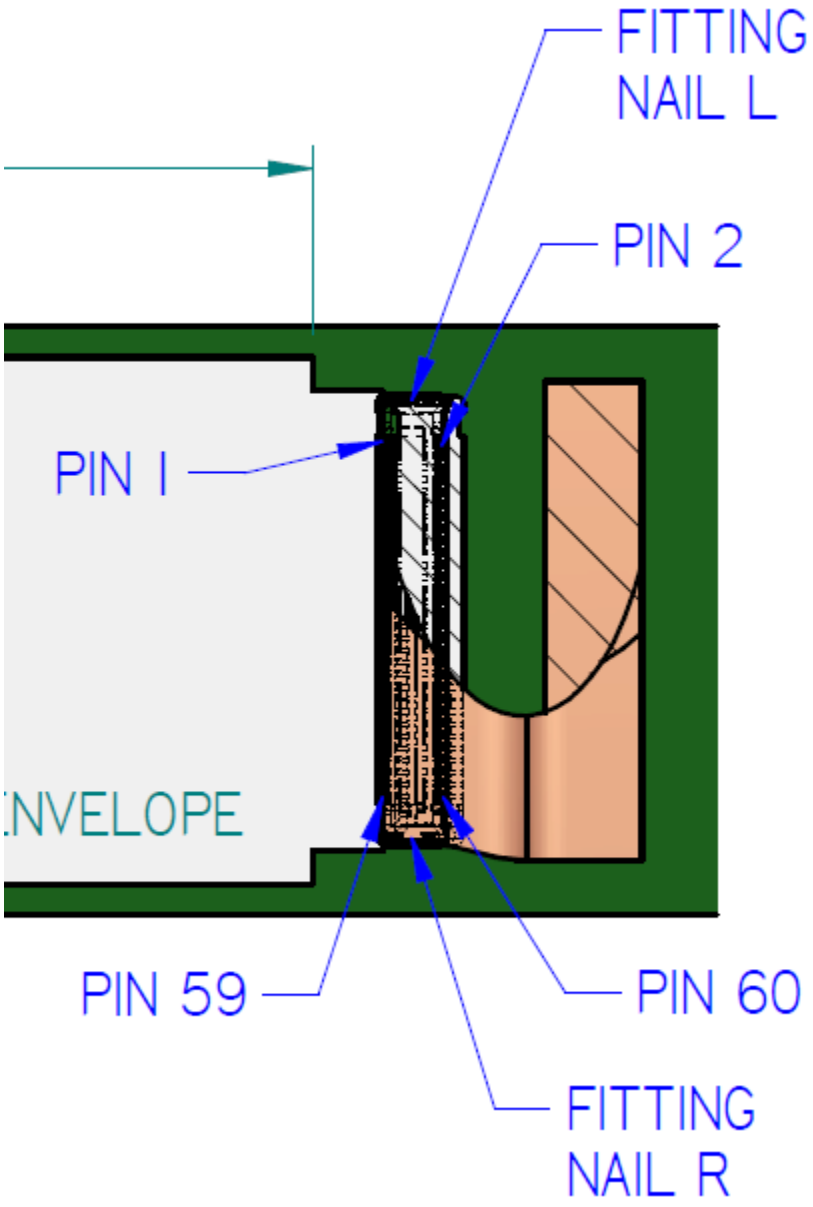


Figure 6-3: Type-2 Low Speed Host Connector Pin Designations (Top View of Package)

Table 6-3: Type-2 Low Speed Electrical I/O Map[1]

Pin	Symbol	Description		Pin	Symbol	Description
Nail	GND	Ground		Nail	GND	Ground
1	P0+	P0 supply		2	P0+	P0 supply
3	P0+	P0 supply		4	P0+	P0 supply
5	P1+	P1 supply		6	P1+	P1 supply
7	P1+	P1 supply		8	P1+	P1 supply
9	P1+	P1 supply		10	P1+	P1 supply
11	P5+	P5 supply		12	TEC1 DMD	TEC 1 demand signal
13	TEC2 DMD	TEC2 demand signal		14	TEC3 DMD	TEC3 demand signal
15	TEC1+	TEC1 current positive		16	TEC1+	TEC1 current positive
17	TEC1+	TEC1 current positive		18	TEC1+	TEC1 current positive
19	TEC1 -	TEC1 current negative		20	TEC1-	TEC1 current negative
21	TEC1-	TEC1 current negative		22	TEC1-	TEC1 current negative
23	TEC2-	TEC2 current negative		24	TEC2-	TEC2 current negative
25	TEC2-	TEC2 current negative		26	TEC2-	TEC2 current negative
27	TEC2+	TEC2 current positive		28	TEC2+	TEC2 current positive
29	TEC2+	TEC2 current positive		30	TEC2+	TEC2 current positive
31	TEC3+	TEC3 current positive		32	TEC3+	TEC3 current positive
33	TEC3+	TEC3 current positive		34	TEC3-	TEC3 current negative
35	TEC3-	TEC3 current negative		36	TEC3-	TEC3 current negative
37	TWI_SDA	Two-wire interface Serial Data		38	TEC_EN	Thermo-electric cooler enable
39	TWI_SCL	Two-wire interface Serial Clock		40	GND	Ground
41	MOD_SEL	Module select		42	VS	Vendor specific
43	VS	Vendor specific		44	VS	Vendor specific
45	VS	Vendor specific		46	VS	Vendor specific
47	RFU	Reserved future use		48	RFU	Reserved future use
49	INT_SRQ	Interrupt/Service request		50	TX_DIS	Transmit disable
51	P2-	P2 supply		52	RESET	Reset
53	P4-	P4 supply		54	RX_LOS	Receive Loss of Signal
55	P3+	P3 supply		56	P3+	P3 supply
57	P3+	P3 supply		58	P3+	P3 supply
59	P6+	P6 supply		60	P6+	P6 supply
Nail	GND	Ground		Nail	GND	Ground

Notes:

1. TECn+ positive current generates cooling. TECn+ negative current generates heat.

7. Environmental and Operating Characteristics

Basic operating characteristics are listed in Table 7-1.

Table 7-1: Environmental & Operating Characteristics

Parameter		Unit	Min	Typ	Max	Notes
Operating temperature	Standard	°C	-5		75	1
	Preferred		-5		80	
Operating humidity (non-condensing)		%RH	5		85	
Short-term ambient peak temperature exposure for solder reflow and rework		°C	Vendor Specified			2

Notes:

1. The operating temperature is defined as the minimum/maximum of the IC-TROSA case "hot zone" surface temperature.
2. Applies only to Type-1 package using lead-free solder. Refer to IPC/JEDEC J-STD-020E for guidance on typical solder reflow temperature levels, ramp rates, and soak times. Refer to vendor specification for reflow/rework requirements for a Type-1 package.

8. Electro-Optical Characteristics

In this revision of the IA electro-optical (EO) characteristics are provided for three classes of IC-TROSA (Class 20, 30 and 40), corresponding to devices having S_{21} bandwidths of 20GHz, 30GHz, and 40GHz, respectively. The RF frequency response specifications specific to each class are given in Section 8.4.

8.1. Laser Electro-Optic Characteristics (Type-2 Only)

Table 8-1: Laser Electro-Optic Characteristics (Type-2 only)

Parameter	Unit	Min	Typ	Max	Notes
Frequency tuning range	THz	191.35		196.20	Informative 1
Frequency stability	GHz	-1.8		1.8	Informative 2
Frequency coarse tuning capability (grid support)	GHz	3.125		100	Informative 1
Fine tune frequency range	GHz	-6		6	Informative 1
Optical linewidth (instantaneous)	KHz				Informative 2

Notes:

1. Supported values are advertised in the IC-TROSA register map.
2. Application Specific

8.2. Transmitter Electro-Optic Characteristics

Table 8-2: Transmitter Electro-Optic Characteristics

Parameter	Unit	Min.	Typ.	Max.	Notes
Optical insertion loss	dB				For Type-1 only, 1
Optical reflectance	dB			-27	Reflected power to network
Optical input power (LASER-IN)	dBm			18	Type—1 only
Optical output power (TX)	dBm				Type-2 only, 1
Optical output power stability (TX)	dB	-1.5		1.5	Over operating temperature
Disabled optical output power (TX)	dBm			-35	Laser source disabled
X-Y Output power imbalance	dB			1.5	
Parent MZ extinction ratio	dB	22			
Child MZ extinction ratio	dB	25			
S21 E/O bandwidth Class 20, 30, 40	GHz				See Sect. 8.4.1.1 S21, S11 compliance masks
S11 Electrical Return loss Class 20, 30, 40	dBe				
Max differential input swing	mVppd	500			5 For XI, XQ, YI, YQ data inputs
Min differential input swing	mVppd			300	5 For XI, XQ, YI, YQ data inputs
RF differential impedance	Ohm		100		
I/Q skew	ps			50	2
Total skew	ps			100	3
I/Q skew variation	ps			1.5	2, 4
Total skew variation	ps			4	3
Low frequency cutoff	MHz			1	
Polarization extinction	dB		20		
TX OSNR	dB/0.1nm	37			Type-2 only

Notes:
1 - Application specific – covering a range of applications for this component.
2 - I/Q Skew is the skew between channel pairs XI and XQ, and YI and YQ.
3 - Total skew is the maximum skew between any of the four physical channels XI, XQ, YI and YQ.
4 - The objective of this specification is to minimize skew variation between I and Q. I/Q skew variation is a key parameter for system operation in some DSPs.
5 - The input swing between 300mVppd and 500mVppd is normative; input voltage swings outside this range are informative (optional).

8.3. Receiver Electro-Optical Characteristics

Table 8-3: Receiver Electro-Optic Characteristics

Parameter		Unit	Min	Typ	Max	Notes
Operating signal power		dBm			0	1, 11
Operating total input power		dBm			16	1, 11, 12
Optical reflectance		dB			-27	7
S21 E/O bandwidth Class 20, 30, 40		GHz				See Sect. 8.4.1.2
S22 Electrical Return loss Class 20, 30, 40		dBe				
Maximum differential output swing		mVppd	600			2
Minimum differential output swing		mVppd			300	2
DC common mode rejection ratio ($CMRR_{DC}$)	Sig to I&Q	dBe			-20	3
	LO to I&Q				-16	
RF common mode rejection ratio ($CMRR_{RF}$)	Sig to I&Q	dBe			-16	3, 4
	LO to I&Q				-14	
Low frequency cut-off		MHz			1	5
Phase error		Deg	-7.5		+7.5	6
Skew between complimentary signals within a channel (informative)		ps			1	
Channel skew		ps			50	8
X/Y skew variation		ps			3.0	9
I/Q skew variation	Class 20	ps			2.0	10, 11
	Class 30				1.5	
	Class 40				1.0	

Notes:

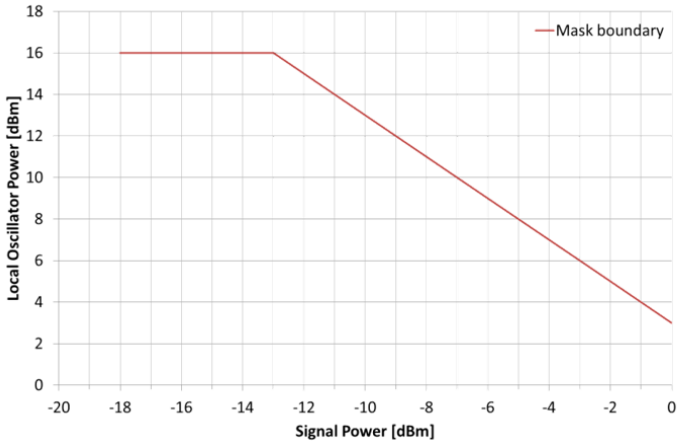
1. At high RX powers, the maximum desired local oscillator power is limited by the maximum TIA differential input current for linear operation. Figure 8-1: provides an informative example calculation for the allowed LO power as a function of the input signal. In implementations with a VOA in the RX path, the RX power can be attenuated such that no adjustment to the LO power is required.
2. Peak to peak, differential, AC coupled output amplitude that can be achieved by controlling the output adjust (OA) in AGC mode, given sufficiently strong input Signal and LO powers. The output voltage swing between 300mVppd and 600mVppd is normative; output voltage swings outside this range are informative (optional).
3. CMRR = $20 \cdot \log(|\Delta I| / \sum I)$, where ΔI is the difference in photocurrent between the PDs in a differential pair (XI, XQ, YI, or YQ) and $\sum I$ is the sum of the photocurrents from the PDs in the same PD pair. Note CMRR may not be directly measureable by the customer if no individual PD (p,n) bias pins are available on the low speed electrical interface.
4. RF CMRR is measured at 20GHz, 30GHz, and 40GHz for Class 20, 30, and 40 ICRs, respectively. The single-port rejection ratio (SPRR) measurement technique can be used to provide a suitable representation of the RF CMRR. The limits for Class 30 and 40 ICRs may be revised in a future revision of the document as more component and system level performance data becomes available.
5. AC coupled.
6. Between RX-XI and RX-XQ and between RX-YI and RX-YQ.
7. RX and LO ports. Per ITU-T G.959.1
8. Time difference between earliest and latest channel (RX-XI, RX-XQ, RX-YI, RX-YQ). Includes X/Y and I/Q skew variation.
9. Variation in the skew between X and Y over case temperature, wavelength, input optical power, amplifier gain, and aging. The time for a polarization is defined as the average of I and Q, and the time for an individual I or Q channel is the average of p and n.

10. Variation in the skew between RX-XI and RX-XQ or between RX-YI and RX-YQ over case temperature, wavelength, input optical power, amplifier gain, and aging. The time for an individual I or Q channel is the average of p and n. It is noted that the measurement accuracy of currently available skew measurement techniques may not be sufficient to confirm compliance to limits below 2.0ps.
11. Application Specific
12. Total input power including cases where multiple channels are incident on the receiver input with additional ASE noise.

8.3.1. The TIA differential input current [mA] is calculated as:

$$I_{diff,pp} = 8\sqrt{R_{SIG} \cdot R_{LO} \cdot 10^{(P_{SIG,S}+P_{LO})/10}}$$

where RSIG and RLO are the Signal and LO PD responsivities [A/W], PSIG, S is the Signal power [dBm] in a single polarization (S = X or Y), and P_{LO} is the local oscillator power [dBm]. Assuming a Signal responsivity of 0.10 A/W and an LO responsivity of 0.05 A/W, as well as a 0.80 mA peak to peak differential linear input dynamic range, then a mask for the maximum LO power as a function of Signal power can be calculated as shown in Figure 8-1:.



RX power [dBm]	LO power [dBm]	Diff. input current [mA]
0	3	0.80
-3	6	0.80
-6	9	0.80
-10	13	0.80
-13	16	0.80
-16	16	0.57
-18	16	0.45

Figure 8-1: Informative Example: Recommended Maximum LO Power Versus RX Signal Power

Note for Figure 8-1: For a receiver with R_{SIG} = 0.10 A/W, R_{LO} = 0.05 A/W, and peak-to-peak differential linear input dynamic range of 0.80 mA.

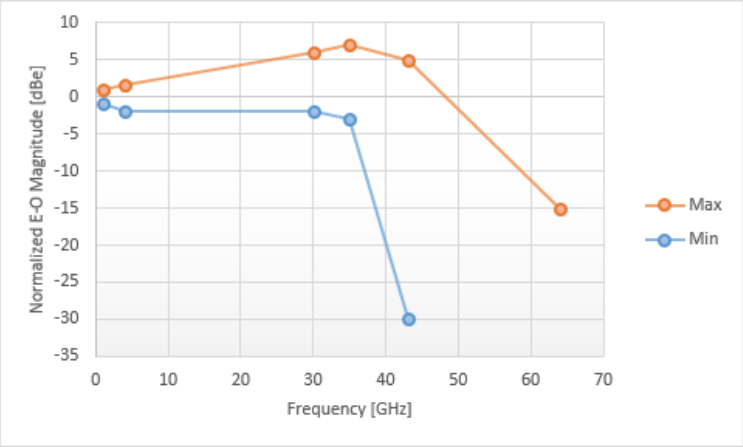
8.4. RF Frequency Response

8.4.1. Measurement Methods

The optical-to-electrical and electrical-to-optical S_{21} transfer function and S_{11} and S_{22} electrical return loss frequency responses shall be measured *differentially* to evaluate conformance to the RF compliance masks in Section 8.4.1.1 and Section 8.4.1.2.

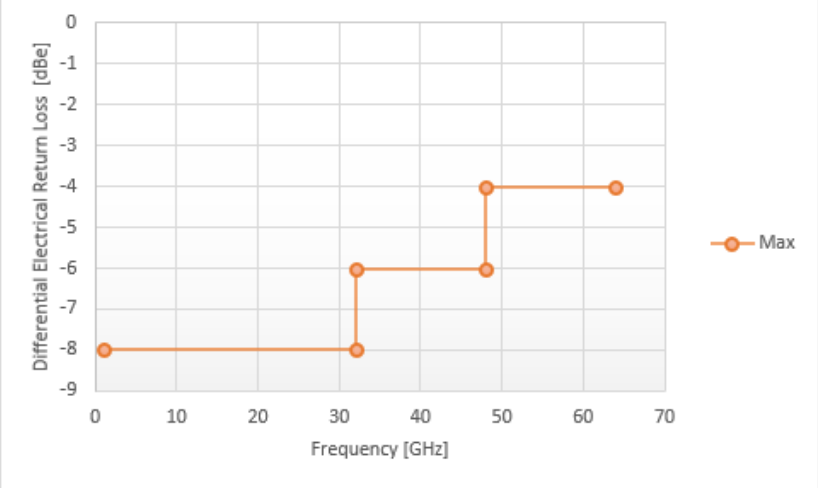
The RF compliance masks show an informative target range for the optical-to-electrical and electrical-to-optical S_{21} transfer function and S_{11} and S_{22} electrical return loss frequency responses allowing for component to component variations.

8.4.1.1. Transmitter (TX) Transfer Function Masks



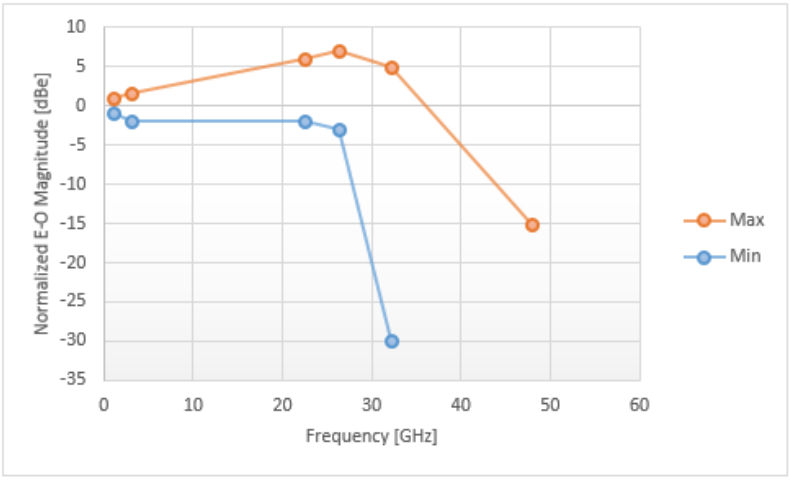
Class 40		
Freq GHz	dBe Min	dBe Max
1	-1	1
4	-2	1.5
30	-2	6
35	-3	7
43	-30	5
64		-15

Figure 8-2: TX Class 40, Differential S21



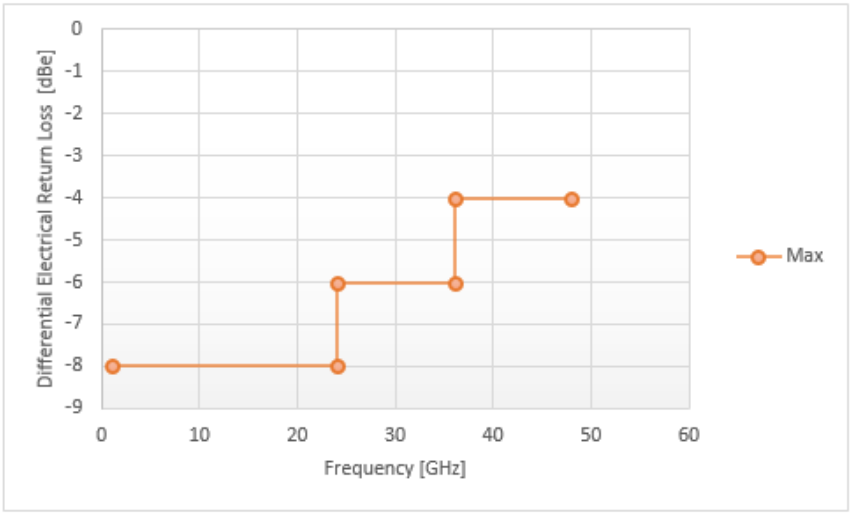
Class 40	
Freq GHz	dBe Max
1	-8
32	-8
32	-6
48	-6
48	-4
64	-4

Figure 8-3: TX Class 40, Differential S11



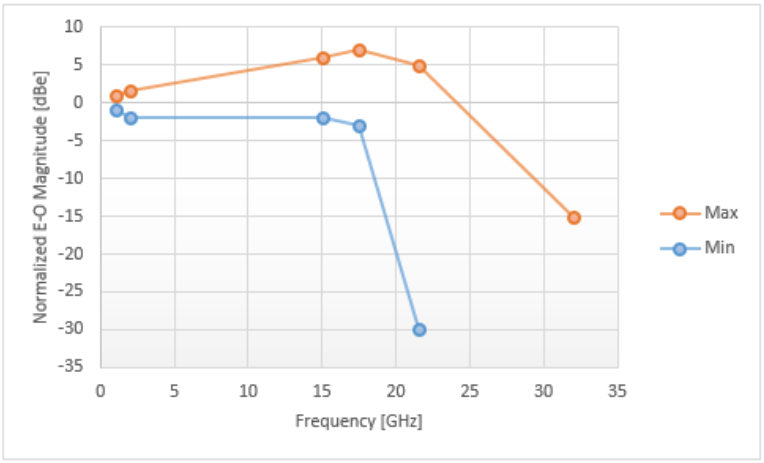
Class 30		
Freq GHz	dBe Min	dBe Max
1	-1	1
3	-2	1.5
23	-2	6
26	-3	7
32	-30	5
48		-15

Figure 8-4: TX Class 30, Differential S21



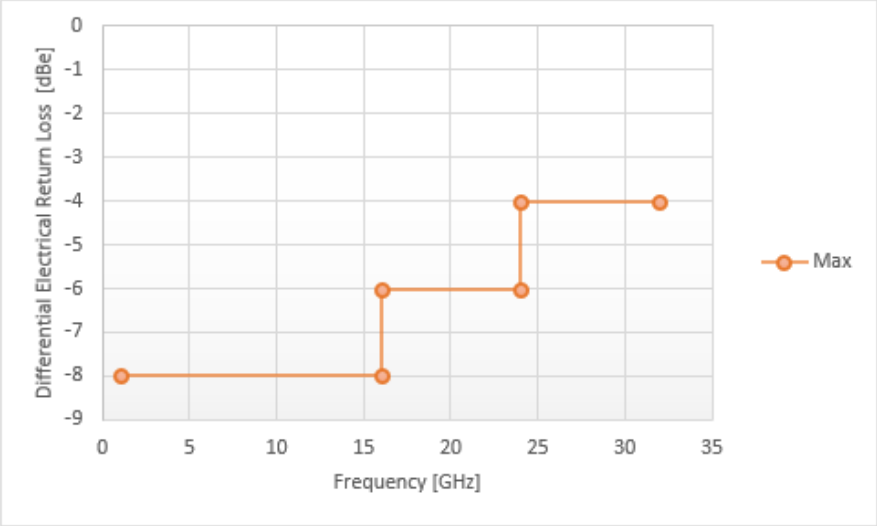
Class 30	
Freq GHz	dBe Max
1	-8
24	-8
24	-6
36	-6
36	-4
48	-4

Figure 8-5: TX Class 30, Differential S11



Class 20		
Freq GHz	dBe Min	dBe Max
1	-1	1
2	-2	1.5
15	-2	6
18	-3	7
22	-30	5
32		-15

Figure 8-6: TX Class 20, Differential S21



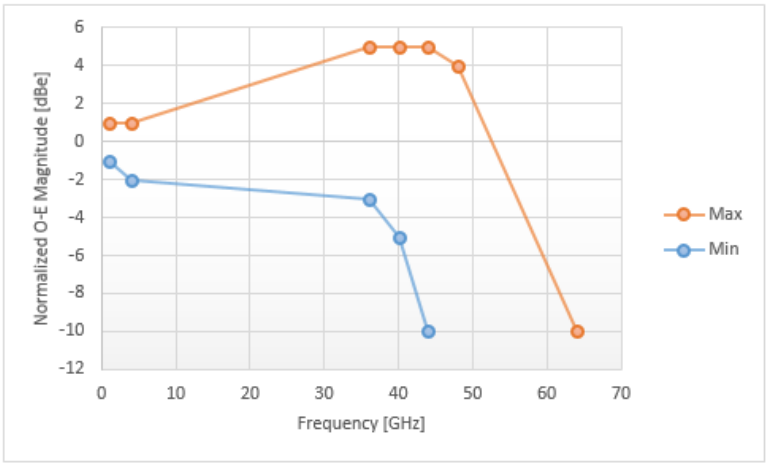
Class 20	
Freq GHz	dBe Max
1	-8
16	-8
16	-6
24	-6
24	-4
32	-4

Figure 8-7: TX Class 20, Differential S11

8.4.1.2. Receiver (RX) Transfer Function Masks

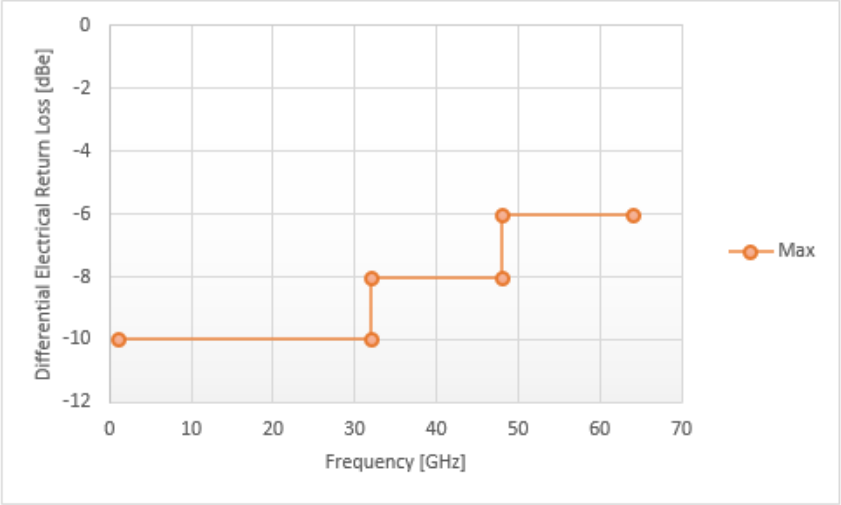
The ideal RF frequency response for the receiver chain of a coherent modem consisting of the ICR, the differential signal traces between the Intradyne Coherent Receiver (ICR) and the DSP ASIC, and the ADCs at the input of the ASIC is a low pass response which is flat up to the targeted signal bandwidth and rolls off steeply beyond that. Given that the losses of the signal traces between the ICR and the DSP ASIC increase gradually with frequency, it is generally preferred to have the RF frequency response of the ICR to increase gradually with frequency up to the targeted signal bandwidth, and then roll off steeply.

The S_{21} transfer functions shall be measured at a TIA gain condition and ICR temperature that is agreed with the customer. All S_{21} responses shall be normalized to the response at 1GHz. It is assumed that any TIA functionality that manipulates the S_{21} transfer function (e.g. bandwidth adjust functions) can be utilized to obtain compliance with the masks provided in this section.



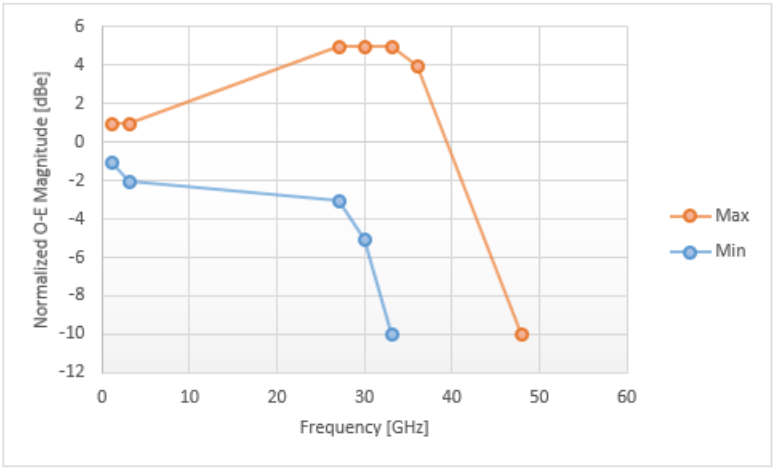
Class 40		
Freq GHz	dBe Min	dBe Max
1	-1	1
4	-2	1
36	-3	5
40	-5	5
44	-10	5
48		4
64		-10

Figure 8-8: RX Class 40, Differential S21



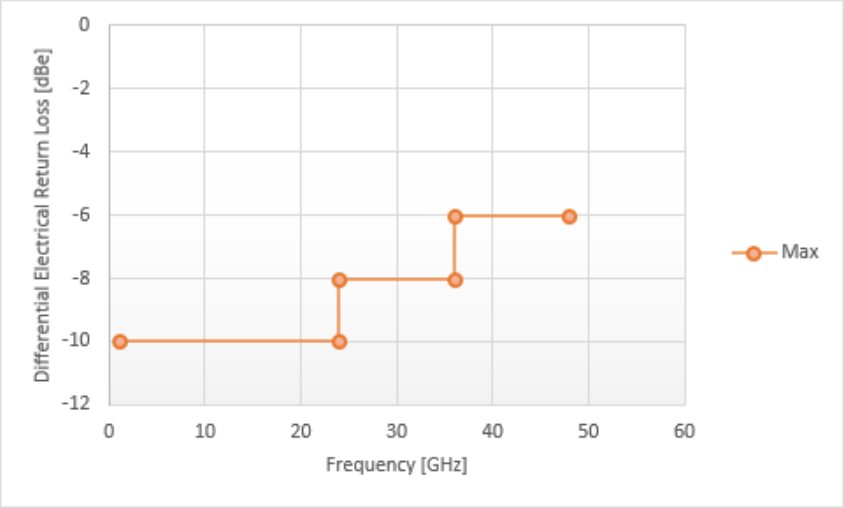
Class 40	
Freq GHz	dBe Max
1	-10
32	-10
32	-8
48	-8
48	-6
64	-6

Figure 8-9: RX Class 40, Differential S22



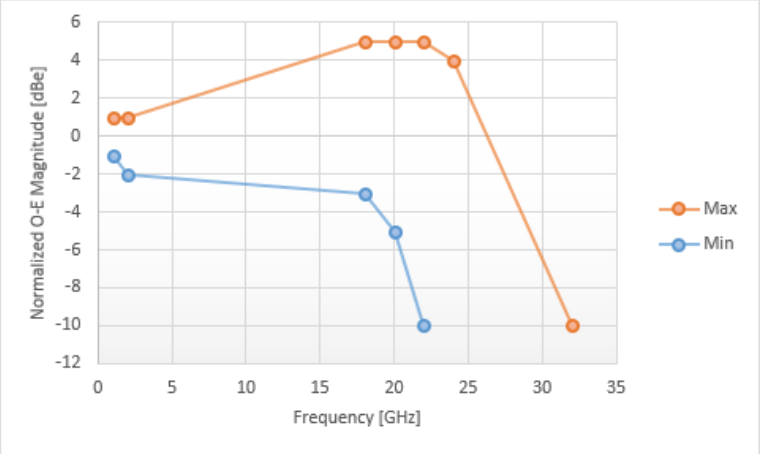
Class 30		
Freq GHz	dBe Min	dBe Max
1	-1	1
3	-2	1
27	-3	5
30	-5	5
33	-10	5
36		4
48		-10

Figure 8-10: RX Class 30, Differential S21



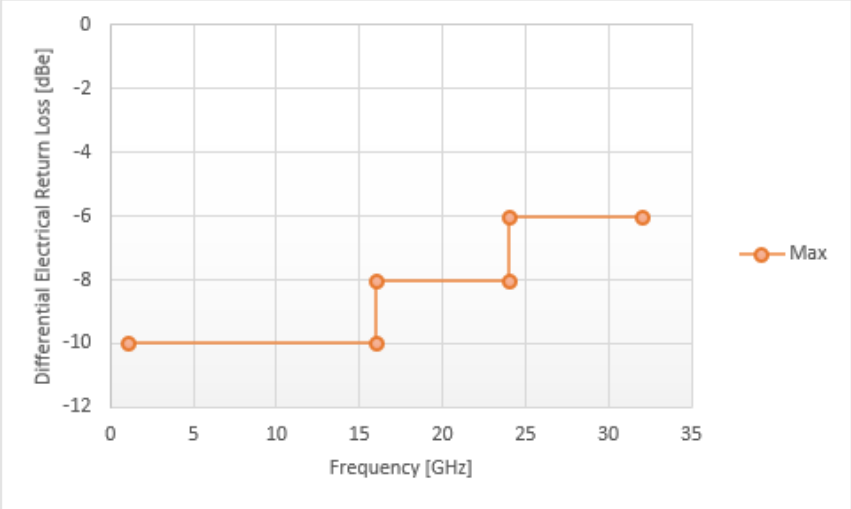
Class 30	
Freq GHz	dBe Max
1	-10
24	-10
24	-8
36	-8
36	-6
48	-6

Figure 8-11: RX Class 30, Differential S22



Class 20		
Freq GHz	dBe Min	dBe Max
1	-1	1
2	-2	1
18	-3	5
20	-5	5
22	-10	5
24		4
32		-10

Figure 8-12: RX Class 20, Differential S21



Class 20	
Freq GHz	dBe Max
1	-10
16	-10
16	-8
24	-8
24	-6
32	-6

Figure 8-13: RX Class 20, Differential S22

9. Mechanical Specifications

9.1. General Overview and Fiber Types

Two primary electro-mechanical form factors are defined in this revision of the IC-TROSA IA. For both form factors the optical fiber interfaces and the RF electrical interfaces are located on opposite ends of the package.

The optical fiber types for both package styles are defined in Table 9-1. PM fiber is only applicable to Type-1 packages requiring an external laser source.

Table 9-1 Optical Fiber Interface Characteristics for Type-1 & Type-2

Type	Parameter		Unit	Min	Typ	Max	Note
PMF	Operating optical frequency		THz	C-Band or L-Band			
	Bend radius		mm	7.5			1, 2, 7
	Bend loss for 10 turns at 7.5mm bend radius @1550nm		dB			1	6, 7
	Fiber coating color for "laser Input" port		---	Natural (un-colored)			3
	Fiber cladding diameter		µm	124	125	126	
	Fiber coating diameter (un-colored)		µm	230	245	260	
	Polarization mode crosstalk		dB	25	30		
SMF	Operating optical frequency		THz	C-band or L-Band			
	Bend radius	Option 1	mm	5.0			4, 7
		Option 2		7.5			5, 7
	Bend loss for 10 turns at 5.0mm (Option 1) or 7.5mm (Option 2) bend radius @1550nm		dB			1	6, 7
	Fiber coating color for "TX" port		--	Black			3
	Fiber coating color for "RX" port		--	Red			3
	Fiber cladding diameter		µm	124	125	126	
	Fiber coating diameter (colored)		µm	235	250	265	

Notes:

1. The polarization state in the PM fiber shall be aligned to the slow axis of the PM fiber.
2. The slow axis of the PM fiber shall be aligned to the connector key.
3. Fiber colors shall be compliant to ANSI/TIA-598-D-2014
4. The Option 1 SMF shall be compliant to ITU-T Recommendations G.657.B3 and G.652.D.
5. The Option 2 SMF shall be compliant to ITU-T Recommendations G.657.B2 and G.652.D.
6. Receiver responsivity shall be measured with straight fibers and shall not include bend loss.
7. Depending upon fiber coatings used, Type-1 may require larger bend radius to meet solder reflow requirements to be agreed between supplier and customer.

9.2. Type-1 Mechanical Form Factor

Electro-mechanical form factor Type-1 uses a surface mount configuration consistent with a BGA (Ball Grid Array) package. For this package, all electrical interface signals are located on the bottom of the package in a two dimensional array of solder ball contacts. The high speed contacts are located on an outer row of contacts located opposite the optical port. The Type-1 mechanical drawing is shown in Figure 9-1 and the dimensions are provided in Table 9-2. Note also the thermal transfer path for a Type-1 IC-TROSA shall be from the *Hot-Zone* located on the top surface of the package, as defined in Figure 9-1, transferring upward toward a heat sink or other thermally dissipative structure. This package is compatible with many pluggable transceiver form factors having heat sink capability located on the top surface of the transceiver housing. The mechanical dimensions in Table 9-2 allow both Standard width and Reduced width implementations. Both package widths are electrically and mechanically compliant to the Standard width landing pattern. For small form factor

applications the user may choose to implement a reduced width landing pattern matching the reduced width IC-TROSA ball pattern.

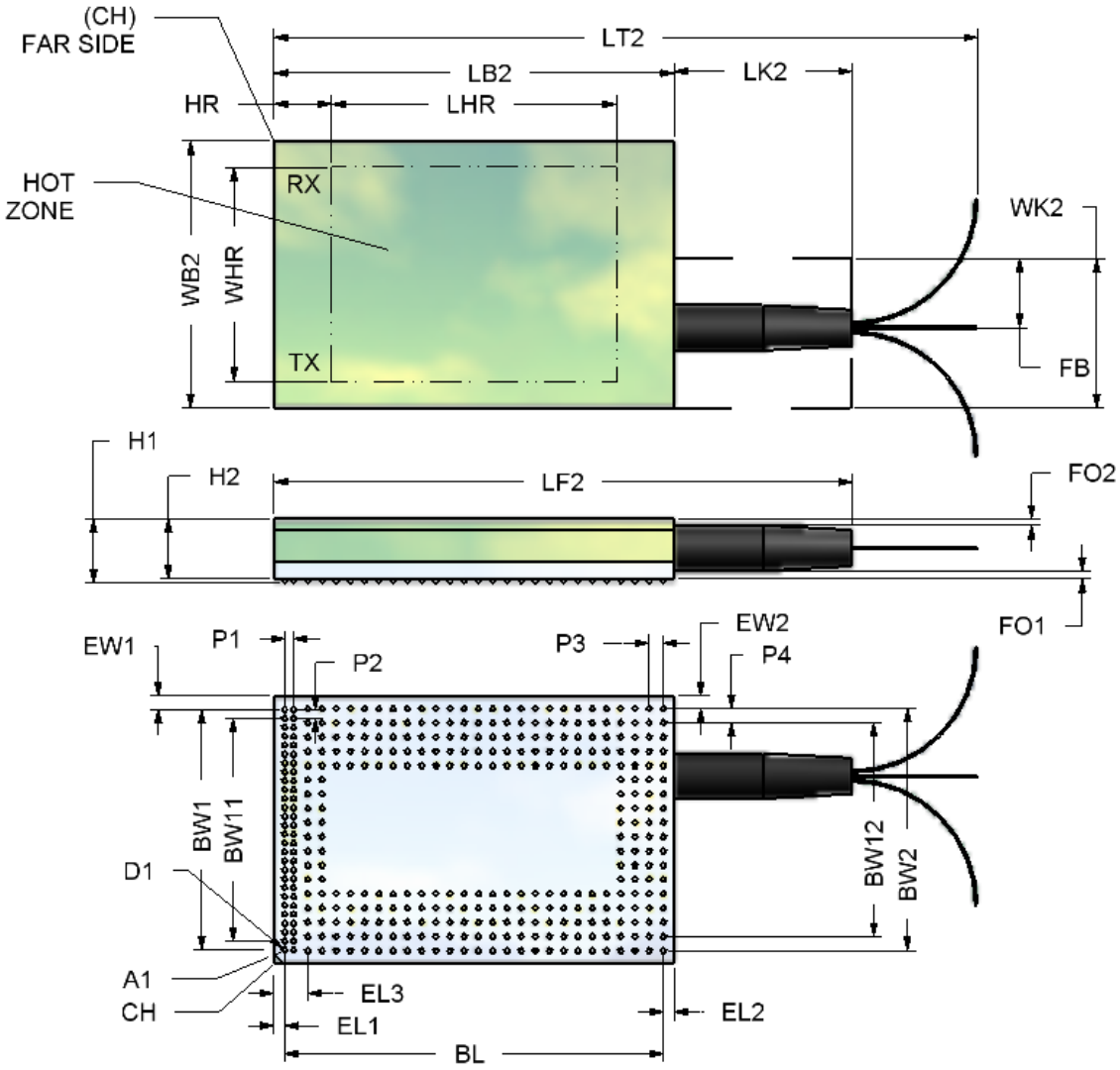


Figure 9-1 Mechanical drawing for Type-1 package

Table 9-2: Type-1 Mechanical Dimensions

Sym	Description	Dimensions (mm)			Notes
		Min	Nom	Max	
LB2	Length of package			22.5	
LT2	Total length including 90 degree fiber bends			39.5	
LF2	Full length of package including fiber boots			32.5	
WB2	Width of package	13.5		15.0	Max=Standard Min=Reduced
H1	Height including solder balls			3.60	
H2	Height excluding solder balls		3.30		
FB	Fiber Boot Offset	0	3.75	5	
LK2	Length of boot area keep-out region	(max LF2) – LB2			Max
WK2	Width of boot area keep-out region			0.5 x WB2	Max
FO1	Clearance between boot and cold side	0.3			Cold Side
FO2	Clearance between boot and hot side	0.4			Hot Side
HR	Location of hot region relative to package end	2		4	
WHR	Width of hot region			WB2	
LHR	Length of hot region			LB2	
BW1	Distance between first and last solder ball centers (0.5mm pitch RF contacts)		13.5		Standard width package. Includes outer "NC" contact rows A, AE, AF, AZ
BW2	Distance between first and last solder ball centers (0.8mm pitch DC contacts)		13.6		
EW1	Distance from edge to first solder ball center (0.5mm pitch RF contacts)		0.75		
EW2	Distance from edge to first solder ball center (0.8mm pitch DC contacts)		0.70		
BW11	Distance between first and last solder ball centers (0.5mm pitch RF contacts)		12.5		Optional Reduced width package. Removes outer "NC" contact rows A, AE, AF, AZ
BW12	Distance between first and last solder ball centers (0.8mm pitch DC contacts)		12.0		
EW1	Distance from edge to first solder ball center (0.5mm pitch RF contacts)		0.5		

Sym	Description	Dimensions (mm)			Notes
		Min	Nom	Max	
EW2	Distance from edge to first solder ball center (0.8mm pitch DC contacts)		0.75		
BL	Distance between first and last solder ball centers		21.0		
EL1	Distance from edge to first solder ball centers		0.6		
EL2	Distance from edge to first solder ball centers		0.6		
EL3	Distance from edge to third solder ball centers	(EL1 + P1 +P3)			
D1	Diameter of solder ball		0.30		
P1	Pitch along dimension shown BL		0.50		
P2	Pitch along dimension shown BW1		0.50		
P3	Pitch along dimension shown BL		0.80		
P4	Pitch along dimension shown BW2		0.80		
CH	Location of Chamfer on LGA Substrate				Ref Only
A1	Location of first Pad on LGA Substrate				Ref Only

9.3. Type-2 Mechanical Form Factor

Electro-mechanical form factor Type-2 employs flexible PCBs for both the RF and low speed electrical I/O interfaces. The Type-2 package has two options for the optical interface. Type-2 with fiber interface mechanical drawing is shown in Figure 9-2 and Type-2 with LC ferrules is shown in Figure 9-3 and the dimensions for both types are provided in Table 9-3. The length, width, and height dimensions of the main body are specified as a boundary which includes the mechanical package plus the low speed flex cable attach point and any required routing of the low speed flex along the sides or bottom of the mechanical package.

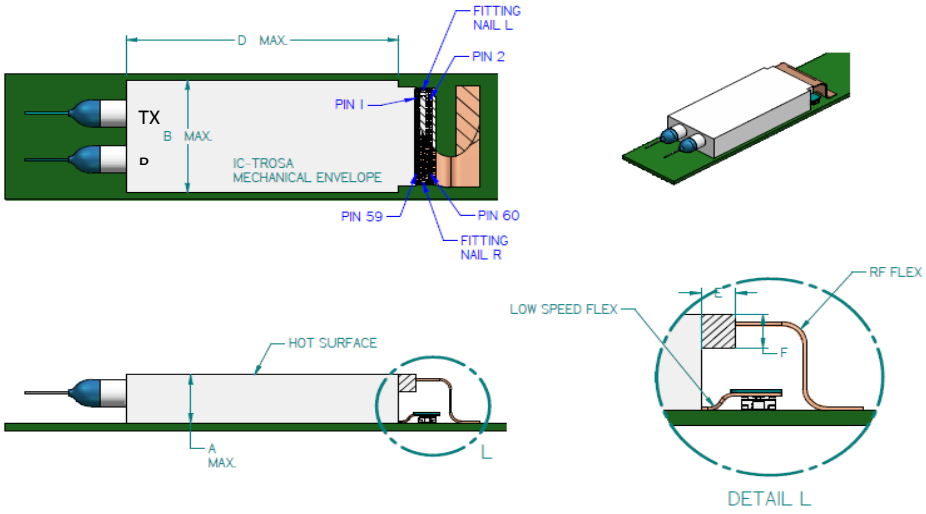


Figure 9-2: Type-2 Package with Fiber Interface and Low Speed Pin Mapping

The use of flexible PCB in Type-2 allows for a customizable RF connection between a vendor-specific interface on the package and the normative landing pattern interface located on the host PCB. The flex cable can provide routing, pitch adjustment and path equalization as needed. The Type-2 IC-TROSA may be surface mounted on a host PCB, sub-mounted in a PCB with a suitable cutout for suspending the IC-TROSA, or alternately this package may be mounted on any other suitable support structure having suitable proximity to the required electrical connections on a nearby host PCB. The hot zone of the Type-2 IC-TROSA is located on the top surface of the package. The thermal conduction path is then from the top of the package to a suitable heat sink. This package is compatible with most pluggable transceiver form factors having heat sink capability located on the top surface of the transceiver housing.

9.4. An alternative optical interface is also available for the IC-TROSA. The interface shown in Figure 9-3 may be useful in applications where a direct interface is desired from the IC-TROSA to the faceplate of an optical line card or pluggable interface.

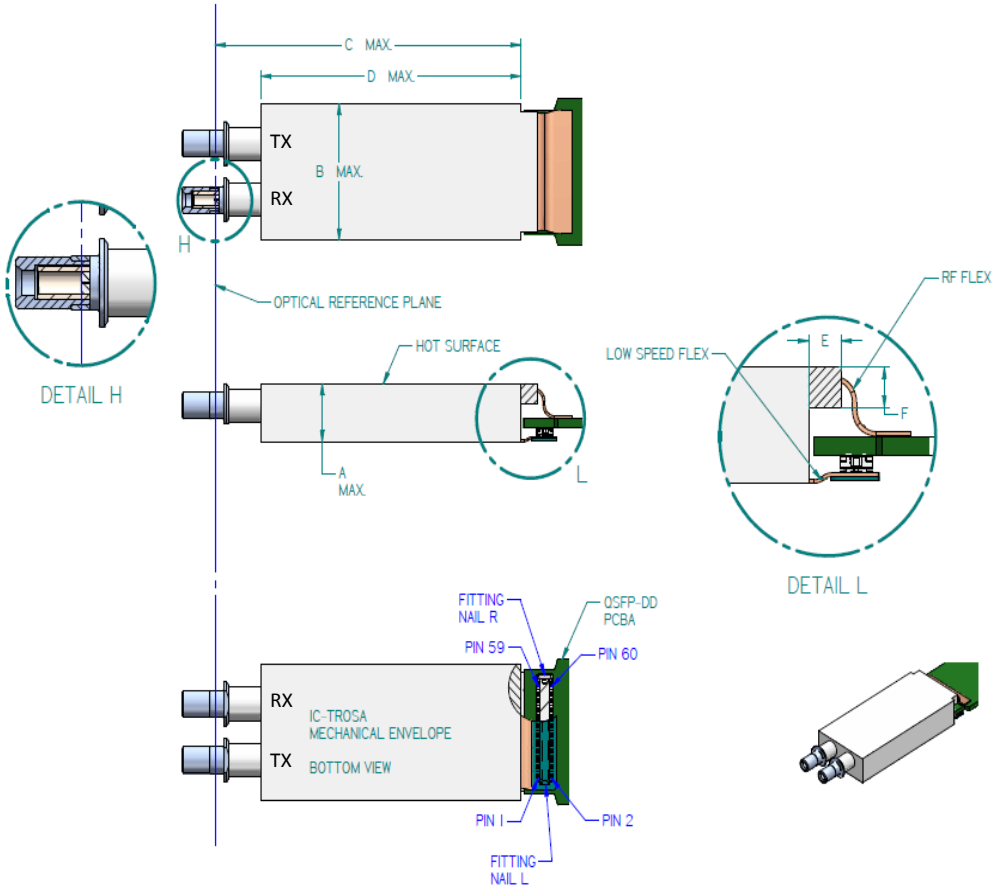


Figure 9-3: Type-2 Package with LC Ferrules and Low Speed Pin Mapping

Table 9-3: Type-2 Mechanical Dimensions

Sym	Description	Dimensions (mm)			Notes
		Min	Nom	Max	
A	Height – body + (optional) flex cable routing			6.5	1
B	Width – body + (optional) flex cable attach			15.1	1, 2
C	Length – body rear to optical ref plane			34.1	3, 4
D	Length – body only			30.0	3
E	Length – HS flex ceramic support			3.1	
F	Height – HS flex ceramic support			2.0	3

Notes:

1. Includes all low speed flex cable attach points and space required for flex cable routing along outer surfaces of package. Flex cable routing along top surface is not possible as this surface is used for heat sink attach.
2. Ceramic support maximum width must be ≤ dimension B.
3. Ceramic support may extend beyond dimensions C and D in accordance with maximum dimension E.
4. Dimension C does not apply to Type-2 package with fiber interface.

10. Packaging and Mounting

10.1. Type-1

10.1.1. Packaging, Storage, and Pre-Solder Preparation

10.1.1.1. Normative Requirement

Non-hermetic packages are susceptible to internal moisture accumulation. An electronic package having internal moisture is susceptible to damage when exposed to a sudden elevation in ambient temperature such as induced during the soldering process. To prevent damage when soldering non-hermetic IC-TROSA packages to host PCBs care must be taken during the packaging, shipping, storage, and solder preparation stages of its lifecycle. The supplier shall provide the customer with the appropriate handling, packing, shipping, and pre-solder reflow preparations (e.g. baking) in accordance with the product's established susceptibility to moisture.

10.1.1.2. Informative Recommendation

For Type-1 packages designed for commonly used Pb-free solder reflow processes, IPC/JEDEC J-STD-020E (or latest revision) recommendations for Pb-Free reflow soldering should be used by the vendor during the product qualification process to define the Moisture Sensitivity Rating of any implementation of IC-TROSA Type-1 according to levels defined within the IPC/JEDEC standard. The supplier shall provide the customer with the package's Moisture Sensitivity Rating as well as appropriate handling, packing, shipping, and pre-solder reflow preparations (e.g. baking) as recommended by IPC/JEDEC J-STD-033C (or latest revision) in accordance with the product's established Moisture Sensitivity Rating.

10.1.2. Solder Reflow Design Reliability

Type-1 shall maintain full performance & reliability specification compliance after subjection to the lead-free solder thermal profile as specified by the IC-TROSA vendor's mounting instructions. Unless low temperature solders, or specialized solder temperature and profiles are explicitly specified for joining the Type-1 to the host PCB, then it is recommended for vendor and customer to use the recommended temperature profile as specified in IPC/JEDEC J-STD-020E (or latest revision) for Pb-free solders which specifies 150 seconds above liquidous temperature ≥215 Deg-C including minimum 30 seconds at peak temperature 260 +/-5 Deg-C. The thermal ramp rate shall not exceed 3 Deg-C/second. The IC-TROSA vendor shall further specify to customer the

number of accumulated thermal profile iterations, over the device lifetime, for which this device is designed to comply.

Unless a Type-1 IC-TROSA is specified for only mechanical mounting processes, then it is a minimum requirement for the IC-TROSA to withstand a single solder reflow process while meeting the performance requirements stated within this Implementation Agreement. Furthermore, it is a strong recommendation for the Type-1 be able to withstand a minimum of 3 solder cycles over its lifetime. This provides the possibility for a second solder attempt after an initial solder attempt and subsequent re-balling process on the BGA package.

10.1.3. Type-1 Host Board Landing Pattern

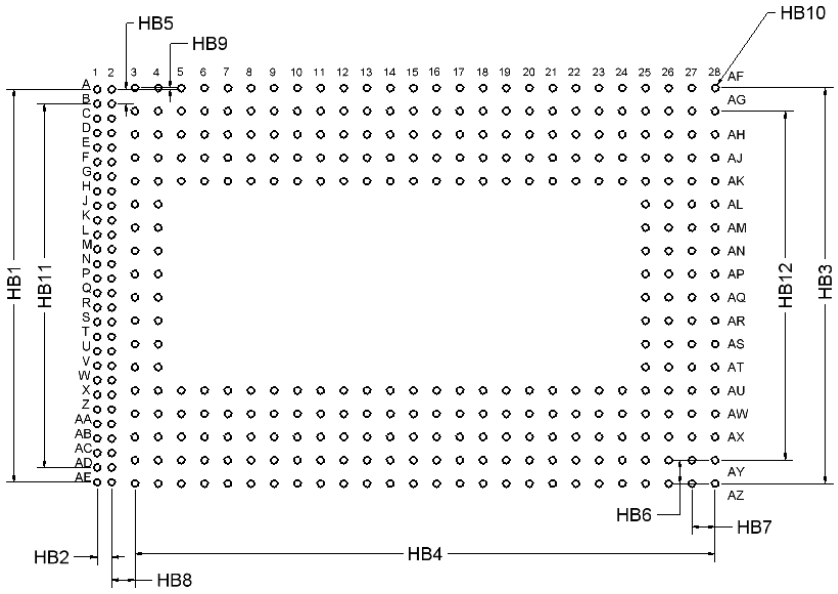


Figure 10-1: Type-1 Host PCB Landing Pattern – Top View

Table 10-1: Type-1 Landing Pattern Dimensions

Sym	Parameter	Dimension		
		Min	Nom	Max
HB1	Distance between first and last row high speed pads		13.50	
HB2	Distance between first and last column high speed pads		0.50	
HB3	Distance between first and last row low speed pads		13.60	
HB4	Distance between first and last column low speed pads		20.00	
HB5	Vertical pitch high speed pads		0.50	
HB6	Vertical pitch low speed pads		0.80	
HB7	Horizontal pitch low speed pads		0.80	
HB8	Offset between last column high speed pads and first column low speed pads		0.80	
HB9	Offset between first row high speed pads and first row low speed pads		0.05	
HB10	Diameter Landing pad (Typical)		0.25	
HB11	Distance between second and second to last row high speed pads		12.50	
HB12	Distance between second and second to last row low speed pads		12.00	

10.1.4. Type-1 Mechanical Mounting Option

The Type-1 package is intended to be a surface mount package compatible with standard solder reflow processes. However, the Type-1 base design also supports an alternative mechanical mounting method to the host PCB. The package itself is the same for both mounting methods. No changes to pin map, contact pitch, or package mechanical dimensions are present. However, mechanical mounting of a Type-1 IC-TROSA, which is a solderless process, requires an electrical interposer and mounting hardware which slightly increases the required surface area of the mounted package as shown in Figure 10-2. Also, this mechanical mounting method does not use solder balls for contacts. Instead it uses the landing pads found directly on the bottom surface of the IC-TROSA making it a Land Grid Array (LGA) SMT package. The direct use of the Type-1 package's electrical landing pads results in the elimination of an extra process step typically required in the Type-1 IC-TROSA assembly process which is to apply the solder balls to the landing pads of the IC-TROSA. For the mechanical mounting option the customer must specify a Type-1 IC-TROSA with landing pads only, in effect making the IC-TROSA an LGA (Land Grid Array) package. An additional benefit of the mechanical mount Type-2 package is the relaxation of the thermal performance of the package. This relaxation is the result of eliminating the heat involved in the solder reflow process. During this solder reflow process the internal components within the BGA must withstand the short term heating required. The manufacturer and customer must both agree on the thermal performance required from the package, but generally it must, at minimum, support the operating and storage conditions of the IC-TROSA as specified in this document. Additionally, in the case where the host PCB thickness is equal or less than 1.5mm, it is recommended to add additional support structures underneath the host PCB in the area directly underneath the IC-TROSA. Support along the IC-

TROSA outer edges and center is highly recommended in order to ensure the PCB surface flatness which is necessary to achieve good contact force between the host PCB landing pads, the interposer, and the IC-TROSA landing pads.

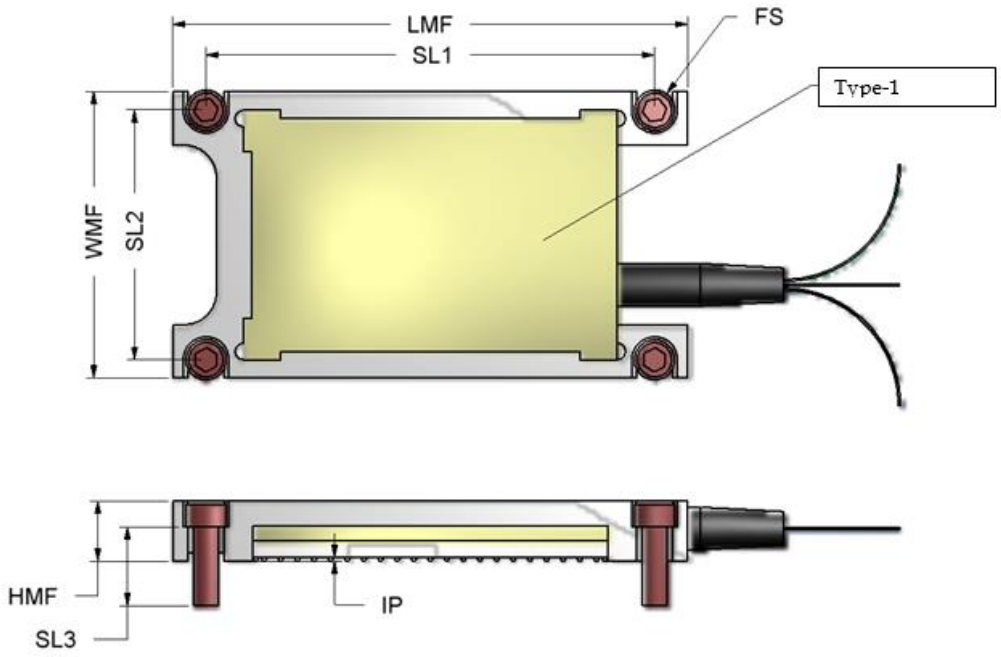


Figure 10-2: Type-1 IC-TROSA with Optional Mechanical Mounting Hardware

Table 10-5: Type-1 Mechanical Mounting Dimensions

Symbol	Parameter	Type-1 Mounting Frame Dimension			Notes
		Min	Nom	Max	
LMF	Length of mechanical mounting frame		31.0		
WMF	Width of mechanical mounting frame		17.20	17.44	Max width package only
HMF	Height of mechanical mounting frame			3.60	
SL1	Center distance of fastener along package length		27.0		
SL2	Center distance of fastener along package width		15.0		Max width package only
SL3	Length of Fastener	3.175			
FS	#0-80 Socket Head fastener	QTY: 4			
IP	Interposer height		0.30	0.40	Informational only. Actual values are specified by interposer vendor.

Notes:

1. Above dimensions are compliant with maximum width Type-1 dimensions. Reduced width Type-1 dimensions will require corresponding reductions for dimensions SL2 and WMF.
2. To prevent excessive compression of the interposer, a mechanical stop is usually required to be integrated into the compression frame between the frame and the host PCB. When designing the compression frame, the IC-TROSA user should follow interposer vendor's recommendations for minimum interposer compressed height.
3. It is recommended for the host application designer to perform modeling of the host PCB deformation underneath IC-TROSA while applying the specified compressive forces.

10.2. Type-2

10.2.1. Type-2 High Speed I/O Landing Pattern

The high speed flex cable described in Section 4.4 is soldered to the host board having a landing pattern as shown in Figure 10-3 and dimensions specified in Table 10-2.

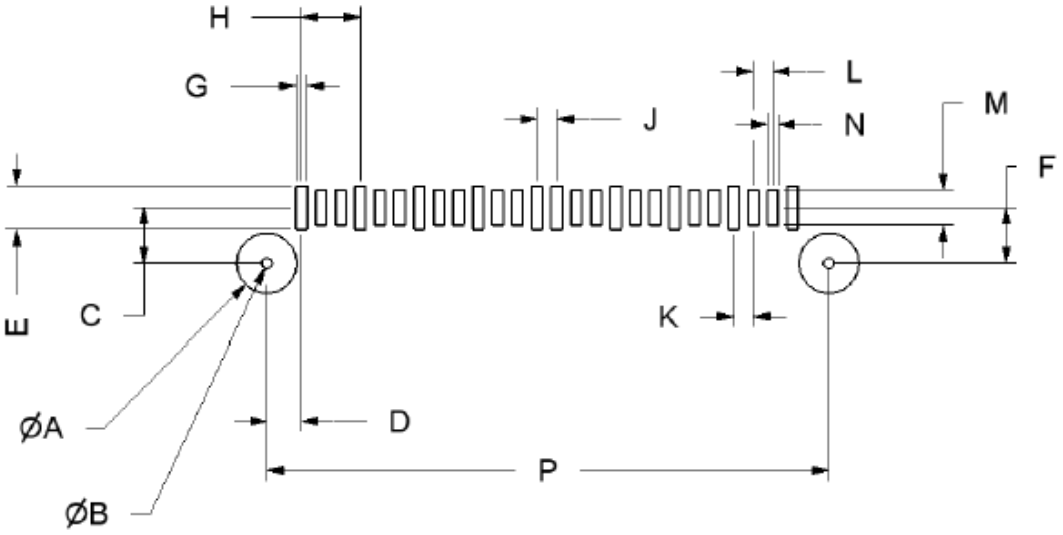


Figure 10-3: Type-2 High Speed I/O Host Board Landing Pattern (Top View)

Table 10-2: Type-2 High Speed I/O Host Board Landing Pattern Dimensions

Symbol	Parameter				Note
		Min	Nom	Max	
ØA	Alignment Feature Outer Diameter		1.375		1
ØB	Alignment Feature Inner Diameter		0.250		
C	Alignment Feature center to Pad horizontal center Line		1.270		
D	Alignment Feature center to nearest Ground Pad vertical centerline		0.813		
E	Ground Pad Length		1.000		
F	Alignment Feature center to Pad horizontal center Line		1.270		
G	Ground Pad width	0.190		0.260	2
H	Ground Pad pitch		1.350		
J	Ground Pad to adjacent Ground Pad vertical centerlines		0.450		
K	Ground Pad to adjacent Signal Pad vertical centerlines		0.450		
L	Signal Pad pitch		0.450		
M	Signal Pad length		0.800		
N	Signal Pad width	0.190		0.260	2
P	Alignment Feature center-to-center		12.875		

Notes:
1. Alignment Feature may be used for a physical guide pin, or as a visual alignment fiducial.
2. Pad width should be optimized for RF cross-talk performance based on target application's baud rate and host board signal routing design.

11. Management Interface

11.1. Management Interface Overview

An IC-TROSA implementation shall have a Two-Wire Interface (TWI) as detailed herein. The TWI shall be used for IC-TROSA control and monitoring functions in conjunction with the management register map as defined in this IA. The TWI, in the context of IC-TROSA, is a controller-to-controller digital interface. The IC-TROSA is defined as the *Client* or *Slave* device while the host hardware's controller is defined as the *Master* device. IC-TROSA's default bi-directional TWI data rate is 100kb/s (Standard Mode), but data rates of 400kb/s (Fast Mode) and 1Mb/s (Fast Mode Plus) may also be supported if the bus design includes appropriate measures to reduce capacitance as indicated in the detailed specification below. The host controller shall initiate communications with IC-TROSA at the Standard Mode data rate. Once communications is established between host and IC-TROSA controllers, the host may query the appropriate IC-TROSA control registers for the TWI and determine the TWI speed capabilities of each slave IC-TROSA. Subsequent TWI communications may then be made at the highest available rate supported by each slave device.

The TWI is comprised of a bi-directional *Data* (TWI_DAT) and a *Clock* (TWI_CLK) which is driven by the bus Master. The IC-TROSA utilizes a third hardware interface I/O (MOD_SEL) in order to select a single IC-TROSA as the active slave device among several IC_TROSA and/or other devices sharing the same TWI communications bus. The MOD_SEL input to IC-TROSA is controlled by the Master controller located on the host application. See Section 5 of this IA for more information regarding MOD_SEL specifications. An IC-TROSA having its MOD_SEL input pulled high shall not respond to, or acknowledge, any TWI communications.

IC-TROSA's TWI shall support clock stretching.

11.2. TWI Protocol Definitions

The following protocol definitions are consistent with SFF-8636 Revision 2.9:

START

A high-to-low transition of SDA with SCL high is a START. All two-wire bus operations shall begin with a START condition.

STOP

A low-to-high transition of SDA with SCL high is STOP condition. All two-wire bus operations shall end with a STOP condition.

ACKNOWLEDGE

After sending each 8-bit word, the side driving the 2-wire bus releases the SDA line for one bit time, during which the monitoring side of the 2-wire bus is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word. Write data operations shall be acknowledged by the slave for all bytes. Read data operations shall be acknowledged by the master for all but the final byte read, for which the master shall respond with a non-acknowledge (NACK) by permitting SDA to remain high and followed by a STOP.

11.3. TWI Flow Control

Write Flow Control is required for all register writes within B000h to BBFFh and C000h to C0FFh. Register bit B050.15 shall be used as the primary flow control bit. If B050.15 is clear then writes to IC-TROSA shall not be initiated. Bulk Data Transfer Block registers use the more efficient Sequential Write framing as shown in Figure 11-3.

TWI Write Flow Control functionality is specified to prevent possible overrun of commands from the host to module that may take relatively longer response time due to software processing, such as setting a laser channel. TWI Write Flow Control is achieved by defining a status register that has a bit which provides status regarding the completion of the last initiated

command and that could also generate an interrupt when command completion occurred. The Host is responsible for querying this register or waiting for a completion interrupt before issuing subsequent TWI Write transactions. No restrictions are present on TWI Read instructions. The Host may execute these commands anytime and as many times per second. The Host and Module interaction for a TWI Write transaction to command registers is illustrated in Figure 11-1.

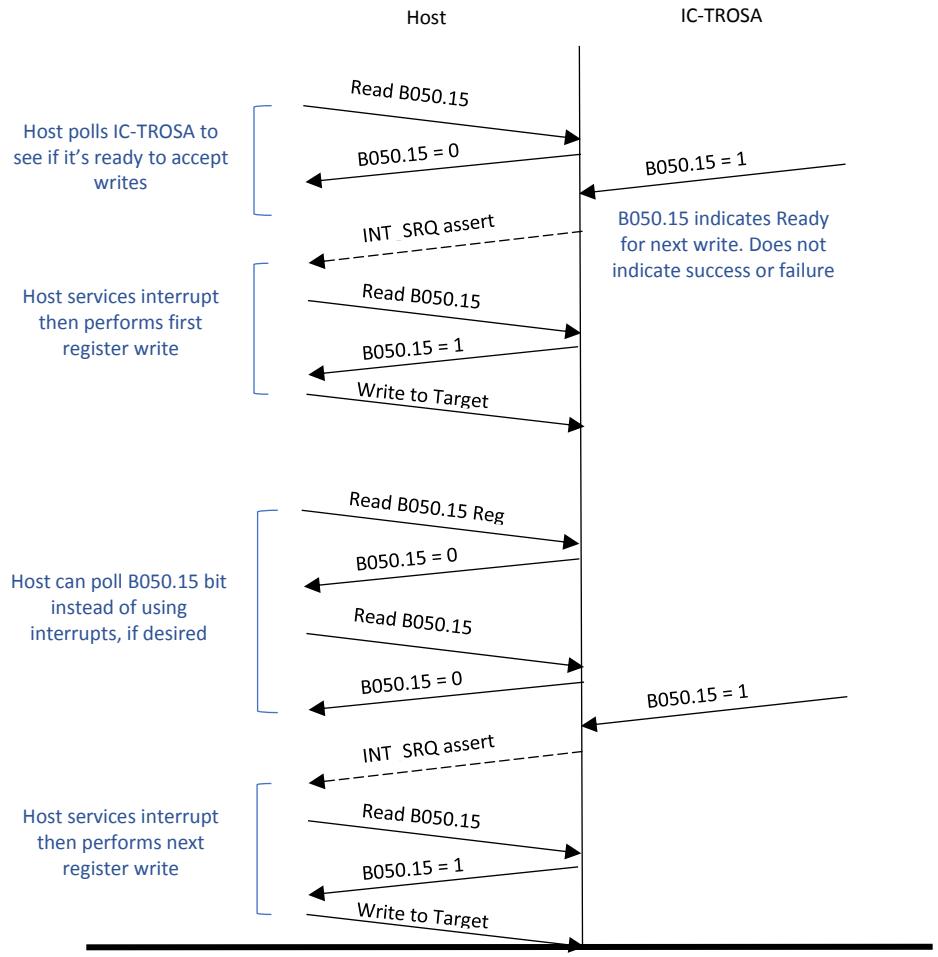


Figure 11-1: TWI Flow Control for Command Registers

Write flow control to BC00h to BDFFh Bulk Data Transfer Block is provided by the registers defined in Module Extended Functions Control Registers. If the Host writes a register with an inappropriate value for a field (e.g., power setting not in supported range), the module will set the command error status bit. In addition, the module will provide the register address at which the error occurred, the data which caused the error, a mask of the specific bits in the data which were in error, and a cause of the error. The host will be informed that an error occurred through the command error status bit, either by polling or as an interrupt. The host can then obtain further details about the error through the supporting Command Error registers. The intent

of this facility is to be a diagnostic aid for the host in situations where incorrect data for a register is written. It is not intended for circumstances where a command is correctly written to a register, but due to a device error could not be completed successfully, such as if a laser's channel cannot set successfully. Such errors are raised as a fault, alarm or warning as appropriate, via the GLB_ALRMn and INT_SRQ interrupt mechanism.

11.4. Framing & Addressing

The IC-TROSA TWI framing structure is similar to the structure specified by SFF-8636 Revision 2.9 with the exception that IC-TROSA uses 16-bit addressing and 16-bit data width for all read and write operations consistent with CFP-MSA-Management Interface Specification Version 2.6 r06a and OIF-CFP2-ACO-01.0.

IC-TROSA shall comply with SFF-8636 Revision 2.9 read/write operations with regard to:

- Slave memory address counter
- Current address read
- Random address read
- Sequential read
- Byte write
- Sequential write
- Write operation acknowledge polling

The IC-TROSA TWI supports in-frame addressing, but as a default operating mode this in-frame addressing is not dynamic and is set to a static 7-bit default address "1010000" and the 8th bit (WRITE) is used as a Read/Write control bit.

TWI error conditions shall result in the update of registers B00Ch though B00Fh to provide information on the source of the error condition.

11.3.1 Write Data Frame

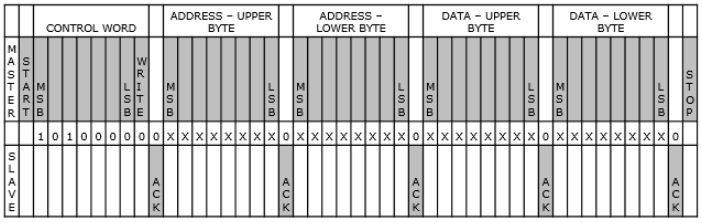


Figure 11-2: TWI "Write" Data Frame

- If only a partial address or data word is received, IC-TROSA shall discard the command and nothing shall be written. The Current Address shall be set to invalid, the Command Error bit B050h.14 shall be set, the Command Error Status

TWI Protocol Error bit B00Fh.10 shall be set, and the Command Error Address B00Ch shall be set to 0.

11.3.2 Sequential Write Data Frame

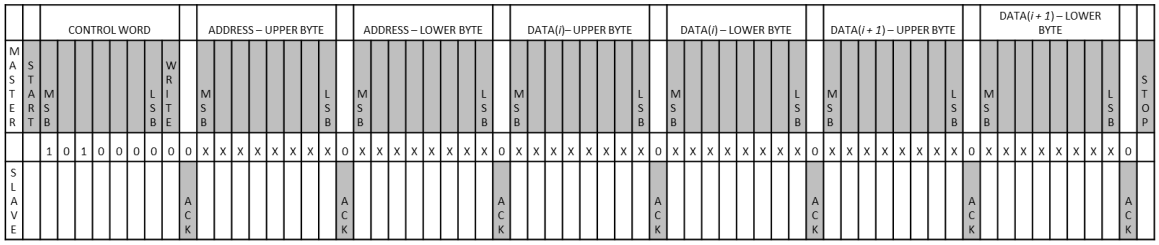


Figure 11-3: TWI "Sequential Write" Data Frame

- IC-TROSA shall support up to 512 sequential word writes to registers BC00h-BDFFh, Host-To-Module Bulk Data Transfer Block, without repeatedly sending slave address and memory address information.
- If only a partial data word is received, IC-TROSA shall discard the partial word write. The Current Address shall be set to the previous valid address, the Command Error bit B050h.14 shall be set, the Command Error Status TWI Protocol Error bit B00Fh.10 shall be set, the Command Error Address B00Ch shall be set to the address of the partial word, and the Command Error Data shall be set to the partial word MSB.
- Sequential Write Data Framing may not be used for registers where flow control is required according to Section 11.3 of this IA.

11.3.3 Current Address Read Data Frame

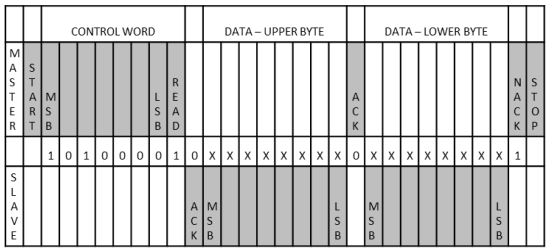


Figure 11-4: TWI "Current Address Read" Data Frame

- If NACK/STOP is received before the Upper and Lower Byte are read, IC-TROSA shall set the Current Address to invalid. The Command Error bit B050h.14 shall be set, the Command Error Status TWI Protocol Error bit B00Fh.10 shall be set, and the Command Error Address B00Ch shall be set to 0.

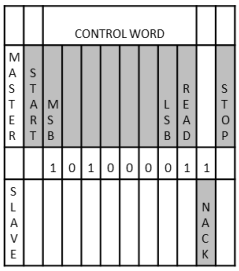


Figure 11-5: TWI "Current Address Read" with Invalid Current Address

- If the Current Address is invalid, IC-TROSA shall NACK the command. The Command Error bit B050h.14 shall be set, the Command Error Status TWI Protocol Error bit B00Fh.10 shall be set, and the Command Error Address B00Ch shall be set to 0.

11.3.4 Random Read Data Frame

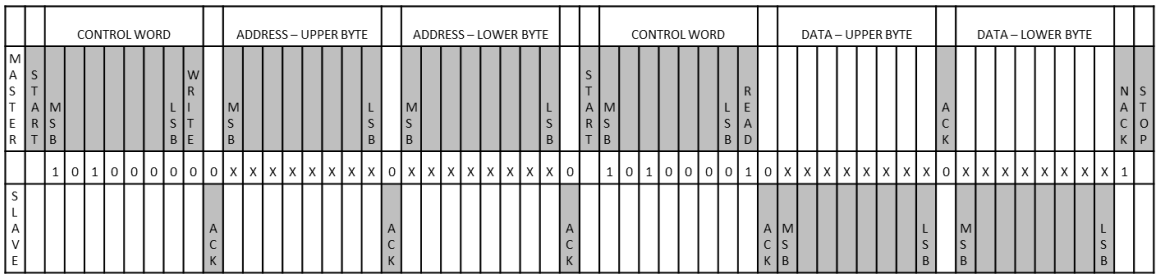


Figure 11-6: TWI "Random Read" Data Frame

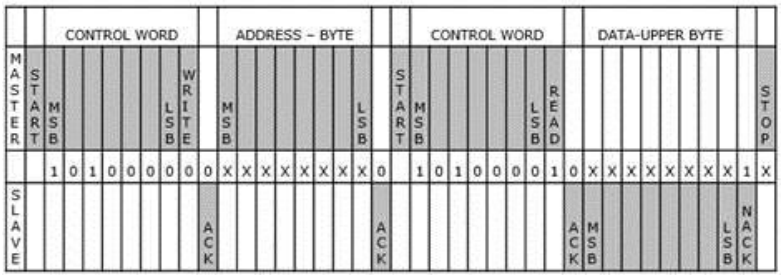


Figure 11-7: TWI "Random Read" with Invalid Address Sent

- If only a partial address is received, IC-TROSA shall NACK the Upper Data Byte read. The Current Address shall be set to invalid, the Command Error bit B050h.14 shall be set, the Command Error Status TWI Protocol Error bit B00Fh.10 shall be set, and the Command Error Address B00Ch shall be set to 0.

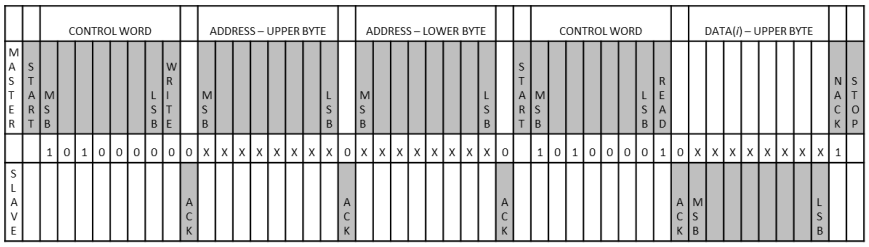


Figure 11-8: TWI "Random Read" with Invalid Read Sequence

- If NACK/STOP is received before the Upper and Lower Byte are read, IC-TROSA shall set the Current Address to invalid. The Command Error bit B050h.14 shall be set, the Command Error Status TWI Protocol Error bit B00Fh.10 shall be set, and the Command Error Address B00Ch shall be set to 0.

11.3.5 Sequential Current Address Read Data Frame

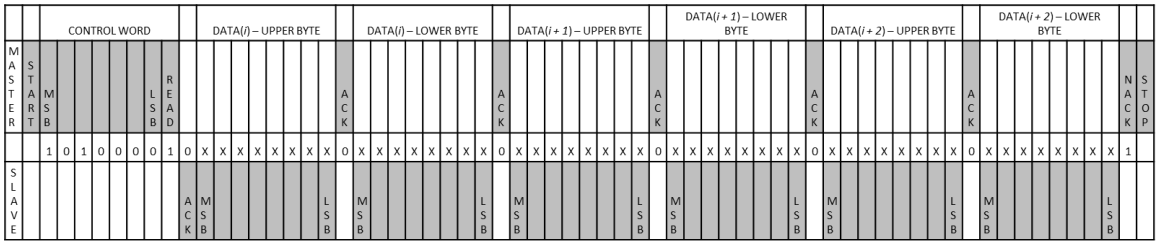


Figure 11-9: TWI "Sequential Read" at Current Address

- If the Current Address is invalid, IC-TROSA shall NACK the command. The Command Error bit B050h.14 shall be set, the Command Error Status TWI Protocol Error bit B00Fh.10 shall be set, and the Command Error Address B00Ch shall be set to 0.
- If NACK/STOP is received before the Upper and Lower Byte are read, IC-TROSA shall set the Current Address to invalid. The Command Error bit B050h.14 shall be set, the Command Error Status TWI Protocol Error bit B00Fh.10 shall be set, and the Command Error Address B00Ch shall be set to 0.

11.3.6 Sequential Random Read Data Frame

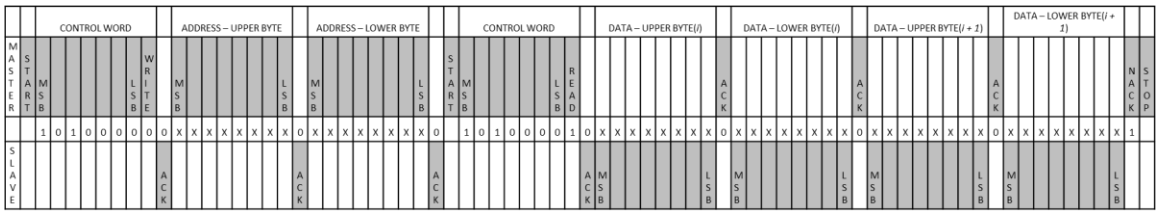


Figure 11-10: TWI "Sequential Read" Starting with Random Read

- If only a partial address is received, IC-TROSA shall NACK the Upper Data Byte read. The Current Address shall be set to invalid, the Command Error bit

B050h.14 shall be set, the Command Error Status TWI Protocol Error bit B00Fh.10 shall be set, and the Command Error Address B00Ch shall be set to 0.

- If NACK/STOP is received before the Upper and Lower Byte are read, IC-TROSA shall set the Current Address to invalid. The Command Error bit B050h.14 shall be set, the Command Error Status TWI Protocol Error bit B00Fh.10 shall be set, and the Command Error Address B00Ch shall be set to 0.

11.5. Digital Communications Hardware Interface

The TWI Data and Clock lines utilize an open drain design employing pull-up resistors to VDD which, in the case of the IC-TROSA implementation the term "VDD" is replaced with "Primary Power Supply P0" (see Figure 5-1 and Figure 5-2). The use of P0 power supply allows for managed initialization of the IC-TROSA's internal controller and the TWI for communications. Further configuration by the host controller is then possible prior to other IC-TROSA functions being enabled.

11.5.1. Communications Interface Voltage and Timing Specifications

The key voltage and control specifications are summarized in Table 11-1. The external pull-up devices connected to the bus lines must be adapted to accommodate the shorter maximum permissible rise time for the Fast-mode bus. In Fast Mode, and for bus loads up to 200 pF, the pull-up device for each bus line can be a resistor; for bus loads between 200 pF and 400 pF, the pull-up device can be a current source (3 mA max.) or a switched resistor circuit.

The drivers in Fast-mode Plus parts are strong enough to satisfy the Fast-mode Plus timing specification with the same 400 pF load as Standard-mode parts. To be backward compatible with Standard-mode, they are also tolerant of the 1000 ns rise time of Standard-mode parts. In applications where only Fast-mode Plus parts are present, the high drive strength and tolerance for slow rise and fall times allow the use of larger bus capacitance as long as set-up, minimum LOW time and minimum HIGH time for Fast-mode Plus are all satisfied and the fall time and rise time do not exceed the 300 ns t_f and 1000 ns t_r specifications of Standard-mode. Bus speed can be traded against load capacitance to increase the maximum capacitance by about a factor of ten.

Table 11-1 outlines the electrical characteristics of a Two-Wire Interface based in NXP I2C Bus Specification and User Manual Rev-6 with "VDD" being replaced by "P0" to indicate the IC-TROSA's TWI pull-up resistors being tied to IC-TROSA primary power supply P0.

Table 11-1: Two-Wire Electrical Characteristics [1]

Sym	Parameter	Condition	Standard Mode (100Kb/s) Default Mode		Fast Mode (400Kb/s) Optional Mode		Fast Mode Plus (1Mb/s) Optional Mode		Unit
			Min	Max	Min	Max	Min	Max	
V_{IL}	LOW input[3]		-0.5	0.3P0	-0.5	0.3P0	-0.5	0.3P0	V
V_{IH}	HIGH input[3]		0.7P0	[3]	0.7P0	[3]	0.7P0	[3]	V
V_{hys}	Hysteresis of inputs		--	--	0.05P0	--	0.05P0	--	V
V_{OL1}	LOW output 1	Open drain or collector, 3mA sink, P0>2V[4]	0	0.4	0	0.4	0	0.4	V
V_{OL2}	LOW output 2	Open drain or collector, 2mA sink[5], P0≤2V	--	--	0	0.2P0	0	0.2P0	V
I_{OL}	LOW output current	V_{OL}=0.4V	3	--	3	--	20	--	mA
		V_{OL}=0.6V[6]	--	--	6	--	--	--	mA
t_{OF}	Output fall time V_{IHmin} to V_{ILmax}		--	250[7]	20x(P0/5.5V) [8]	250[6]	20x(P0/5.5V) [8]	120[9]	ns
t_{SP}	Pulse width of spikes to be suppressed		--	--	0	50[10]	0	50[10]	ns
I_i	Input current each I/O pin[12]	0.1P0<V_i<0.9 $P0_{max}$	-10	+10[11]	-10[11]	+10[11]	-10[11]	+10[11]	µA
C_i	Capacitance for each I/O pin		--	10	--	10	--	10	pF

Notes:

1. In this table IC-TROSA primary power supply indicator “P0” replaces the generic term “VDD” as the TWI power supply voltage.
2. Some legacy Standard-Mode devices had fixed input levels of V_{IL}=1.5V and V_{IH}=3.0V.
3. Maximum VIH=P0max +0.5V or 5.5V whichever is lower.
4. The same resistor value to drive 3mA at 3.0V provides the same RC time constant when using <2V with a smaller current draw.
5. In order to drive full bus load at 400KHz, 6mA I_{OL} is required at 0.6V V_{OL}. Parts meeting this specification can still function, but not at 400KHz and 400pF.
6. The maximum t_F for SDA and SCL (300ns) is longer than the specified maximum t_{OF} for the output stages (250ns). This allows series protection resistors (Rs) to be placed between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum t_F.
7. Necessary to be backwards compatible with Fast Mode.
8. In Fast Mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
9. Input filters on the SDA and SCL inputs suppress noise spikes of less than 50ns.
10. If P0 is switched off, I/O pins of Fast Mode and Fast Mode Plus devices must not obstruct the SDA and SCL lines.
11. Special purpose devices such as multiplexers and switches may exceed this capacitance because they connect multiple paths together.

Table 11-2: Two-Wire Interface Timing & RC Specifications[1]

Sym	Parameter	Condition	Standard Mode (100Kb/s) Default Mode		Fast Mode (400Kb/s) Optional Mode		Fast Mode Plus (1Mb/s) Optional Mode		
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL frequency		0	100	0	400	0	1000	KHz
MOD_ SEL_{SU}	Module Select SETUP time	Time period before start of bus sequence	2	--	2	--	2	--	ms
MOD_ SEL_{hold}	Module Select HOLD time	MOD_SEL stable after completion of bus sequence	2	--	2	--	2	--	ms
$t_{HD;STA}$	Hold time START condition	1st clock pulse generated after this period	4.0	--	0.6	--	0.26	--	µs
t_{LOW}	Low period of SCL		4.7	--	1.3	--	0.5	--	µs
t_{HIGH}	High period of SCL		4.0	--	0.6	--	0.26	--	µs
$t_{SU;STA}$	Set-up time for repeated START condition		4.7	--	0.6	--	0.26	--	µs
$t_{HD;DAT}$	Data hold time[2]		0[3]	--[4]	0[3]	--[4]	0	--	µs
$t_{SU;DAT}$	Data setup time		250	--	100[5]	--	50	--	ns
t_r	Rise time of SDA and SCL		--	1000	20	300	--	120	ns
t_f	Fall time of SDA and SCL[3] [6] [7]		--	300	20x(P0/ 5.5V)	300	20x(P 0/5.5 V) [8]	120	ns
$t_{SU;STO}$	Setup time for STOP		4.0	--	0.6	--	0.26	--	µs
t_{BUF}	Bus free time between STOP and START		20	--	20	--	1	--	µs
C_b	Capacitive load for		--	400	--	400	--	550	pF

	each bus line[9]								
$t_{VD;DAT}$	Data valid time[10]		--	3.45[4]	--	0.9[4]	--	0.45[4]	µs
$t_{VD;ACK}$	Data valid acknowledge time[11]		--	3.45[4]	--	0.9[4]	--	0.45[4]	µs
Clock_Hold	Clock Holdoff / Clock Stretching	Slave hold SCL line low	--	500	--	500	--	500	µs
V_{nL}	Noise margin @ LOW level	For each connected device, incl hysteresis	0.1P0	--	0.1P0	--	0.1P0	--	V
V_{nH}	Nose margin @ HIGH level	For each connected device, incl hysteresis	0.2P0	--	0.2P0	--	0.2P0	--	V
$R_{P(max)}$	Pull-up resistor value for SDA and SCL lines		$Rp(\max) = \mathrm{tr}/(0.8473 \times Cb)$						

Notes:

1. In this table IC-TROSA primary power supply indicator "P0" replaces the generic term "VDD" as the TWI power supply voltage.
2. All values referred to $V_{IH(min)}$ and $V_{IL(max)}$ levels.
3. $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL, applies to data in the transmission and the acknowledge.
4. A device must internally provide a hold time of at least 300ns for the SDA signal (with respect to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
5. The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard Mode and Fast Mode, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the setup time before it releases the clock.
6. A Fast-mode bus device can be used in a Standard-mode bus system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line
   $t_{r(max)} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.
7. The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
8. In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
9. Necessary to be backwards compatible to Fast-mode.
10. The maximum bus capacitance allowable may vary from this value depending on the actual operating voltage and frequency of the application.
11. $t_{VD;DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

12. $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

11.6. State Machine

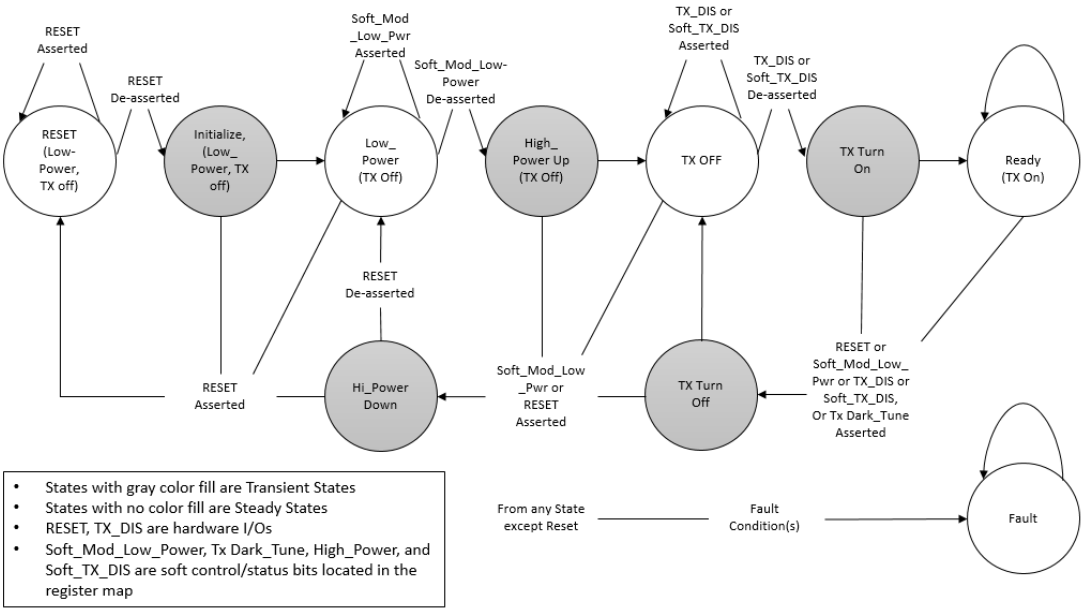


Figure 11-11: IC-TROSA State Machine

11.7. Module Power Up/Down

The following Figures demonstrate the sequence of primary events and associated IC-TROSA states during IC-TROSA power-up and power-down.

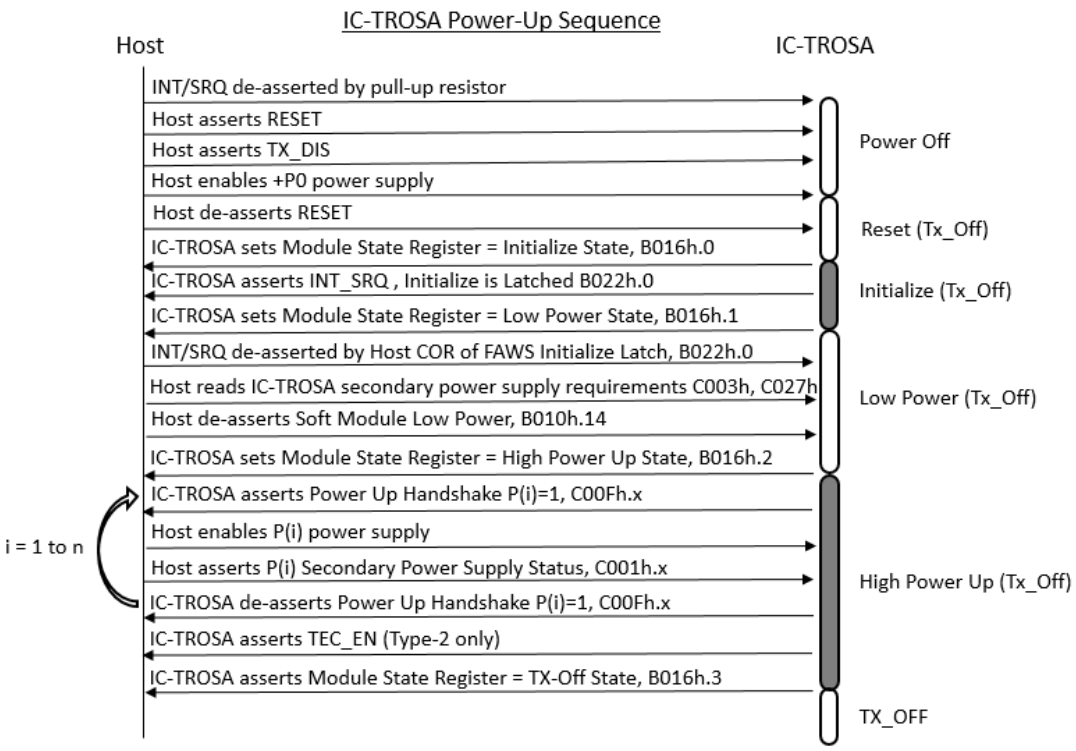


Figure 11-12: Power-Up Sequence

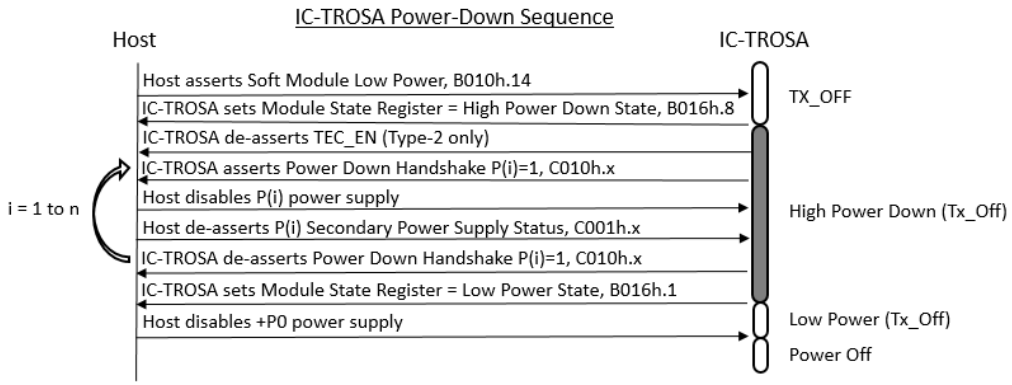


Figure 11-13: Power-Down Sequence

11.8. Type-2 Tx Channel Tuning

The following Tx Channel Tuning sub-sections apply only to Type-2 IC-TROSA.

11.8.1. **Changing Tx Channel on Defined Grid ("Dark Tuning")**

The Tx channel change sequence is illustrated in Figure 11-14. If a Tx channel change command (write to register B400h) is received when the

IC-TROSA is in the Ready State (Tx-On), the IC-TROSA will transition from Ready (Tx-On) through Tx-Turn-off, Tx-Off (where the laser is tuned), Tx-Turn-on and back to Ready (Tx-On). This is called “Dark Tuning”. If the IC-TROSA is already in the Tx-Off state when a TX channel change command is received, then the module will remain in the Tx-Off state.

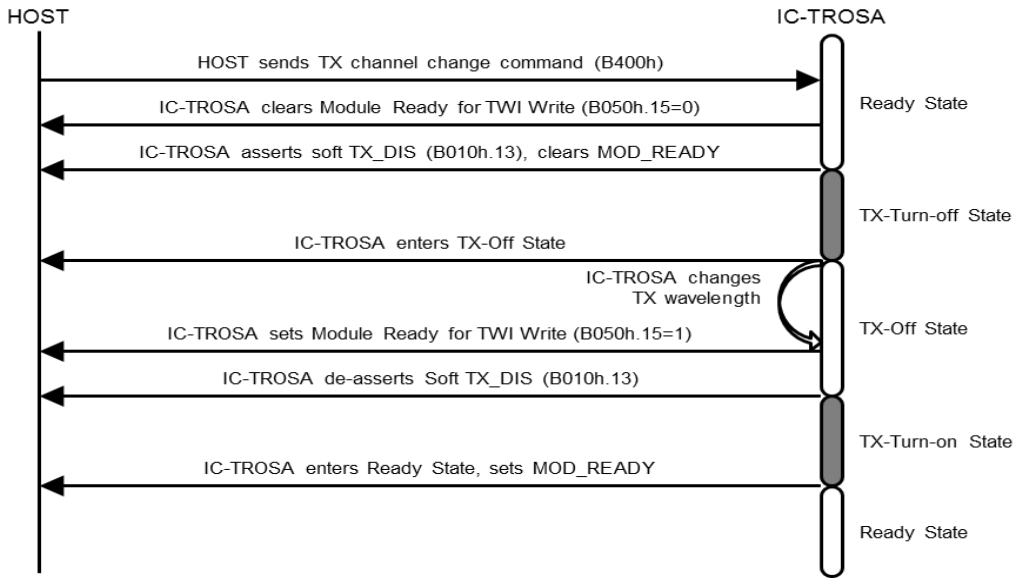


Figure 11-14: Tx Channel Change

From the Ready State, when the Host submits the Tx channel change command (B400h), the IC-TROSA module first de-asserts the “Module Ready for TWI Write” (B050h.15 = 0) to inform the Host a channel change operation is now in progress. The module then asserts Soft_TX_DIS (B010h.13) to turn off the optical output and transitions the module to the Tx-Off State. After the channel change sequence completes the IC-TROSA module sets the “Module Ready for TWI Write” (B050h.15 = 1) to inform the completion of the channel change to the Host. The module then de-asserts Soft_TX_DIS (B010h.13) to turn on the optical output power and transition the module to the Ready State.

The Host should not assert/de-assert Soft_TX_DIS (B010h.13) during the channel change operation, and the use of hard TX_DIS is discouraged. When the B430h Tx Fine Tune Frequency (FTF) register is called from the Ready State (Tx-On), the corresponding laser source output remains on and the IC-TROSA remains in the Ready State (Tx-On). This is called bright tuning. Register BB0Ah.15 (Tx Fine Tune Frequency B430h In Progress) will remain asserted as long as the laser is tuning

11.8.2. Changing Tx Channel Using High Resolution Tuning Registers

To enable use of the high-resolution tuning registers, the Host should set bit 10 in register B400h to 1. This can only be done when the module is in

the Tx-Off State. The Tx channel (wavelength) change sequence is illustrated in Figure 11-15. From the Ready State (Tx-On), the Host should first disable the transmitter by asserting either the Soft_TX_DIS (B010h.13) or hard TX_DIS. Once the module is in the Tx-Off State, the Host can write to the high-resolution tuning registers. In order to trigger a channel change, the Host needs to write to all three high resolution tuning registers (B490h, B491h, B492h), even if any of the register values remains unchanged. Upon completion of the third write command, the IC-TROSA module first de-asserts the "Module Ready for TWI Write" (B050h.15 = 0) to inform the Host a channel change operation is now in progress. After the channel change sequence completes the IC-TROSA module sets the "Module Ready for TWI Write" (B050h.15 = 1) to inform the completion of the channel change to the Host. The Host can then de-assert Soft_TX_DIS (B010h.13) and/or hard TX_DIS to turn on the optical output power and transition the module to the Ready State (Tx-On).

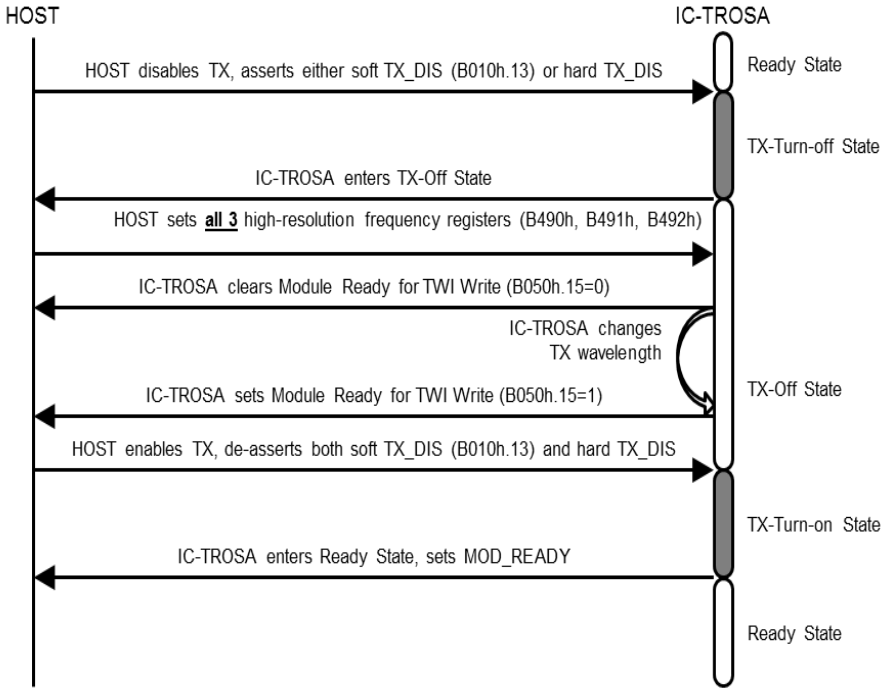


Figure 11-15: Tx Wavelength Change Using High Resolution Tuning Registers

11.9. Type-1 Tx_Turn_On

Type-1 IC-TROSA utilizes an external laser source. Therefore, the Host application manages all set points associated with the laser. The Type-1 IC-TROSA utilizes the TX_DIS hardware input to determine Host's request for state changes between TX_ON and TX_OFF. Type-1 must also utilize internal optical power monitor information available in the Tx Subsystem Registers BB11h through BB2Bh to verify sufficient optical power is present within its internal TX subsystem to achieve proper operation and phase control of the modulators. Since the Type-1 has no direct feedback control path to the

laser, the TX_LOSF alarm is used to inform the Host controller of a general performance alarm regarding the TX. Many TX failure conditions, including inability to properly achieve desired power levels, should trigger the TX_LOSF alarm. If alarm is enabled by setting bit B200h.7, a Lane TX_LOSF alarm will activate the SRQ_INT hardware output to the Host.

11.10. Behavior of FAWS in IC-TROSA Module States

IC-TROSA FAWS behavior mirrors the FAWS behavior as described in CFP-MSA-Management Interface Specification 2.6 r06a Section 4.5. The IC-TROSA module shall eliminate the spurious FAWS signals in various IC-TROSA module states based on a set of rules previously defined by CFP MSA. All GLB_ALRM contributing FAWS are classified into three types: FAWS_TYPE_A, FAWS_TYPE_B, and FAWS_TYPE_C. The applicable TYPE for each FAWS signal is listed in Table 11-4: IC-TROSA Register Map.

Table 11-3: Behavior of FAWS TYPE in Different IC-TROSA States

FAWS TYPE	IC-TROSA Module State									
	Reset	Initialize	Low-Power	Hi-Power-Up	TX-Off	TX-Turn-On	Ready	TX-Turn-Off	Hi-Power-Down	Fault
TYPE_A	OFF	OFF	A	A	A	A	A	A*	A*	A
TYPE_B	OFF	OFF	OFF	OFF	A	A	A	A*	OFF	A
TYPE_C	OFF	OFF	OFF	OFF	OFF	OFF	A	OFF	OFF	A
A=FAWS sources are allowed (i.e. not masked). Status and Latch registers are functional. A/D values reflect the actual measurements.										
A*=OFF if RESET is asserted										
OFF=FAWS sources (status bits) are gated off by IC-TROSA. As a result corresponding latch registers will not capture (latch) new events. Latch and Enable registers are kept unchanged from previous states. A/D values reflect the actual measurements, although they all may not be available in the Low-Power state depending upon module implementation.										

11.11. Firmware Upgrades

IC-TROSA Firmware upgrades generally follow the CFP-MIS procedures and register structure for firmware upgrades. IC-TROSA firmware downloads do not affect traffic or performance monitoring. However, during the execution of a “Run Image” command performance monitoring may be suspended and traffic may be disrupted.

Further details on the use of Module Upgrade related registers can be found in CFP MIS Section 6.2.6 and 6.2.9.1

The following registers are used for IC-TROSA firmware upgrades:

- B04Ch Module Upgrade Data
- B04Dh Module Upgrade Control
- B050h Module Extended Functions Status

- B051h Module Upgrade Status
- BC00h Host to Module Bulk Data Transfer Block
- BE00h Module to Host Bulk Data Transfer Block

11.11.1. Firmware Upgrade Procedure

1. Host initiates a “Download Start” by setting B04Dh.[15:12] to 0001b.
2. Host polls register B050h until bit 15 is set.
3. Host polls register B051h to determine if bits 15:14 equal a value of 1.
4. Host reads a record from the hex image file (or binary image file).
5. Host calculates CRC-32 checksum of record.
6. Host transmits bytes of record, and CRC-32 checksum to BC00h+ register space.
7. Host signals that block is ready by setting bit B04Ch.15 to 1.
8. Host polls register B050h until bit 15 is set.
9. Host polls register B04Ch until bit B04Ch.15 to be cleared to 0. Bits [14:12] indicate whether the block transfer was successful, and if not, why not.
10. Host repeats above steps (4 thru 9) until all blocks are transmitted.
11. Host writes the value 2 to bits 15 thru 12 in Register B04Dh (Download Complete)
12. Host polls register B050h until bit 15 is set.
13. Host polls register B051h to determine if bits 15:14 equal a value of 1.
14. Host writes the value 4 to bits 15 thru 12 in register B04Dh (Upgrade Command=Run Image-B, assuming we started with Image-A as the committed image)
15. Once successfully booted from Image B and new FW load is validated, host writes the value “9” to bits 15:12 in register B04Dh (Upgrade Command=Commit Image-B)

11.12. IC-TROSA Register Map

Acronym definitions for Table 11-4: IC-TROSA Register Map

Required / Optional:

R – Required for Type-1 and Type-2
R1 – Required only for Type-1
R2- Required only for Type-2
O – Optional for Type-1 and Type-2

Access Type:

RO – Read Only
WO – Write Only
RW – Read and Write
COR – Clear On Read (transition triggered)
SC – Self Clearing
LH – Latched High (Set on rising edge)

Table 11-4: IC-TROSA Register Map

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
8000-801D	30				IC-TROSA NVR 1. Basic ID Registers	Reserved	Reserved	N/A
801E	1	7-0	RO	R	IC-TROSA NVR 1. Basic ID Registers	Maximum Power Consumption in Low Power Mode	Unsigned 8 bit value * 20 mW. Value 0 = undefined.	20mW
801F	1				IC-TROSA NVR 1. Basic ID Registers	Reserved	Reserved	N/A
8020	1				IC-TROSA NVR 1. Basic ID Registers	Reserved	Reserved	N/A
8021	16	7-0	RO	R	IC-TROSA NVR 1. Basic ID Registers	Vendor Name	Vendor (manufacturer) name in any combination of letters and/or digits in ASCII code, left aligned and padded on the right with ASCII spaces (20h). The vendor name shall be the full name of the corporation, a commonly accepted abbreviation of the name or the stock exchange code for the corporation. Vendor is the IC-TROSA module vendor.	N/A

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
8031	3				IC-TROSA NVR 1. Basic ID Registers	Reserved	Reserved	N/A
8034	16	7-0	RO	R	IC-TROSA NVR 1. Basic ID Registers	Vendor Part Number	Vendor (manufacturer) part number in any combination of letters and/or digits in ASCII code, left aligned and padded on the right with ASCII spaces (20h). All zero value means undefined. Vendor is the IC-TROSA module vendor.	N/A
8044	16	7-0	RO	R	IC-TROSA NVR 1. Basic ID Registers	Vendor Serial Number	Vendor (manufacturer) serial number in any combination of letters and/or digits in ASCII code, left aligned and padded on the right with ASCII spaces (20h). All zero means undefined.	N/A
8054	8	7-0	RO	R	IC-TROSA NVR 1. Basic ID Registers	Date Code	Vendor (manufacturer) date code in ASCII characters, in the format YYYYMMDD (e.g., 20090310 for March 10, 2009). One character at each TWI address. 1st letter of above format is at smaller address.	N/A
805C	2	7-0	RO	O	IC-TROSA NVR 1. Basic ID Registers	Lot Code	A 2-byte value representing lot code in any combination of letters and/or digits in ASCII code.	N/A
805E	10				IC-TROSA NVR 1. Basic ID Registers	Reserved	Reserved	N/A
8068	1	7-0	RO	R	IC-TROSA NVR 1. Basic ID Registers	OIF IC-TROSA Hardware Specification Revision Number	This register indicates the OIF IC-TROSA Hardware Specification version number. The 8 bits are used to represent the version number times 10. This yields a max of 25.5 revisions.	N/A

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
8069	1	7-0	RO	R	IC-TROSA NVR 1. Basic ID Registers	OIF IC-TROSA Management Interface Specification Revision Number	This register indicates the OIF IC-TROSA Management Interface Specification / Implementation Agreement version number supported by the transceiver. The 8 bits are used to represent the version number times 10. This yields a max of 25.5 revisions.	N/A
806A	2	7-0	RO	R	IC-TROSA NVR 1. Basic ID Registers	Module Hardware Version Number	A two-register vendor specified number in the format of x.y with x at lower address and y at higher address. All zero value indicates undefined.	N/A
806C	2	7-0	RO	R	IC-TROSA NVR 1. Basic ID Registers	Module Firmware Version Number	A two-register vendor specified number in the format of x.y with x at lower address and y at higher address. All zero value indicates undefined.	N/A
806E-807A	13				IC-TROSA NVR 1. Basic ID Registers	Reserved	Reserved	N/A
807B	2	7-0	RO	O	IC-TROSA NVR 1. Basic ID Registers	Module Firmware B Version Number	A two-register vendor specified number in the format of x.y with x at lower address and y at higher address.	N/A
807D	1	7-0	RO	R	IC-TROSA NVR 1. Basic ID Registers	Maximum TWI Ready Time	An 8-bit unsigned number representing Maximum TWI Ready Time due to module software upgrade introduced TWI down time in seconds.	
807E	1				IC-TROSA NVR 1. Basic ID Registers	Reserved	Reserved	N/A
807F	1	7-0	RO	R	IC-TROSA NVR 1. Basic ID Registers	IC-TROSA NVR 1 Checksum	The 8-bit unsigned sum of all NVR 1 contents from address 8000h	N/A

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							through 807Eh inclusive.	
8080	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	Transceiver Temp High Alarm Threshold	These thresholds are a signed 16-bit integer with LSB = 1/256 of a degree Celsius representing a range from -128 to + 127, 255/256 degree C. Valid range is between – 40 and +125C." MSB stored at low address, LSB stored at high address.	1/256 degC
8082	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	Transceiver Temp High Warning Threshold	(See above)	
8084	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	Transceiver Temp Low Warning Threshold	(See above)	
8086	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	Transceiver Temp Low Alarm Threshold	(See above)	
8088	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	+P0 Primary Power Supply High Alarm Threshold	These thresholds are an unsigned 16-bit integer with LSB = 0.1 mV, representing a range of voltage from 0 to 6.5535 V. MSB stored at low address, LSB stored at high address.	0.1mV
808A	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	+P0 Primary Power Supply High Warning Threshold	(see above)	0.1mV
808C	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	+P0 Primary Power Supply Low Warning Threshold	(see above)	0.1mV
808E	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	+P0 Primary Power Supply Low Alarm Threshold	(see above)	0.1mV
8090	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	SOA Bias Current High Alarm Threshold	These threshold values are an unsigned 16-bit integer with LSB =8 uA by default, representing max value of 524.280 mA. MSB stored at low address, LSB stored at high address.	8 uA
8092	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	SOA Bias Current High Warning Threshold	(See above)	8 uA

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
8094	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	SOA Bias Current Low Warning Threshold	(See above)	8 uA
8096	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	SOA Bias Current Low Alarm Threshold	(See above)	8 uA
8098	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	Auxiliary 1 Monitor High Alarm Threshold		
809A	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	Auxiliary 1 Monitor High Warning Threshold		
809C	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	Auxiliary 1 Monitor Low Warning Threshold		
809E	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	Auxiliary 1 Monitor Low Alarm Threshold		
80A0	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	Auxiliary 2 Monitor High Alarm Threshold		
80A2	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	Auxiliary 2 Monitor High Warning Threshold		
80A4	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	Auxiliary 2 Monitor Low Warning Threshold		
80A6	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	Auxiliary 2 Monitor Low Alarm Threshold		
80A8	2	7-0	RO	R2	IC-TROSA NVR 2. Extended ID Registers	Laser Bias Current High Alarm Threshold	Alarm and warning thresholds for measured laser bias current. MSB stored at low address, LSB stored at high address. Measured laser bias current in %, a 16-bit unsigned integer with LSB = 100%/65535, representing a total measurement range of 0 to 100%	
80AA	2	7-0	RO	R2	IC-TROSA NVR 2. Extended ID Registers	Laser Bias Current High Warning Threshold	(See above)	
80AC	2	7-0	RO	R2	IC-TROSA NVR 2. Extended ID Registers	Laser Bias Current Low Warning Threshold	(See above)	
80AE	2	7-0	RO	R2	IC-TROSA NVR 2. Extended ID Registers	Laser Bias Current Low Alarm Threshold	(See above)	
80B0	2	7-0	RO	R	IC-TROSA NVR 2. Extended ID Registers	TX Output Power High Alarm Threshold	Alarm and warning thresholds for measured transmitter output	See also B330h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							power. MSB stored at low address, LSB stored at high address. 16-bit signed integer with LSB=0.01dBm	
80B2	2	7-0	RO	R	IC-TROSA NVR 2. Extended ID Registers	TX Output Power High Warning Threshold	(See above)	
80B4	2	7-0	RO	R	IC-TROSA NVR 2. Extended ID Registers	TX Output Power Low Warning Threshold	(See above)	
80B6	2	7-0	RO	R	IC-TROSA NVR 2. Extended ID Registers	TX Output Power Low Alarm Threshold	(See above)	
80B8	2	7-0	RO	R2	IC-TROSA NVR 2. Extended ID Registers	Laser Temperature High Alarm Threshold	Alarm and warning thresholds for measured received input power. Internally measured temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 degC. valid range between –40 and +125C. Minimum accuracy is +/- 3 degC over temperature range. MSB stored at low address, LSB stored at high address.	
80BA	2	7-0	RO	R2	IC-TROSA NVR 2. Extended ID Registers	Laser Temperature High Warning Threshold	(See above)	
80BC	2	7-0	RO	R2	IC-TROSA NVR 2. Extended ID Registers	Laser Temperature Low Warning Threshold	(See above)	
80BE	2	7-0	RO	R2	IC-TROSA NVR 2. Extended ID Registers	Laser Temperature Low Alarm Threshold	(See above)	
80C0	2	7-0	RO	R	IC-TROSA NVR 2. Extended ID Registers	Receive Optical Power High Alarm Threshold	Alarm and warning thresholds for measured received input power. A 16-bit signed integer with LSB = 0.01 dBm. MSB stored at low address, LSB stored at high address.	

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
80C2	2	7-0	RO	R	IC-TROSA NVR 2. Extended ID Registers	Receive Optical Power High Warning Threshold	(See above 80C0h description)	
80C4	2	7-0	RO	R	IC-TROSA NVR 2. Extended ID Registers	Receive Optical Power Low Warning Threshold	(See above 80C0h description)	
80C6	2	7-0	RO	R	IC-TROSA NVR 2. Extended ID Registers	Receive Optical Power Low Alarm Threshold	(See above 80C0h description)	
80C8-80DF	24				IC-TROSA NVR 2. Extended ID Registers	Reserved	Reserved	N/A
80E0	2	7-0	RO	R	IC-TROSA NVR 2. Extended ID Registers	TX Modulator Bias High Alarm	Definition specified by module vendor. MSB stored at low address. LSB stored at high address.	
80E2	2	7-0	RO	R	IC-TROSA NVR 2. Extended ID Registers	TX Modulator Bias High Warning	Definition specified by module vendor. MSB stored at low address. LSB stored at high address.	
80E4	2	7-0	RO	R	IC-TROSA NVR 2. Extended ID Registers	TX Modulator Bias Low Warning	Definition specified by module vendor. MSB stored at low address. LSB stored at high address.	
80E6	2	7-0	RO	R	IC-TROSA NVR 2. Extended ID Registers	TX Modulator Bias Low Alarm	Definition specified by module vendor. MSB stored at low address. LSB stored at high address.	
80E8	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	Host Configured Receive Optical Power High Alarm Permissible Minimum Threshold	A 16-bit signed integer with LSB = 0.01 dBm. MSB stored at low address, LSB stored at high address. 0000h indicates feature not supported and hence this range check is skipped.	N/A
80EA	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	Host Configured Receive Optical Power High Warning Permissible Minimum Threshold	See definition 80E8h	N/A
80EC	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	Host Configured Receive Optical Power Low Warning Permissible Minimum Threshold	See definition 80E8h	N/A
80EE	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	Host Configured Receive Optical Power Low Alarm Permissible Minimum Threshold	See definition 80E8h	N/A
80F0	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	Host Configured Receive Optical Power High Alarm Permissible Maximum Threshold	See definition 80E8h	N/A

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
80F2	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	Host Configured Receive Optical Power High Warning Permissible Maximum Threshold	See definition 80E8h	N/A
80F4	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	Host Configured Receive Optical Power Low Warning Permissible Maximum Threshold	See definition 80E8h	N/A
80F6	2	7-0	RO	O	IC-TROSA NVR 2. Extended ID Registers	Host Configured Receive Optical Power Low Alarm Permissible Maximum Threshold	See definition 80E8h	N/A
80F8-80FE	7				IC-TROSA NVR 2. Extended ID Registers	Reserved	Reserved	0
80FF	1	7-0	RO	R	IC-TROSA NVR 2. Extended ID Registers	NVR 2 Checksum	The 8-bit unsigned sum of all NVR 2 contents from address 8080h through 80FEh inclusive.	N/A
8100-817F	128				IC-TROSA NVR 3. Network Lane BOL Measurement Registers	Reserved	Reserved	N/A
8180	1				IC-TROSA NVR 3. Network Lane BOL Measurement Registers	Reserved for IC-TROSA NVR 3 Checksum	Reserved for IC-TROSA NVR 3 Checksum	N/A
8181-8189	9				IC-TROSA NVR 4. Extended ID Registers	Reserved	Reserved	
818A	2	7-0	RO	R2	IC-TROSA NVR 4. Extended ID Registers	TX Minimum Laser Frequency 1	An unsigned 16-bit integer with LSB = 1THz. MSB stored at low address. LSB stored at high address.	N/A
818C	2	7-0	RO	R2	IC-TROSA NVR 4. Extended ID Registers	TX Minimum Laser Frequency 2	An unsigned 16-bit integer with LSB = 0.05 GHz. Value should not exceed 19999. MSB stored at low address. LSB stored at high address.	N/A
818E	2	7-0	RO	R2	IC-TROSA NVR 4. Extended ID Registers	TX Maximum Laser Frequency 1	An unsigned 16-bit integer with LSB = 1THz. MSB stored at low address. LSB stored at high address.	N/A
8190	2	7-0	RO	R2	IC-TROSA NVR 4. Extended ID Registers	TX Maximum Laser Frequency 2	An unsigned 16-bit integer with LSB = 0.05 GHz. Value should not exceed 19999. MSB stored at low address. LSB	N/A

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							stored at high address.	
8192	2				IC-TROSA NVR 4. Extended ID Registers	Reserved	Reserved	0000h
8194	2	7-0	RO	O	IC-TROSA NVR 4. Extended ID Registers	TX Laser Fine Tune Frequency Range (FTF) (Optional)	Laser's bright tuning range as described in CFP2-ACO IA section 12.6 expressed with an unsigned 16-bit integer with LSB = 1 MHz. The range covers the min/max range symmetrically about 0. Set to zero if FTF is not supported. MSB stored at low address. LSB stored at high address.	0000h
8196-81FE	105				IC-TROSA NVR 4. Extended ID Registers	Reserved	Reserved	
81FF	1	7-0	RW	R2	IC-TROSA NVR 4. Extended ID Registers	IC-TROSA NVR 4 Checksum	The 8-bit unsigned sum of all CFP NVR 4 contents from address 8181h through 81FEh inclusive.	N/A
8400-847F	128			O	Vendor NVR 1. Vendor Data Registers	Reserved for Vendor Specific Use		
8480-84FF	128			O	Vendor NVR 2. Vendor Data Registers	Reserved for Vendor Specific Use		
8500-87FF	768			O	Additional Vendor NVR Data Registers Per OIF-CFP2-ACO-01.0	Reserved for Vendor Specific Use		
8800-88FF	256			O	User Data Registers	Reserved for User Data		
B000	2	15-0	WO	O	VR1 Module Command/Setup Registers	Password Entry (Optional)	Password for module register access control. 2-word value. MSW is in lower address.	0000h 0000h
B002	2	15-0	WO	O	VR1 Module Command/Setup Registers	Password Change (Optional)	New password entry. A 2-word value. MSW is in lower address.	0000h 0000h
B004	1			O	VR1 Module Command/Setup Registers	NVR Access Control	User NVRs Restore/Save command	0000h
		15-9			VR1 Module Command/Setup Registers	Reserved	Reserved	0

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		8-6			VR1 Module Command/Setup Registers	Reserved	Reserved	0
		5	RW	O	VR1 Module Command/Setup Registers	User Restore and Save Command	0: Restore the User NVR section, 1: Save the User NVR section.	0
		4			VR1 Module Command/Setup Registers	Reserved		0
		3-2	RO	O	VR1 Module Command/Setup Registers	Command Status	00b: Idle, 01b: Command completed successfully, 10b: Command in progress, 11b: Command failed.	00b
		1-0	RW	O	VR1 Module Command/Setup Registers	Extended Commands	00b: Vendor specific, 01b: Vendor specific, 10b: Save User Password. If bit 5 = 0, command has no effect. 11b: Restore/Save the User NVRs.	00b
B005-B00A	6				VR1 Module Command/Setup Registers	Reserved	Reserved	
B00B	1			O	VR1 Module Command/Setup Registers	Module Operating Control		
		15-12			VR1 Module Command/Setup Registers	Reserved	Reserved	
		11	RW/ SC	O	VR1 Module Command/Setup Registers	Performance Monitor Tick Synchronization	1: Synchronizes the current one second interval as the start of the multi-second performance monitor data accumulation period specified by the Performance Monitor Interval field. Note: Refer to register C02Eh for other functions related to PM Interval control	0b
		10	RW	O	VR1 Module Command/Setup Registers	Performance Monitor Tick Source	0: Internal 1: External Note: Refer to register C02Eh for other functions	0b

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							related to PM Interval control	
		9-4	RW	O	VR1 Module Command/Setup Registers	Performance Monitor Interval	Performance monitoring interval 0-63: Represents the number of one second Performance Monitor Tick Intervals plus one for which the Module will accumulate and provide Performance Monitor data. A value of 0 will result in the module providing PM data every 1 second. A value of 9 will result in the module providing PM data every 10 seconds. Note: Refer to register C02Eh for other functions related to PM Interval control	00h
		3-0			VR1 Module Command/Setup Registers	Reserved	Reserved	
B00C	1	15-0	RO	R	VR1 Module Command/Setup Registers	Command Error Address	Address of last command that had an error	0000h
B00D	1	15-0	RO	R	VR1 Module Command/Setup Registers	Command Error Data	Command data written of last command that generated an error	0000h
B00E	1	15-0	RO	R	VR1 Module Command/Setup Registers	Command Error Data Mask	Mask signifying which bits of command data generated error	0000h
B00F	1			R	VR1 Module Command/Setup Registers	Command Error Status	Provides reason of last command that generated an error	0000h
		15	RO	R	VR1 Module Command/Setup Registers	Out of Range Value	0: No Error, 1: Error	0
		14	RO	R	VR1 Module Command/Setup Registers	Incorrect Value	0: No Error, 1: Error	0
		13	RO	R	VR1 Module Command/Setup Registers	Command Not Valid	0: No Error, 1: Error	0
		12	RO	R	VR1 Module Command/Setup Registers	TWI Write Done while Module Busy	0: No Error, 1: Error	0

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		11	RO	R	VR1 Module Command/Setup Registers	Vendor Specific Error	0: No Error, 1: Error	0
		10	RO	R	VR1 Module Command/Setup Registers	TWI Protocol Error	0: No Error, 1: Error	0
		9-0			VR1 Module Command/Setup Registers	Reserved	Reserved	0
B010	1			R	VR1 Module Control Register	Module General Control		
		15	RW/ SC/LH	R	VR1 Module Control Register	Soft Module Reset	Register bit for module reset function. Writing a 0 to this bit has no effect regardless if it was 0 or 1 previously. 1: Module reset assert.	0
		14	RW	R	VR1 Module Control Register	Soft Module Low Power	Register bit for module low power function. 1: Assert.	1
		13	RW	R	VR1 Module Control Register	Soft TX Disable	Register bit for TX Disable function. 1: Assert.	0
		12-10			VR1 Module Control Register	Reserved	Reserved	0
		9	RW	O	VR1 Module Control Register	Soft GLB_ALRM Test	Command bit for software forced test signal. When this bit is asserted it generates GLB_ALRM signal. 1: Assert.	0
		8	RW/ SC	R	VR1 Module Control Register	Processor Reset	Register bit for processor reset function. This bit is self-clearing. Register settings are not affected. This is a Non- Service Affecting reset. 1: Assert.	0
		7-6			VR1 Module Control Register	Reserved	Reserved	0
		5	RO	R	VR1 Module Control Register	TX_DIS Pin State	Logical state of the TX_DIS pin. 1: Assert.	0
		4	RO	R	VR1 Module Control Register	MOD_LOPWR State	Logical state of the MOD_LOPWR. Set by IC-TROSA as a response to B010.14 asserted by host application 1: Assert.	0
		3-0			VR1 Module Control Register	Reserved	Reserved	0

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
B011-B014	4				VR1 Module Control Register	Reserved	Reserved	N/A
B015	1			O	VR1 Module Control Register			
		15-10			VR1 Module Control Register	Reserved	Reserved	
		9	RW	O	VR1 Module Control Register	RX Power Monitor Alarm/Warning Threshold Select	0: MSA default registers 80C0h-80C7h, 1: Host Configured Receive Optical Power Threshold registers B03Ch-B03Fh.	0
		8-0			VR1 Module Control Register	Reserved	Reserved	
B016	1			R	Module State Register	Module State	IC-TROSA Module state. Only a single bit set at any time.	0000h
		15-9			Module State Register	Reserved		0
		8	RO	R	Module State Register	High-Power-down State	1: Corresponding state is active. Word value = 0100h.	0
		7	RO	R	Module State Register	TX-Turn-off State	1: Corresponding state is active. Word value = 0080h.	0
		6	RO	R	Module State Register	Fault State	1: Corresponding state is active. Word value = 0040h. (Also referred to as MOD_FAULT)	0
		5	RO	R	Module State Register	Ready State	1: Corresponding state is active. Word value = 0020h. (Also referred to as MOD_READY)	0
		4	RO	R	Module State Register	TX-Turn-on State	1: Corresponding state is active. Word value = 0010h.	0
		3	RO	R	Module State Register	TX-Off State	1: Corresponding state is active. Word value = 0008h.	0
		2	RO	R	Module State Register	High-Power-up State	1: Corresponding state is active. Word value = 0004h.	0
		1	RO	R	Module State Register	Low-Power State	1: Corresponding state is active. Word value = 0002h.	0
		0	RO	R	Module State Register	Initialize State	1: Corresponding state is active. Word value = 0001h.	0
B017	1				Module Alarm Summary Register	Reserved	Reserved	N/A
B018	1				Module Alarm Summary Register	Global Alarm Summary		0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		15	RO	R	Module Alarm Summary Register	GLB_ALRM Assertion Status	Internal status of global alarm output. 1: Asserted.	0
		14			Module Alarm Summary Register	Reserved	Reserved	0
		13	RO	R	Module Alarm Summary Register	Network Lane Fault and Status Summary	Logical OR of all the bits in the Network Lane Fault and Status Summary register.	0
		12	RO	R	Module Alarm Summary Register	Network Lane Alarm and Warning 1 Summary	Logical OR of all the bits in the Network Lane Alarm and Warning 1 Summary register.	0
		11	RO	R	Module Alarm Summary Register	Module Alarm and Warning 2 Summary	Logical OR of all the enabled bits of Module Alarm and Warning 2 Latch register.	0
		10	RO	R	Module Alarm Summary Register	Module Alarm and Warning 1 Summary	Logical OR of all the enabled bits of Module Alarm and Warning 1 Latch register.	0
		9	RO	R	Module Alarm Summary Register	Module Fault Summary	Logical OR of all the enabled bits of Module Fault Status Latch register.	0
		8	RO	R	Module Alarm Summary Register	Module General Status Summary	Logical OR of all the enabled bits of Module General Status Latch register.	0
		7	RO	R	Module Alarm Summary Register	Module State Summary	Logical OR of all the enabled bits of Module State Latch register.	0
		6	RO	R	Module Alarm Summary Register	Network Lane Alarm and Warning 2 Summary	Logical OR of all the enabled bits of Network Lane Alarm and Warning 2 Summary register	0
		5			Module Alarm Summary Register	Reserved	Reserved	0
		4	RO	R	Module Alarm Summary Register	Module Extended Functions Status Summary	Logical OR of all the enabled bits of Module Extended Functions Latch register.	0
		3	RO	O	Module Alarm Summary Register	Vendor Specific FAWS	Logical OR of all the enabled bits of Vendor Specific FAWS Latch register.	0

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		2-1			Module Alarm Summary Register	Reserved		0
		0	RO	O	Module Alarm Summary Register	Soft GLB_ALRM Test Status	Soft GLB_ALRM Test bit Status.	0
B019	1			R	Module Alarm Summary Register	Network Lane Alarm and Warning 1 Summary	Each bit is the logical OR of all enabled bits in each of Network Lane Alarm and Warning 1 Latch registers.	0000h
		15-0	RO	R	Module Alarm Summary Register	Lane n Alarm and Warning Summary	Logical OR of all enabled bits in Latched Lane n Network Lane Alarm and Warning Register. 1 = Fault asserted. n ranges from 0 to 15.	0
B01A	1			R	Module Alarm Summary Register	Network Lane Fault and Status Summary	Each bit is the logical OR of all enabled bits in each of the Network Lane fault and Status Latch registers.	0000h
		15-0	RO	R	Module Alarm Summary Register	Lane n Fault and Status Summary	Logical OR of all enabled bits in Latched Lane n Network Lane Fault and Status Register. 1 = Fault asserted. Lane number n ranges from 0 to 15.	
B01B	1				Module Alarm Summary Register	Reserved	Reserved	N/A
B01C	1		RO	R	Module Alarm Summary Register	Network Lane Alarm and Warning 2 Summary	Each bit is the logical OR of all enabled bits in each of Network Lane Alarm and Warning 2 Latch registers.	N/A
		15-0	RO	R	Module Alarm Summary Register	Lane n Alarm and Warning 2 Summary	Logical OR of all enabled bits in Latched Lane-n Network Lane Alarm and Warning 2 Register. 1=Fault asserted.	N/A
B01D	1			R	Module FAWS Registers			N/A
		15-8			Module FAWS Registers	Reserved	Reserved	N/A
		7	RO	R	Module FAWS Registers	TX_LOSF	Transmitter Loss of Signal Functionality. Logic OR of all of Network Lanes TX_LOSF bits. (FAWS_TYPE_C,	0

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							since the TX must be enabled). Note: The corresponding latch register is set to 1 on any change (0-->1 or 1 --> 0) of this status signal. 0: all transmitter signals functional, 1: any transmitter signal not functional.	
		6			Module FAWS Registers	Reserved	Reserved	N/A
		5	RO	R	Module FAWS Registers	RX_LOS	Receiver Loss of Signal. Logic OR of all of network lane RX_LOS bits. (FAWS_TYPE_B). Note: The corresponding latch register is set to 1 on any change (0-->1 or 1 --> 0) of this status signal. 0: No network lane RX_LOS bit asserted, 1: Any network lane RX_LOS bit asserted.	0
		4			Module FAWS Registers	Reserved	Reserved	N/A
		3			Module FAWS Registers	Reserved	Reserved	N/A
		2	RO	R	Module FAWS Registers	Performance Monitor Interval Complete	0: Not Done 1:Done.	0
		1	RO	R	Module FAWS Registers	HIPWR_ON	Status bit representing the condition of module in high power status. FAWS Type is not applicable.	0
		0			Module FAWS Registers	Reserved	Reserved	N/A
B01E	1			R	Module FAWS Registers	Module Fault Status	Module Fault Status bit pattern. Only fatal faults that are potentially harmful to the module can trigger the bits here. All the bits are 0: Normal; 1: fault detected. When any bit in this register is a '1', The Module State register will also be set to the Fault State.	0000h
		15			Module FAWS Registers	Reserved	Reserved for extension of “other	0

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							faults" in case of all the bits used up in this register.	
		14-7			Module FAWS Registers	Reserved	Reserved	0
		6	RO	R	Module FAWS Registers	PLD or Flash Initialization Fault	PLD, CPLD, or FPGA initialization fault. (FAWS_TYPE_A)	0
		5	RO	O	Module FAWS Registers	Power Supply Fault	1: Power supply is out of range. (FAWS_TYPE_A). Logic OR of all IC-TROSA power supply fault registers C002h (also 'OR' with B01Fh.7-4 if these optional +P0 registers are being used.)	0
		4-2	RO		Module FAWS Registers	Reserved	Reserved	000b
		1	RO	R	Module FAWS Registers	Checksum Fault	1: IC-TROSA Checksum failed. (FAWS_TYPE_A)	0
		0			Module FAWS Registers	Reserved	Reserved	0
B01F	1			O	Module FAWS Registers	Module Alarm and Warning 1		0000h
		15-12			Module FAWS Registers	Reserved	Reserved	0000b
		11	RO	O	Module FAWS Registers	Mod Temp High Alarm	Mod temp high Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
		10	RO	O	Module FAWS Registers	Mod Temp High Warning	Mod temp high Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
		9	RO	O	Module FAWS Registers	Mod Temp Low Warning	Mod temp low Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
		8	RO	O	Module FAWS Registers	Mod Temp Low Alarm	Mod temp low Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
		7	RO	O	Module FAWS Registers	Mod +P0 High Alarm	Input +P0 primary power supply high Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
		6	RO	O	Module FAWS Registers	Mod +P0 High Warning	Input +P0 primary power supply high	0

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	
		5	RO	O	Module FAWS Registers	Mod +P0 Low Warning	Input +P0 primary power supply low Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
		4	RO	O	Module FAWS Registers	Mod +P0 Low Alarm	Input +P0 primary power supply low Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
		3	RO	O	Module FAWS Registers	Mod SOA Bias High Alarm	SOA bias current high alarm. (FAWS_TYPE_B) 0: Normal, 1: Asserted.	0
		2	RO	O	Module FAWS Registers	Mod SOA Bias High Warning	SOA bias current high warning. (FAWS_TYPE_B) 0: Normal, 1: Asserted.	0
		1	RO	O	Module FAWS Registers	Mod SOA Bias Low Warning	SOA bias current low warning. (FAWS_TYPE_B) 0: Normal, 1: Asserted.	0
		0	RO	O	Module FAWS Registers	Mod SOA Bias Low Alarm	SOA bias current low alarm. (FAWS_TYPE_B) 0: Normal, 1: Asserted.	0
B020	1			O	Module FAWS Registers	Module Alarm and Warning 2		0000h
		15-8			Module FAWS Registers	Reserved	Reserved	
		7	RO	O	Module FAWS Registers	Mod Aux 1 High Alarm	Module aux ch 1 high alarm. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
		6	RO	O	Module FAWS Registers	Mod Aux 1 High Warning	Module aux ch 1 high warning. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
		5	RO	O	Module FAWS Registers	Mod Aux 1 Low Warning	Module aux ch 1 low warning. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
		4	RO	O	Module FAWS Registers	Mod Aux 1 Low Alarm	Module aux ch 1 low alarm. (FAWS Type is vendor TBD)	0

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							0: Normal, 1: Asserted.	
		3	RO	O	Module FAWS Registers	Mod Aux 2 High Alarm	Module aux ch 2 high alarm. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
		2	RO	O	Module FAWS Registers	Mod Aux 2 High Warning	Module aux ch 2 high warning. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
		1	RO	O	Module FAWS Registers	Mod Aux 2 Low Warning	Module aux ch 2 low warning. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
		0	RO	O	Module FAWS Registers	Mod Aux 2 Low Alarm	Module aux ch 2 low alarm. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
B021	1		RO	O	Module FAWS Registers	Vendor Specific FAWS	(Optional) Vendor Specified Module Fault, Alarm, Warning and Status. Contents are specified by the vendor.	0000h
B022	1			R	Module FAWS Latch Registers	Module State Latch		0000h
		15-9			Module FAWS Latch Registers	Reserved	Reserved	0
		8	RO/LH/COR	R	Module FAWS Latch Registers	High-Power-down State Latch	1: Latched.	0
		7	RO/LH/COR	R	Module FAWS Latch Registers	TX-Turn-off State Latch	1: Latched.	0
		6	RO/LH/COR	R	Module FAWS Latch Registers	Fault State Latch	1: Latched.	0
		5	RO/LH/COR	R	Module FAWS Latch Registers	Ready State Latch	1: Latched.	0
		4	RO/LH/COR	R	Module FAWS Latch Registers	TX-Turn-on State Latch	1: Latched.	0
		3	RO/LH/COR	R	Module FAWS Latch Registers	TX-Off State Latch	1: Latched.	0
		2	RO/LH/COR	R	Module FAWS Latch Registers	High-Power-up State Latch	1: Latched.	0
		1	RO/LH/COR	R	Module FAWS Latch Registers	Low-Power State Latch	1: Latched.	0

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		0	RO/LH/COR	R	Module FAWS Latch Registers	Initialize State Latch	1: Latched.	0
B023	1			R	Module FAWS Latch Registers	Module General Status Latch		0000h
		15-8			Module FAWS Latch Registers	Reserved	Reserved	N/A
		7	RO/LH/COR	R	Module FAWS Latch Registers	TX_LOSF Latch	1: Latched. Note: Set to 1 on any change (0-->1 or 1 --> 0) of the corresponding status signal.	0
		6			Module FAWS Latch Registers	Reserved	Reserved	N/A
		5	RO/LH/COR	R	Module FAWS Latch Registers	RX_LOS Latch	1: Latched. Note: Set to 1 on any change (0-->1 or 1 --> 0) of the corresponding status signal.	0
		4			Module FAWS Latch Registers	Reserved	Reserved	N/A
		3			Module FAWS Latch Registers	Reserved	Reserved	N/A
		2	RO/LH/COR	R	Module FAWS Latch Registers	Performance Monitor Interval Complete Latch	1: Latched.	0
		1	RO/LH/COR	R	Module FAWS Latch Registers	HIPWR_ON Latch	1: Latched.	0
		0			Module FAWS Latch Registers	Reserved	Reserved	N/A
B024	1			R	Module FAWS Latch Registers	Module Fault Status Latch	Module Fault Status latched bit pattern.	0000h
		15-7			Module FAWS Latch Registers	Reserved	Reserved	N/A
		6	RO/LH/COR	R	Module FAWS Latch Registers	PLD or Flash Initialization Fault Latch	1: Latched.	0
		5	RO/LH/COR	R	Module FAWS Latch Registers	Power Supply Fault Latch	1: Latched.	0
		4-2			Module FAWS Latch Registers	Reserved	Reserved	N/A
		1	RO/LH/COR	R	Module FAWS Latch Registers	Checksum Fault Latch	1: Latched.	0
		0			Module FAWS Latch Registers	Reserved	Reserved	N/A
B025	1			R	Module FAWS Latch Registers	Module Alarm and Warning 1 Latch		0000h
		15-12			Module FAWS Latch Registers	Reserved	Reserved	0000b
		11	RO/LH/COR	R	Module FAWS Latch Registers	Mod Temp High Alarm Latch	1: Latched.	0

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		10	RO/LH/COR	R	Module FAWS Latch Registers	Mod Temp High Warning Latch	1: Latched.	0
		9	RO/LH/COR	R	Module FAWS Latch Registers	Mod Temp Low Warning Latch	1: Latched.	0
		8	RO/LH/COR	R	Module FAWS Latch Registers	Mod Temp Low Alarm Latch	1: Latched.	0
		7	RO/LH/COR	O	Module FAWS Latch Registers	Mod +P0 Primary Power Supply High Alarm Latch	1: Latched.	0
		6	RO/LH/COR	O	Module FAWS Latch Registers	Mod +P0 Primary Power Supply High Warning Latch	1: Latched.	0
		5	RO/LH/COR	O	Module FAWS Latch Registers	Mod +P0 Primary Power Supply Low Warning Latch	1: Latched.	0
		4	RO/LH/COR	O	Module FAWS Latch Registers	Mod +P0 Primary Power Supply Low Alarm Latch	1: Latched.	0
		3	RO/LH/COR	O	Module FAWS Latch Registers	Mod SOA Bias High Alarm Latch	1: Latched.	0
		2	RO/LH/COR	O	Module FAWS Latch Registers	Mod SOA Bias High Warning Latch	1: Latched.	0
		1	RO/LH/COR	O	Module FAWS Latch Registers	Mod SOA Bias Low Warning Latch	1: Latched.	0
		0	RO/LH/COR	O	Module FAWS Latch Registers	Mod SOA Bias Low Alarm Latch	1: Latched.	0
B026	1			O	Module FAWS Latch Registers	Module Alarm and Warning 2 Latch		0
		15-8			Module FAWS Latch Registers	Reserved	Reserved	N/A
		7	RO/LH/COR	O	Module FAWS Latch Registers	Mod Aux 1 High Alarm Latch	1: Latched.	0
		6	RO/LH/COR	O	Module FAWS Latch Registers	Mod Aux 1 High Warning Latch	1: Latched.	0
		5	RO/LH/COR	O	Module FAWS Latch Registers	Mod Aux 1 Low Warning Latch	1: Latched.	0
		4	RO/LH/COR	O	Module FAWS Latch Registers	Mod Aux 1 Low Alarm Latch	1: Latched.	0
		3	RO/LH/COR	O	Module FAWS Latch Registers	Mod Aux 2 High Alarm Latch	1: Latched.	0
		2	RO/LH/COR	O	Module FAWS Latch Registers	Mod Aux 2 High Warning Latch	1: Latched.	0
		1	RO/LH/COR	O	Module FAWS Latch Registers	Mod Aux 2 Low Warning Latch	1: Latched.	0

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		0	RO/LH/COR	O	Module FAWS Latch Registers	Mod Aux 2 Low Alarm Latch	1: Latched.	0
B027	1		RO/LH/COR	O	Module FAWS Latch Registers	Vendor Specific FAWS Latch	(Optional) Vendor Specified Module Fault, Alarm, Warning and Status Latch. Contents are specified by the vendor.	0000h
B028	1			R	Module FAWS Enable Registers	Module State Enable	GLB_ALRM Enable register for Module State change. One bit for each state.	006Ah
		15-9			Module FAWS Enable Registers	Reserved	Reserved	N/A
		8	RW	R	Module FAWS Enable Registers	High-Power-down State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		7	RW	R	Module FAWS Enable Registers	TX-Turn-off State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		6	RW	R	Module FAWS Enable Registers	Fault State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence.)	1
		5	RW	R	Module FAWS Enable Registers	Ready State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence.)	1
		4	RW	R	Module FAWS Enable Registers	TX-Turn-on State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		3	RW	R	Module FAWS Enable Registers	TX-Off State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence.)	1
		2	RW	R	Module FAWS Enable Registers	High-Power-up State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		1	RW	R	Module FAWS Enable Registers	Low-Power State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow	1

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							GLB_ALRM in startup sequence)	
		0	RO	R	Module FAWS Enable Registers	Initialize State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
B029	1			R	Module FAWS Enable Registers	Module General Status Enable	1: Enable signal to assert GLB_ALRM. Bits 14-0 are AND'ed with corresponding bits in the Module General Status Latch register; the result is used to assert GLB_ALRM. Bit 15 is the master enable of GLB_ALRM and it is AND'ed with the output of the "OR" gate output in Global Alarm Signal Aggregation, Figure 10.	A7F8h
		15	RW	R	Module FAWS Enable Registers	GLB_ALRM Master Enable	1: Enable.	1
		14-8			Module FAWS Enable Registers	Reserved	Reserved	N/A
		7	RW	R	Module FAWS Enable Registers	TX_LOSF Enable	1: Enable.	1
		6			Module FAWS Enable Registers	Reserved	Reserved	1
		5	RW	R	Module FAWS Enable Registers	RX_LOS Enable	1: Enable.	1
		4			Module FAWS Enable Registers	Reserved	Reserved	N/A
		3			Module FAWS Enable Registers	Reserved	Reserved	N/A
		2	RW	R	Module FAWS Enable Registers	Performance Monitor Interval Complete Enable	1: Enable.	1
		1	RW	R	Module FAWS Enable Registers	HIPWR_ON Enable	1: Enable.	1
		0			Module FAWS Enable Registers	Reserved	Reserved	N/A
B02A	1			R	Module FAWS Enable Registers	Module Fault Status Enable	These bits are AND'ed with corresponding bits in the Module Fault Latch register; the	0062h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							result is used to assert GLB_ALRM. Optional features that are not implemented shall have their Enable bit forced to '0'.	
		15-7			Module FAWS Enable Registers	Reserved		0
		6	RW	R	Module FAWS Enable Registers	PLD or Flash Initialization Fault Enable	1: Enable.	1
		5	RW	O	Module FAWS Enable Registers	Power Supply Fault Enable	1: Enable. Logical OR of all IC-TROSA Power Supply Alarm Status bits C002h	1
		4-2			Module FAWS Enable Registers	Reserved	Reserved	N/A
		1	RW	R	Module FAWS Enable Registers	Checksum Fault Enable	1: Enable.	1
		0			Module FAWS Enable Registers	Reserved	Reserved	N/A
B02B	1			R	Module FAWS Enable Registers	Module Alarm and Warning 1 Enable	These bits are AND'ed with corresponding bits in the Module Alarm and Warning 1 Latch register; the result is used to assert GLB_ALRM. Optional features that are not implemented shall have their Enable bit forced to '0'.	0FFFh
		15-12			Module FAWS Enable Registers	Reserved	Reserved	N/A
		11	RW	R	Module FAWS Enable Registers	Mod Temp Hi Alarm Enable	1: Enable.	1
		10	RW	R	Module FAWS Enable Registers	Mod Temp Hi Warn Enable	1: Enable.	1
		9	RW	R	Module FAWS Enable Registers	Mod Temp Low Warning Enable	1: Enable.	1
		8	RW	R	Module FAWS Enable Registers	Mod Temp Low Alarm Enable	1: Enable.	1
		7	RW	O	Module FAWS Enable Registers	Mod P0 High Alarm Enable	1: Enable.	1

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		6	RW	O	Module FAWS Enable Registers	Mod P0 High Warning Enable	1: Enable.	1
		5	RW	O	Module FAWS Enable Registers	Mod P0 Low Warning Enable	1: Enable.	1
		4	RW	O	Module FAWS Enable Registers	Mod P0 Low Alarm Enable	1: Enable.	1
		3	RW	O	Module FAWS Enable Registers	Mod SOA Bias High Alarm Enable	1: Enable.	1
		2	RW	O	Module FAWS Enable Registers	Mod SOA Bias High Warning Enable	1: Enable.	1
		1	RW	O	Module FAWS Enable Registers	Mod SOA Bias Low Warning Enable	1: Enable.	1
		0	RW	O	Module FAWS Enable Registers	Mod SOA Bias Low Alarm Enable	1: Enable.	1
B02C	1			O	Module FAWS Enable Registers	Module Alarm and Warning 2 Enable	These bits are AND'ed with corresponding bits in the Module Alarm and Warning 2 Latch register; the result is used to assert GLB_ALRM. Optional features that are not implemented shall have their Enable bit forced to '0'.	00FFh
		15-8			Module FAWS Enable Registers	Reserved	Reserved	N/A
		7	RW	O	Module FAWS Enable Registers	Mod Aux 1 High Alarm Enable	1: Enable.	1
		6	RW	O	Module FAWS Enable Registers	Mod Aux 1 High Warning Enable	1: Enable.	1
		5	RW	O	Module FAWS Enable Registers	Mod Aux 1 Low Warning Enable	1: Enable.	1
		4	RW	O	Module FAWS Enable Registers	Mod Aux 1 Low Alarm Enable	1: Enable.	1
		3	RW	O	Module FAWS Enable Registers	Mod Aux 2 High Alarm Enable	1: Enable.	1
		2	RW	O	Module FAWS Enable Registers	Mod Aux 2 High Warning Enable	1: Enable.	1
		1	RW	O	Module FAWS Enable Registers	Mod Aux 2 Low Warning Enable	1: Enable.	1

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		0	RW	O	Module FAWS Enable Registers	Mod Aux 2 Low Alarm Enable	1: Enable.	1
B02D	1		RW	O	Module FAWS Enable Registers	Vendor Specific FAWS Enable	(Optional) Vendor Specified Module Fault, Alarm, Warning and Status Enable. Contents are specified by the vendor.	0000h
		15-2			Module FAWS Enable Registers	Reserved	Reserved	N/A
		1		O	Module FAWS Enable Registers	HW/SW incompatible Enable	1: Latched.	
		0		O	Module FAWS Enable Registers	Mod Internal power supply out of range alarm Enable Logical OR of all Power Supply Alarm Status registers	1: Latched.	
B02E	1				Module FAWS Enable Registers	Reserved	Reserved	N/A
B02F	1	15-0	RO	O	Module Analog A/D Value Registers 1	Module Temp Monitor A/D Value	Internally measured temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 degC. MSA valid range is between –40 and +125C. Accuracy shall be better than +/- 3 degC over the whole temperature range.	0000h
B030	1	15-0	RO	O	Module Analog A/D Value Registers 2	Module Power Supply Monitor A/D Value	Internally measured transceiver supply voltage, a 16-bit unsigned integer with LSB = 1 mV, yielding a total measurement range of 0 to 65.535 V. Accuracy shall be better than +/- 3% of the nominal value over specified temperature and voltage ranges.	0000h
B031	1	15-0	RO	O	Module Analog A/D Value Registers 3	SOA Bias Current A/D Value	These threshold values are an unsigned 16-bit integer	0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							with LSB =2 uA by default, representing 131.07 mA. For the case of coherent module (8003h = 02, 10 or 11) LSB = 8uA, representing a range of current from 0 to 524.280 mA. MSB stored at low address, LSB stored at high address. Measured SOA bias current in uA, a 16-bit unsigned integer with LSB = 2 uA, representing a total range of from 0 to 131.072 mA. Accuracy shall be better than +/- 10% of the nominal value over specified temperature and voltage.	
B032	1	15-0	RO	O	Module Analog A/D Value Registers 4	Module Auxiliary 1 Monitor A/D Value	Definition depending upon the designated use.	0000h
B033	1	15-0	RO	O	Module Analog A/D Value Registers 5	Module Auxiliary 2 Monitor A/D Value	Definition depending upon the designated use.	0000h
B034	4				Module Analog A/D Value Registers 6	Reserved	Reserved	N/A
B038	1				Module PRBS Registers	Reserved	Reserved	N/A
B039	1				Module PRBS Registers	Reserved	Reserved	N/A
B03A	2	15-0	RW	O	Module Analog A/D Value Registers 2	Real-Time Second Clock	Represents number of seconds since Jan. 1, 1970. (MSB at 0xB03Ah, LSB at 0xB03Bh). Write to address B03Ah triggers reading both B03Ah and B03Bh registers	0000h
B03C	1	15-0	RW	O	Module Analog A/D Value Registers 2	Host Configured Receive Optical Power High Alarm Threshold	A 16-bit signed integer with LSB = 0.01 dBm. Valid if the value is between "Host Configured Receive Optical Power High Alarm Permissible	0

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							Minimum Threshold" (0x80C8-0x80C9) and "Host Configured Receive Optical Power High Alarm Permissible Maximum Threshold" (0x80D0-0x80D1)	
B03D	1	15-0	RW	O	Module Analog A/D Value Registers 3	Host Configured Receive Optical Power High Warning Threshold	A 16-bit signed integer with LSB = 0.01 dBm. Valid if the value is between "Host Configured Optical Power High Warning Permissible Minimum Threshold" (0x80CA-0x80CB) and "Host Configured Optical Power High Warning Permissible Maximum Threshold" (0x80D2-0x80D3)	0
B03E	1	15-0	RW	O	Module Analog A/D Value Registers 4	Host Configured Receive Optical Power Low Warning Threshold	A 16-bit signed integer with LSB = 0.01 dBm. Valid if the value is between "Host Configured Optical Power Low Warning Permissible Minimum Threshold" (0x80CC-0x80CD) and "Host Configured Optical Power Low Warning Permissible Maximum Threshold" (0x80D4-0x80D-0x80D7)	0
B03F	1	15-0	RW	O	Module Analog A/D Value Registers 5	Host Configured Receive Optical Power Low Alarm Threshold	A 16-bit signed integer with LSB = 0.01 dBm. Valid if the value is between "Host Configured Receive Optical Power Low Alarm Permissible Minimum Threshold" (0x80CE-0x80CF) and "Host Configured Receive Optical Power Low Alarm Permissible	0

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							Maximum Threshold" (0x80D6-0x80D7)	
B040-B042	10				Module Extended Functions Control Registers	Reserved	Reserved	N/A
B04A	1			O	Module Extended Functions Control Registers	Upload Control		0000h
		15	RW/ SC	O	Module Extended Functions Control Registers	Upload Start Request	Register bit to request initiation of upload. This bit is self-clearing.	0
		14	RW	O	Module Extended Functions Control Registers	Upload Block Processed	1: DONE. 0: NOT DONE.	0
		13	RW	O	Module Extended Functions Control Registers	Upload Abort	1: Abort the Upload.	0
		12-11	RW	O	Module Extended Functions Control Registers	Upload Block Error Code	0: No Error 1: CRC Image Error 2-7: Reserved.	0
		10-8			Module Extended Functions Control Registers	Reserved	Reserved	0
		7-0	RW	O	Module Extended Functions Control Registers	Upload Type	Field to specify type of upload data. Values are vendor specific.	0
B04B	1			O	Module Extended Functions Control Registers	Upload Data		0001h
		15	RO	O	Module Extended Functions Control Registers	Upload Data Block Ready	Set the flag when module completes writing the block to the 0xBC00 address.	0
		14-0	RW	O	Module Extended Functions Control Registers	Maximum Upload Data Block Size	Host sets Upload Data Block Size.	1
B04C	1			R	Module Extended	Module Upgrade Data		0001h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
					Functions Control Registers			
		15	RW/ SC	R	Module Extended Functions Control Registers	Upgrade Data Block Ready	Set the flag when host completes writing the block to the 0xBC00 address. When cleared by the Module, the Host can then write the next block.	0
		14-12	RO	R	Module Extended Functions Control Registers	Upgrade Data Block Status	0 = no error 1 = block length error (zero or block too long) 2 = crc error 3 = fatal error, eg. flash write error or image too large (B051 contains status)	1
		11-0	RO	R	Module Extended Functions Control Registers	Maximum Upgrade Data Block Size	Module sets Maximum Upgrade Data Block Size.	1
B04D	1			R	Module Extended Functions Control Registers	Module Upgrade Control		
		15-12	RW	R	Module Extended Functions Control Registers	Upgrade Command	0: No operation 1: Download Start 2: Download Complete 3: Run Image A 4: Run Image B 5: Abort image download 6: Copy Image A to B 7: Copy Image B to A 8: Commit Image A 9: Commit Image B	
		11-8	RO	R	Module Extended Functions Control Registers	TWI upgrade ready time	During the sw upgrade procedure, after the host issues run image command, the TWI is not available. TWI upgrade ready time gives a maximum time for the interface to be ready. Value X 5 seconds	0
		7-0			Module Extended Functions	Reserved	Reserved	0

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
					Control Registers			
B04E	2	15-0			Module Extended Functions Control Registers	Reserved	Reserved	N/A
B050	1			R	Module Extended Functions Control Registers	Module Extended Functions Status		0000h
		15	RO	R	Module Extended Functions Control Registers	Module Ready for TWI Write	0: Not Ready, 1: Ready This bit is used to indicate TWI write completion. It does not indicate success or failure of last write.	0
		14	RO	R	Module Extended Functions Control Registers	Command Error	0: No Error, 1: Error	0
		13-9			Module Extended Functions Control Registers	Reserved	Reserved	0
		8	RO	O	Module Extended Functions Control Registers	Upload Data Available	0: No Data Available, 1: Data Available	0
		7	RO	O	Module Extended Functions Control Registers	Upload Data Complete	0: Not Done, 1: Done	0
		6-0			Module Extended Functions Control Registers	Reserved	Reserved	0
B051	1			R	Module Extended Functions Control Registers	Module Upgrade Status		0000h
		15-14	RO	R	Module Extended Functions Control Registers	Upgrade Command Status	00: Idle. 01: Command completed successfully. 10: Command in progress. 11: Command failed.	0

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		13	RO	R	Module Extended Functions Control Registers	Download Image Service Affecting Status	0: Upgrade to Currently Downloaded Image will Not be Service Affecting 1: Upgrade to Currently Downloaded Image will be Service Affecting	0
		12	RO	R	Module Extended Functions Control Registers	Image Running	0: Image A 1: Image B	0
		11-10	RO	R	Module Extended Functions Control Registers	Image A Status	00: No Image 01: Valid Image Present 10: Image Present is Bad 11: Reserved	0
		9-8	RO	O	Module Extended Functions Control Registers	Image B Status	00: No Image 01: Valid Image Present 10: Image Present is Bad 11: Reserved	0
		7	RO	R	Module Extended Functions Control Registers	Image Committed	0: Image A 1: Image B	0
		6-0	RO	R	Module Extended Functions Control Registers	Upgrade Command Failure Reason	0: No Error 1: CRC Image Error 2: Length Image Error 3: Flash Write Error 4: Bad Image Error 5-127: Reserved	0
B052	2				Module Extended Functions Control Registers	Reserved	Reserved	N/A
B054	1			R	Module Extended Functions Latch Registers	Module Extended Functions Latch		0000h
		15	RO/LH/COR	R	Module Extended Functions Latch Registers	Module Ready for TWI Write Latch	0: Not Latched, 1: Latched	0
		14	RO/LH/COR	R	Module Extended Functions Latch Registers	Command Error Latch	0: Not Latched, 1: Latched	0
		13-9			Module Extended Functions Latch Registers	Reserved	Reserved	0

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		8	RO/LH/COR	O	Module Extended Functions Latch Registers	Upload Data Available Latch	0: Not Latched, 1: Latched	0
		7	RO/LH/COR	O	Module Extended Functions Latch Registers	Upload Data Complete Latch	0: Not Latched, 1: Latched	0
		6-0			Module Extended Functions Latch Registers	Reserved	Reserved	0
B055	2				Module Extended Functions Latch Registers	Reserved	Reserved	N/A
B057	1			R	Module Extended Functions Enable Registers	Module Extended Functions Enable		0000h
		15	RW	R	Module Extended Functions Enable Registers	Module Ready for TWI Write Enable	0: Disabled, 1: Enable	0
		14	RW	R	Module Extended Functions Enable Registers	Command Error Enable	0: Disabled, 1: Enable	0
		13-9			Module Extended Functions Enable Registers	Reserved	0: Disabled, 1: Enable	0
		8	RW	O	Module Extended Functions Enable Registers	Upload Data Available Enable	0: Disabled, 1: Enable	0
		7	RW	O	Module Extended Functions Enable Registers	Upload Data Complete Enable	0: Disabled, 1: Enable	0
		6-0			Module Extended Functions Enable Registers	Reserved	Reserved	0
B058-B07F	40				Module Extended Functions Enable Registers	Reserved	Reserved	N/A
B100	16			O	VR3 Network Lane Module Extended	Network Lane n Vendor Specific FAWS	16 registers, one for each network lane, represent 16 network lanes. n =	0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
					Functions Data Registers		0, 1, …, N-1. N_max = 16. Actual N is module dependent.	
		15-0	RO	O	VR3 Network Lane Module Extended Functions Data Registers	Vendor Specific FAWS	0: Normal; 1: Asserted.	0
B110	16			O	VR3 Network Lane Module Extended Functions Data Registers	Network Lane n Vendor Specific FAWS Latch	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.	0000h
		15-0	RO	O	VR3 Network Lane Module Extended Functions Data Registers	Vendor Specific FAWS Latch	0: Normal; 1: Asserted.	0
B120	16			O	VR3 Network Lane Module Extended Functions Data Registers	Network Lane n Vendor Specific FAWS Enable	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.	0000h
		15-0	RO	O	VR3 Network Lane Module Extended Functions Data Registers	Vendor Specific FAWS Enable	0: Disabled; 1: Enabled.	0
B130	16	15-0			VR3 Network Lane Module Extended Functions Data Registers	Reserved		
B140	16	15-0	RO	O	VR3 Network Lane Module Extended Functions Data Registers	Network Lane n Vendor Specific Auxiliary 1 Monitor A/D Value	Definition provided by vendor. FAWS mapped to Network Lane n Vendor Specific FAWS bit 15, related to 8090h.	0000h
B150	16	15-0	RO	O	VR3 Network Lane Module Extended Functions Data Registers	Network Lane n Vendor Specific Auxiliary 2 Monitor A/D Value	Definition provided by vendor. FAWS mapped to Network Lane n Vendor Specific FAWS bit 14, related to 8098h	0000h
B160	16	15-0	RO	O	VR3 Network Lane Module Extended Functions Data Registers	Network Lane n Vendor Specific Auxiliary 3 Monitor A/D Value	Definition provided by vendor. FAWS mapped to Network Lane n Vendor Specific FAWS bit 13, related to 80A0.	0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
B170	16	15-0	RO	O	VR3 Network Lane Module Extended Functions Data Registers	Network Lane n Vendor Specific Auxiliary 4 Monitor A/D Value	Definition provided by vendor. FAWS mapped to Network Lane n Vendor Specific FAWS bit 12, related to 80A8.	0000h
B180	16			R	VR1 Network Lane Network Lane FAWS Registers	Network Lane n Alarm and Warning 1	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.	0000h
		15	RO	R2	VR1 Network Lane Network Lane FAWS Registers	Laser Bias High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
		14	RO	R2	VR1 Network Lane Network Lane FAWS Registers	Laser Bias High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
		13	RO	R2	VR1 Network Lane Network Lane FAWS Registers	Laser Bias Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
		12	RO	R2	VR1 Network Lane Network Lane FAWS Registers	Laser Bias Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
		11	RO	R	VR1 Network Lane Network Lane FAWS Registers	TX Power High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
		10	RO	R	VR1 Network Lane Network Lane FAWS Registers	TX Power High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
		9	RO	R	VR1 Network Lane Network Lane FAWS Registers	TX Power Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
		8	RO	R	VR1 Network Lane Network Lane FAWS Registers	TX Power Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
		7	RO	R2	VR1 Network Lane Network Lane FAWS Registers	Laser Temperature High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
		6	RO	R2	VR1 Network Lane Network Lane FAWS Registers	Laser Temperature High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
		5	RO	R2	VR1 Network Lane Network Lane FAWS Registers	Laser Temperature Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		4	RO	R2	VR1 Network Lane Network Lane FAWS Registers	Laser Temperature Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
		3	RO	R	VR1 Network Lane Network Lane FAWS Registers	RX Power High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B) The thresholds for the RX Power High/Low Alarm/Warning are determined by the RX Power Monitor Alarm/Warning Threshold Select in B015h. This comment applies to bits 2-0 as well.	0
		2	RO	R	VR1 Network Lane Network Lane FAWS Registers	RX Power High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
		1	RO	R	VR1 Network Lane Network Lane FAWS Registers	RX Power Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
		0	RO	R	VR1 Network Lane Network Lane FAWS Registers	RX Power Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
B190	16			R	VR1 Network Lane Network Lane FAWS Registers	Network Lane n Alarm and Warning 2	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.	0000h
		15-4			VR1 Network Lane Network Lane FAWS Registers	Reserved	Reserved	0
		3	RO	R	VR1 Network Lane Network Lane FAWS Registers	Tx Modulator Bias High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
		2	RO	R	VR1 Network Lane Network Lane FAWS Registers	Tx Modulator Bias High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
		1	RO	R	VR1 Network Lane Network Lane FAWS Registers	Tx Modulator Bias Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
		0	RO	R	VR1 Network Lane Network Lane FAWS Registers	Tx Modulator Bias Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
B1A0	16			R	VR1 Network Lane	Network Lane n Fault and Status	represent 16 network lanes. n = 0, 1, …, N-1. N_max	0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
					Network Lane FAWS Registers		= 16. Actual N is module dependent.	
		15	RO	R2	VR1 Network Lane Network Lane FAWS Registers	Lane TEC Fault	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
		14	RO	R2	VR1 Network Lane Network Lane FAWS Registers	Lane Wavelength Unlocked Fault	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
		13-8			VR1 Network Lane Network Lane FAWS Registers	Reserved	Reserved	N/A
		7	RO	R	VR1 Network Lane Network Lane FAWS Registers	Lane TX_LOSF	0: Normal; 1: Asserted. (PMD) (FAWS_TYPE_C)	0
		6-5			VR1 Network Lane Network Lane FAWS Registers	Reserved	Reserved	N/A
		4	RO	R	VR1 Network Lane Network Lane FAWS Registers	Lane RX_LOS	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
		3-2			VR1 Network Lane Network Lane FAWS Registers	Reserved	Reserved	N/A
		1	RO	O	VR1 Network Lane Network Lane FAWS Registers	Lane RX TEC Fault	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
		0			VR1 Network Lane Network Lane FAWS Registers	Reserved	Reserved	N/A
B1B0	16			R	VR1 Network Lane FAWS Latch Registers	Network Lane n Alarm and Warning 1 Latch	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.	0000h
		15	RO/LH/COR	R2	VR1 Network Lane FAWS Latch Registers	Laser Bias High Alarm Latch	1: Latched	0
		14	RO/LH/COR	R2	VR1 Network Lane FAWS Latch Registers	Laser Bias High Warning Latch	1: Latched	0
		13	RO/LH/COR	R2	VR1 Network Lane FAWS Latch Registers	Laser Bias Low Warning Latch	1: Latched	0

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		12	RO/LH/COR	R2	VR1 Network Lane FAWS Latch Registers	Laser Bias Low Alarm Latch	1: Latched	0
		11	RO/LH/COR	R	VR1 Network Lane FAWS Latch Registers	TX Power High Alarm Latch	1: Latched	0
		10	RO/LH/COR	R	VR1 Network Lane FAWS Latch Registers	TX Power High Warning Latch	1: Latched	0
		9	RO/LH/COR	R	VR1 Network Lane FAWS Latch Registers	TX Power Low Warning Latch	1: Latched	0
		8	RO/LH/COR	R	VR1 Network Lane FAWS Latch Registers	TX Power Low Alarm Latch	1: Latched	0
		7	RO/LH/COR	R2	VR1 Network Lane FAWS Latch Registers	Laser Temperature High Alarm	1: Latched	0
		6	RO/LH/COR	R2	VR1 Network Lane FAWS Latch Registers	Laser Temperature High Warning	1: Latched	0
		5	RO/LH/COR	R2	VR1 Network Lane FAWS Latch Registers	Laser Temperature Low Warning	1: Latched	0
		4	RO/LH/COR	R2	VR1 Network Lane FAWS Latch Registers	Laser Temperature Low Alarm Latch	1: Latched	0
		3	RO/LH/COR	R	VR1 Network Lane FAWS Latch Registers	RX Power High Alarm Latch	1: Latched	0
		2	RO/LH/COR	R	VR1 Network Lane FAWS Latch Registers	RX Power High Warning Latch	1: Latched	0
		1	RO/LH/COR	R	VR1 Network Lane FAWS Latch Registers	RX Power Low Warning Latch	1: Latched	0
		0	RO/LH/COR	R	VR1 Network Lane FAWS Latch Registers	RX Power Low Alarm Latch	1: Latched	0
B1C0	16			R	VR1 Network Lane FAWS Latch Registers	Network Lane n Alarm and Warning 2 Latch	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.	0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		15-4			VR1 Network Lane FAWS Latch Registers	Reserved	Reserved	0
		3	RO/LH/COR	R	VR1 Network Lane FAWS Latch Registers	Tx Modulator Bias High Alarm Latch	1: Latched	0
		2	RO/LH/COR	R	VR1 Network Lane FAWS Latch Registers	Tx Modulator Bias High Warning Latch	1: Latched	0
		1	RO/LH/COR	R	VR1 Network Lane FAWS Latch Registers	Tx Modulator Bias Low Warning Latch	1: Latched	0
		0	RO/LH/COR	R	VR1 Network Lane FAWS Latch Registers	Tx Modulator Bias Low Alarm Latch	1: Latched	0
B1D0	16			R	VR1 Network Lane FAWS Latch Registers	Network Lane n Fault and Status Latch	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.	0000h
		15	RO/LH/COR	R2	VR1 Network Lane FAWS Latch Registers	Lane TEC Fault Latch	1: Latched	0
		14	RO/LH/COR	R2	VR1 Network Lane FAWS Latch Registers	Lane Wavelength Unlocked Fault Latch	1: Latched	0
		13-8			VR1 Network Lane FAWS Latch Registers	Reserved	Reserved	N/A
		7	RO/LH/COR	R	VR1 Network Lane FAWS Latch Registers	Lane TX_LOSF Latch	1: Latched	0
		6-5			VR1 Network Lane FAWS Latch Registers	Reserved	Reserved	N/A
		4	RO/LH/COR	R	VR1 Network Lane FAWS Latch Registers	Lane RX_LOS Latch	1: Latched	0
		3-2			VR1 Network Lane FAWS Latch Registers	Reserved	Reserved	N/A
		1	RO/LH/COR	O	VR1 Network Lane FAWS Latch Registers	Lane RX TEC Fault Latch	1: Latched	0

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		0			VR1 Network Lane FAWS Latch Registers	Reserved	Reserved	N/A
B1E0	16			R	VR1 Network Lane FAWS Latch Registers	Network Lane n Alarm and Warning 1 Enable	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.	FFFFh
		15	RW	R2	VR1 Network Lane FAWS Latch Registers	Laser Bias High Alarm Enable	0: Disable, 1: Enable.	1
		14	RW	R2	VR1 Network Lane FAWS Latch Registers	Laser Bias High Warning Enable	0: Disable, 1: Enable.	1
		13	RW	R2	VR1 Network Lane FAWS Latch Registers	Laser Bias Low Warning Enable	0: Disable, 1: Enable.	1
		12	RW	R2	VR1 Network Lane FAWS Latch Registers	Laser Bias Low Alarm Enable	0: Disable, 1: Enable.	1
		11	RW	R	VR1 Network Lane FAWS Latch Registers	TX Power High Alarm Enable	0: Disable, 1: Enable.	1
		10	RW	R	VR1 Network Lane FAWS Latch Registers	TX Power High Warning Enable	0: Disable, 1: Enable.	1
		9	RW	R	VR1 Network Lane FAWS Latch Registers	TX Power Low Warning Enable	0: Disable, 1: Enable.	1
		8	RW	R	VR1 Network Lane FAWS Latch Registers	TX Power Low Alarm Enable	0: Disable, 1: Enable.	1
		7	RW	R2	VR1 Network Lane FAWS Latch Registers	Laser Temperature High Alarm Enable	0: Disable, 1: Enable.	1
		6	RW	R2	VR1 Network Lane FAWS Latch Registers	Laser Temperature High Warning Enable	0: Disable, 1: Enable.	1
		5	RW	R2	VR1 Network Lane FAWS Latch Registers	Laser Temperature Low Warning Enable	0: Disable, 1: Enable.	1
		4	RW	R2	VR1 Network Lane FAWS Latch Registers	Laser Temperature Low Alarm Enable	0: Disable, 1: Enable.	1

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		3	RW	R	VR1 Network Lane FAWS Latch Registers	RX Power High Alarm Enable	0: Disable, 1: Enable.	1
		2	RW	R	VR1 Network Lane FAWS Latch Registers	RX Power High Warning Enable	0: Disable, 1: Enable.	1
		1	RW	R	VR1 Network Lane FAWS Latch Registers	RX Power Low Warning Enable	0: Disable, 1: Enable.	1
		0	RW	R	VR1 Network Lane FAWS Latch Registers	RX Power Low Alarm Enable	0: Disable, 1: Enable.	1
B1F0	16			R	VR1 Network Lane FAWS Latch Registers	Network Lane n Alarm and Warning 2 Enable	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.	FFFFh
		15-4			VR1 Network Lane FAWS Latch Registers	Reserved	Reserved	1
		3	RW	R	VR1 Network Lane FAWS Latch Registers	Tx Modulator Bias High Alarm Enable	0: Disable, 1: Enable.	1
		2	RW	R	VR1 Network Lane FAWS Latch Registers	Tx Modulator Bias High Warning Enable	0: Disable, 1: Enable.	1
		1	RW	R	VR1 Network Lane FAWS Latch Registers	Tx Modulator Bias Low Warning Enable	0: Disable, 1: Enable.	1
		0	RW	R	VR1 Network Lane FAWS Latch Registers	Tx Modulator Bias Low Alarm Enable	0: Disable, 1: Enable.	1
B200	16			R	VR1 Network Lane FAWS Latch Registers	Network Lane n Fault and Status Enable	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.	E0DCh
		15	RW	R2	VR1 Network Lane FAWS Latch Registers	Lane TEC Fault Enable	0: Disable, 1: Enable.	1
		14	RW	R2	VR1 Network Lane FAWS Latch Registers	Lane Wavelength Unlocked Fault Enable	0: Disable, 1: Enable.	1

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		13-8			VR1 Network Lane FAWS Latch Registers	Reserved	Reserved	N/A
		7	RW	R	VR1 Network Lane FAWS Latch Registers	Lane TX_LOSF Enable	0: Disable, 1: Enable.	1
		6			VR1 Network Lane FAWS Latch Registers	Reserved	Reserved	N/A
		5			VR1 Network Lane FAWS Latch Registers	Reserved	Reserved	N/A
		4	RW	R	VR1 Network Lane FAWS Latch Registers	Lane RX_LOS Enable	0: Disable, 1: Enable.	1
		3			VR1 Network Lane FAWS Latch Registers	Reserved	Reserved	N/A
		2			VR1 Network Lane FAWS Latch Registers	Reserved	Reserved	N/A
		1	RW	R2	VR1 Network Lane FAWS Latch Registers	Lane RX TEC Fault Enable	0: Disable, 1: Enable.	1
		0			VR1 Network Lane FAWS Latch Registers	Reserved	Reserved	N/A
B210-B2FF	240				VR1 Network Lane TX Status Registers	Reserved	Reserved	N/A
B300-B31F	32				VR2 Network Lane Control 1 Registers	Reserved	Reserved	N/A
B320	16	15-0	RO	R2	VR2 Network Lane Control 1 Registers	Network Lane n TX Laser Bias Current monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. Measured laser bias current in %, a 16-bit unsigned integer with LSB = 100/65535%	0000h
B330	16	15-0	RO	R	VR2 Network Lane Control 1 Registers	Network Lane n TX Output Power monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n =	0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							0, 1, …, N-1. N_max = 16. Actual N is module dependent. Measured TX laser output power in dBm, a signed 16-bit integer with LSB = 0.01 dBm. Accuracy must be better than +/- 2 dB over temperature and voltage range. Relative accuracy must be better than 1 dB.	
B340	16	15-0	RO	R2	VR2 Network Lane Control 1 Registers	Network Lane n TX Laser Temp Monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. Internally measured temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 degC. MSA valid range is between –40 and +125C. Minimum accuracy is +/- 3 degC over temperature range.	0000h
B350	16	15-0	RO	R	VR2 Network Lane Control 1 Registers	Network Lane n RX Input Power monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. Measured received input power in dBm, A 16-bit signed integer with LSB = 0.01 dBm. Value can represent either average received power or OMA depending upon how bit 3 of Register 8080h is set. Accuracy must be better than +/- 2dB over	0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus cable plant loss per the appropriate standard. Relative accuracy shall be better than 1 dB over the received power range, temperature range, voltage range, and the life of the product.	
B360	16				VR2 Network Lane Control 1 Registers	Reserved	Reserved	0000h
B370-B39F	48				VR2 Network Lane Control 1 Registers	Reserved	Reserved	0000h
B3A0	16	15-0	RO	R	VR2 Network Lane Control 1 Registers	TX Modulator Bias X/I Monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. TX Modulator Bias, a 16-bit unsigned integer with LSB =100/65535%.	0000h
B3B0	16	15-0	RO	R	VR2 Network Lane Control 1 Registers	TX Modulator Bias X/Q Monitor A/D value	(See above)	0000h
B3C0	16	15-0	RO	R	VR2 Network Lane Control 1 Registers	TX Modulator Bias Y/I Monitor A/D value	(See above)	0000h
B3D0	16	15-0	RO	R	VR2 Network Lane Control 1 Registers	TX Modulator Bias Y/Q Monitor A/D value	(See above)	0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
B3E0	16	15-0	RO	R	VR2 Network Lane Control 1 Registers	TX Modulator Bias X_Phase Monitor A/D value	(See above)	0000h
B3F0	16	15-0	RO	R	VR2 Network Lane Control 1 Registers	TX Modulator Bias Y_Phase Monitor A/D value	(See above)	0000h
B400	16			R2	VR2 Network Lane Control 2 Registers	TX Channel Control	Desired TX channel number and grid spacing. 16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.	0001h
		15-13	RW	R2	VR2 Network Lane Control 2 Registers	Grid Spacing	000b: 100 GHz grid spacing 001b: 50 GHz grid spacing 010b: 33 GHz grid spacing 011b: 25 GHz grid spacing 100b: 12.5 GHz grid spacing 101b: 6.25 GHz grid spacing 110b: 3.125 GHz grid spacing 111b: 75 GHz grid spacing Note: See C02Fh for Laser Grid Availability	000b
		12-11			VR2 Network Lane Control 2 Registers	Reserved	Reserved	N/A
		10	RW	R2	VR2 Network Lane Control 2 Registers	Arbitrary Settable Tx Minimum Laser Frequency Registers Enabled	1: Enabled 0: Disabled With bit set to 1:Enabled the high resolution registers detailed in Section 12.6 shall be used. With the bit set to 0: Not Enabled wavelength tuning is compatible with the Ref. [2] MIS.	0
		9-0	RW	R2	VR2 Network Lane Control 2 Registers	Channel number	Tx channel number. Channel 0 is an undefined channel number.	001h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
B410	16	15-0	RW	R2	VR2 Network Lane Control 2 Registers	TX Output Power	Desired TX output power. 16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. A signed 16-bit integer with the LSB = 0.01dBm Values at -99dBm or less indicate the module shall shutter to its maximal capability. There are anticipated modules that will contain only a shutter function.	0000h
B420	16				VR2 Network Lane Control 2 Registers	Reserved	Reserved	0001h
B430	16	15-0	RW	O	VR2 Network Lane Control 2 Registers	TX Fine Tune Frequency (Optional)	A signed 16-bit integer with LSB = 1 MHz.	000h
B440	16				VR2 Network Lane Control 2 Registers	Reserved	Reserved	000h
B450	16	15-0	RO	R2	VR2 Network Lane Control 2 Registers	TX Frequency 1	Current module TX Frequency 1. An unsigned 16-bit integer with LSB = 1THz.	N/A
B460	16	15-0	RO	R2	VR2 Network Lane Control 2 Registers	TX Frequency 2	Current module TX Frequency 2. An unsigned 16-bit integer with LSB = 0.05GHz. Value should not exceed 19999.	N/A
B470	16	15-0			VR2 Network Lane Control 2 Registers	Reserved	Reserved	N/A
B480	16	15-0			VR2 Network Lane Control 2 Registers	Reserved	Reserved	N/A
B490	1		RW	O	High Resolution Tuning Registers	Tx Minimum Laser Frequency 1 [High Resolution]	See Section 11.7.2 for details on Laser Tuning	

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
B491	1		RW	O	High Resolution Tuning Registers	Tx Minimum Laser Frequency 2 [High Resolution]	See B490h description	
B492	1		RW	O	High Resolution Tuning Registers	Tx Minimum Laser Frequency 3 [High Resolution]	See B490h description	
B493-B495	3				High Resolution Tuning Registers	Reserved	Reserved	
B496	1		RO	O	High Resolution Tuning Registers	Tx Laser Frequency 1 [High Resolution]	See B490h description	
B497	1		RO	O	High Resolution Tuning Registers	Tx Laser Frequency 2 [High Resolution]	See B490h description	
B498	1		RO	O	High Resolution Tuning Registers	Tx Laser Frequency 3 [High Resolution]	See B490h description	
B499-B49F	7				High Resolution Tuning Registers	Reserved	Reserved	
B4A0	16	15-0	RO	R	VR2 Network Lane TX Performance Monitoring Statistics Registers	Current Output Power	A signed 16-bit integer with the LSB = 0.01 dBm.	0000h
B4B0	16	15-0	RO	R	VR2 Network Lane TX Performance Monitoring Statistics Registers	Average Output Power over PM interval	A signed 16-bit integer with the LSB = 0.01 dBm.	0000h
B4C0	16	15-0	RO	R	VR2 Network Lane TX Performance Monitoring Statistics Registers	Minimum Output Power over PM interval	A signed 16-bit integer with the LSB = 0.01 dBm.	0000h
B4D0	16	15-0	RO	R	VR2 Network Lane TX Performance Monitoring Statistics Registers	Maximum Output Power over PM interval	A signed 16-bit integer with the LSB = 0.01 dBm.	0000h
B4E0	16	15-0	RO	R	Network Lane RX Performance Monitoring Statistics Registers	Current Input Power [Total Rx Optical Input]	A signed 16-bit integer with the LSB = 0.01 dBm.	0000h
B4F0	16	15-0	RO	R	Network Lane RX Performance Monitoring Statistics Registers	Average Input Power over PM interval [Total Rx Optical Input]	A signed 16-bit integer with the LSB = 0.01 dBm.	0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
B500	16	15-0	RO	R	Network Lane RX Performance Monitoring Statistics Registers	Minimum Input Power over PM interval [Total Rx Optical Input]	A signed 16-bit integer with the LSB = 0.01 dBm.	0000h
B510	16	15-0	RO	R	Network Lane RX Performance Monitoring Statistics Registers	Maximum Input Power over PM interval [Total Rx Optical Input]	A signed 16-bit integer with the LSB = 0.01 dBm.	0000h
B520	96	15-0			Network Lane RX Performance Monitoring Statistics Registers	Reserved	Reserved	
B580-B7FF	640				Reserved	Reserved	Reserved	
B800-BADF	1024				Network RX Performance Monitoring Statistics Registers (Optional)	Reserved	Reserved	
BAE0	1	15-0	RO	O	Tx De-Skew and Equalization	Tx Skew XI to XI	The skew between XI and XI. Value is usually zero. A signed 16-bit integer with 1 LSB = 0.1ps	0000h
BAE1	1	15-0	RO	O	Tx De-Skew and Equalization	Tx Skew XI to YI	The skew between XI and YI. A signed 16-bit integer with 1 LSB = 0.1ps	0000h
BAE2	1	15-0	RO	O	Tx De-Skew and Equalization	Tx Skew XI to XQ	The skew between XI and XQ. A signed 16-bit integer with 1 LSB = 0.1ps	0000h
BAE3	1	15-0	RO	O	Tx De-Skew and Equalization	Tx Skew YI to YQ	The skew between YI and YQ. A signed 16-bit integer with 1 LSB = 0.1ps	0000h
BAE4	1	15-0	RO	O	Tx De-Skew and Equalization	Module Temperature for Tx Calibration Data	Module case temperature in degrees Celsius for the calibration data set, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 degC. MSA valid range is between –40 and +125C.	0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
BAE5	1	15-0	RO	O	Tx De-Skew and Equalization	Tx S21 Data Start Frequency	The start frequency of the Tx frequency response data stored on the device. A 16-bit unsigned integer in MHz. Valid range is between 0 and 65535 MHz.	0000h
BAE6	1	15-0	RO	O	Tx De-Skew and Equalization	Tx S21 Data Stop Frequency	The stop frequency of the Tx frequency response data stored on the device. A 16-bit unsigned integer in MHz. Valid range is between 0 and 65535 MHz.	0000h
BAE7	1	15-0	RO	O	Tx De-Skew and Equalization	Tx S21 Data Frequency Spacing	The frequency spacing of the Rx frequency response data stored on the device. An unsigned integer in MHz. Valid range is between 0 and 65535 MHz.	0000h
BAE8	1	15-0	RO	O	Rx De-Skew and Equalization	Rx Skew XI to XI	The skew between XI and XI. Value is usually zero. A signed 16-bit integer with 1 LSB = 0.1ps.	0000h
BAE9	1	15-0	RO	O	Rx De-Skew and Equalization	Rx Skew XI to YI	The skew between XI and YI. A signed 16-bit integer with 1 LSB = 0.1ps.	0000h
BAEA	1	15-0	RO	O	Rx De-Skew and Equalization	Rx Skew XI to XQ	The skew between XI and XQ. A signed 16-bit integer with 1 LSB = 0.1ps.	0000h
BAEB	1	15-0	RO	O	Rx De-Skew and Equalization	Rx Skew YI to YQ	The skew between YI and YQ. A signed 16-bit integer with 1 LSB = 0.1ps.	0000h
BAEC	1	15-0	RO	O	Rx De-Skew and Equalization	Module Temperature for Rx Calibration Data	Module case temperature in degrees Celsius for the calibration data set, a 16-bit signed integer with LSB = 1/256 of a degree Celsius,	0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							representing a total range from -128 to + 127 255/256 degC. MSA valid range is between –40 and +125C.	
BAED	1	15-0	RO	O	Rx De-Skew and Equalization	Rx S21 Data Start Frequency	The start frequency of the Rx frequency response data stored on the device. A 16-bit unsigned integer in MHz. Valid range is between 0 and 65535 MHz.	0000h
BAEE	1	15-0	RO	O	Rx De-Skew and Equalization	Rx S21 Data Stop Frequency	The stop frequency of the Rx frequency response data stored on the device. A 16-bit unsigned integer in MHz. Valid range is between 0 and 65535 MHz.	0000h
BAEF	1	15-0	RO	O	Rx De-Skew and Equalization	Rx S21 Data Frequency Spacing	The frequency spacing of the Rx frequency response data stored on the device. An unsigned integer in MHz. Valid range is between 0 and 65535 MHz.	0000h
BAF0	1	15-0	RW	O	S Parameter Data Registers	Table Index	Index number which allows access to magnitude and phase data in memory. Starting at 0. Last index is (Stop Frequency – Start Frequency) / Frequency Step.	0000h
BAF1	1			O	S Parameter Data Registers	Table Select		0000h
		15-2			S Parameter Data Registers	Reserved		
		1-0	RW		S Parameter Data Registers	Table Select	0 = Reserved 1 = TX Data 2 = RX Data 3 = Reserved	00b
BAF2	1			O	S Parameter Data Registers	Table Status		0000h
		15-2			S Parameter Data Registers	Reserved		
		1-0	RO	O	S Parameter Data Registers	Table Status	0 = Not Initialised 1 = Busy 2 = Data Ready	00b

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							3 = Error This register will have value = 0 at module startup. Writing an index value to the Table Index register BAF0 will initiate reading data from internal memory and populating the data registers BAF8-BAFF. During this time this register will have value = 1 (Busy). When all data registers have been populated this register will have either value = 2 (Data Ready) if the command completed successfully, or value = 3 (Error), if the Table Index or Table Select registers have invalid values or if there was a fault.	
BAF3	1	15-0	RW	O	S Parameter Data Registers	Table Format Version	Table Format Version – register to track changes to format of data registers BAF8 – BAFF.	0000h
BAF4	4	15-0			S Parameter Data Registers	Reserved		0000h
BAF8	1	15-0	RO	O	S Parameter Data Registers	XI Amplitude Value	Amplitude response for XI tributary normalized to 1GHz A 16-bit signed integer with 1 LSB = 0.01dBe.	0000h
BAF9	1	15-0	RO	O	S Parameter Data Registers	XI Phase Value	Unwrapped Phase response for XI tributary. A 16-bit signed integer with 1 LSB = 0.1deg.	0000h
BAFA	1	15-0	RO	O	S Parameter Data Registers	YI Amplitude Value	Amplitude response for YI tributary normalized to 1GHz A 16-bit signed integer with 1 LSB = 0.01dBe.	0000h
BAFB	1	15-0	RO	O	S Parameter Data Registers	YI Phase Value	Unwrapped Phase response for YI tributary. A 16-bit signed	0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							integer with 1 LSB = 0.1deg.	
BAFC	1	15-0	RO	O	S Parameter Data Registers	XQ Amplitude Value	Amplitude response for XQ tributary normalized to 1GHz. A 16-bit signed integer with 1 LSB = 0.01dBe.	0000h
BAFD	1	15-0	RO	O	S Parameter Data Registers	XQ Phase Value	Unwrapped Phase response for XQ tributary. A 16-bit signed integer with 1 LSB = 0.1deg.	0000h
BAFE	1	15-0	RO	O	S Parameter Data Registers	YQ Amplitude Value	Amplitude response for YQ tributary normalized to 1GHz. A 16-bit signed integer with 1 LSB = 0.01dBe.	0000h
BAFF	1	15-0	RO	O	S Parameter Data Registers	YQ Phase Value	Unwrapped Phase response for YQ tributary. A 16-bit signed integer with 1 LSB = 0.1deg.	0000h
BB00	1		RO	R	Tx Subsystem General	Tx RF Channel Mapping		
		15	RO	R	Tx Subsystem General	X:Y mapping	0 = X:Y 1 = Y:X As defined in CFP2-ACO IA Section 9.7 and Table 3	0b
		14-13	RO	R	Tx Subsystem General	I,Q mapping	00 = I,Q:I,Q 01 =Q,I:Q,I 10 = I,Q:Q,I 11 = Q,I:I,Q As defined in CFP2-ACO IA Section 9.7 and Table 3.	00b
		12-10	RO	R	Tx Subsystem General	P/N mapping	000 = p/n,p/n:p/n,p/n 001 = n/p,n/p:n/p,n/p 010 = p/n,p/n:n/p,n/p 011 = n/p,n/p:p/n,p/n 100 = p/n,n/p:p/n,n/p 101 = n/p,p/n:n/p,p/n 110 = p/n,n/p:n/p,p/n 111 = n/p,p/n:p/n,n/p As defined in CFP2-ACO IA Section 9.7 and Table 3.	000b

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		9	RO	O	Tx Subsystem General	Tx Skew Values	0 = Not stored on device 1 = Stored on device (see CFP2-ACO IA Section 12.7 for details on storage format.)	0b
		8	RO	O	Tx Subsystem General	Tx frequency response amplitude data	(See above)	0b
		7	RO	O	Tx Subsystem General	Tx frequency response phase data	(See above)	0b
		6-0			Tx Subsystem General	Reserved		
BB01	1				Tx Subsystem General	Reserved	Reserved	
BB02	1				Tx Subsystem General	Reserved	Reserved	
BB03	1				Tx Subsystem General	Reserved	Reserved	
BB04	1			O	Tx Subsystem General	Tx Driver Features	Summary of available TX Driver features	
		15-14	RO	O	Tx Subsystem General	TX RF Driver Type	00=Limiting 01=Linear 10=Reserved 11=Reserved	
		13	RO	O	Tx Subsystem General	Tx RF Driver Enable/Disable (BB5F) by Channel	0: Not available 1: Available,	
		12	RO	O	Tx Subsystem General	Tx RF Driver Adjustable Gain (BB64) / Amplitude (BB6C) by Channel		
		11	RO	O	Tx Subsystem General	Tx RF Driver Adjustable Current (BB68) / Crossing (BB70) by Channel		
		10	RO	O	Tx Subsystem General	Tx RF Driver Transfer Function Equalization (BB74) by Channel		
		9	RO	O	Tx Subsystem General	Tx RF Driver Output Detector (BB75) by Channel		
		8	RO	O	Tx Subsystem General	Tx RF Driver Control to Target (BB5B) by Channel		
		7-6	RO	O	Tx Subsystem General	Tx RF Driver Output Detector Type	00: Peak, 01: Average 10: Reserved 11: Reserved	
		5-0			Tx Subsystem General	Reserved	Reserved	
BB05	1			R	Tx Subsystem General	Modulation Format Availability	Modulation format availability for the IC-TROSA.	
		15-14	RO	R	Tx Subsystem General	DP-QPSK	00 = Unsupported, 01 = NRZ, 10 = RZ, 11 = Both	0b

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		13-12	RO	R	Tx Subsystem General	DP-BPSK	00 = Unsupported, 01 = NRZ, 10 = RZ, 11 = Both	0b
		11-10	RO	R	Tx Subsystem General	DP-8QAM	00 = Unsupported, 01 = NRZ, 10 = RZ, 11 = Both	0b
		9-8	RO	R	Tx Subsystem General	DP-16QAM	00 = Unsupported, 01 = NRZ, 10 = RZ, 11 = Both	0b
		7-6	RO	R	Tx Subsystem General	DP-32QAM	00 = Unsupported, 01 = NRZ, 10 = RZ, 11 = Both	0b
		5-4	RO	R	Tx Subsystem General	DP-64QAM	00 = Unsupported, 01 = NRZ, 10 = RZ, 11 = Both	0b
		3-2	RO	R	Tx Subsystem General	DP-128QAM	00 = Unsupported, 01 = NRZ, 10 = RZ, 11 = Both	0b
		1-0	RO	R	Tx Subsystem General	DP-256QAM	00 = Unsupported, 01 = NRZ, 10 = RZ, 11 = Both	0b
BB06	1		RW	R	Tx Subsystem General	Modulation Format Select	Modulation format select for IC-TROSA	
		15-14	RW	O	Tx Subsystem General	RZ/NRZ Encoding	00 = Undefined, 01 = NRZ, 10 = RZ, 11 = Reserved.	
		13	RW	O	Tx Subsystem General	Differential Encoding Status	0: Non-Differentially Encoded 1: Differentially Encoded	
		12-10	RW	O	Tx Subsystem General	Nyquist Spectral Shaping Factor	000: None 001: Beta = 0.1 010: Beta = 0.2 011: Beta = 0.3 100: Beta = 0.4 101: Beta = 0.5 110: Beta = 0.6 111: Beta = Unspecified	
		9			Tx Subsystem General	Reserved	Reserved	
		8			Tx Subsystem General	Reserved	Reserved	
		7-0	RW	R	Tx Subsystem General	Modulation Format	00h – DP-QPSK 01h – DP-BPSK 02h – DP-8QAM 03h – DP-16QAM 04h – DP-32QAM 05h – DP-64QAM 06h – DP-128QAM 07h - DP-256QAM 08-FF Reserved	
BB07	1	15-0	RW	O	Tx Subsystem General	Baud Rate	Set register for IC-TROSA Baud Rate. An unsigned 16-bit integer with 1 LSB=0.001GBaud	0000h
BB08	8				Tx Subsystem General	Reserved	Reserved	

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
BB0A	1			O	Tx Subsystem General	Module Tx Hardware Response Pending Flags		
		15	RO	O	Tx Subsystem General	Tx Fine Tune Frequency (B430) In Progress	0:Deasserted, 1:Asserted	0b
		14-0			Tx Subsystem General	Reserve		
BB10	1	15-0	RO	O	Tx Subsystem Output-Referred Optical Power Monitoring	Tx Optical Power Monitor, Current Post Pol-Mux In-Line	A signed 16-bit integer with 1 LSB = 0.01dBm.	0000h
BB11	1	15-0	RO	O	Tx Subsystem Output-Referred Optical Power Monitoring	Tx Optical Power Monitor, Average Post Pol-Mux In-Line over PM interval	A signed 16-bit integer with 1 LSB = 0.01dBm.	0000h
BB12	1	15-0	RO	O	Tx Subsystem Output-Referred Optical Power Monitoring	Tx Optical Power Monitor, Minimum Post Pol-Mux In-Line over PM interval	A signed 16-bit integer with 1 LSB = 0.01dBm.	0000h
BB13	1	15-0	RO	O	Tx Subsystem Output-Referred Optical Power Monitoring	Tx Optical Power Maximum Post Pol-Mux In-Line over PM interval	A signed 16-bit integer with 1 LSB = 0.01dBm.	0000h
BB14	1	15-0	RO	O	Tx Subsystem Output-Referred Optical Power Monitoring	Tx Optical Power Monitor, Current X-Pol.	A signed 16-bit integer with 1 LSB = 0.01dBm.	0000h
BB15	1	15-0	RO	O	Tx Subsystem Output-Referred Optical Power Monitoring	Tx Optical Power Monitor, Average X-Pol. over PM interval	A signed 16-bit integer with 1 LSB = 0.01dBm.	0000h
BB16	1	15-0	RO	O	Tx Subsystem Output-Referred Optical Power Monitoring	Tx Optical Power Monitor, Minimum X-Pol. over PM interval	A signed 16-bit integer with 1 LSB = 0.01dBm.	0000h
BB17	1	15-0	RO	O	Tx Subsystem Output-Referred Optical Power Monitoring	Tx Optical Power Monitor, Maximum X-Pol. over PM interval	A signed 16-bit integer with 1 LSB = 0.01dBm.	0000h
BB18	1	15-0	RO	O	Tx Subsystem Output-Referred Optical Power Monitoring	Tx Optical Power Monitor, Current Y-Pol.	A signed 16-bit integer with 1 LSB = 0.01dBm.	0000h
BB19	1	15-0	RO	O	Tx Subsystem Output-Referred Optical Power Monitoring	Tx Optical Power Monitor, Average Y-Pol. over PM interval	A signed 16-bit integer with 1 LSB = 0.01dBm.	0000h
BB1A	1	15-0	RO	O	Tx Subsystem Output-Referred	Tx Optical Power Monitor, Minimum Y-Pol. over PM interval	A signed 16-bit integer with 1 LSB = 0.01dBm.	0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
					Optical Power Monitoring			
BB1B	1	15-0	RO	O	Tx Subsystem Output-Referred Optical Power Monitoring	Tx Optical Power Monitor, Maximum Y-Pol. over PM interval	A signed 16-bit integer with 1 LSB = 0.01dBm.	0000h
BB1C	4	15-0	RO	O	Tx Subsystem Output-Referred Optical Power Monitoring	Tx Optical Power Monitor, Current PMQ Channel [XI, XQ, YI, YQ]	4 registers, one for each PMQ channel [XI, XQ, YI, YQ] complementary power monitor. A signed 16-bit integer with 1 LSB = 0.01dBm.	0000h
BB20	4	15-0	RO	O	Tx Subsystem Output-Referred Optical Power Monitoring	Tx Optical Power Monitor, Average PMQ Channel [XI, XQ, YI, YQ] over PM interval	4 registers, one for each PMQ channel [XI, XQ, YI, YQ] complementary power monitor. A signed 16-bit integer with 1 LSB = 0.01dBm.	0000h
BB24	4	15-0	RO	O	Tx Subsystem Output-Referred Optical Power Monitoring	Tx Optical Power Monitor, Minimum PMQ Channel [XI, XQ, YI, YQ] over PM interval	4 registers, one for each PMQ channel [XI, XQ, YI, YQ] complementary power monitor. A signed 16-bit integer with 1 LSB = 0.01dBm.	0000h
BB28	4	15-0	RO	O	Tx Subsystem Output-Referred Optical Power Monitoring	Tx Optical Power Monitor, Maximum PMQ Channel [XI, XQ, YI, YQ] over PM interval	4 registers, one for each PMQ channel [XI, XQ, YI, YQ] complementary power monitor. A signed 16-bit integer with 1 LSB = 0.01dBm.	0000h
BB2C	1		RW	O	Tx Subsystem Power Control [14.4 Provides Existing Tx Total Output Power Control Registers]	Tx. Power Control		
		15	RW	O	Tx Subsystem Power Control [14.4 Provides Existing Tx Total Output Power Control Registers]	Tx. Total Power Control to Target	1: Enable, 0: Disable	0b
		14	RW	O	Tx Subsystem Power Control [14.4 Provides Existing Tx Total Output Power Control Registers]	Tx. X-Pol. Power Control to Target	1: Enable, 0: Disable	0b

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		13	RW	O	Tx Subsystem Power Control [14.4 Provides Existing Tx Total Output Power Control Registers]	Tx. Y-Pol. Power Control to Target	1: Enable, 0: Disable	0b
		12	RW	O	Tx Subsystem Power Control [14.4 Provides Existing Tx Total Output Power Control Registers]	Tx. Optical Output Enable	1: Tx VOA/shutter open, 0: Tx. VOA/Shutter blocked.	0b
		11-0		O	Tx Subsystem Power Control [14.4 Provides Existing Tx Total Output Power Control Registers]	Reserved		0
BB2D	1	15-0	RW	O	Tx Subsystem Power Control [14.4 Provides Existing Tx Total Output Power Control Registers]	Tx X-Pol. Optical Power Target	Power Target at Tx X Pol. Optical Power Monitor. A signed 16-bit integer with the LSB = 0.01dBm. Dependent on modulation format and modulation depth.	0000h
BB2E	1	15-0	RW	O	Tx Subsystem Power Control [14.4 Provides Existing Tx Total Output Power Control Registers]	Tx Y-Pol. Optical Power Target	Power Target at Tx Y Pol. Optical Power Monitor. A signed 16-bit integer with the LSB = 0.01dBm. Dependent on modulation format and modulation depth.	0000h
BB2F	1	15-0	RW	O	Tx Subsystem Power Control [14.4 Provides Existing Tx Total Output Power Control Registers]	Tx X-Pol. Optical Power Controller Drive Signal (A.U.)	An unsigned 16-bit integer with the LSB = A.U. X-Pol. optical power will respond monotonically to this drive signal register. This register can be written if the "Tx X-Pol. Control to Target" is disabled. The A.U. resolution is such that 1 LSB shall not result in a change of X-Pol. optical power >0.1dB. Anticipated implementations are a VOA or SOA. The 90% settling	0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							time of a change to this drive signal should be less than 100ms. The settling time includes any TWI/processing latency, and the actual hardware settling time.	
BB30	1	15-0	RW	O	Tx Subsystem Power Control [14.4 Provides Existing Tx Total Output Power Control Registers]	Tx Y-Pol. Optical Power Controller Drive Signal (A.U.)	An unsigned 16-bit integer with the LSB = A.U. Y-Pol. optical power will respond monotonically to this drive signal register. This register can be written if the "Tx Y-Pol. Control to Target" is disabled. The A.U. resolution is such that 1 LSB shall not result in a change of Y-Pol. optical power >0.1dB. Anticipated implementations are a VOA or SOA. The 90% settling time of a change to this drive signal should be less than 100ms. The settling time includes any TWI/processing latency, and the actual hardware settling time.	0000h
BB31	1	15-0	RW	O	Tx Subsystem Power Control [14.4 Provides Existing Tx Total Output Power Control Registers]	Tx Post Pol. Mux Total Optical Power Controller Drive Signal (A.U.)	A signed 16-bit integer with the LSB = A.U. The post Pol. Mux total optical power will respond monotonically to this drive signal register. This register can be written if the "Tx Total Output Power Control to Target" is disabled. The A.U. resolution is such that 1 LSB shall not result in a change of the total optical power >0.1dB. Anticipated implementations are a VOA, a SOA or	0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							an EDFA. The 90% settling time of a change to this drive signal should be less than 100ms. The settling time includes any TWI/processing latency, and the actual hardware settling time.	
BB32	1	15-0	RW	O	Tx Subsystem Power Control [14.4 Provides Existing Tx Total Output Power Control Registers]	Laser Output Power Enable/Disable	This register can only be controlled at the TX-off State or later, including the Ready State. The module State should be independent of BB32. A change in this register should not impact the module State, and vice versa. The default is 0: Disable, and this shall remain until being changed by the Host.	0
		15	RW	O	Tx Subsystem Power Control [14.4 Provides Existing Tx Total Output Power Control Registers]	Tx Laser Output Power Enable	1: Enable, Laser output power is turned on. 0: Disable, Laser output power is turned off; however, the laser controller, TEC, etc. should remain on.	
		14			Tx Subsystem Power Control [14.4 Provides Existing Tx Total Output Power Control Registers]	Reserved	Reserved	
		13-0			Tx Subsystem Power Control [14.4 Provides Existing Tx Total Output Power Control Registers]	Reserved	Reserved	
BB33	1		RW	O	PMQ Operation Control	PMQ Inner MZ Bias Point Targets		
		15-13	RW	O	PMQ Operation Control	XI MZ Bias Target Point	Min=MZ output minimum, Max=MZ output maximum, Quad=MZ output at quadrature. Min	000b

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							1(2) corresponds to the first (second) Min point found as the bias is increased from its minimum value to its maximum value. Max 1(2) is similarly defined. 000 = Min 1, 001 = Min 2 010 = Max 1, 011 = Max 2 100 = Quad 1, 101 = Quad 2 110 = Reserved, 111 = Reserved.	
		12-10	RW	O	PMQ Operation Control	XQ MZ Bias Target Point	(See above)	000b
		9-7	RW	O	PMQ Operation Control	YI MZ Bias Target Point	(See above)	000b
		6-4	RW	O	PMQ Operation Control	YQ MZ Bias Target Point	(See above)	000b
		3-0	RW	O	PMQ Operation Control	Reserved		0000b
BB34	1		RW	O	PMQ Operation Control	PMQ Outer MZ Bias Point Targets		
		15-13	RW	O	PMQ Operation Control	X Pol. Outer MZ Bias Target Point	Min=MZ output minimum, Max=MZ output maximum, Quad=MZ output at quadrature. Min 1(2) corresponds to the first (second) Min point found as the bias is increased from its minimum value to its maximum value. Max 1(2) is similarly defined. 000 = Min 1, 001 = Min 2 010 = Max 1, 011 = Max 2 100 = Quad 1, 101 = Quad 2 110 = Reserved, 111 = Reserved.	100b
		12-10	RW	O	PMQ Operation Control	Y Pol. Outer MZ Bias Target Point	(See above)	100b
		9-0			PMQ Operation Control	Reserved		0
BB35	1		RW	O	PMQ Operation Control	PMQ Bias and Per Pol. Power Control		
		15-14			PMQ Operation Control	Reserved		0b
		13	RW	O	PMQ Operation Control	Tx X-Pol. Outer MZ Bias Point Control to Target	1: Enable, 0: Disable	0b

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		12	RW	O	PMQ Operation Control	Tx Y-Pol. Outer MZ Bias Point Control to Target	1: Enable, 0: Disable	0b
		11	RW	O	PMQ Operation Control	XI MZ Bias Point Control to Target	1: Enable, 0: Disable	0b
		10	RW	O	PMQ Operation Control	XQ MZ Bias Point Control to Target	1: Enable, 0: Disable	0b
		9	RW	O	PMQ Operation Control	YI MZ Bias Point Control to Target	1: Enable, 0: Disable	0b
		8	RW	O	PMQ Operation Control	YQ MZ Bias Point Control to Target	1: Enable, 0: Disable	0b
		7-0			PMQ Operation Control	Reserved		0
BB36	1				PMQ Operation Control	Reserved	Reserved	
BB37	1				PMQ Operation Control	Reserved	Reserved	
BB38	12	15-0	RW	O	PMQ Operation Control	PMQ Inner/Outer MZ Phase Controller Drive Signal (A.U.)	12 registers, one for each possible inner/outer MZ arm phase control electrode [XL, XR, YL, YR, XIp, XIn, XQp, XQn, YIp, YIn, YQp, YQn.] An unsigned 16-bit integer with the LSB = A.U. The selected MZ arm phase will respond monotonically to this drive signal register. These registers can be written if the appropriate "MZ Bias Point Control to Target" is disabled. The A.U. resolution is such that 1 LSB shall not result in a change of MZ arm phase > 5 milliradians. The 90% settling time of a change to this drive signal should be less than 100ms. The settling time includes any TWI/processing latency, and the actual hardware settling time.	???
BB44	8	15-0	RO	O	PMQ Operation Control	PMQ RF Phase Shifter Applied DC Bias	8 registers, one for each RF phase shifter DC bias [XIp, XIn, XQp, XQn, YIp, YIn, YQp, YQn]. A 16-bit signed integer with 1 LSB = 2mV.	0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
BB4C	1	15-0	RO	O	PMQ Operation Control	PMQ Case Temperature	Measured temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 degC. MSA valid range is between -40 and +125C. Accuracy shall be better than +/- 3 degC over the whole temperature range.	0000h
BB4D	1	15-0	RO	O	PMQ Operation Control	PMQ Chip Temperature	Measured temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 degC. MSA valid range is between –40 and +125C. Accuracy shall be better than +/- 3 degC over the whole temperature range.	0000h
BB4E	6				PMQ Operation Control	Reserved	Reserved	
BB54	1		RW	R	Linear/Limiting Tx Driver Control	Host Tx RF Enabled Status	This register is intended to be set by the Host to indicate the status of the Host Tx RF input signals to the module.	
		15	RW	R	Linear/Limiting Tx Driver Control	XI Tx Channel RF Input Active	1: True, 0: False	0b
		14	RW	R	Linear/Limiting Tx Driver Control	XQ Tx Channel RF Input Active	1: True, 0: False	0b
		13	RW	R	Linear/Limiting Tx Driver Control	YI Tx Channel RF Input Active	1: True, 0: False	0b
		12	RW	R	Linear/Limiting Tx Driver Control	YQ Tx Channel RF Input Active	1: True, 0: False	0b
		11-0			Linear/Limiting Tx Driver Control	Reserved		

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
BB55	1		RO	O	Linear/Limiting Tx Driver Control	Module Confirmation of Host Tx RF Enabled Status	Module conformation of the Host Tx RF Enabled status.	
		15	RO	O	Linear/Limiting Tx Driver Control	XI Tx Channel RF Input Active	1: True, 0: False	0b
		14	RO	O	Linear/Limiting Tx Driver Control	XQ Tx Channel RF Input Active	1: True, 0: False	0b
		13	RO	O	Linear/Limiting Tx Driver Control	YI Tx Channel RF Input Active	1: True, 0: False	0b
		12	RO	O	Linear/Limiting Tx Driver Control	YQ Tx Channel RF Input Active	1: True, 0: False	0b
		11-0			Linear/Limiting Tx Driver Control	Reserved		
BB56	4	15-0	RW	O	Linear/Limiting Tx Driver Control	Driver Input Amplitude Peak to Average Power Ratio (PAPR) by Channel	4 registers, one for each channel [XI, XQ, YI, YQ]. An unsigned 16-bit integer with 1 LSB=0.002%.	0000h
BB5A	1		RW	O	Linear/Limiting Tx Driver Control	Normalized Tx RF Drive Level		
		15-9	RW	O	Linear/Limiting Tx Driver Control	Peak Tx RF Drive Level as a Percentage of 2*Vpi	Values in the range 0 to 100%. An unsigned 6 bit number with 1 LSB = 2%. Anticipated typical range from 50% to 70%.	
		8-0			Linear/Limiting Tx Driver Control	Reserved		0
BB5B	4	15-0	RW	O	Linear/Limiting Tx Driver Control	Tx Driver RF Output Target	The Tx driver RF output target is provided as a peak or average value, matching the RF Output Detector Type returned by Tx Driver Features. 4 registers, one for each Tx channel [XI, XQ, YI, YQ]. An unsigned 16-bit integer with 1 LSB = The voltage for 0.1 milliradians of channel RF optical phase shift assuming the driver output amplitude is	0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							linearly normalized to the channel Vpi.	
BB5F	1		RW	O	Linear/Limiting Tx Driver Control	Tx Driver Control	The 'Tx Driver Channel RF Enable' bits can only be enabled from the 'Tx-Off State' defined by the CFP MSA	
		15	RW	O	Linear/Limiting Tx Driver Control	Tx Driver XI Channel RF Enable	1: Enable, 0: Disable.	0b
		14	RW	O	Linear/Limiting Tx Driver Control	Tx Driver XQ Channel RF Enable	1: Enable, 0: Disable.	0b
		13	RW	O	Linear/Limiting Tx Driver Control	Tx Driver YI Channel RF Enable	1: Enable, 0: Disable.	0b
		12	RW	O	Linear/Limiting Tx Driver Control	Tx Driver YQ Channel RF Enable	1: Enable, 0: Disable.	0b
		11	RW	O	Linear/Limiting Tx Driver Control	Tx Driver XI Channel RF Output Control to Target	1: Enable, 0: Disable.	0b
		10	RW	O	Linear/Limiting Tx Driver Control	Tx Driver XQ Channel RF Output Control to Target	1: Enable, 0: Disable.	0b
		9	RW	O	Linear/Limiting Tx Driver Control	Tx Driver YI Channel RF Output Control to Target	1: Enable, 0: Disable.	0b
		8	RW	O	Linear/Limiting Tx Driver Control	Tx Driver YQ Channel RF Output Control to Target	1: Enable, 0: Disable.	0b
		7-0			Linear/Limiting Tx Driver Control	Reserved		0
BB60	4		RO		Linear/Limiting Tx Driver Control	Reserved	Reserved	
BB64	4	15-0	RW	O	Linear/Limiting Tx Driver Control	Linear Tx Driver Gain by Channel	4 registers, one for each Tx channel [XI, XQ, YI, YQ]. An unsigned 16-bit integer with 1 LSB = 0.001dB	0000h
BB68	4	15-0	RW	O	Linear/Limiting Tx Driver Control	Linear Tx Driver Current by Channel	4 registers, one for each Tx channel [XI, XQ, YI, YQ]. An unsigned 16-bit integer with 1 LSB = 10µA.	0000h
BB6C	4	15-0			Linear/Limiting Tx Driver Control	Reserved	Reserved	
BB70	4	15-0			Linear/Limiting Tx Driver Control	Reserved	Reserved	

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
BB74	1		RW	O	Linear/Limiting Tx Driver Control	RF Transfer Function Equalization provided by Tx Driver		
		15-12	RW	O	Linear/Limiting Tx Driver Control	XI RF Channel Equalization	Channel RF Transfer Function Equalization provided by the Tx Driver. 4-bit unsigned integer with LSB = A.U. Equalization capability is vendor specific.	000b
		11-8	RW	O	Linear/Limiting Tx Driver Control	XQ RF Channel Equalization	(See above)	000b
		7-4	RW	O	Linear/Limiting Tx Driver Control	YI RF Channel Equalization	(See above)	000b
		3-0	RW	O	Linear/Limiting Tx Driver Control	YQ RF Channel Equalization	(See above)	000b
BB75	4	15-0	RO	O	Linear Tx Driver Monitoring	Tx Driver Current RF Output Detector by Channel	4 registers, one for each Tx channel [XI, XQ, YI, YQ]. An unsigned 16-bit integer with 1 LSB = The voltage for 0.1 milliradians of channel RF optical phase shift assuming the driver output amplitude is linearly normalized to the channel Vpi. RF detector type is provided by the Tx Driver Features register.	0000h
BB79	4	15-0	RO	O	Linear Tx Driver Monitoring	Tx Driver Average RF Output Detector by Channel over PM interval	4 registers, one for each Tx channel [XI, XQ, YI, YQ]. An unsigned 16-bit integer with 1 LSB = The voltage for 0.1 milliradians of channel RF optical phase shift assuming the driver output amplitude is linearly normalized to the channel Vpi. RF detector type is provided by the Tx Driver Features register.	0000h
BB7D	4	15-0	RO	O	Linear Tx Driver Monitoring	Tx Driver Minimum RF Output Detector by	4 registers instances, one for each Tx channel [XI,	0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
						Channel over PM interval	XQ, YI, YQ]. An unsigned 16-bit integer with 1 LSB = The voltage for 0.1 milliradians of channel RF optical phase shift assuming the driver output amplitude is linearly normalized to the channel Vpi. RF detector type is provided by the Tx Driver Features register.	
BB81	4	15-0	RO	O	Linear Tx Driver Monitoring	Tx Driver Maximum RF Output Detector by Channel over PM interval	4 registers instances, one for each Tx channel [XI, XQ, YI, YQ]. An unsigned 16-bit integer with 1 LSB = The voltage for 0.1 milliradians of channel RF optical phase shift assuming the driver output amplitude is linearly normalized to the channel Vpi. RF detector type is provided by the Tx Driver Features register.	0000h
BB85	1	15-0	RO	O	Linear Tx Driver Monitoring	Tx Driver Temperature Monitor	Measured temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 degC. MSA valid range is between –40 and +125C. Accuracy shall be better than +/- 3 degC over the whole temperature range.	0000h
BB86	4				Linear Tx Driver Monitoring	Reserved		
BB8A	1		RO	R	Rx Subsystem General	Rx RF Channel Mapping		
		15	RO	R	Rx Subsystem General	X:Y mapping	0 = X:Y 1 = Y:X As defined in CFP2-ACO IA Section 8.3 and Table 3.	0b
		14-13	RO	R	Rx Subsystem General	I,Q mapping	00 = I,Q:I,Q 01 =Q,I:Q,I	00b

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							10 = I,Q:Q,I 11 = Q,I:I,Q As defined in CFP2-ACO IA Section 8.3 and Table 3.	
		12-10	RO	R	Rx Subsystem General	P/N mapping	000 = p/n,p/n:p/n,p/n 001 = n/p,n/p:n/p,n/p 010 = p/n,p/n:n/p,n/p 011 = n/p,n/p:p/n,p/n 100 = p/n,n/p:p/n,n/p 101 = n/p,p/n:n/p,p/n 110 = p/n,n/p:n/p,p/n 111 = n/p,p/n:p/n,n/p As defined in CFP2-ACO IA Section 8.3 and Table 3.	000b
		9	RO	R	Rx Subsystem General	Rx Skew Values	0 = not stored on device 1 = stored on device (see CFP2-ACO IA Section 12.7 for details on storage format.)	0b
		8	RO	O	Rx Subsystem General	Rx frequency response amplitude data	(See above)	0b
		7	RO	O	Rx Subsystem General	Rx frequency response phase data	(See above)	0b
		6-0			Rx Subsystem General	Reserved		
BB8B	1				Rx Subsystem General	Reserved	Reserved	
BB8C	1				Rx Subsystem General	Reserved	Reserved	
BB8D	1		RW	R	Rx Subsystem General	Rx Subsystem Control		
		15	RW	R	Rx Subsystem General	TIA/VGA MGC/AGC for Y Pol.	0: MGC Mode, 1: AGC Mode. If TIA/VGA MGC/AGC Selection by Pol. [BB8Ch-7] is not available then changing either bit[15] or bit [14] will change both polarizations.	0b
		14	RW	R	Rx Subsystem General	TIA/VGA MGC/AGC for X Pol.	(See above)	0b
		13	RW	R	Rx Subsystem General	RF Output Shutdown for Y Pol. Enable	1: Shutdown Enabled, 0: Shutdown Disabled. If RF Shutdown by Pol. [BB8Ch-15] is	0b

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							not available then setting either bit [13] or bit [12] to "1" will lead to RF output shutdown on both polarizations.	
		12	RW	R	Rx Subsystem General	RF Output Shutdown for X Pol. Enable	(See above)	0b
		11	RW	R	Rx Subsystem General	High Speed Photodiode Bias (All)	1: Enable, 0: Disable.	0b
		10	RW	R	Rx Subsystem General	X Pol. Rx VOA Control to Attenuation Target	1: Enable, 0: Disable. If a Total Power Rx VOA is present then enabling either bit 9 or bit 10 will enable the Rx VOA Control to Attenuation Target.	0b
		9	RW	R	Rx Subsystem General	Y-Pol. Rx VOA Control to Attenuation Target	1: Enable, 0: Disable. If a Total Power Rx VOA is present then enabling either bit 9 or bit 10 will enable the Rx VOA Control to Attenuation Target.	0b
		8			Rx Subsystem General	Reserved	Reserved	
		7-0			Rx Subsystem General	Reserved	Reserved	
BB8E	1		RW	O	Rx Subsystem General	Rx RF Channel Pre-Emphasis		
		15-12	RW	O	Rx Subsystem General	XI Rx channel RF Pre-Emphasis	Rx channel pre-emphasis provided within the ACO. 4-bit unsigned integer with LSB = A.U. Pre-emphasis capability is vendor specific. An anticipated implementation maps the TIA/VGA analog gain peaking over frequency adjustment function to this register.	0
		11-8	RW	O	Rx Subsystem General	XQ Rx channel RF Pre-Emphasis	(See above)	0
		7-4	RW	O	Rx Subsystem General	YI Rx channel RF Pre-Emphasis	(See above)	0
		3-0	RW	O	Rx Subsystem General	YQ Rx channel RF Pre-Emphasis	(See above)	0
BB8F	4				Rx Subsystem General	Reserved	Reserved	
BB93	2	15-0	RW	O	Rx Optical Power VOA	Rx VOA Input-Referred Attenuation Target	2 registers are allocated. The 1st	0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							register is used for the total input power VOA attenuation target and the 2nd register is unused, unless the Rx input attenuation function is implemented as independent X and Y VOA's. In this circumstance, the 1st register is used for the X VOA attenuation target and the 2nd register is used for the Y VOA attenuation target. Register instances are unsigned 16-bit integers with 1 LSB = 0.01dB.	
BB95	2	15-0	RO	O	Rx Optical Power VOA	Rx VOA Input-Referred Maximum Selectable Attenuation	2 registers are allocated (See BB93 Rx VOA Input-Referred Attenuation Target.) Register instances are unsigned 16-bit integers with 1 LSB = 0.01dB.	
BB97	2	15-0	RO	O	Rx Optical Power VOA	Rx VOA Input-Referred Current Attenuation	2 registers are allocated (See BB93 Rx VOA Input-Referred Attenuation Target.) Register instances are unsigned 16-bit integers with 1 LSB = 0.01dB.	0000h
BB99	2	15-0	RO	O	Rx Optical Power VOA	Rx VOA Input-Referred Average Attenuation over PM interval	2 registers are allocated (See BB93 Rx VOA Input-Referred Attenuation Target.) Register instances are unsigned 16-bit integers with 1 LSB = 0.01dB.	0000h
BB9B	2	15-0	RO	O	Rx Optical Power VOA	Rx VOA Input-Referred Minimum Attenuation over PM interval	2 registers are allocated (See BB93 Rx VOA Input-Referred Attenuation Target.) Register instances are unsigned 16-bit integers with 1 LSB = 0.01dB.	0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
BB9D	2	15-0	RO	O	Rx Optical Power VOA	Rx VOA Input-Referred Maximum Attenuation over PM interval	2 registers are allocated (See BB93 Rx VOA Input-Referred Attenuation Target.) Register instances are unsigned 16-bit integers with 1 LSB = 0.01dB.	0000h
BB9F	2	15-0	RW	O	Rx Optical Power VOA	Rx VOA Controller Drive Signal (A.U.)	2 registers are allocated (See BB93 Rx VOA Input-Referred Attenuation Target.) An unsigned 16-bit integer with the LSB = A.U. The Rx VOA will respond monotonically to this drive signal register with 0000h the bright condition. This register can be written if the "Rx VOA Control to Target" is disabled. The A.U. resolution is such that 1 LSB shall not result in a change of optical power >0.1dB.	0000h
BBA1	2	15-0	RO	O	Rx Optical Power VOA	Rx VOA Controller Drive DAC Value at Minimum Attenuation	2 registers are allocated (See BB93 Rx VOA Input-Referred Attenuation Target.) Rx VOA controller drive DAC value at the Rx VOA minimum attenuation.	
BBA3	2	15-0	RO	O	Rx Optical Power VOA	Rx VOA Controller Drive DAC Value at Maximum Attenuation	2 registers are allocated (See BB93 Rx VOA Input-Referred Attenuation Target.) Rx VOA controller drive DAC value at the Rx VOA maximum attenuation.	
BBA5	8	15-0	RO	O	ICR Monitoring	ICR Individual PD Current Photocurrent	8 registers, one for each ICR individual PD [XIp, XIn, XQp, XQn, YIp, YIn, YQp, YQn]. An unsigned 16-bit integer with 1 LSB = 1uA.	0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
BBAD	8	15-0	RO	O	ICR Monitoring	ICR Individual PD Average Photocurrent over PM interval	8 registers, one for each ICR individual PD [XIp, XIn, XQp, XQn, YIp, YIn, YQp, YQn]. An unsigned 16-bit integer with 1 LSB = 1uA.	0000h
BBB5	4	15-0	RO	O	ICR Monitoring	ICR PD Current Photocurrent by Channel	4 registers, one for each ICR channel [XI, XQ, YI, YQ]. An unsigned 16-bit integer with the LSB = 1uA.	0000h
BBB9	4	15-0	RO	O	ICR Monitoring	ICR PD Average Photocurrent by Channel over PM interval	4 registers, one for each ICR channel [XI, XQ, YI, YQ]. An unsigned 16-bit integer with the LSB = 1uA.	0000h
BBBD	2	15-0	RO	O	ICR Monitoring	ICR PD Current Photocurrent by Polarization	2 registers, one for each ICR polarization [X, Y]. An unsigned 16-bit integer with the LSB = 1uA.	0000h
BBBF	2	15-0	RO	O	ICR Monitoring	ICR PD Average Photocurrent by Polarization over PM interval	2 registers, one for each ICR polarization [X, Y]. An unsigned 16-bit integer with the LSB = 1uA.	0000h
BBC1	2	15-0	RO	O	ICR Monitoring	ICR PD Minimum Photocurrent by Polarization over PM interval	2 registers, one for each ICR polarization [X, Y]. An unsigned 16-bit integer with the LSB = 1uA.	0000h
BBC3	2	15-0	RO	O	ICR Monitoring	ICR PD Maximum Photocurrent by Polarization over PM interval	2 registers, one for each ICR polarization [X, Y]. An unsigned 16-bit integer with the LSB = 1uA.	0000h
BBC5	1	15-0	RO	O	ICR Monitoring	ICR Internal Temperature	Internally measured temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 degC. MSA valid range is between -40 and +125C. Accuracy shall be better than +/- 3 degC over the whole temperature range.	0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
BBC6	2				ICR Monitoring	Reserved		
BBC8	4	15-0	RW	O	ICR RF Output Gain Control and RF Monitoring	TIA/VGA Gain Control Voltage by Channel	4 registers, one for each ICR channel [XI, XQ, YI, YQ]. Register can be written only when the corresponding Rx Subsystem Control register bit 15-14 is 0: MGC Mode. An unsigned 16-bit integer with 1 LSB = 60uV.	0000h
BBCC	4	15-0	RW	O	ICR RF Output Gain Control and RF Monitoring	TIA/VGA RF Output Target Adjust by Channel	4 registers, one for each ICR channel [XI, XQ, YI, YQ]. Register applicable only when the corresponding Rx Subsystem Control register bit 15-14 is 1: AGC Mode. A signed 16-bit integer with 1 LSB = 25µVppd. RF output detector type is provided by the Rx TIA/VGA Features register.	0000h
BBD0	4	15-0	RO	O	ICR RF Output Gain Control and RF Monitoring	LO Optical Power Monitor	The LO optical power input to the ICR. A signed integer in dBm*100. Equivalent to ITLA 0x42 OOP command.	0
BBD1	4	15-0	RW	O	ICR RF Output Gain Control and RF Monitoring	LO Optical Power Set-Point	Sets the LO optical power input to the ICR. A signed integer in dBm*100. Equivalent to ITLA 0x31 PWR command.	
BBD2	4	15-0	RO	O	ICR RF Output Gain Control and RF Monitoring	LO Optical Power Minimum Setting	Returns the minimum allowed LO optical power input to the ICR. A signed integer in dBm*100. Equivalent to ITLA 0x50 OPSL command.	
BBD3	4	15-0	RO	O	ICR RF Output Gain Control and RF Monitoring	LO Optical Power Maximum Setting	Returns the maximum allowed LO optical power input to the ICR. A signed integer in dBm*100. Equivalent to ITLA	

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							0x50 OPSH command.	
BBD4	4	15-0	RO	O	ICR RF Output Gain Control and RF Monitoring	TIA/VGA Current RF Output Detector by Channel	4 registers, one for each ICR channel [XI, XQ, YI, YQ]. A signed 16-bit integer with 1 LSB = 25µVppd. RF output detector type is provided by the Rx TIA/VGA Features register.	0000h
BBD8	4	15-0	RO	O	ICR RF Output Gain Control and RF Monitoring	TIA/VGA Average RF Output Detector by Channel over PM interval	4 registers, one for each ICR channel [XI, XQ, YI, YQ]. A signed 16-bit integer with 1 LSB = 25µVppd. RF output detector type is provided by the Rx TIA/VGA Features register.	0000h
BBDC	4	15-0	RO	O	ICR RF Output Gain Control and RF Monitoring	TIA/VGA Minimum RF Output Detector by Channel over PM interval	4 registers, one for each ICR channel [XI, XQ, YI, YQ]. A signed 16-bit integer with 1 LSB = 25µVppd. RF output detector type is provided by the Rx TIA/VGA Features register.	0000h
BBE0	4	15-0	RO	O	ICR RF Output Gain Control and RF Monitoring	TIA/VGA Maximum RF Output Detector by Channel over PM interval	4 registers, one for each ICR channel [XI, XQ, YI, YQ]. A signed 16-bit integer with 1 LSB = 25µVppd. RF output detector type is provided by the Rx TIA/VGA Features register.	0000h
BBE4	4	15-0	RO	O	ICR RF Output Gain Control and RF Monitoring	TIA/VGA Current RF Input Detector by Channel	4 registers, one for each ICR channel [XI, XQ, YI, YQ]. RF input detector type is provided by the Rx TIA/VGA Features register. For an RSSI type, units are input referred power [dBm], a signed 16-bit integer with 1 LSB=0.01dBm. For Peak and Mean types, units are uAppd, an unsigned 16-bit integer with 1 LSB = 0.1 uAppd.	0000h

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
BBE8	4	15-0	RO	O	ICR RF Output Gain Control and RF Monitoring	TIA/VGA Average RF Input Detector by Channel over PM interval	4 registers, one for each ICR channel [XI, XQ, YI, YQ]. RF input detector type is provided by the Rx TIA/VGA Features register. For an RSSI type, units are input referred power [dBm], a signed 16-bit integer with 1 LSB = 0.01dBm. For Peak and Mean types, units are Appd, an unsigned 16-bit integer with 1 LSB = 0.1 uAppd.	0000h
BBEC	4	15-0	RO	O	ICR RF Output Gain Control and RF Monitoring	TIA/VGA Minimum RF Input Detector by Channel over PM interval	4 registers, one for each ICR channel [XI, XQ, YI, YQ]. RF input detector type is provided by the Rx TIA/VGA Features register. For an RSSI type, units are input referred power [dBm], a signed 16-bit integer with 1 LSB=0.01dBm. For Peak and Mean types, units are Appd, an unsigned 16-bit integer with 1 LSB = 0.1 uAppd.	0000h
BBF0	4	15-0	RO	O	ICR RF Output Gain Control and RF Monitoring	TIA/VGA Maximum RF Input Detector by Channel over PM interval	4 registers, one for each ICR channel [XI, XQ, YI, YQ]. RF input detector type is provided by the Rx TIA/VGA Features register. For an RSSI type, units are input referred power [dBm], a signed 16-bit integer with 1 LSB=0.01dBm. For Peak and Mean types, units are Appd, an unsigned 16-bit integer with 1 LSB = 0.1 uAppd.	0000h
BBF4	1	15-0	RO	O	Rx Provisioned Channel Power Monitoring [Colorless Line Systems]	Current Provisioned Channel Power	The current input power in the provisioned channel. This register will differ from B4E0 in	

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							colorless network applications. A signed 16-bit integer with the LSB = 0.01dBm.	
BBF5	1	15-0	RW	O	Rx Provisioned Channel Power Monitoring [Colorless Line Systems]	Average Provisioned Channel Power over PM interval	The average input power in the provisioned channel over the PM interval. This register will differ from B4F0 in colorless network applications. A signed 16-bit integer with the LSB = 0.01dBm.	
BBF6	1	15-0	RO	O	Rx Provisioned Channel Power Monitoring [Colorless Line Systems]	Minimum Provisioned Channel Power over PM interval	The minimum input power in the provisioned channel over the PM interval. This register will differ from B500 in colorless network applications. A signed 16-bit integer with the LSB = 0.01dBm.	
BBF7	1	15-0	RO	O	Rx Provisioned Channel Power Monitoring [Colorless Line Systems]	Maximum Provisioned Channel Power over PM interval	The maximum input power in the provisioned channel over the PM interval. This register will differ from B510 in colorless network applications. A signed 16-bit integer with the LSB = 0.01dBm.	
BBF8	2	15-0	RO	O	Rx Optical Power Monitoring	Current Post-VOA Total Power	2 registers are allocated (See BB93 Rx VOA Input-Referred Attenuation Target.) Register instances are signed 16-bit integers with 1 LSB = 0.01dBm.	
BBFA	2	15-0	RO	O	Rx Optical Power Monitoring	Average Post-VOA Total Power over PM interval	2 registers are allocated (See BB93 Rx VOA Input-Referred Attenuation Target.) Register instances are signed 16-bit integers with 1 LSB = 0.01dBm.	

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
BBFC	2	15-0	RO	O	Rx Optical Power Monitoring	Minimum Post-VOA Total Power over Interval	2 registers are allocated (See BB93 Rx VOA Input-Referred Attenuation Target.) Register instances are signed 16-bit integers with 1 LSB = 0.01dBm.	
BBFE	2	15-0	RO	O	Rx Optical Power Monitoring	Maximum Post-VOA Total Power over Interval	2 registers are allocated (See BB93 Rx VOA Input-Referred Attenuation Target.) Register instances are signed 16-bit integers with 1 LSB = 0.01dBm.	
BC00	512	15-0	WO	O	VR2 Network Host-To-Module Bulk Data Transfer block (Optional)	Host-To-Module Bulk Data Transfer block	Variable size bulk data transfer block for transactions from Host to Module.	0
BE00	512	15-0	RO	O	VR2 Network Module to Host Bulk Data Transfer Block (Optional)	Module-To-Host Bulk Data Transfer block	Variable size bulk data transfer block for transactions from Module to Host.	0
C000	1			R	NVR IC-TROSA Control	OIF Bandwidth Classification		
		15-3			NVR IC-TROSA Control	Reserved	Reserved	0
		2	RO	R	NVR IC-TROSA Control	40GHz E-O Bandwidth Class	0: Not supported, 1: Supported.	0
		1	RO	R	NVR IC-TROSA Control	30GHz E-O Bandwidth Class	0: Not supported, 1: Supported.	0
		0	RO	R	NVR IC-TROSA Control	20GHz E-O Bandwidth Class	0: Not supported, 1: Supported.	0
C001	1			R	NVR IC-TROSA Control	Secondary Power Supply Enable Status	Used in conjunction with Secondary Power Supply handshake registers. This status bit is set by external host controller based on secondary power supply Pn power-up/down status	
		15-6	RW		NVR IC-TROSA Control	Reserved	Reserved	0

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		5	RW	R	NVR IC-TROSA Control	P6 Secondary Supply voltage Enabled Status	0: Not Enabled 1: Enabled	0
		4	RW	R	NVR IC-TROSA Control	P5 Secondary Supply voltage Enabled status		0
		3	RW	R	NVR IC-TROSA Control	P4 Secondary Supply voltage Enabled Status		0
		2	RW	R	NVR IC-TROSA Control	P3 Secondary Supply voltage Enabled Status		0
		1	RW	R	NVR IC-TROSA Control	P2 Secondary Supply voltage Enabled Status		0
		0	RW	R	NVR IC-TROSA Control	P1 Secondary Supply voltage Enabled Status		0
C002	1			O	NVR IC-TROSA Control	Power Supply Alarm Status Optional use. Alarm condition as reported by IC-TROSA. May be used to provide detailed information regarding Power Supply Fault condition (B01Eh, B02Ah)	For usage refer to FAWS register B01Eh bit 5	
		15-7			NVR IC-TROSA Control	Reserved	Reserved	
		6	RO	O	NVR IC-TROSA Control	P6 Secondary Supply Voltage Alarm	0: No Alarm 1: Alarm Condition (Voltage not within Vendor Specified Nominal Voltage Setpoint Range. Voltage limits must be located in vendor specific data area) This value is set/cleared by the IC-TROSA controller	0
		5	RO	O	NVR IC-TROSA Control	P5 Secondary Supply Voltage Alarm		0
		4	RO	O	NVR IC-TROSA Control	P4 Secondary Supply Voltage Alarm		0
		3	RO	O	NVR IC-TROSA Control	P3 Secondary Supply Voltage Alarm		0
		2	RO	O	NVR IC-TROSA Control	P2 Secondary Supply Voltage Alarm		0
		1	RO	O	NVR IC-TROSA Control	P1 Secondary Supply Voltage Alarm		0
		0	RO	O	NVR IC-TROSA Control	P0 Primary Supply Voltage Alarm		0
C003	12			R	NVR IC-TROSA Control	Secondary Power Supply Nominal Voltage Setpoints		

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		15-0			NVR IC-TROSA Control	Reserved	Reserved	0
		15-0			NVR IC-TROSA Control	Reserved	Reserved	0
		15-0			NVR IC-TROSA Control	Reserved	Reserved	0
		15-0			NVR IC-TROSA Control	Reserved	Reserved	0
		15-0			NVR IC-TROSA Control	Reserved	Reserved	0
		15-0			NVR IC-TROSA Control	Reserved	Reserved	0
		15-0	RO	R	NVR IC-TROSA Control	P6 Secondary power supply nominal voltage setpoint	16-BIT 2'S complement (signed) binary number representing set point voltage in millivolts	0
		15-0	RO	R	NVR IC-TROSA Control	P5 Secondary power supply nominal voltage setpoint		0
		15-0	RO	R	NVR IC-TROSA Control	P4 Secondary power supply nominal voltage setpoint		0
		15-0	RO	R	NVR IC-TROSA Control	P3 Secondary power supply nominal voltage setpoint		0
		15-0	RO	R	NVR IC-TROSA Control	P2 Secondary power supply nominal voltage setpoint		0
		15-0	RO	R	NVR IC-TROSA Control	P1 Secondary power supply nominal voltage setpoint		0
C00F	1			R	NVR IC-TROSA Control	Secondary Power Supply Power-Up Handshaking State		
		15-6			NVR IC-TROSA Control	Reserved	Reserved	0
		5	RO	R	NVR IC-TROSA Control	P6 Power-Up handshake	0: not ready or complete 1: Ready for power-up	0
		4	RO	R	NVR IC-TROSA Control	P5 Power-Up handshake	0: not ready or complete	0

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							1: Ready for power-up	
		3	RO	R	NVR IC-TROSA Control	P4 Power-Up handshake	0: not ready or complete 1: Ready for power-up	0
		2	RO	R	NVR IC-TROSA Control	P3 Power-Up handshake	0: not ready or complete 1: Ready for power-up	0
		1	RO	R	NVR IC-TROSA Control	P2 Power-Up handshake	0: not ready or complete 1: Ready for power-up	0
		0	RO	R	NVR IC-TROSA Control	P1 Power-Up handshake	0: not ready or complete 1: Ready for power-up	0
C010	1			R	NVR IC-TROSA Control	Secondary Power Supply Power-Down Handshaking State		
		15-6			NVR IC-TROSA Control	Reserved	Reserved	0
		5	RO	R	NVR IC-TROSA Control	P6 Power-Down handshake	0: not ready or complete 1: Ready for power-down	0
		4	RO	R	NVR IC-TROSA Control	P5 Power-Down handshake	0: not ready or complete 1: Ready for power-down	0
		3	RO	R	NVR IC-TROSA Control	P4 Power-Down handshake	0: not ready or complete 1: Ready for power-down	0
		2	RO	R	NVR IC-TROSA Control	P3 Power-Down handshake	0: not ready or complete 1: Ready for power-down	0
		1	RO	R	NVR IC-TROSA Control	P2 Power-Down handshake	0: not ready or complete 1: Ready for power-down	0
		0	RO	R	NVR IC-TROSA Control	P1 Power-Down handshake	0: not ready or complete 1: Ready for power-down	0
C011-C026	22				NVR IC-TROSA Control	Reserved	Reserved	
C027	3			R	NVR IC-TROSA Control	Secondary Power Supply Power-Up Sequence		
		15-12			NVR IC-TROSA Control	Reserved	Reserved	0

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		11-8			NVR IC-TROSA Control	Reserved	Reserved	0
		7-4			NVR IC-TROSA Control	Reserved	Reserved	0
		3-0			NVR IC-TROSA Control	Reserved	Reserved	0
		15-12			NVR IC-TROSA Control	Reserved	Reserved	0
		11-8			NVR IC-TROSA Control	Reserved	Reserved	0
		7-4	RO	R	NVR IC-TROSA Control	Secondary Supply Power-Up Sequence #6	0000: Sequence not used 0001: Secondary Power Supply P1 0010: Secondary Power Supply P2 0011: Secondary Power Supply P3 0100: Secondary Power Supply P4 0101: Secondary Power Supply P5 0110: Secondary Power Supply P6 0111-1111 reserved for future use	0
		3-0	RO	R	NVR IC-TROSA Control	Secondary Supply Power-Up Sequence #5		0
		15-12	RO	R	NVR IC-TROSA Control	Secondary Supply Power-Up Sequence #4		0
		11-8	RO	R	NVR IC-TROSA Control	Secondary Supply Power-Up Sequence #3		0
		7-4	RO	R	NVR IC-TROSA Control	Secondary Supply Power-Up Sequence #2		0
		3-0	RO	R	NVR IC-TROSA Control	Secondary Supply Power-Up Sequence #1		0
C02A	3			R	NVR IC-TROSA Control	Secondary Power Supply Power-Down Sequence		
		15-12			NVR IC-TROSA Control	Reserved	Reserved	0
		11-8			NVR IC-TROSA Control	Reserved	Reserved	0
		7-4			NVR IC-TROSA Control	Reserved	Reserved	0
		3-0			NVR IC-TROSA Control	Reserved	Reserved	0
		15-12			NVR IC-TROSA Control	Reserved	Reserved	0
		11-8			NVR IC-TROSA Control	Reserved	Reserved	0
		7-4	RO	R	NVR IC-TROSA Control	Secondary Supply Power-Down Sequence #6	0000: Sequence not used 0001: Secondary	0

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
		3-0	RO	R	NVR IC-TROSA Control	Secondary Supply Power-Down Sequence #5	Power Supply P1 0010: Secondary Power Supply P2 0011: Secondary Power Supply P3 0100: Secondary Power Supply P4 0101: Secondary Power Supply P5 0110: Secondary Power Supply P6 0111-1111 reserved for future use	0
		15-12	RO	R	NVR IC-TROSA Control	Secondary Supply Power-Down Sequence #4		0
		11-8	RO	R	NVR IC-TROSA Control	Secondary Supply Power-Down Sequence #3		0
		7-4	RO	R	NVR IC-TROSA Control	Secondary Supply Power-Down Sequence #2		0
		3-0	RO	R	NVR IC-TROSA Control	Secondary Supply Power-Down Sequence #1		0
C02D	1			R	NVR IC-TROSA Control	Two-Wire-Interface Configuration		
		15-3			NVR IC-TROSA Control	Two-Wire-Interface Reserved	Reserved	0
		2-0	RO	R	NVR IC-TROSA Control	Two-Wire-Interface Maximum Supported Clock Frequency	000: ≤ 100KHz (Default rate) 001: ≤ 400KHz 010: ≤ 1MHz 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved	000b
C02E	1			O	NVR IC-TROSA Control	External PM Interval Sync Control	Note: Refer to register B00Bh for other functions related to PM Interval control	
		15	RW	O	NVR IC-TROSA Control	External Soft PM Interval Sync Host writes "1" to indicate Latch data request. IC-TROSA clears to "0" when PM data latch is completed.	1: Latch data Request 0: Latch Complete	
		14-0	RW	O	NVR IC-TROSA Control	Tick Source Selection	0: Soft Tick 1: Hardware Tick (Note: Hardware Tick is a Vendor Specific hardware pin which may be assigned to the External Soft PM	

IC-TROSA Addressing								
Hex Address	Size	Bit	Access Type	Required/ Optional	IC-TROSA Register Group	IC-TROSA Register Name Bit Field Name	IC-TROSA Description	Init Val/ LSB Unit
							Interval Sync bit C02E.15)	
C02F	1			R	NVR IC-TROSA Control	Laser Grid Capabilities	MSB stored at low address. LSB stored at high address. See B400.13-15 for current Laser Grid Set point	
		15	RO	R	NVR IC-TROSA Control	3.125 GHz Grid Spacing	1 = Supported, 0 = Not Supported	0
		14	RO	R	NVR IC-TROSA Control	6.25 GHz Grid Spacing	1 = Supported, 0 = Not Supported	0
		13	RO	R	NVR IC-TROSA Control	12.5 GHz Grid Spacing	1 = Supported, 0 = Not Supported	0
		12	RO	R	NVR IC-TROSA Control	25 GHz Grid Spacing	1 = Supported, 0 = Not Supported	0
		11	RO	R	NVR IC-TROSA Control	33 GHz Grid Spacing	1 = Supported, 0 = Not Supported	0
		10	RO	R	NVR IC-TROSA Control	50 GHz Grid Spacing	1 = Supported, 0 = Not Supported	0
		9	RO	R	NVR IC-TROSA Control	75 GHz Grid Spacing	1 = Supported, 0 = Not Supported	0
		8	RO	R	NVR IC-TROSA Control	100 GHz Grid Spacing	1 = Supported, 0 = Not Supported	0
		7-0	RO		NVR IC-TROSA Control	Reserved	Reserved for future Grid Spacing options	0

12. References

12.1.1. Normative references

ANSI/TIA-598-D-2014

ITU-T Recommendation G.657.B3

ITU-T Recommendation G.652.D

NXP I2C Bus Specification and User Manual Rev-6

SFF-8636 Revision 2.9

CFP-MSA-Management Interface Specification 2.6 r06a

OIF-CFP2-ACO-01.0

JEDEC specification JESD8C.01 revision September 2007

12.1.2. Informative references

IPC/JEDEC J-STD-020E

IPC/JEDEC J-STD-033C

13. Appendix A: Glossary

ADC	Analog to Digital Converter
AGC	Automatic Gain Control
ASIC	Application Specific Integrated Circuit
BS	Beam Splitter
BGA	Ball Grid Array
CMRR	Common Mode Rejection Ratio
DPC	Dual Polarization Coherent [legacy IA name]
DSP	Digital Signal Processor
Gbaud	10^9 Symbols per second
IA	Implementation Agreement
ICR	Intradyne Coherent Receiver
LGA	Land Grid Array
LO	Local Oscillator
MPD	Monitor Photodiode
MSA	Multi-Source Agreement
NVR	Non-Volatile Register
OIF	Optical Internetworking Forum
PD	Photodiode
PI	Peak Indicator
PID	Proportional Integral Derivative
PM	Polarization Maintaining
PMF	Polarization Maintaining Fiber
PBS	Polarization Beam Splitter
PCB	Printed Circuit Board
PM	Performance Monitor
PM-QPSK	Polarization Multiplexed Quadrature Phase Shift Keying
SMT	Surface Mount Technology
SPI	Serial Port Interface
S_{21}	Scattering Parameter for two port network, forward gain (loss) input to output
S_{11}	Scattering Parameter for two port network, reflected loss at electrical input
S_{22}	Scattering Parameter for two port network, reflected loss at electrical output
TEC	Thermo-Electric Cooler
TIA	Trans-Impedance Amplifier
THD	Total Harmonic Distortion
TWI	Two-Wire Interface
VOA	Variable Optical Attenuator
VR	Volatile Register

14. Appendix B: Additional Electro-Optical Characteristics (Informative)

Parameter	Unit	Min	Typ	Max	Note
Gain control bandwidth	MHz		5		1
Total harmonic distortion (THD)	%	For further study			
RX MPD responsivity	A/W		0.05		2
RX MPD to LO input optical isolation	dB		45		2

Table 14-1 Additional electro-optical characteristics (informative).

Notes:

1. Measured by applying step at gain control node such that output changes 5%. BW is estimated by 0.22/Tr where Tr is the 20-80% rise/fall time of the output envelope step.
2. Optional feature.

15. Appendix C: Open issues / current work items

There are no open issues or current work items at the time of this document's publication.

16. Appendix D: List of companies belonging to OIF when document is approved

Acacia Communications
ADVA Optical Networking
Alibaba
Alphawave IP Inc.
Amphenol Corp.
AnalogX Inc.
Applied Optoelectronics, Inc.
Arista Networks
BizLink Technology Inc.
Broadcom Inc.
Cadence Design Systems
China information and communication technology Group Corporation
China Telecom Global Limited
Ciena Corporation
Cisco Systems
Corning
Credo Semiconductor (HK) LTD
Dell, Inc.
EFFECT Photonics B.V.
Elenion Technologies, LLC
Epson Electronics America, Inc.
eSilicon Corporation
Finisar Corporation
Foxconn Interconnect Technology, Ltd.
Fujikura
Fujitsu
Furukawa Electric Japan

Global Foundries
Google
Hewlett Packard Enterprise (HPE)
IBM Corporation
Idea Sistemas Electronicos S.A.
Infinera
Innovium
Inphi
Integrated Device Technology
Intel
IPG Photonics Corporation
Juniper Networks
Kandou Bus
KDDI Research, Inc.
Keysight Technologies, Inc.
Lumentum
MACOM Technology Solutions
Marvell Semiconductor, Inc.
Maxim Integrated Inc.
MaxLinear Inc.
MediaTek
Mellanox Technologies
Microsemi Inc.
Microsoft Corporation
Mitsubishi Electric Corporation
Molex
Multilane SAL Offshore
NEC Corporation
NeoPhotonics
Nokia
NTT Corporation
O-Net Communications (HK) Limited
Open Silicon Inc.
Optomind Inc.
Orange
PETRA
Precise-ITC, Inc.
Rambus Inc.
Rianta Solutions, Inc.
Rockley Photonics
Rosenberger Hochfrequenztechnik GmbH & Co. KG
Samtec Inc.
Semtech Canada Corporation
SiFotonics Technologies Co., Ltd.
Socionext Inc.
Spirent Communications
Sumitomo Electric Industries, Ltd.
Sumitomo Osaka Cement
Synopsys, Inc.
TE Connectivity
Tektronix
Telefonica SA
TELUS Communications, Inc.
UNH InterOperability Laboratory (UNH-IOL)

Verizon
Viavi Solutions Deutschland GmbH
Xelic
Xilinx
Yamaichi Electronics Ltd.
ZTE Corporation