

OIF 448Gbps Signaling for AI Workshop April 15-16, 2025

448G Technology:

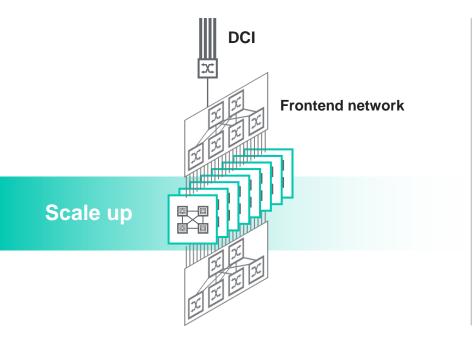
Powering next-gen scale-up and scale-out connectivity

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VP & CTO, Platform Connectivity, Marvell April 15, 2025



Scale-up interconnect

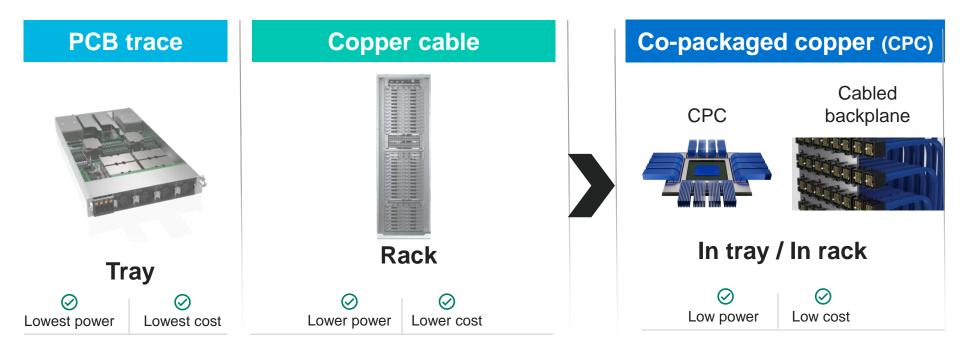


- Multiple XPUs appearing as one
- Extremely low latency and high bandwidth
- Full capacity available to a single task
- Powered by copper connectivity today

Today's scale up is typically: < 500 XPUs

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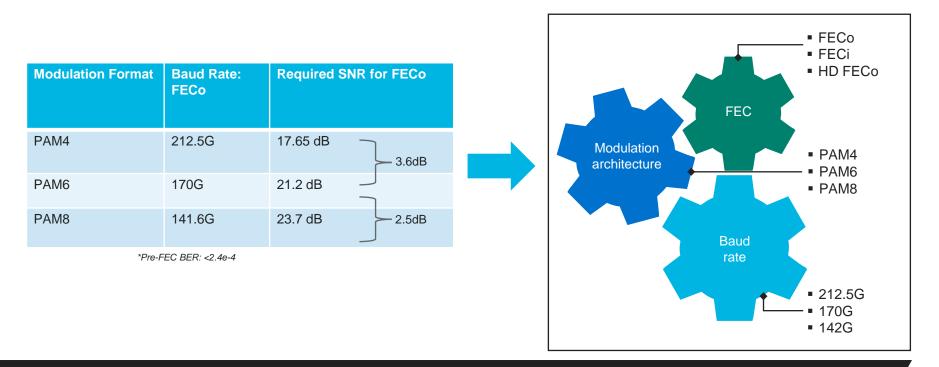
Scale-up interconnect Evolution



CPC: paving the way to extend copper reach for 448G

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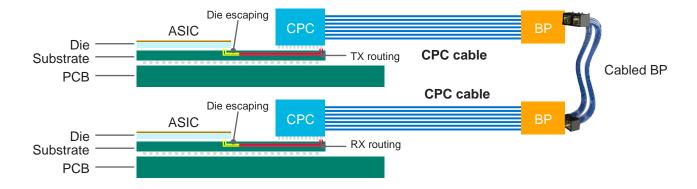
Path towards 448G Copper : PAM-n Modulation



Advanced Equalizer, Higher order Modulation with FEC are the tools to enable 448G

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CPC (copper channel) for 448G scale-up connectivity

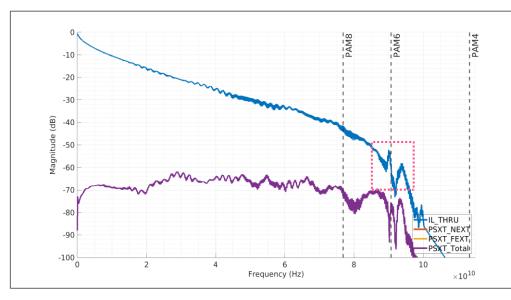


Modulation	Baud rate	Required SNR	Target reach	Insertion loss	Additional note	
PAM4	212.5G	17.65 dB	>1m cabled backplane	>80 dB	Not feasible	
PAM6	170G	21.2 dB	>1m cabled backplane	>50 dB	Optional FECi may be needed	
PAM8	141.6G	23.7 dB	>1m cabled backplane	>40 dB		

448G copper interconnect: PAM4 is a non-starter

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Example of 400G Copper Channel with 1m Copper Cable



*Courtesy - Meta

@ KP Rate

Modulation	Baud rate	IL @Nyquist	Xtalk @ Nyquist	ICR
PAM4	212.5G	Too lossy	NA	NA
PAM6	170G	52 dB	70dB	18 dB
PAM8	141.6G	40 dB	68 dB	28 dB

PAM4 – Loss is too high

• PAM6 – loss looks high as well & it is right on the cliff

• PAM6/PAM8 – ICR looks healthy but may be a bit optimistic

SNR Margin Analysis @ FECo rate

Simulation Criteria:

- Baud rate: FECo rate (KP rate) only
- SerDes Spec: FFE + RC + DFE + a*MLSD mode
- Case-1: Run at FECo rate with PAM6
- Case-2: Run at FECo rate with PAM8

PAM-n	SNR margin @ <u>FECo</u> rate	Simulated BER
PAM4	Not Applicable	NA
PAM6	~ 1dB	<5e-5
PAM8	~ 2.4 dB	<3e-6

Summary:

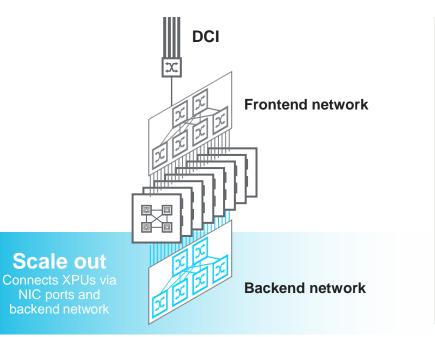
- For this particular channel : Both PAM6 & PAM8 can work but slight advantage to PAM8.
- Both the modulation scheme needs extra boost from additional coding gain from FEC

448G electrical I/O for scale-up interconnect

I/O	I/O Modulation		Power efficiency	
Electrical I/O	PAM8 or PAM6 with optional FECi for Cu	CPC + 1.5m cabled backplane	< 4.25 pJ/bit	
	System technology in		Application: Cabled backplane	
	 Co-packaged c 	opper I/O	 E2E channels spanning 	
	 Reduces loss free extends reach 	rom package;	entire rackPushes boundaries of	
	 Supports 448G 		SerDes reach	

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Scale-Out interconnect

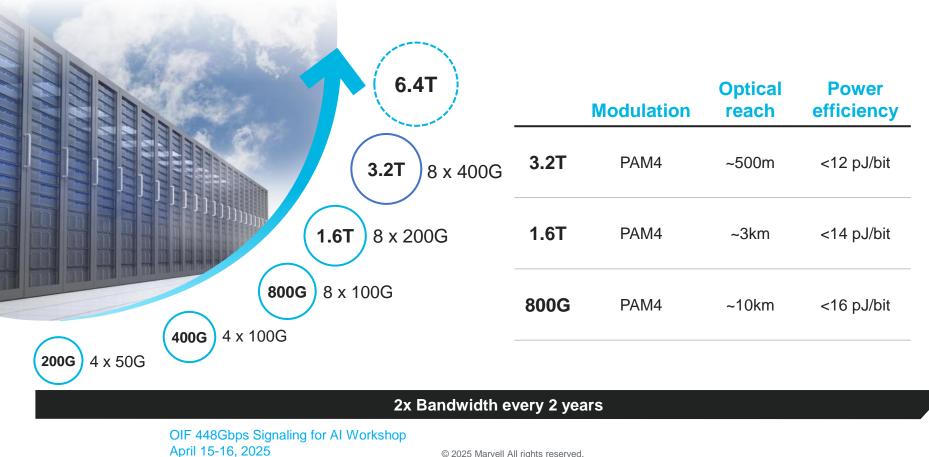


- Connects multiple AI clusters together
- Multi-row-scale interconnects
- Powered by optical connectivity
- Reliability and serviceability is a must
- 1.6T today → next-gen 3.2T

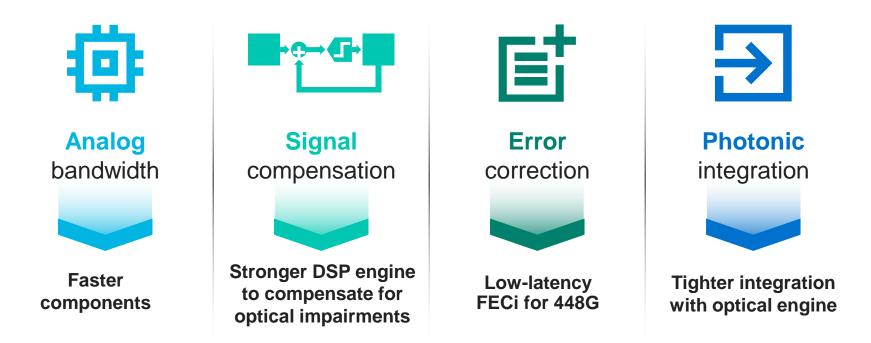
Scale out enables > 100K XPU clusters today

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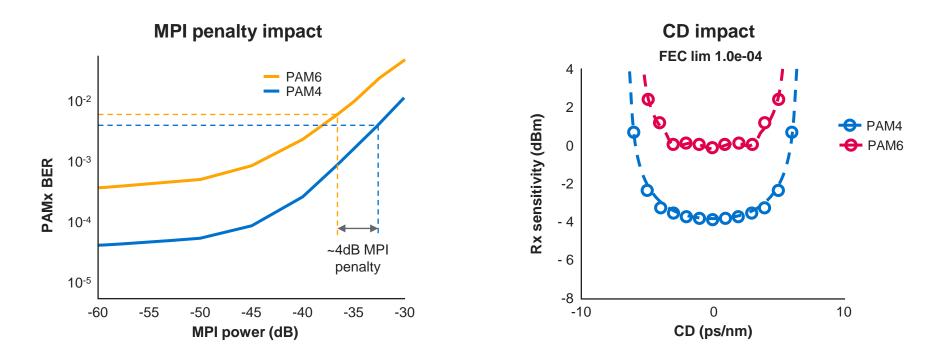
Scale-out interconnect evolution



Path towards 448G/Lambda and beyond



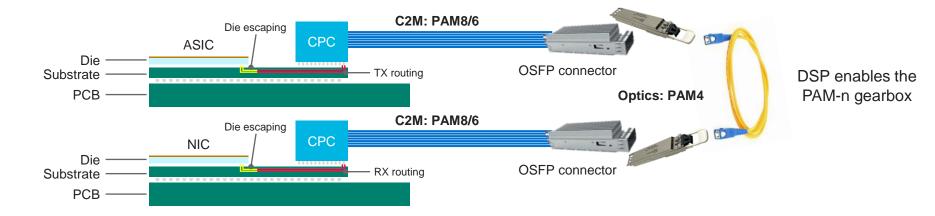
Optical Impairments: PAM4 Vs PAM6



PAM4 offers more resiliency to optical impairments vs. PAM6

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3.2T scale-out connectivity powered by DSP



448G	C2M	Optical	Notes
DSP	PAM8/6	PAM4	\oslash
LRO	PAM8/6	PAM4	\bigotimes
LPO	PAM8/6	PAM4	\bigotimes

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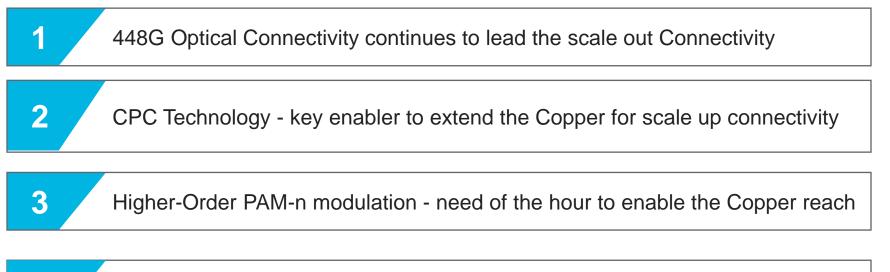
NextGen 448G PAM4 Optical is already here

Real **Silicon** Data – Marvell's 448G Optical TX Eye in OFC 2025



Key takeaways

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Augmenting the FECo with additional coding gain will boost the Link margin







Thank You



Essential technology, done right[™]