Overcoming Signal and Power Integrity Bottlenecks in Next-Generation 448G Interconnects

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- Kaisheng Hu is the Principal Engineer of Signal and Power Integrity at Ciena in Canada. He has over 25 years experience in hardware deign and testing. Before joining Ciena, he was employed at Nortel from 2000 to 2010.
- Research interests include the analysis of chip and package Signal and Power Integrity, power and noise analysis for ASICs, modeling of on-chip passive RF components, IC package design and modeling, as well as high-speed SerDes and PCB interconnects. He holds two U.S. patents and has published 13 papers.

For next-generation 448G electrical connections, both Signal Integrity (SI) and Power Integrity (PI) face significant challenges

Signal Integrity

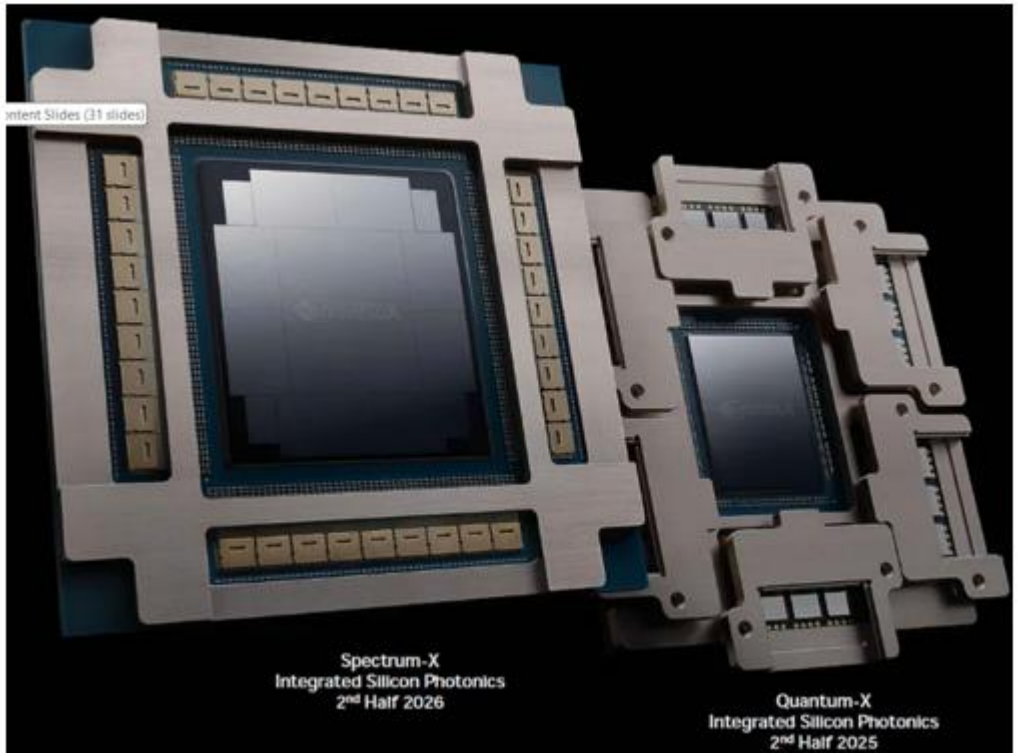
- Transition discontinuities at die-package, vias, flex and connectors
- Bump pitch and escape routing
- Crosstalk and noise coupling in dense routing
- High-frequency loss & material selection at 100G range

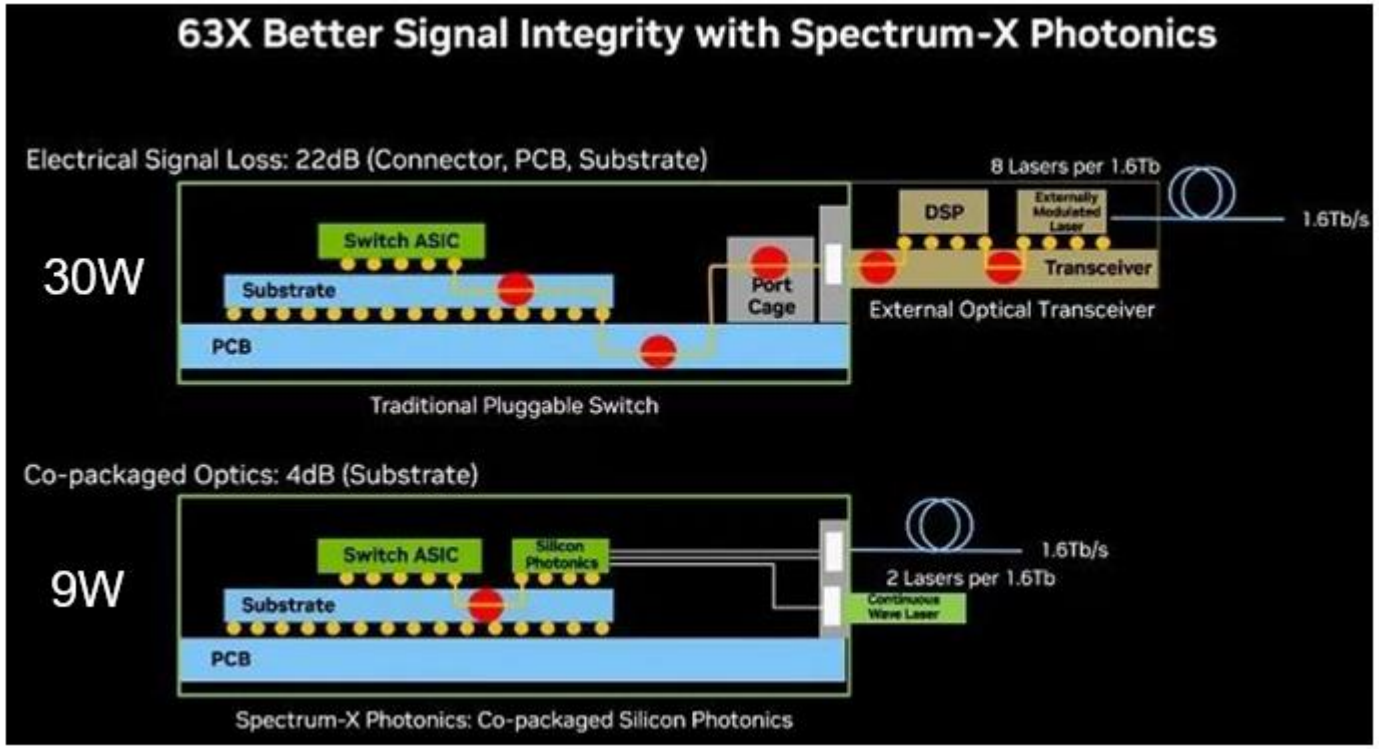
Power Integrity

- For next-generation SerDes design, the TX FFE and RX DFE / MLSE will require more power
- Power density and DvD (Dynamic Voltage Drop) challenges become even more critical due to the higher speed and integration level
- On-die PDN resonance at 10 GHz+ range
- Power Estimation and Efficiency Optimization
- Higher current transients with fast-switching circuits from DSP and equalization for PAM4, PAM6 and PAM8
- Package inductance and ground return path optimization

With the rapid advancement of AI and the soaring demand for bandwidth, greater emphasis is being placed on SI and PI

Die-to-Die interconnections will remain the primary SI bottleneck
Removing signal transitions could save 70% of power

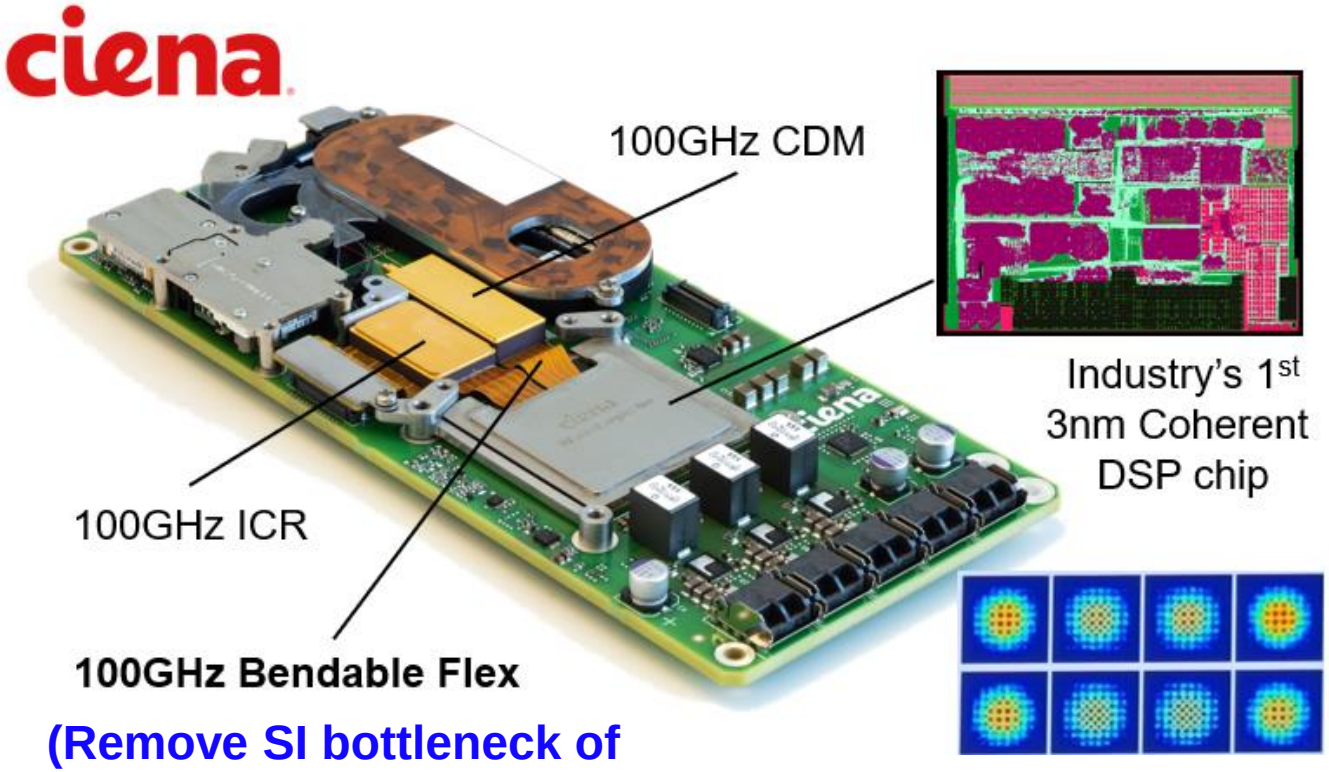




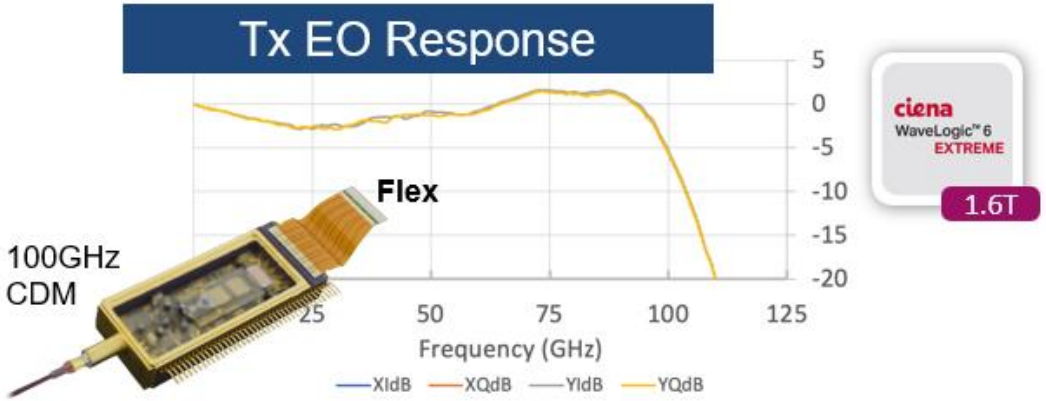
Nvidia Spectrum-X CPO: 63x Better (18 dB) Signal Integrity, 3.5x Higher Power Efficiency - GTC 2025

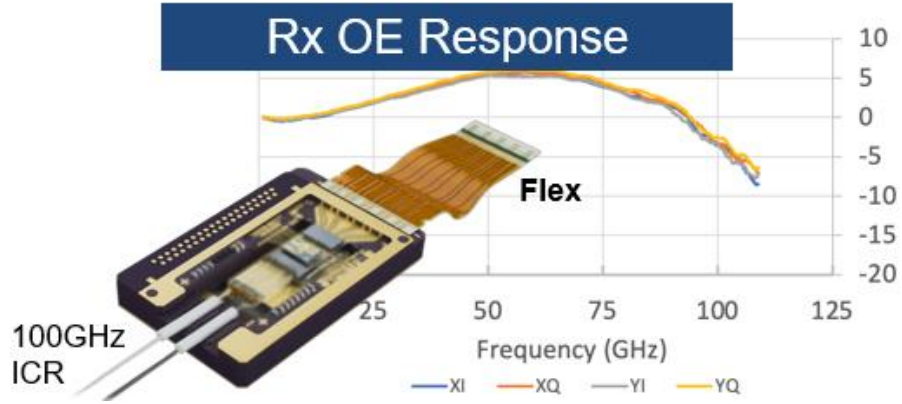
EO/OE, DSP chip and Flex interconnect transitions up to 100 GHz

- Ciena is a global leader in optical networking equipment. During the development of 1.6 T b/s WL6 Photonics products, single electrical channel achieved 100 GHz of analog bandwidth
- The Tx and Rx use Flex interfaces to minimize interconnect losses and crosstalk
- Die-to-package and flex-to-package transitions were carefully optimized using EM simulations



(Remove SI bottleneck of BGA transitions)





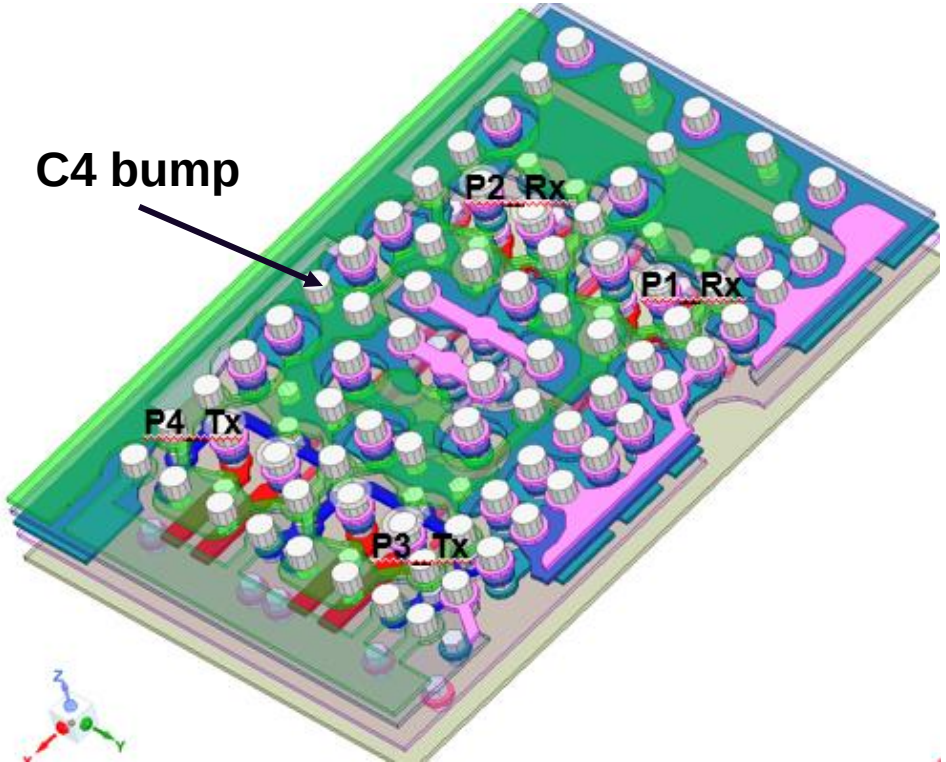
SI Challenges for a High-Density SerDes Bump Layout

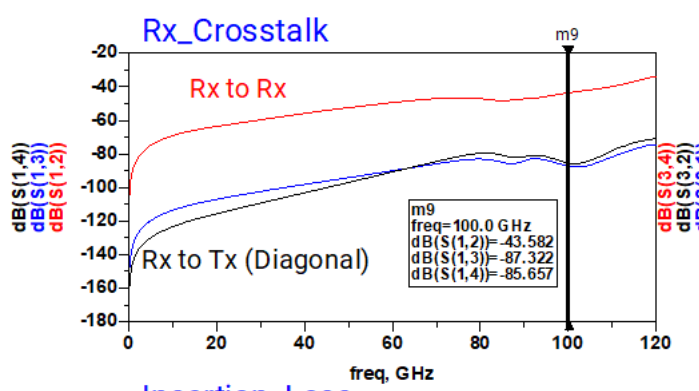
Cause

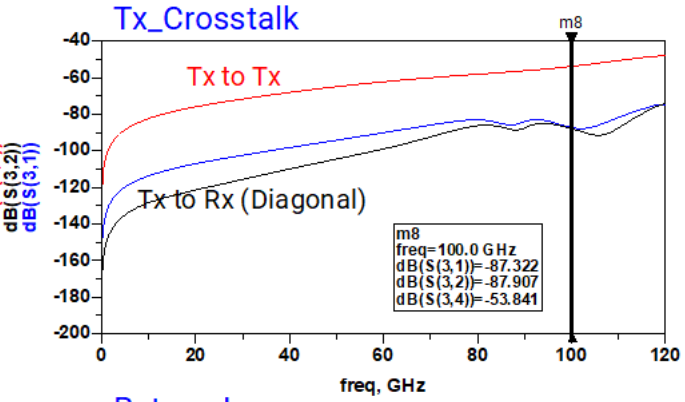
- Tx and Rx Routing on Different Layers
- missing ground stitching vias, high-order modes
- SI vs. PI trade-off
- Return path discontinuities
- Crosstalk from high-density routing
- Stub effects & reflections
- Mode conversion & common-mode noise
- High-frequency loss & material selection

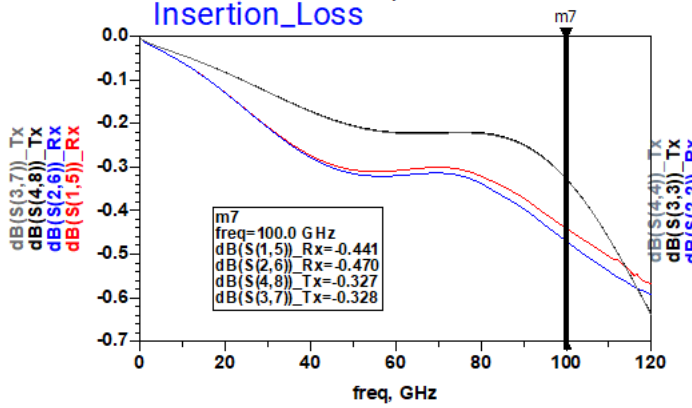
Effect

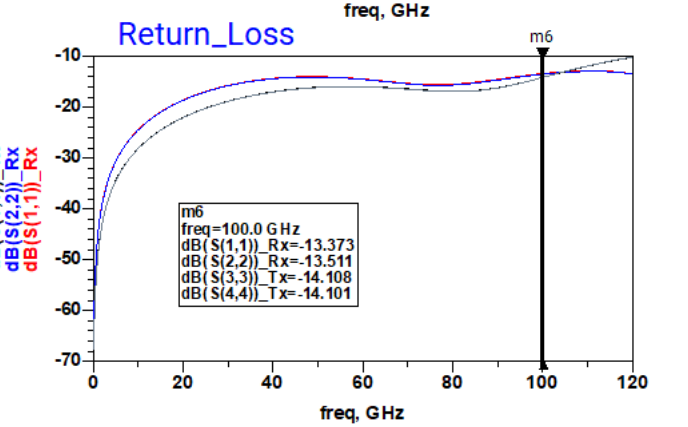
- Via discontinuities, skew
- High crosstalk, poor return path
- PDN noise coupling into signals
- Mode conversion, signal degradation
- Signal distortion
- Resonances, jitter increase
- EMI, signal degradation
- Reduced eye-opening







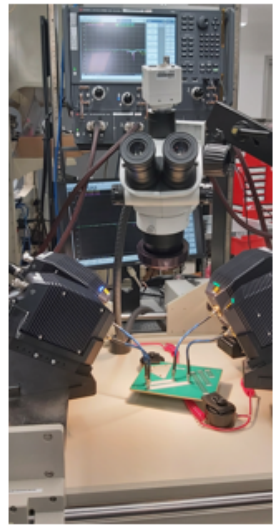


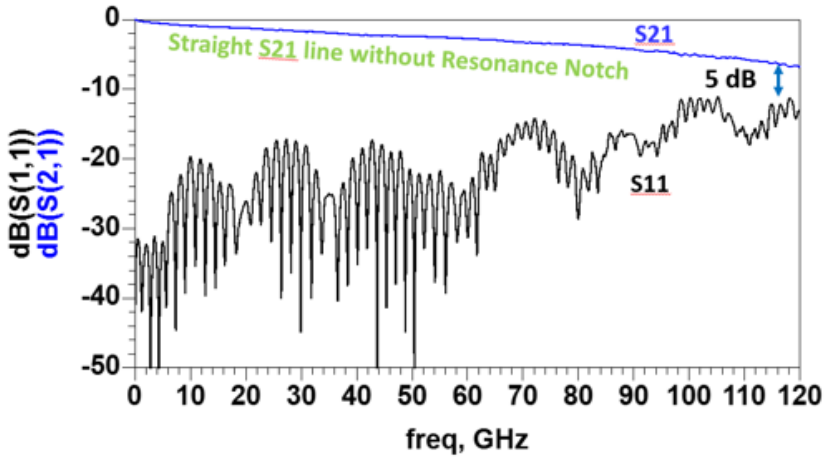


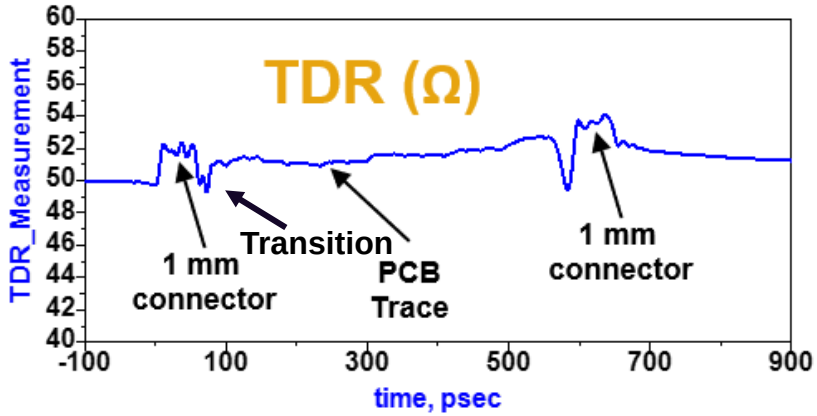
Connector-to-Board Transition up to 120 GHz

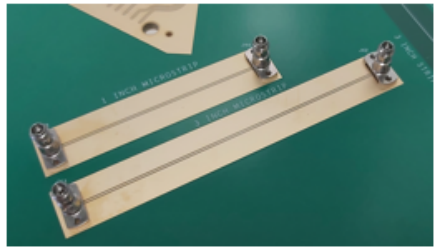
Test result for 1 mm connector – PCB – 1 mm connector

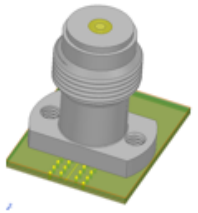
- Test Fixture for 2 X Thru de-embedding
- S21 is close to "linear straight line" up to 120 GHz without resonance notch
- IEEE P370 spec: at least -5 dB delta between S21 and S11 for class A spec
- The transition between 1 mm connector and PCB is crucial for ensuring accurate de-embedding, requiring careful design and HFSS EM optimization

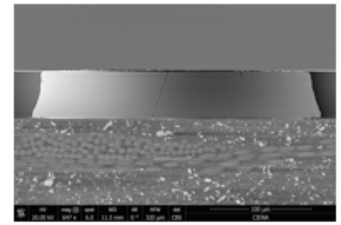












K. Hu, "PCB Parameter Extraction for Frequencies up to 120 GHz", IEEE International Symposium On Electromagnetic Compatibility Signal & Power Integrity, 2024

Material parameters from vendors and datasheets are not accurate for SI analysis

- Material parameters (Dk, Df and surface roughness) are key factors in SI simulations. Dk refers to the Relative Permittivity and Df represents the Loss Tangent.
- Dk values are extracted using traditional resonance methods (such as IPC 2.5.5.13), which differ from actual usage conditions. Surface roughness is often estimated based on factory experience. These parameters can easily change during fabrication and copper treatment at the factory.
- Simulations based on datasheet values often show significant discrepancies vs actual measurements

Datasheet

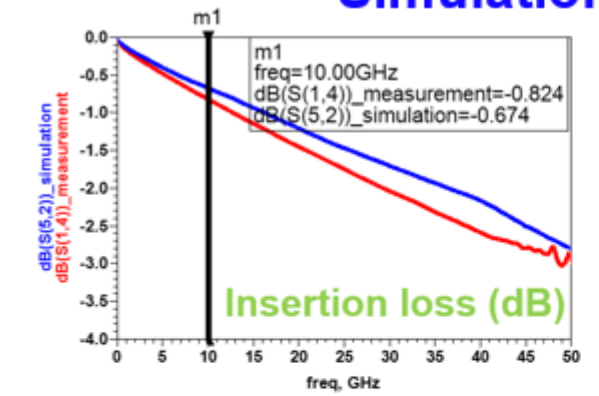
1GHz ; IPC TM650-2.5.5.9
6-50GHz ; Balanced-Type Circular Disk Resonance Method

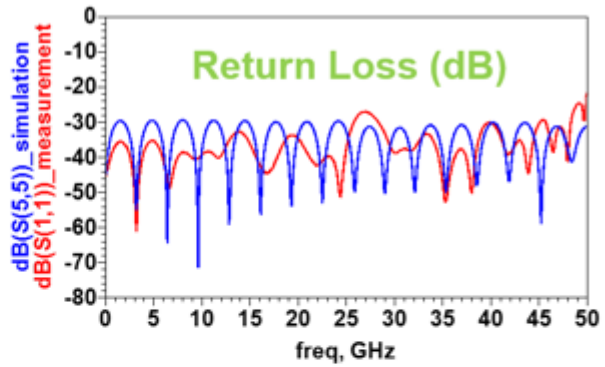
Core Type	Actual Thickness		Cloth Style	ply	Typical Resin Content (%)	Typical Dk									
	mil	mm				1GHz	6GHz	12GHz	18GHz	23GHz	29GHz	34GHz	40GHz	45GHz	50GHz
2	2.0	0.050	1035	1	65	3.46	3.39	3.38	3.37	3.37	3.37	3.37	3.37	3.37	3.37

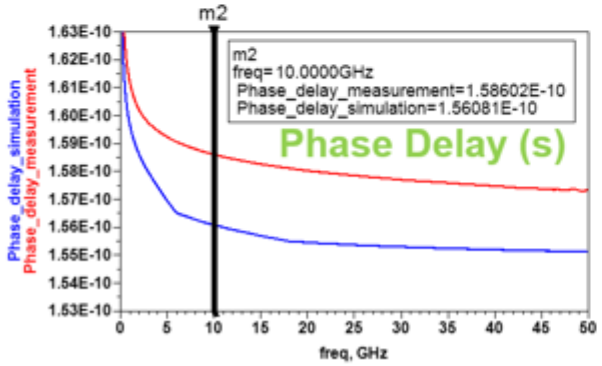
1GHz ; IPC TM650-2.5.5.9
6-50GHz ; Balanced-Type Circular Disk Resonance Method

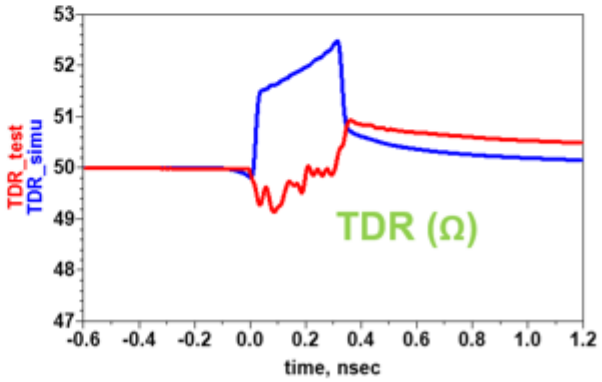
Core Type	Actual Thickness		Cloth Style	ply	Typical Resin Content (%)	Typical Df									
	mil	mm				1GHz	6GHz	12GHz	18GHz	23GHz	29GHz	34GHz	40GHz	45GHz	50GHz
2	2.0	0.050	1035	1	65	0.002	0.004	0.004	0.005	0.005	0.005	0.005	0.005	0.006	0.006

Simulation vs Measurement









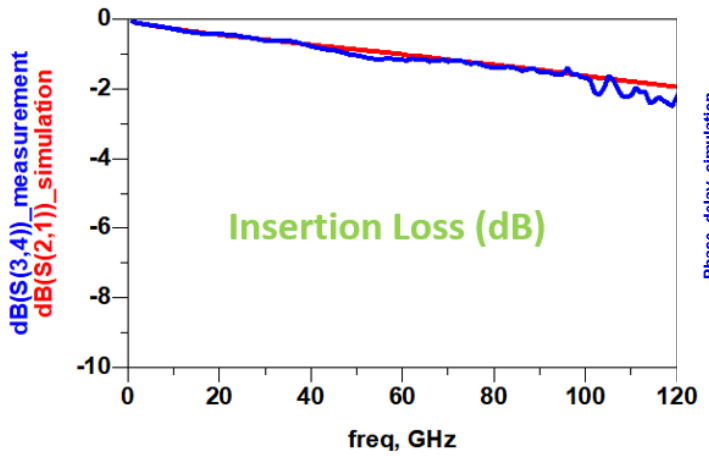
Material parameters can be extracted from lab measurements

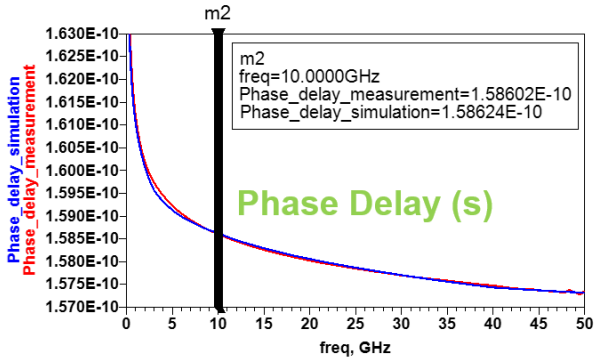
Simulation vs measurement

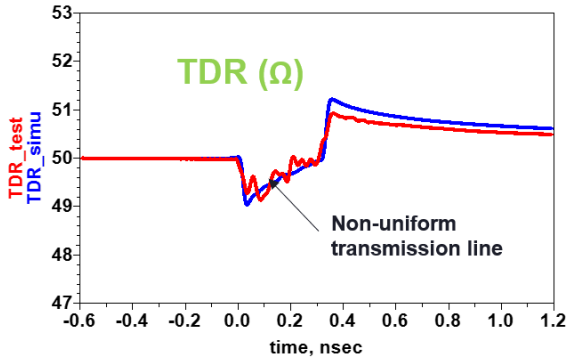
Good agreement with PCB parameters extracted up to 120 GHz

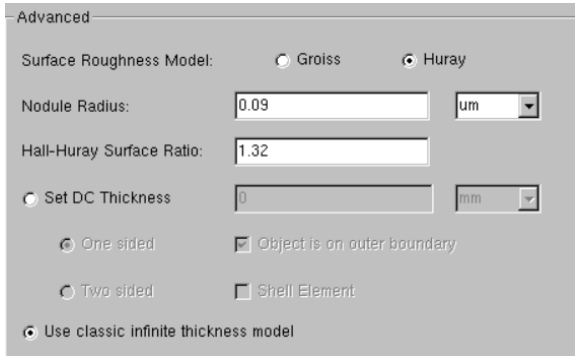
Extracted Dk and Df values

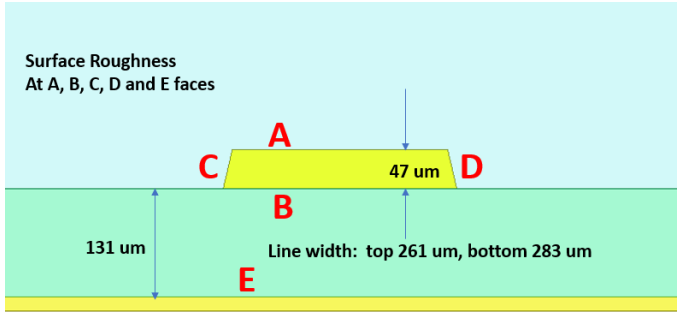
Freq. (GHz)	Dk	Df
1	2.95	0.0016
10	2.96	0.0016
14	2.96	0.0016
20	2.96	0.0018
30	2.96	0.0020
40	2.96	0.0023
50	2.96	0.0023
60	2.96	0.0023
70	2.96	0.0024
80	2.96	0.0024
90	2.97	0.0024
100	2.97	0.0025
110	2.98	0.0025
120	2.98	0.0025

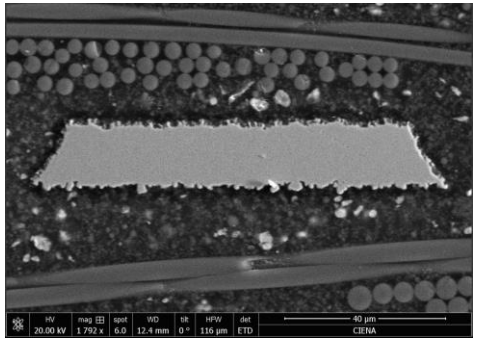








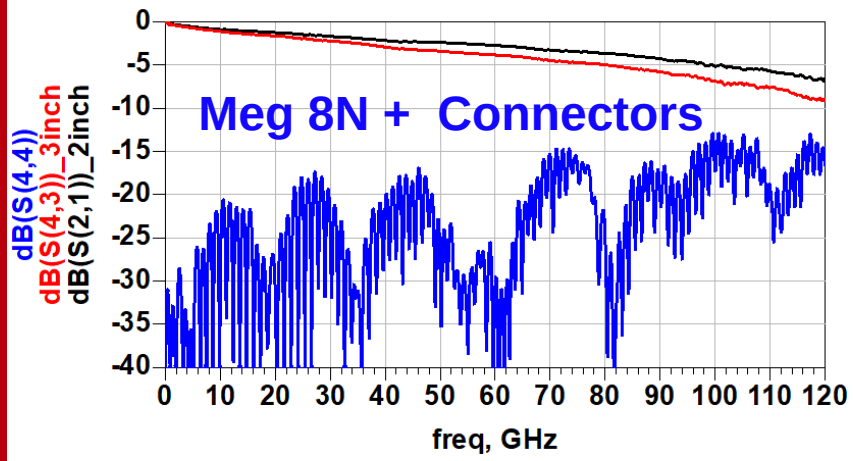


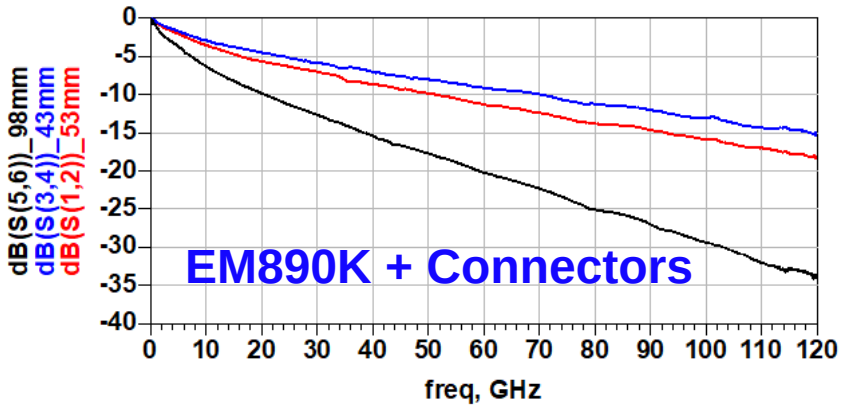


K. Hu, "PCB Parameter Extraction for Frequencies up to 120 GHz", IEEE International Symposium On Electromagnetic Compatibility Signal & Power Integrity, 2024
K. Hu, "Design and measurement for high-speed interconnects between chip package, connector and PCB board", IEEE EPEPS, 2019

Lab Measurement Results for Several Ultra-Low-Loss Materials and Copper Foils

- For Meg 8N & HVLP, 10mils line width, Microstrip IL is **2.2 dB / Inch** at **120 GHz**
- For EM890K & HVLP, 3 mils line width, stripline IL is **6.1 dB / Inch** at **120 GHz**
- For HVLP, Meg 8N is the best; TU933+ comes next; Meg 7 is the worst.
- For copper foil performance: ANP is the best; HVLP2 comes next; HVLP/VLP2/VLP are in the mid-range; RTF is the worst





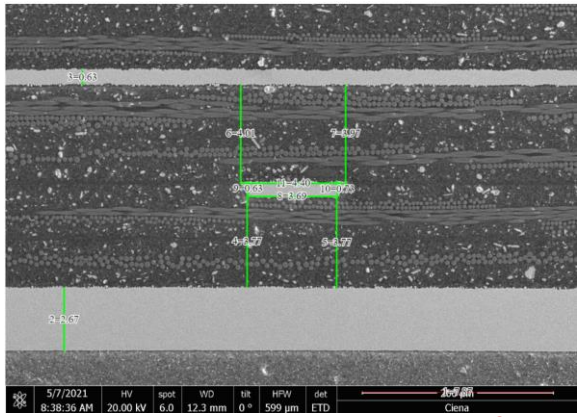
Differential

IL (dB/inch) at 14GHz

	HVLP	RTF	VLP	HVLP2	ANP
TU933+	0.776		0.702		
Meteorwave4000	0.797	0.891			
Tachyon100G	0.814	0.915			0.782
Megtron7	0.858	0.942		0.783	

IL (dB/inch) at 28GHz

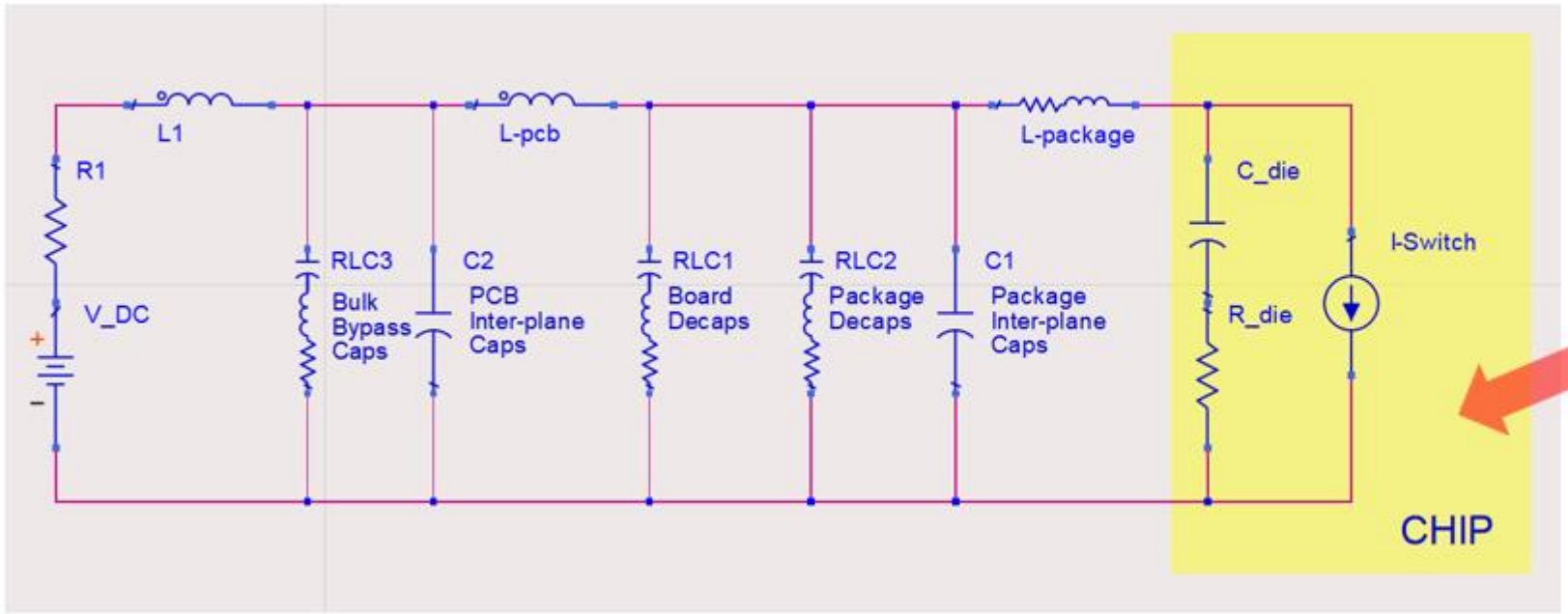
	HVLP	RTF	VLP	HVLP2	ANP
TU933+	1.287		1.224		
Meteorwave4000	1.377	1.485			
Tachyon100G	1.434	1.605			1.438
Megtron7	1.507	1.56		1.501	

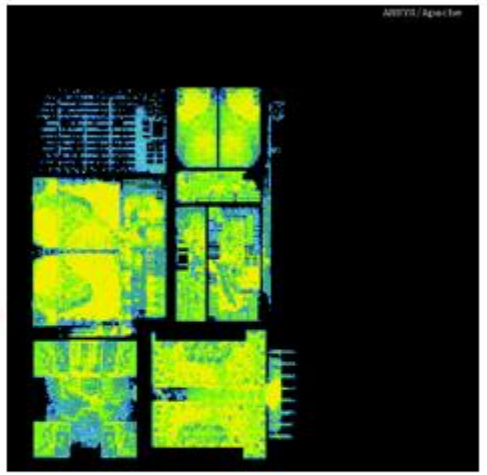


K. Hu, "Design and characterization of differential Signal Integrity interconnects at Millimeter-Wave PCB ", IEEE EMC SI & PI, 2020

PI Challenge: High Power Density and DvD

- The peak current on the die can exceed 200 Amps within a confined area of just a few square millimeters.
- The voltage noise margin decreases rapidly as supply voltage levels shrink across technology nodes (N7-> N5 -> N3 -> N2)
- Accurate chip sign-off for Dynamic Voltage Drop (DvD) requires higher precision
- Traditional Power Distribution Network (PDN) impedance analysis, which considers only the Voltage Regulator Module (VRM), PCB, and package, is insufficient. The chip's behavior must be a key factor in the analysis

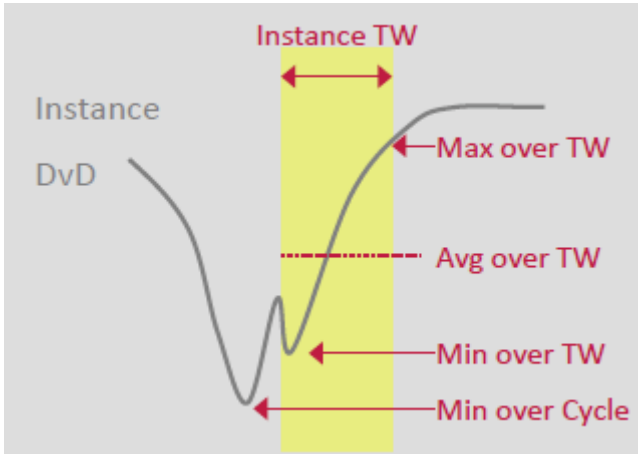




What is Dynamic Voltage Drop (DvD)?

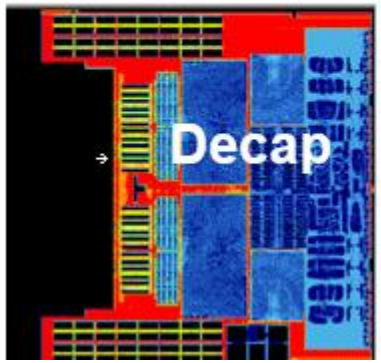
- It is a decrease in voltage that occurs in a chip when many transistors turn on and off at the simultaneously, drawing current from the power grid.
- This phenomenon can result in timing violation and functional failures of active components within chips
- It is primarily determined by two factors
  L-loop: the loop inductance of the PDN
  di/dt: the rate of change of current

$$V_{drop} = I*R + L*di/dt + 1/C * \int i(t)\,dt$$

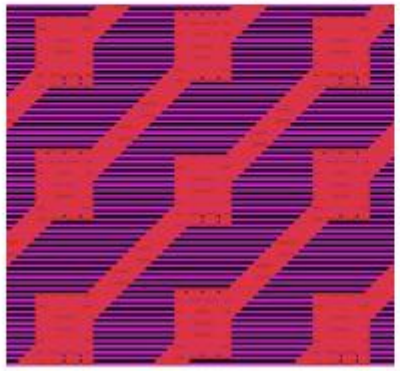


Methods to improve DvD performance:

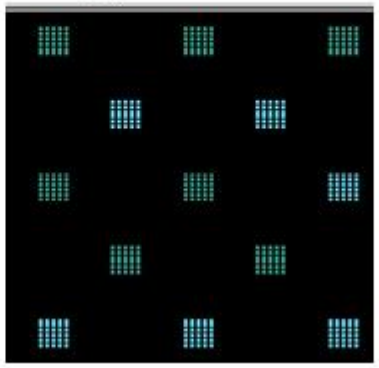
Increase C_die



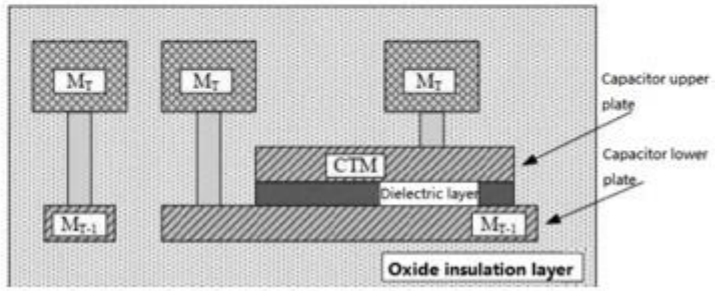
Metal strapping



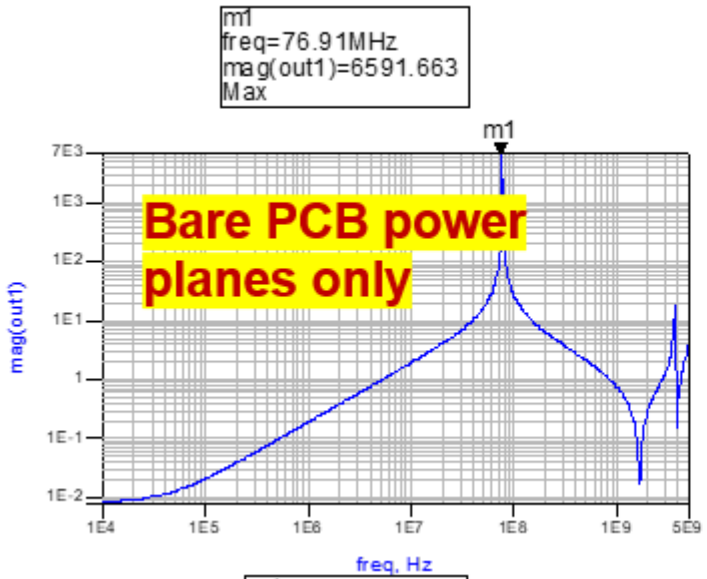
Big via stack

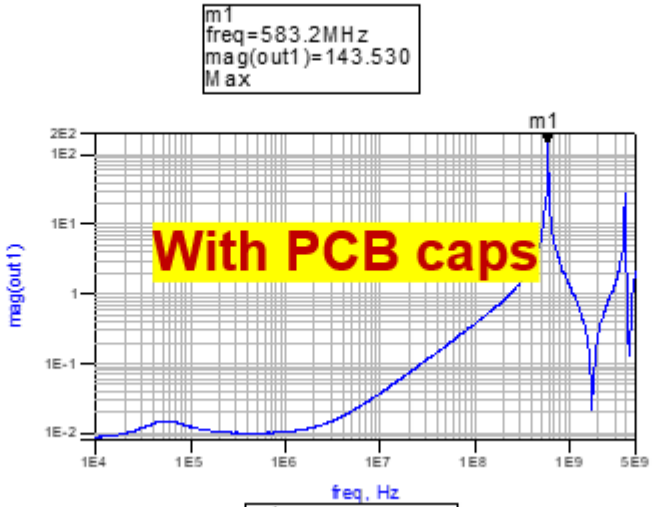


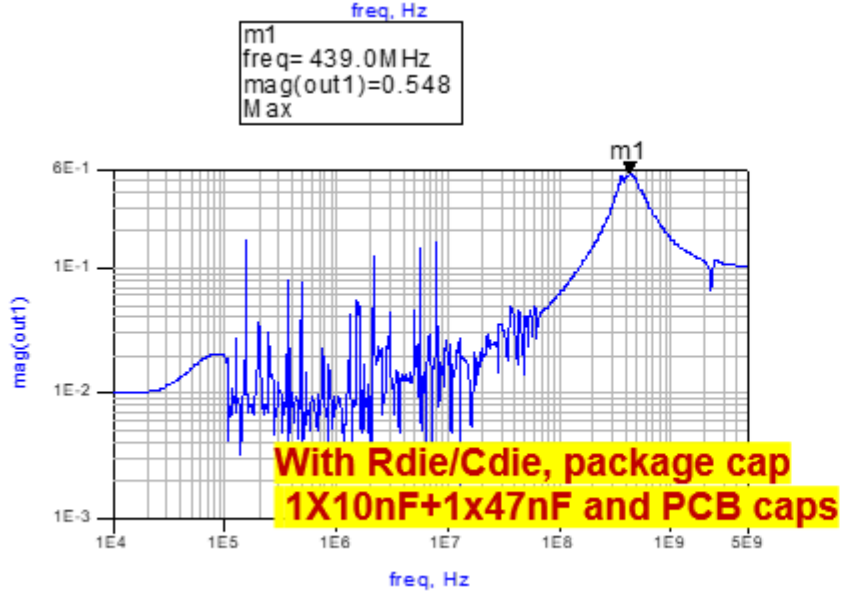
MIM capacitor
(Metal-Insulator-Metal)

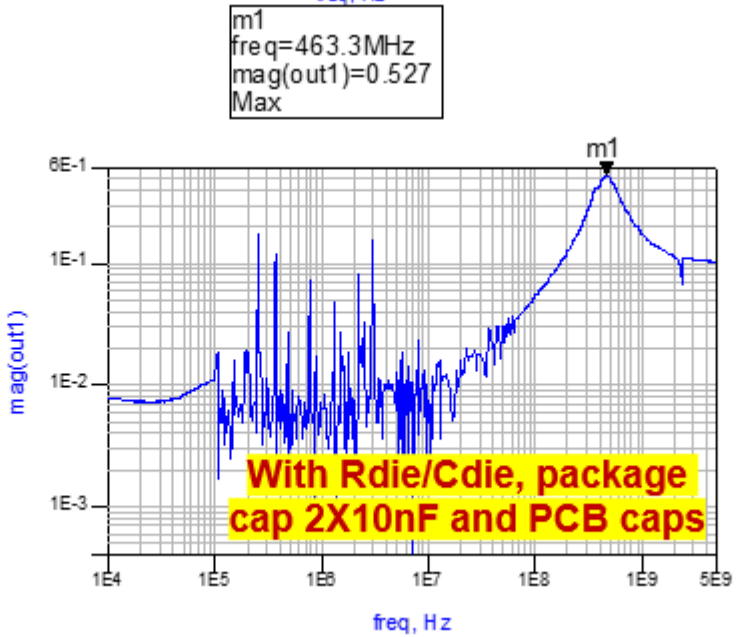


Impedance response (Ohms) with die, package and PCB at 5 GHz range









The resonance peak frequency and Q-factor are determined by the values of C_die, R_die, L_pkg and C_pkg

$$F = \frac{1}{2\pi\sqrt{LC}}$$

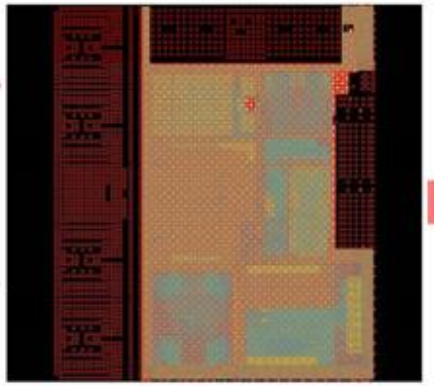
$$Q = \frac{\sqrt{(LC)}}{R}$$

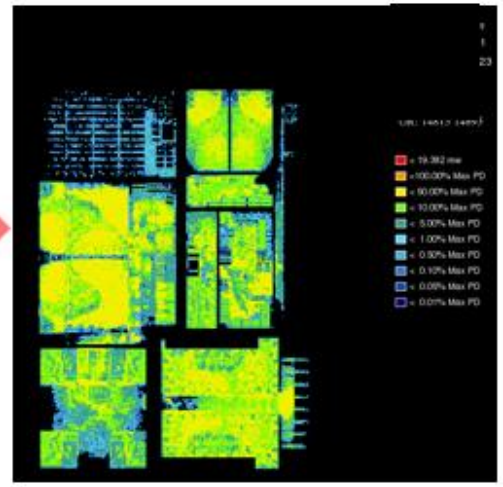
C_die and R_die are not fixed values; they vary with chip activity!

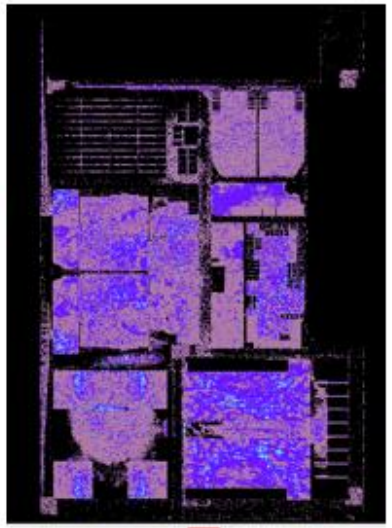
Design flow for performing chip power and IR drop analysis

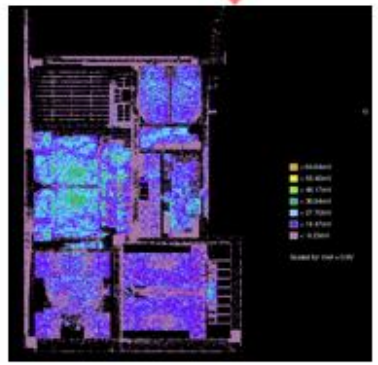
Library Data: LIB, LEF, GDS, APL and TECH files

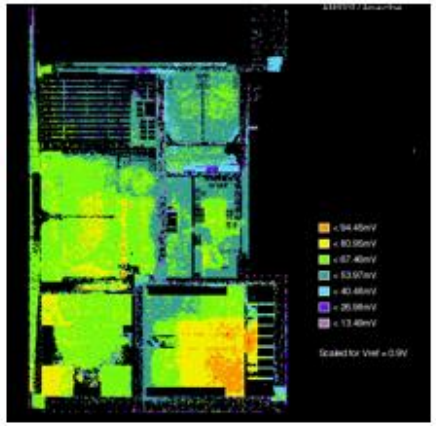
Design data: DEF, SPEF, STA, VCD, Package, Pad files











Simulation Challenge: Server Capacity!

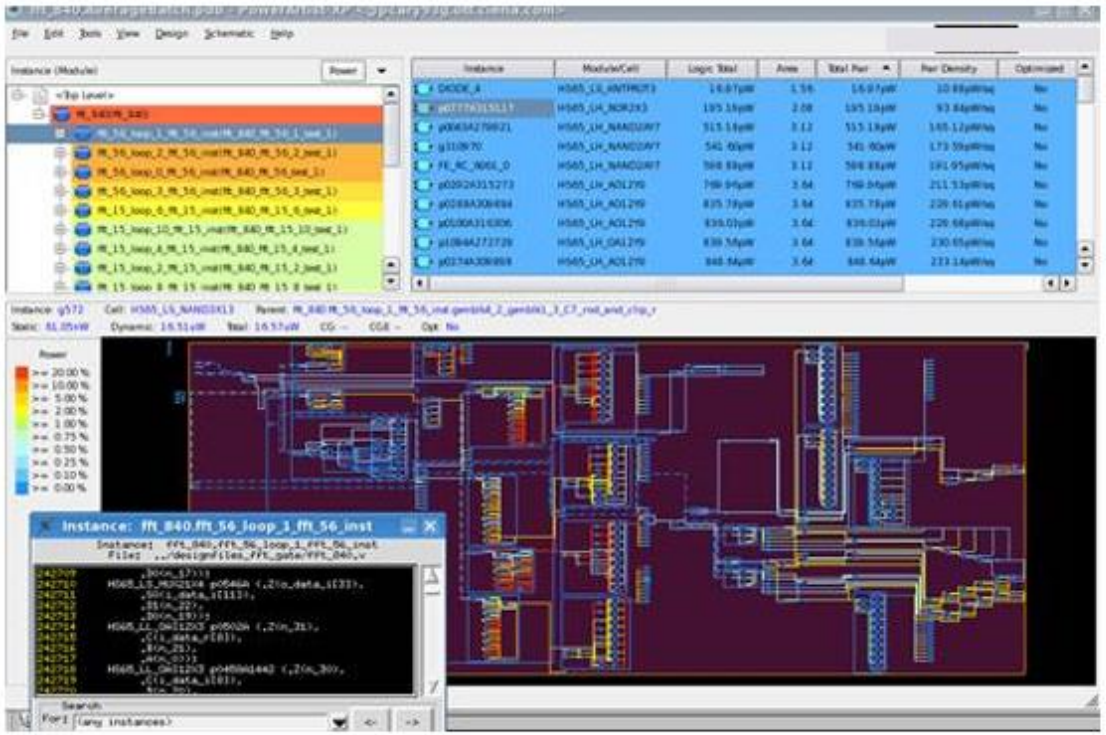
- Analyzing a medium-size 300-million-gate chip requires an LSF with 256 cores and 14 TB of RAM
- Demands 100x more server capacity than a typical HFSS simulation

Sign Off

K. Hu, "Simulation and Measurement for Improving Power Integrity in Chip, Package, and PCB System ", IEEE EMC SI&PI, 2023

Power Estimation and Efficiency Optimization in SerDes Chips

- With the Verilog RTL file, spef file, post CTS and Gate netlist, RTL level VCD and Gate level VCD
- Power Gating, clock gating, Dynamic Voltage and Frequency Scaling (DVFS), On-Die Voltage Regulator (LDO)



1. Total power consumption

Power contribution				Power(Watts) Static	Dynamic	Total
Internal power						
Internal register power	79.7mW	641mW	721mW			
Internal latch power	0W	0W	0W			
Internal memory power	0W	0W	0W			
Other internal power	325mW	1.14 W	1.46 W			
Total internal power				404mW	1.78 W	2.19 W
IP Core power				0W	0W	0W
Pad power				0W	0W	0W
Clock power				25.3mW	382mW	407mW
Internal load power				0W	1.73 W	1.73 W
Total power				430mW	3.9 W	4.33 W

$$P(total) = P(Leakage) + \tfrac{1}{2} * (Internal\text{-}energy * Freq * TR) + \tfrac{1}{2} * C * V^2 * Freq * TR$$

From .lib library file

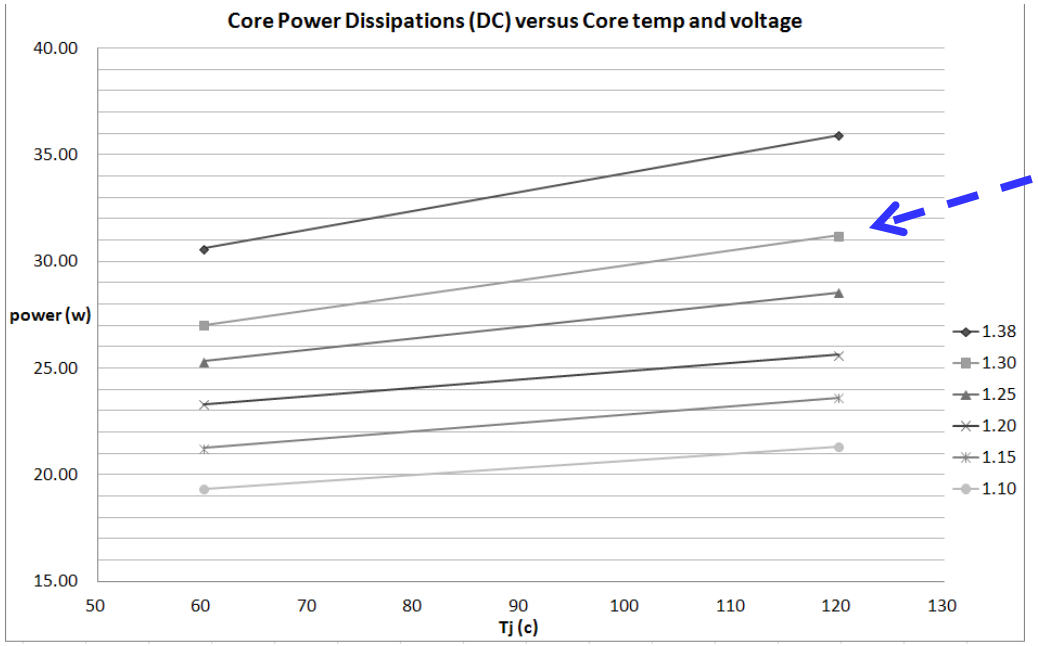
From timing file

From RC-Spef file Extracted

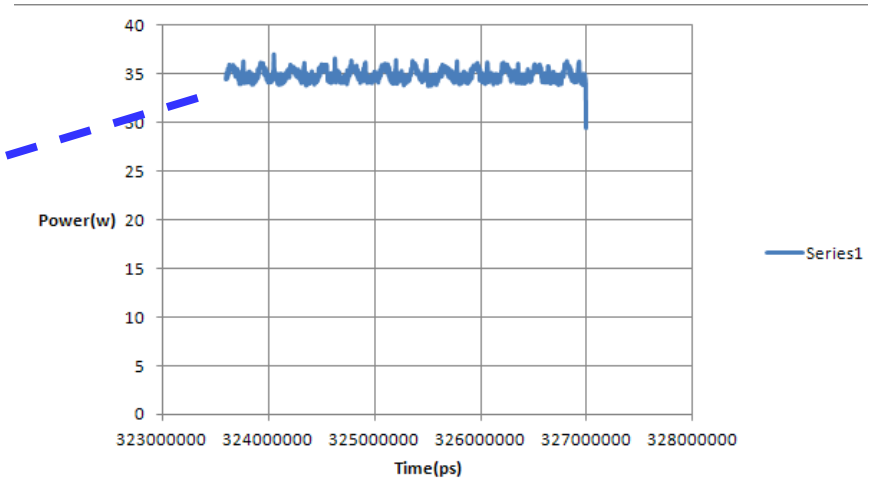
Toggle rate, from VCD/fsdb file

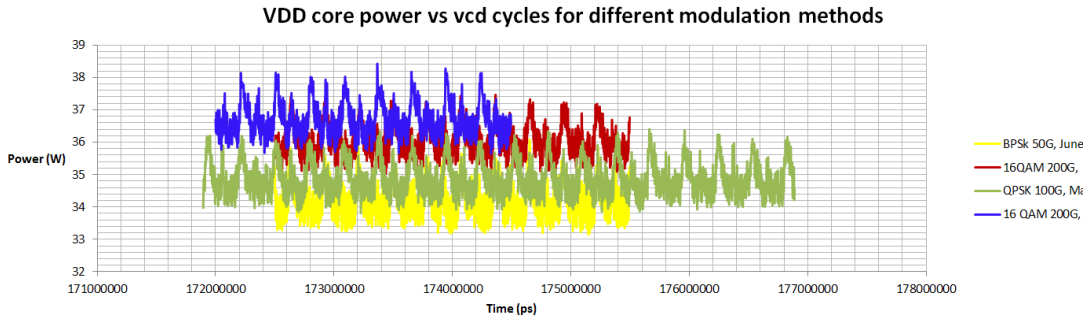
Comparison of Measured and Simulated Chip Power Consumption

Measurement: 31.2 W
At nom, 120C and RC_typ



Simulation: 34.9 W with gate level VCD
At nom, 125C and RC_max corner

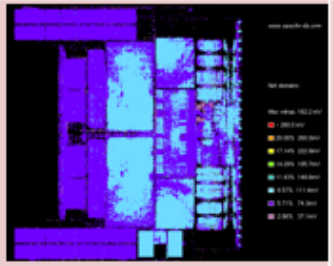
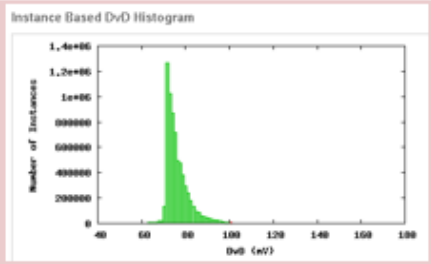
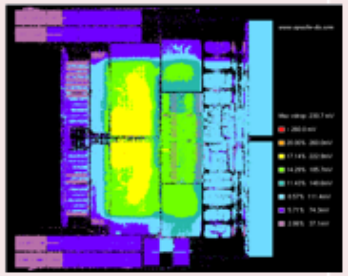
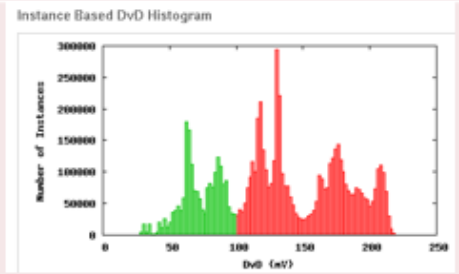
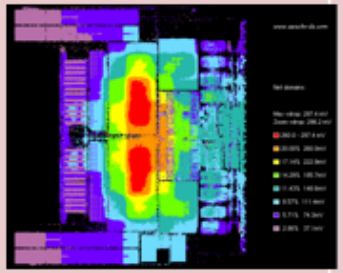
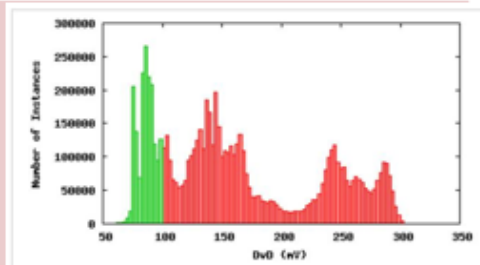




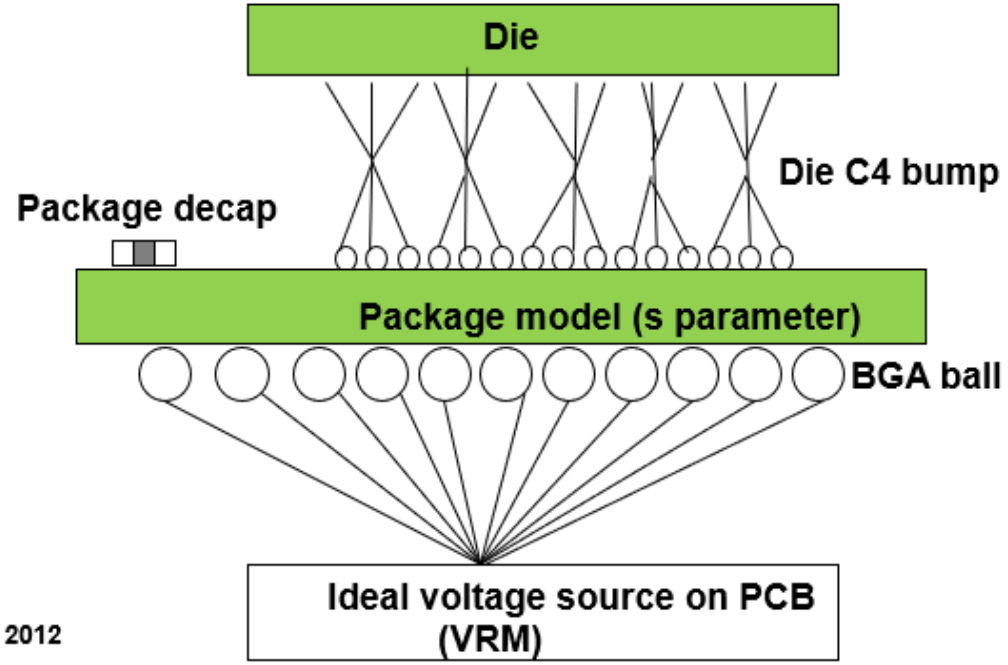
The discrepancy between the measurement and simulation is 3.7 W (10.6%).
This difference can be attributed to two unknown factors;

- The process corners differ: RC_max for simulation and RC_typ in the lab
- The simulation's stimulus, which represents true signal flow is higher than the test pattern used in the lab

Simulation results for die + package with different groupings

	DvD Contour	DVD histogram (Instance based)
Package model has 1x1 grouping		
Package model has 5x5 grouping		
Package model has 10x11 grouping		

- The DvD value is influenced by the current distribution at the package-die interface
- Due to the simulation server's capability limitations, the ports for the package model are divided into several groups (1x1, 5x5 and 10x10) at the die C4 bump side.
- Increasing the number of groups in the package model improves the accuracy of the DvD result

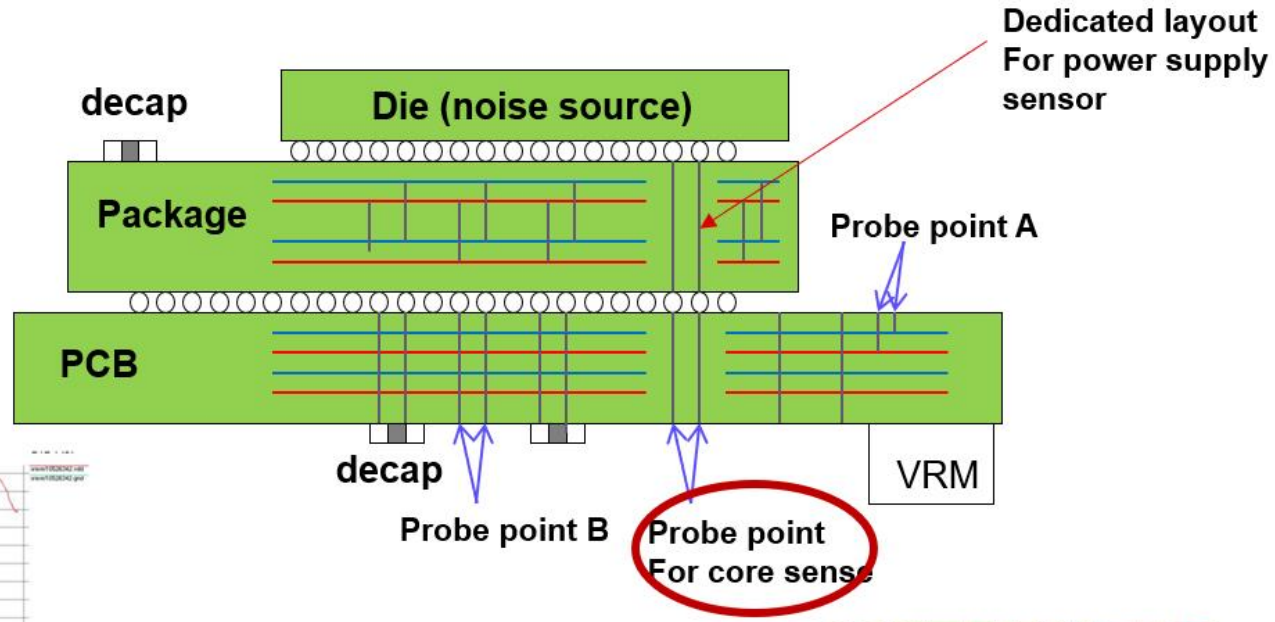


K. Hu, "Power Noise Analysis with Silicon Correlation Results for Complex 32 nm ASIC Designs ",49th DAC, 2012

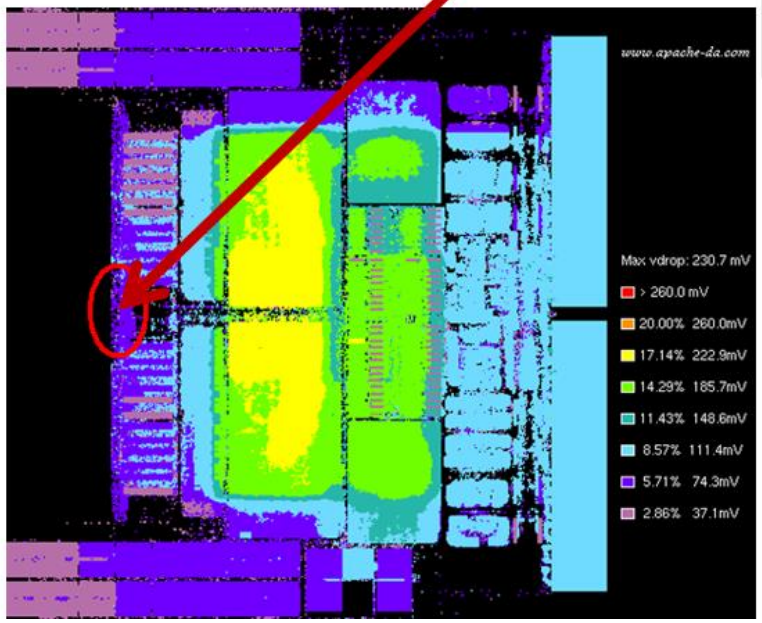
Supply noise waveform measurement

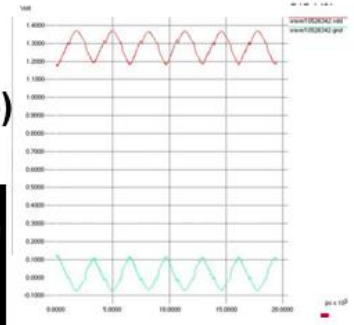
- The measured and simulated supply noise value closely match at the sense point
- Supply noise values vary at different positions of the chip, package and PCB

Measuring noise on the die is tough!

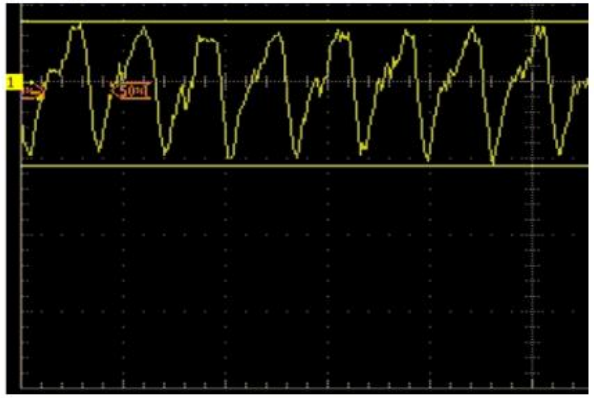


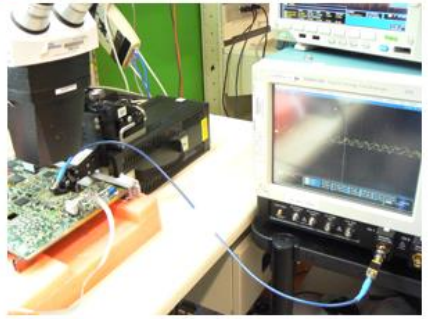
Simulation result : 74.3mV
At core voltage sense point (die)





Lab measurement result : 62.8mV
At pads for core sense (PCB)

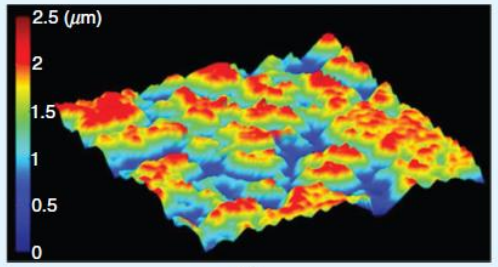




IEEE EPS EDMS Package Benchmarks with Four Typical Industry SI/PI Cases

- **Accurate Correlation Between Modeling and Measurements**
- **Available for download and trial as "open-source"**

https://www.packaging-benchmarks.org/



(a)

Model Name	Model
Hammerstad	$k_{ef} = \left(1 + \frac{2}{\pi}\tan^{-1}\left[1.4\left(\frac{h}{\delta}\right)^2\right]\right)$
Groisse	$k_{ef} = \left(1 + \exp\left(-\frac{\delta}{2h}\right)^{1.6}\right)$
Huray	$k_{ef} = \left(1 + \frac{3}{2}\,SR\,\frac{1}{1 + \frac{\delta}{a} + \frac{\delta^2}{2a^2}}\right)$

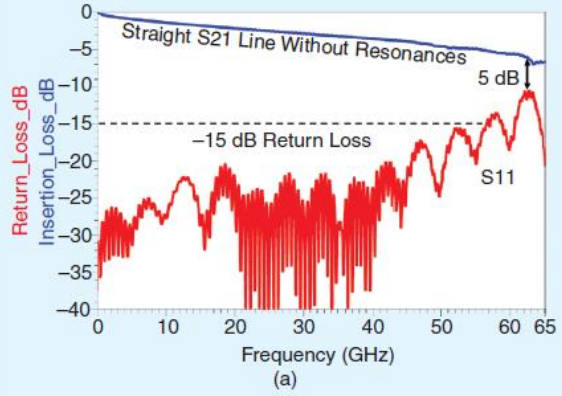
Where
h = Surface Roughness RMS Value

$$\delta = \sqrt{\frac{2}{\omega\mu_0\sigma_{smooth}}}$$

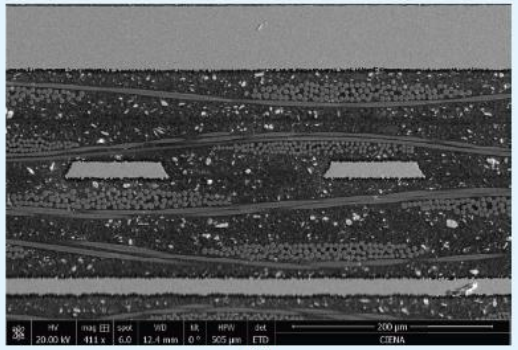
a = Nodule Radius
SR = Surface Ratio

(b)

FIGURE 5. (a) Surface of a rough copper foil and (b) commonly used surface roughness models. RMS: root mean square.

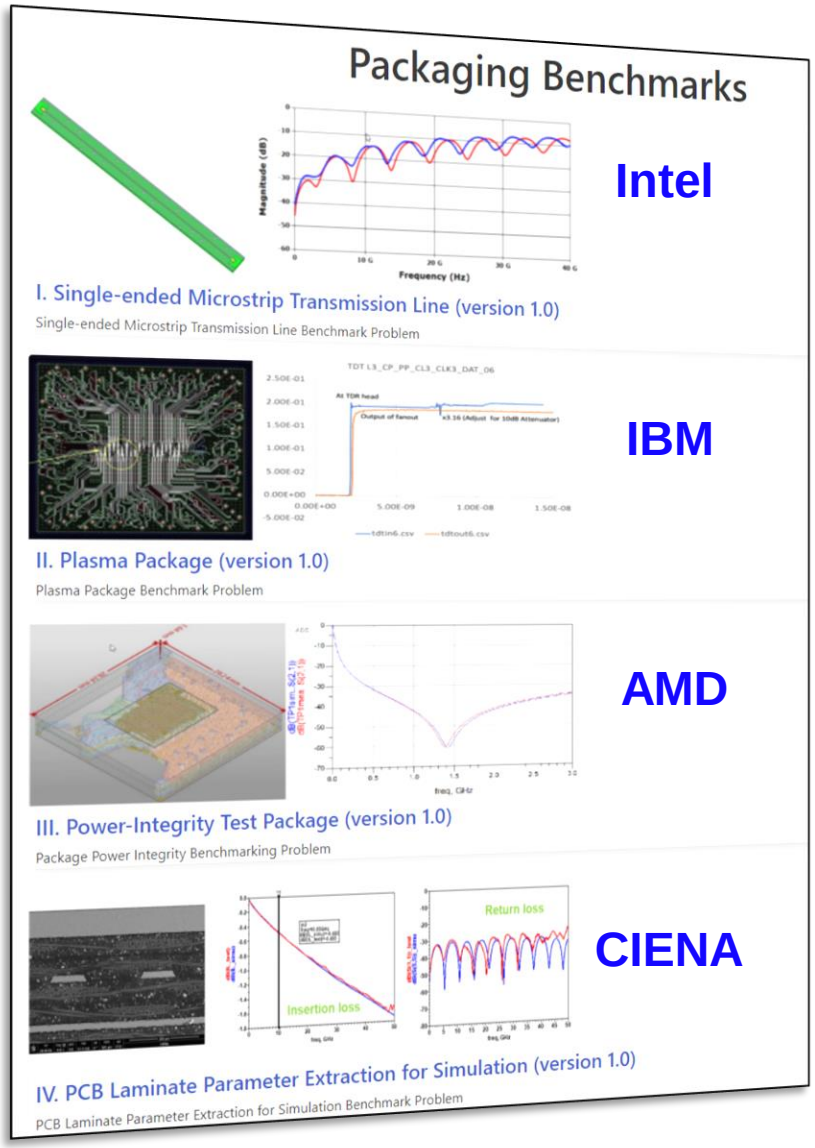


(a)



(b)

FIGURE 7. (a) Raw data for transmission lines and connectors with VNA. (b) Cross-sectional SEM. VNA: vector network analyzer.



H. Barnes, K. Aygun, M. J. Hill, Z. Zhang, k. Hu, J. Aronsson, P. Paladhi, J. Balachandran, B. Shi, R. Sharma, J. Schutt-Aine, V. I. Okhmatovski "Benchmarking and Reproducibility in Computational and Experimental Characterization of Electronic Packages for Signal/Power Integrity" - IEEE ANTENNAS & PROPAGATION MAGAZINE, April 2025

Summary

- SI and PI challenges are introduced, along with solutions for next-generation interconnects
- Sign-off flows for Power and DVD have been presented
- PDN noise analysis has been conducted across chip, package and PCB for a complex chip design
- Lab measurements and simulations show good agreement

Thank You!

Kaisheng (Klaus) Hu

Principal Engineer of SI & PI – Ciena

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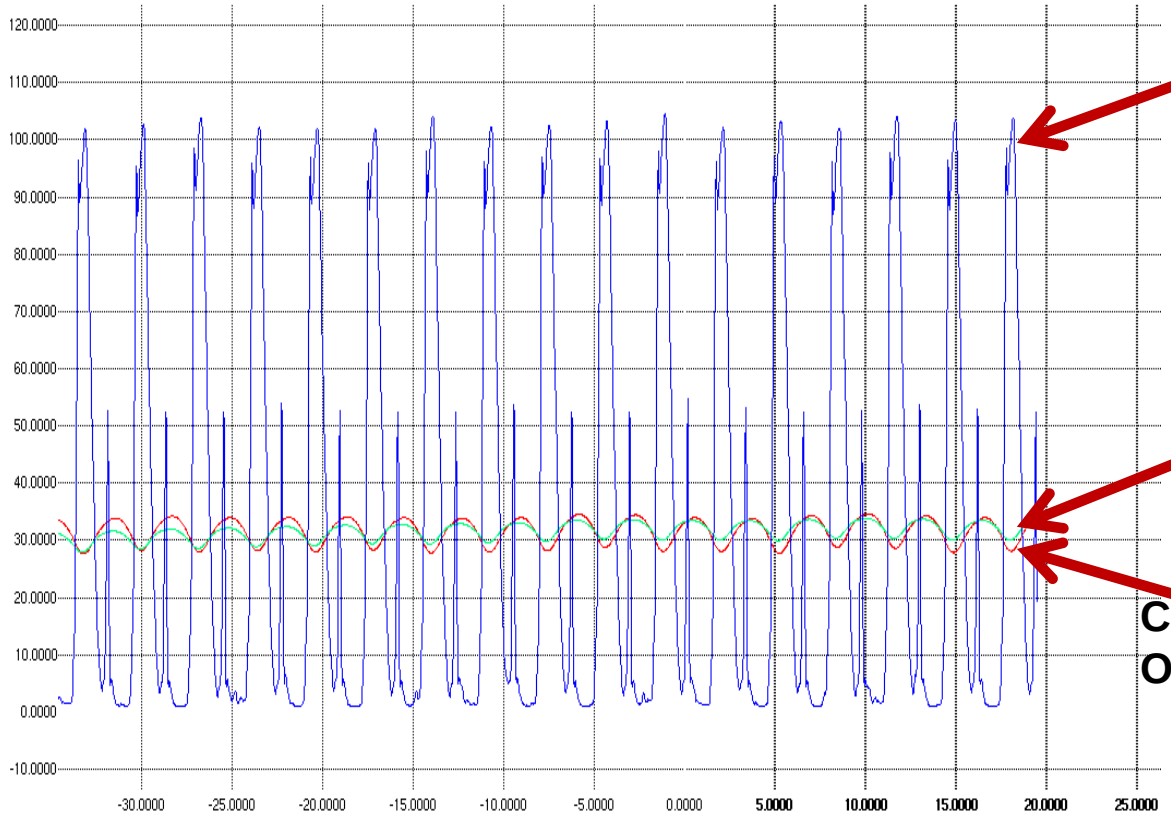
Backup Slide : AC current waveforms at various die and package positions

- Total current demand can be very high at the instance level, peaking at up to 100A
- The local loop inductance between the package decap and the die bump is higher than that between the die bump and the BGA/VRM
- The package decap provides a smaller current compared to the on-die decap
- The difference between demand current and VRM current is related to DvD
- The VRM is assumed to be ideal



Total demand current at instances

Delta current is from On-die decap

Current provided By VRM at BGA

Delta is from Package decap

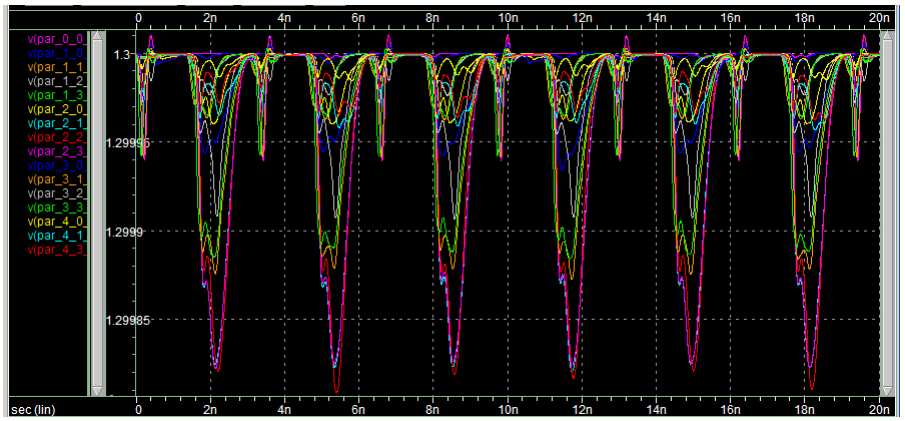
Current flowing Over die C4 bump

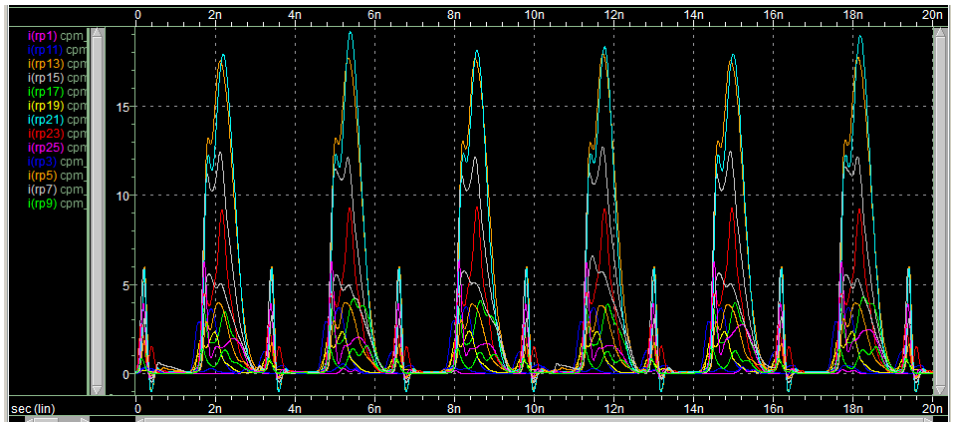
K. Hu, "Signal Integrity and Power Integrity analysis with EDA tools ", 4th Annual Ansys Innovation Conference, 2019

ciena

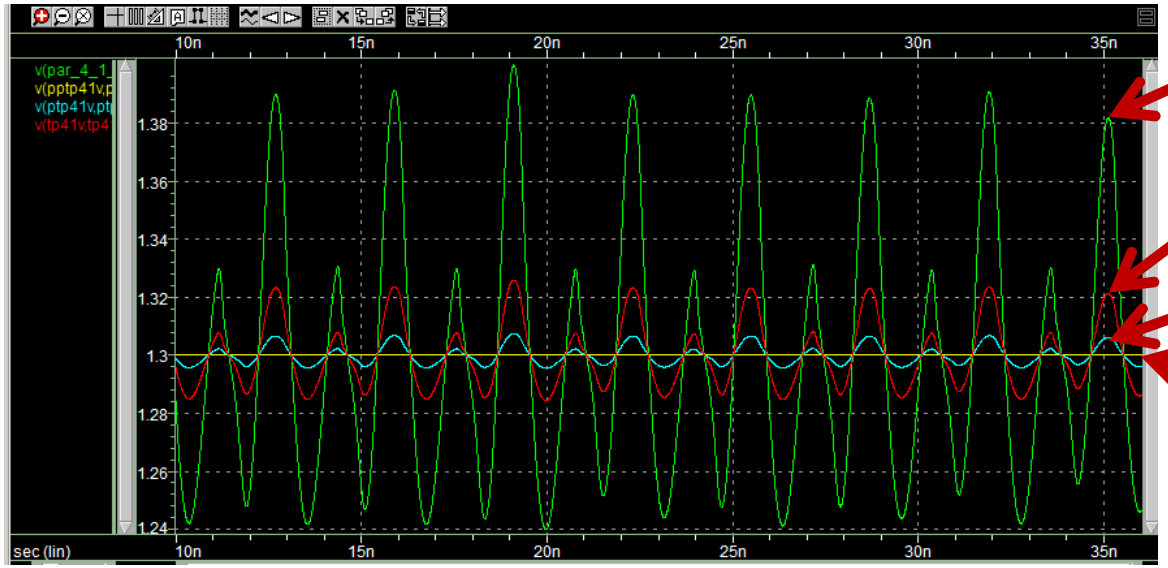
Backup Slide: Noise voltage/current waveforms

1) Noise voltage and current waveforms from CPM with 1 pH package inductance





2) Noise voltage waveform at different positions within the die, package, and PCB link with 4 pH package inductance



Noise waveform at die C4 bump (160mV)

Noise waveform At package BGA pad (45mV)

Noise waveform At PCB close to VRM (10 mV)

Noise waveform At ideal VRM (zero)

The major source of supply noise is the die!