448G Architectures for AI – Addressing the Challenges, Enabling the Future

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 | ECOC 2025

ALPHAWAVE SEMI

OIF - Where the optical networking industry's interoperability work gets done

Who:

- 160+ member companies
  - Network operators
  - System vendors
  - Component vendors
  - Test & measurement vendors
  - Academia & research

What:

- Identify needs, gaps
- Develop interoperable optical, electrical, and control solutions
- Publish Implementation Agreements

Why:

- Accelerate adoption of advanced technology to connect a global, open networked world

Challenge: Support innovation while preserving interoperability, optimizing performance and cost

Accelerating Market Adoption of Optical Networking Technologies

160+ Member Companies ▶ 25+ Years of Service ▶ Member Driven Global Organization

COHERENT OPTICAL

Multi-Vendor Interoperability in Client Form Factors

1600ZR+
- <1000km Multi-Span Coherent DWDM

1600LR, 800LR
- <10km Coherent Point-to-Point

1600ZR, 800ZR, 400ZR
- >80km Coherent DWDM

ELECTRO-OPTICAL

Energy Efficient Interfaces (EEI) –Low Latency/ Optimized Energy Interfaces for AI/ML
- Compute Optics Interface (COI)
- Retimed Tx, Linear Rx (RTLR)
- External Laser Sources (ELSFP)
- Co-Packaged Modules (3.2T)

Common Electrical I/O (CEI)
- High-Speed Building Blocks
- 448G, 224G, 112G, 56G, 28G
- LR, MR, VSR, XSR+, XSR, MCM, Linear
- Protocol Agnostic Link Training

OIF

Identifies Industry Needs and Gaps

Publishes Implementation Agreements (specifications) (100+), Requirements and White Papers

Performs Interoperability Demonstrations (65+)

Advances industry consensus via workshops, webinars, etc.

MANAGEMENT

Common Management Interface Specification (CMIS)
- Single Solution Ranging From Copper to Coherent
- Simplified Bring up Between Host and Module
- Supports Standard and Custom Interfaces

Transport SDN APIs
- Automation, Programmability

Enhanced Network Operations
- Artificial Intelligence
- Digital Twin
- DC Storage and Optical Multi-Layer Coordination

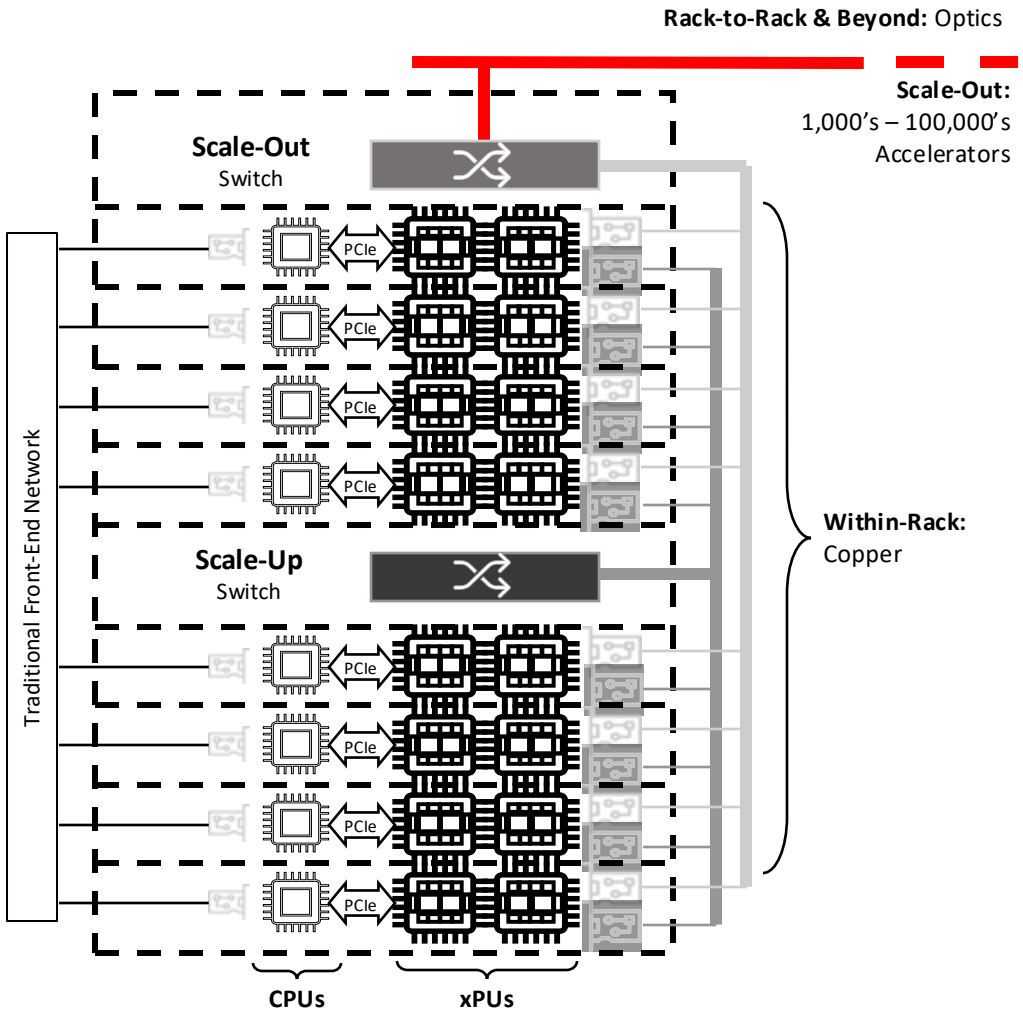
PROTOCOL

Flex Ethernet (FlexE)
- 800 Gb/s Ethernet PHY support

For more information, visit www.oiforum.com

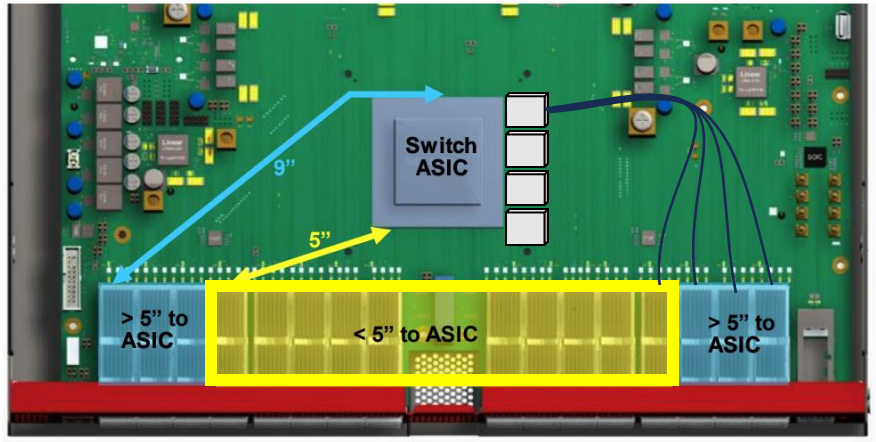
AI is Driving a New Interconnect Era

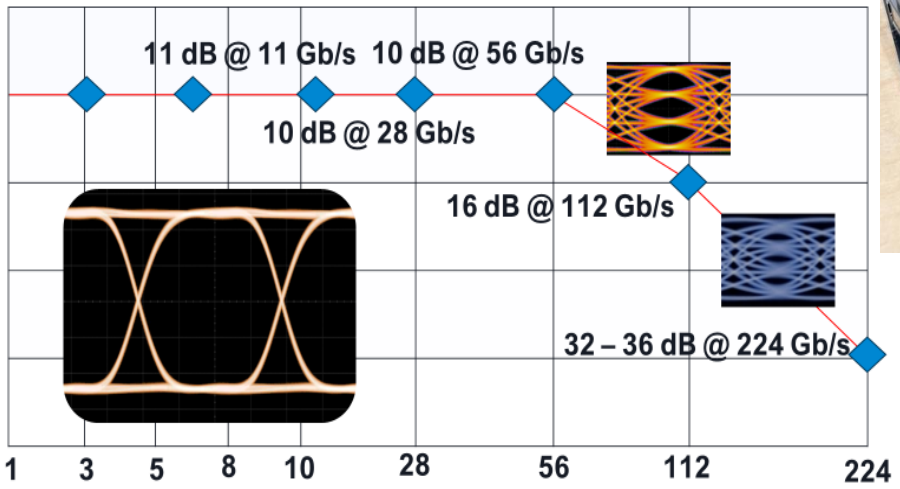
- Frontier AI models grow ~4× annually, driving demand for higher memory, compute, and bandwidth
- Frontier AI models exceed single-accelerator memory, requiring multi-accelerator clusters with hierarchical interconnects:
  - Scale-Up (intra-node)
    - Electrical
  - Scale-Out (inter-node)
    - Optical
  - Front-End (I/O)
- Maximizing accelerators per scale-up domain requires compact rack design
  - Density is Imperative



AI is Driving a New Interconnect Era

- AI's appetite for interconnect bandwidth to keep XPUs computing, not idling is only increasing
- Today - 224G PHYs with low-loss media (cabled hosts, backplanes, advanced PCBs)
  - Limitations in ASICs, PCBs, connectors, and cables
- Industry Collaboration is a necessity to preserve rack density



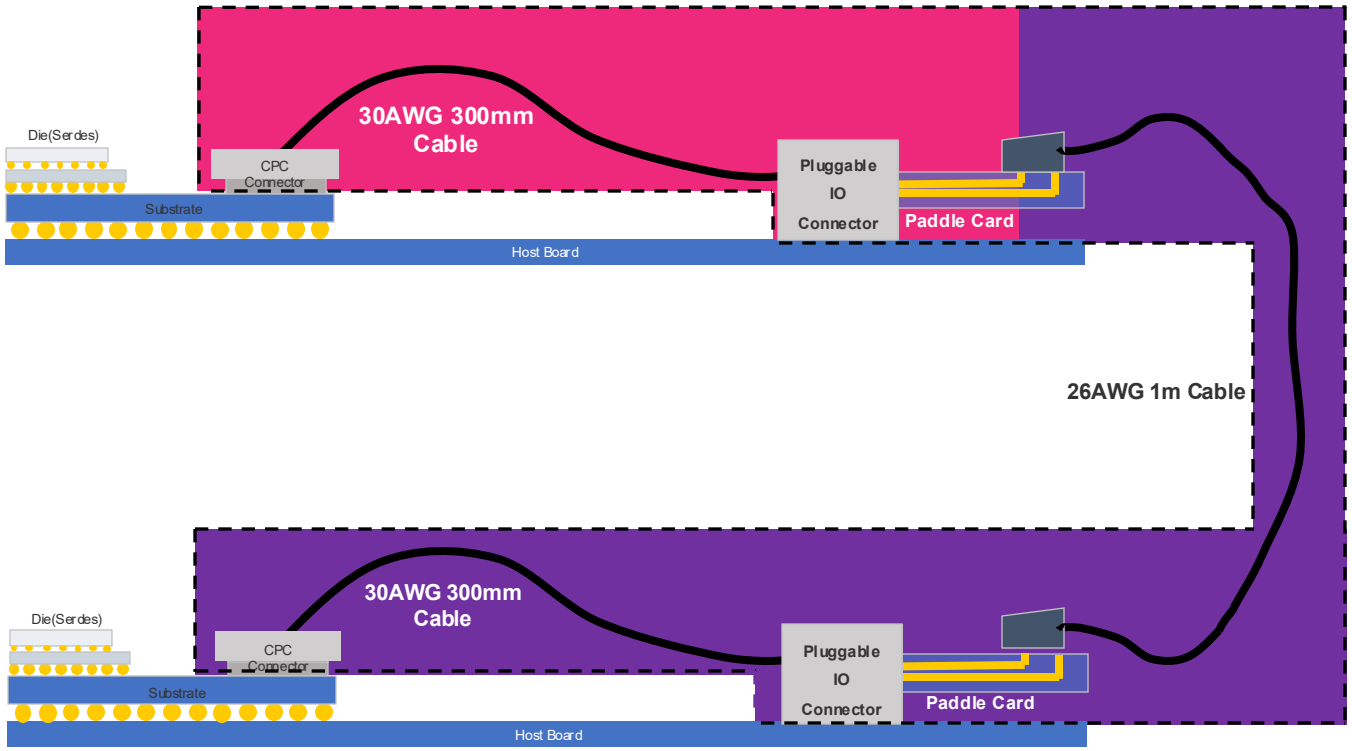


448 Gbps Challenges, Connectors and Channels

- While industry develops alternate architectures, it is inevitable that a higher data rate is required such as 448 Gbps
- Systems can't get smaller, creating a need to maintain current 'reach' based architectures while doubling bandwidth
- What do interconnects and resultant channels look like at these potential data rates?
- Channel reality is critical to know what the solutions must tolerate
- OIF 448G project was started in August 2024, Baseline in Q4 2025

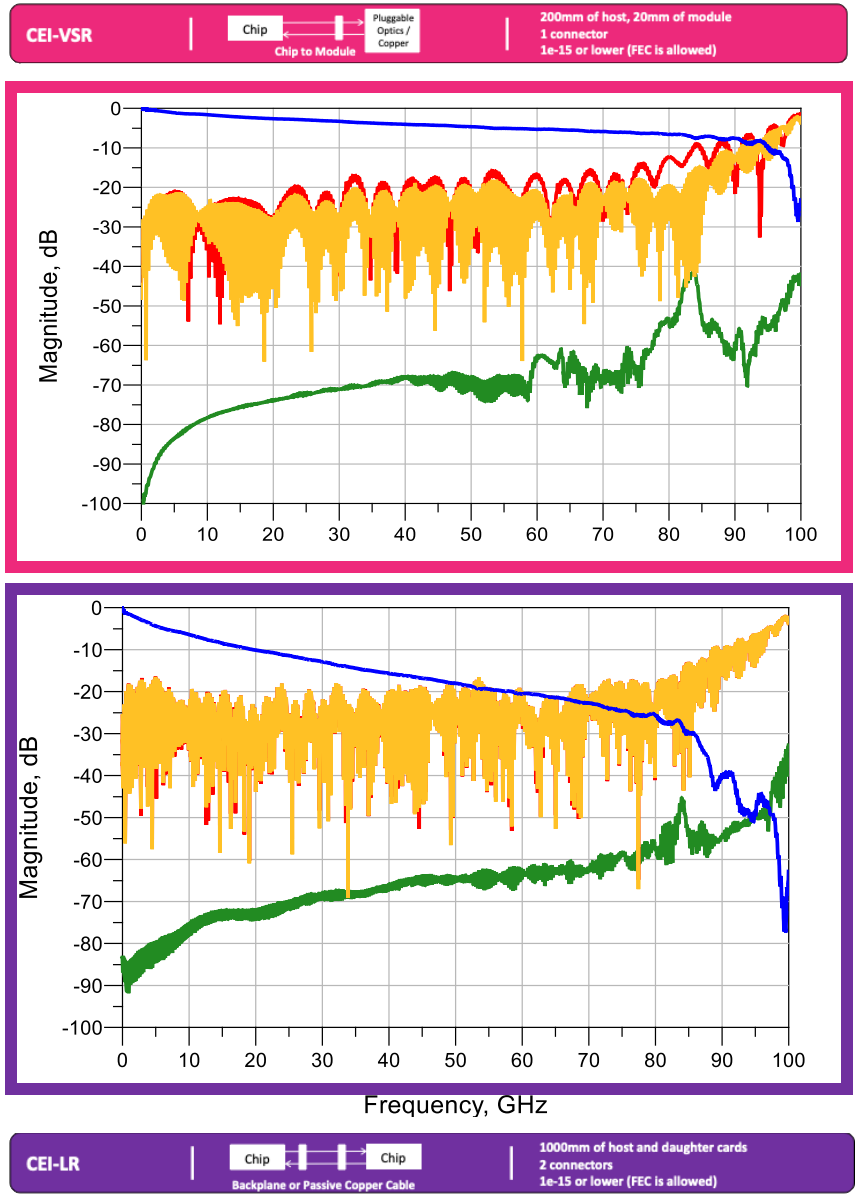
OIF CEI projects	CEI-56G-LR	CEI-112G-LR	CEI-224G-LR	CEI-448G-LR
Timeline	2014-2017	2017-2021	2021-	2026-
Ethernet rate	50/100/200G	100/200/400G	200/400/ 800/1600G	400/800/ 1600G/3200G
Switch capacity	12.5T	50T	100T	200T
Per-lane data rate	56 Gbps	112 Gbps	224 Gbps	448 Gbps
Modulation	PAM4	PAM4	PAM4	TBD
Insertion loss	30dB at 14GHz ball-ball	28dB at 28GHz ball-ball	40dB at 56GHz bump-bump	TBD
Reach objectives	3m copper cable	2m copper cable	1m copper cable	TBD
Pre-FEC BER target	1e-4	1e-4	1e-4	TBD
SerDes architecture	Analog/DSP	Analog/DSP	DSP	TBD

Current Bottlenecks

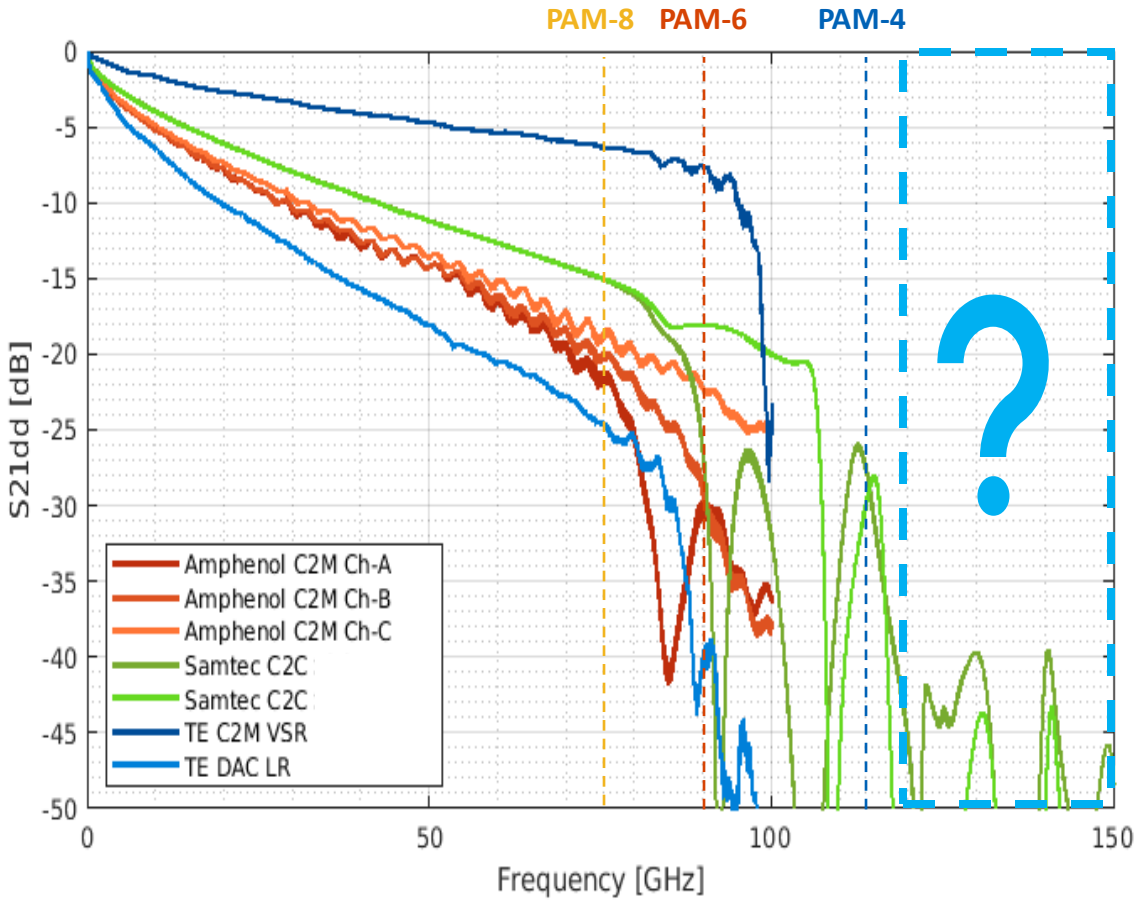


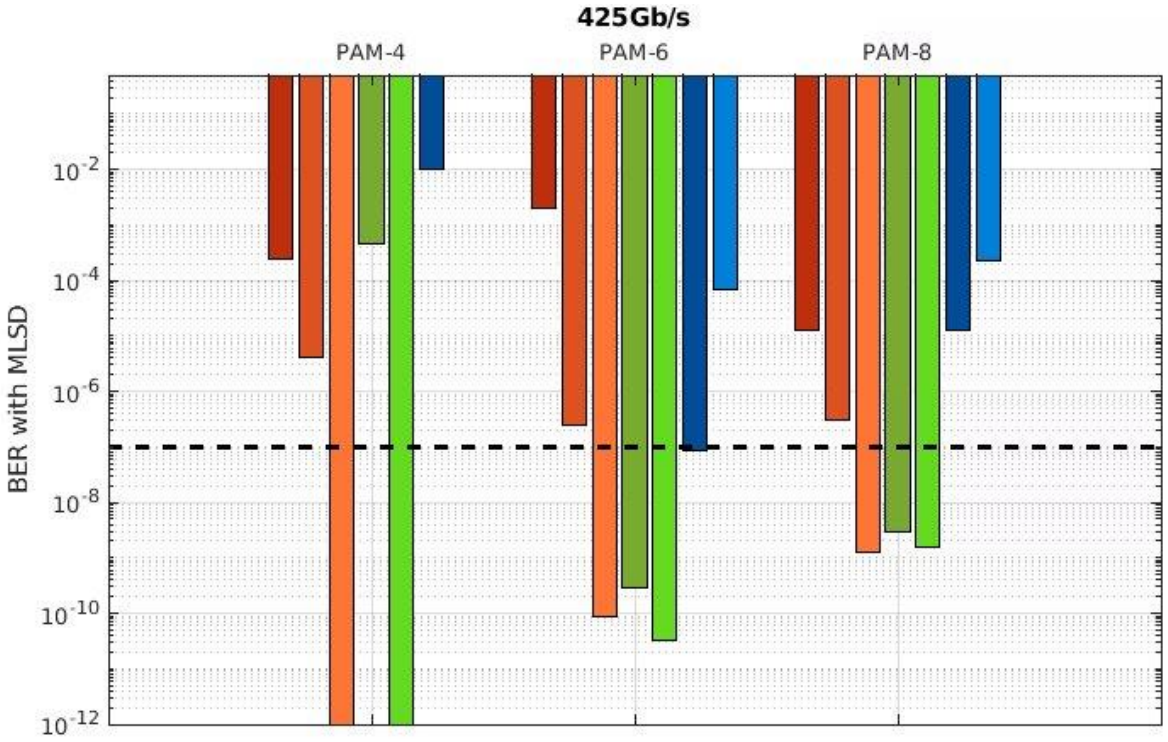
Insertion Loss, Return Loss, Module side

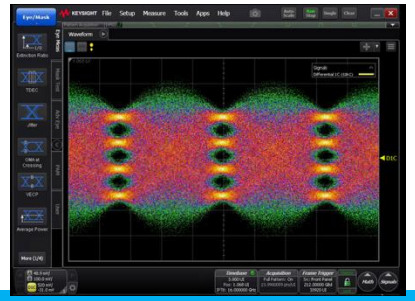
Return Loss, Host side PowerSum Crosstalk

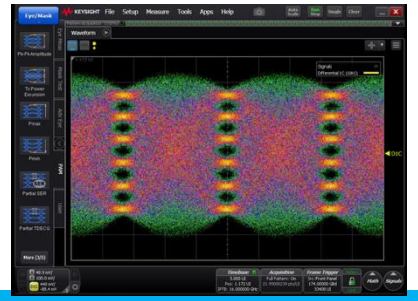


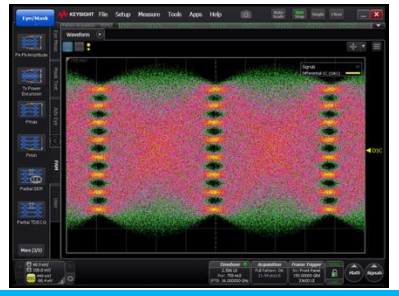
Modulation & Coding Strategies for 448G





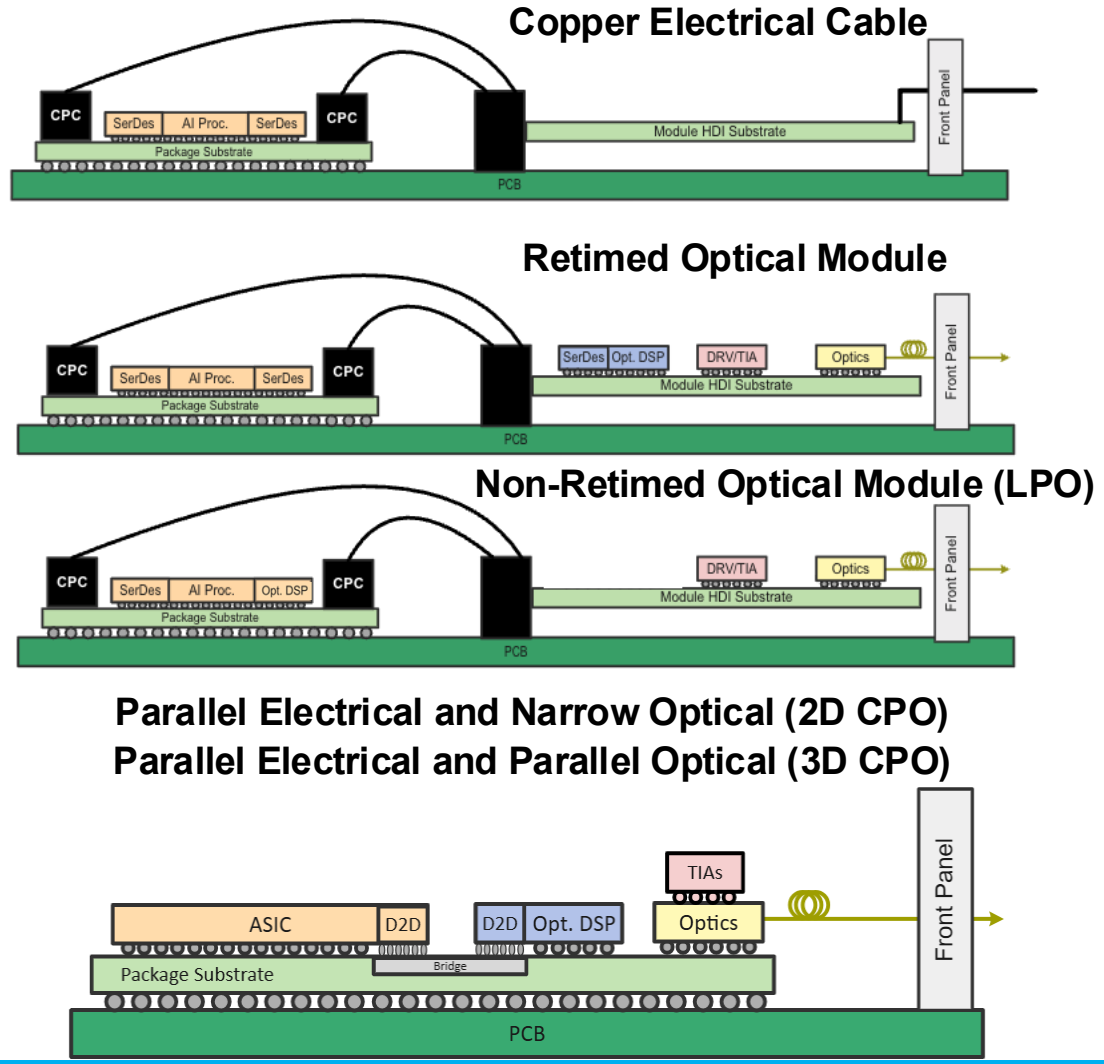






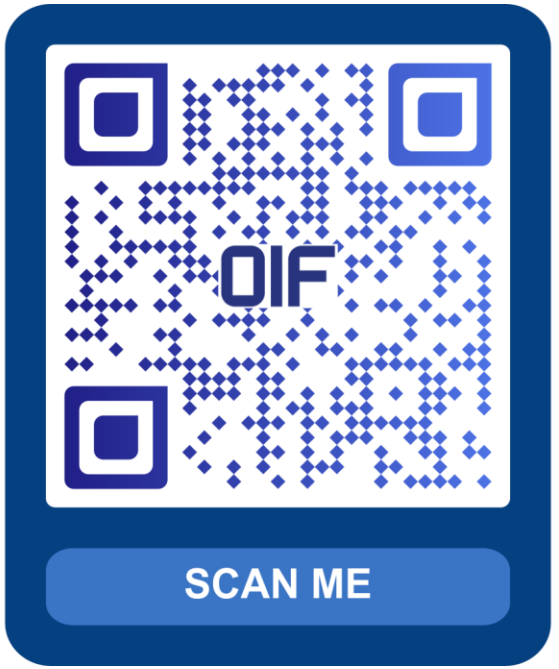
Scale Up AI Architectures Beyond a single Rack

- AI is rapidly driving the next generation of systems
  - Larger radix, cost effective, low latency, dense, and energy efficient interconnections
- Efficient optical connectivity are also being explored
  - conventional optical links fall short in several areas: bandwidth density, latency, and energy efficiency
- Hyperscalers deploying these systems are providing key metrics for the next generation of Compute Optics Interface (COI) links
  - choice of the best architectures to be discussed



Conclusion & Call to action

- Next-gen AI interconnectivity will be enabled by 448 Gbps per lane
- Copper will enable scale-up links at 448G despite the challenges
  - SI, modulation, and packaging are equally critical – no single-silver-bullet but transition to CPC will necessary
- Optical scale-up is also under consideration
  - Performance, reliability and energy efficiency need to be investigated
- Join OIF to contribute towards 448G Framework Document, Common Electrical IO Implementation Agreements, and Next Gen AI Electrical and Optical Compute Interfaces!
  - Live Interoperability Demonstration at ECOC



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