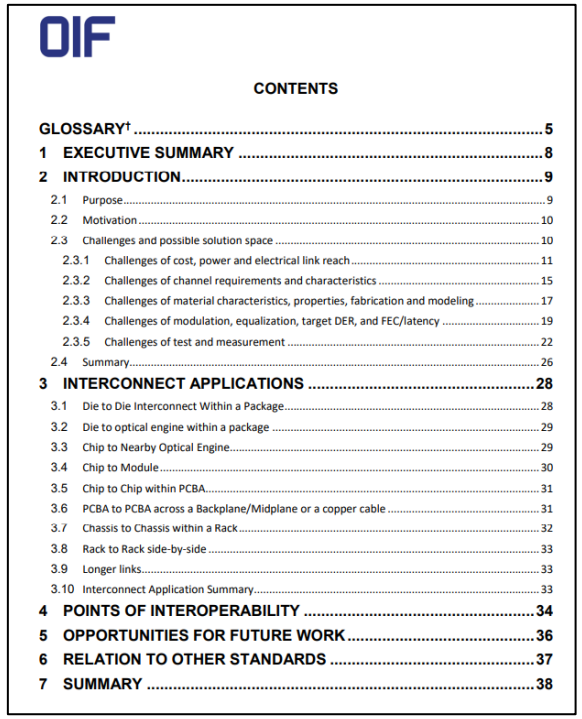
OIF
PLL INTEROP DEMO
ECOC 2024

CEI-112G-Linear & CEI-224G Interoperability Demo ECOC 2024

OIF's Common Electrical I/O (CEI) Work Has Been a Significant Industry Contributor

Name	Rate per pair	Year	Activities that Adopted, Adapted or were influenced by the OIF CEI
CEI-224G	224Gbps	202X	Several channel reach projects in progress, kicked off in 2022
CEI-112G	112Gbps	2022	Five channel projects are complete, two channel projects in progress, IEEE, InfiniBand, T11 (Fibre Channel), Interlaken, ITU.
CEI-56G	56Gbps	2017	IEEE, InfiniBand, T11 (Fibre Channel), Interlaken, ITU
CEI-28G	28 Gbps	2012	InfiniBand EDR, 32GFC, SATA 3.2, SAS-4,100GBASE-KR4, CR4, CAUI4, Interlaken, ITU
CEI-11G	11 Gbps	2008	InfiniBand QDR, 10GBASE-KR, 10GFC, 16GFC, SAS-3, RapidIO v3, Interlaken, ITU
CEI-6G	6 Gbps	2004	4GFC, 8GFC, InfiniBand DDR, SATA 3.0, SAS-2, RapidIO v2, HyperTransport 3.1, Interlaken, ITU
SxI5	3.125 Gbps	2002-3	Interlaken, FC 2G, InfiniBand SDR, XAUI, 10GBASE-KX4, 10GBASE-CX4, SATA 2.0, SAS-1, RapidIO v1, ITU
SPI4, SFI4	1.6 Gbps	2001-2	SPI-4.2, HyperTransport 1.03

CEI-224G: Framework Document



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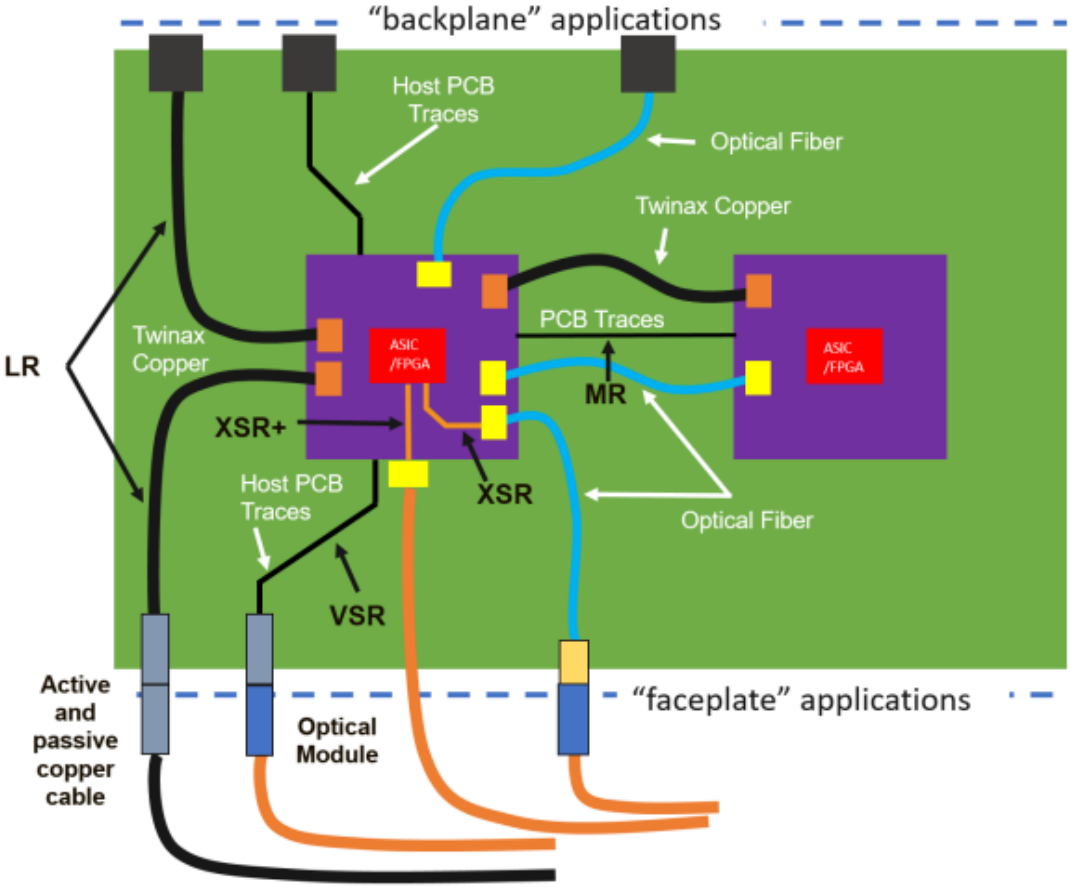
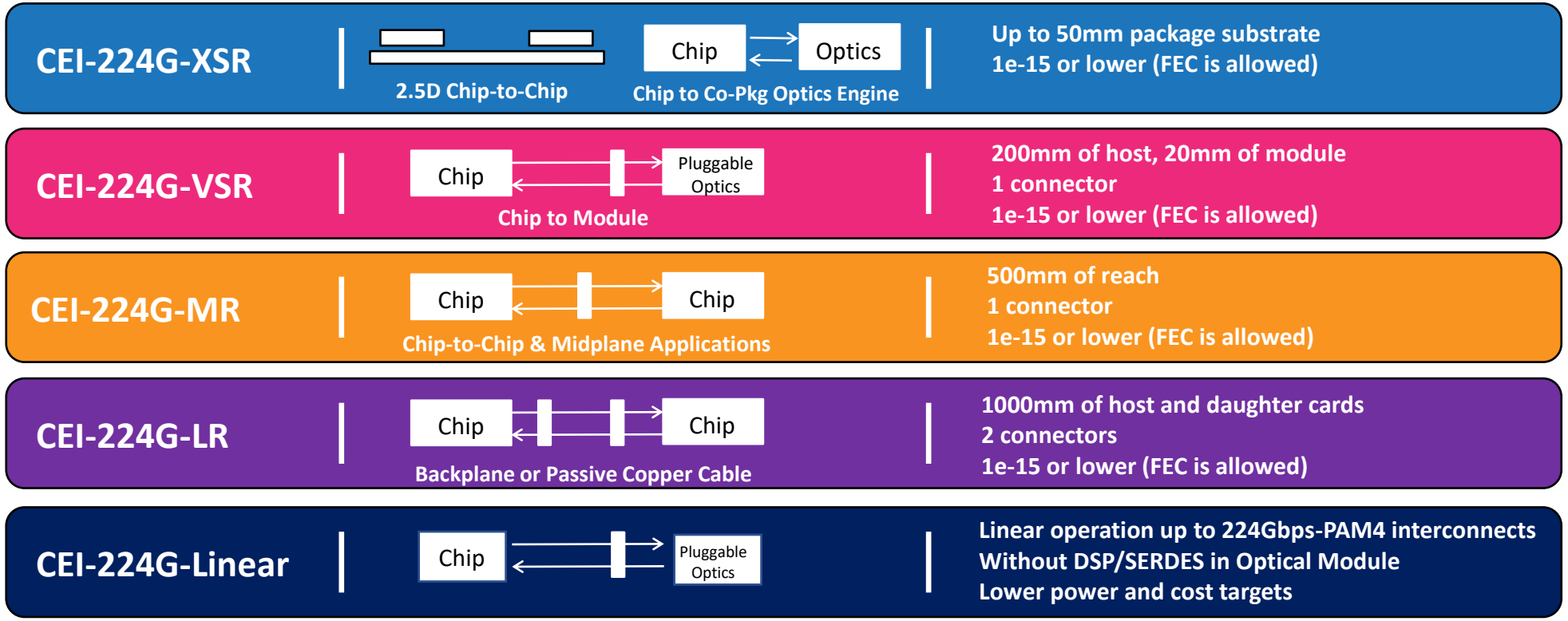
CONTENTS

- Summarizes the consensus findings and guidance for new OIF CEI-224G projects
- Identifies key technical challenges for next generation systems
  - Power, density, performance, reach and cost
- Defines electrical interconnection applications and discusses some of the interoperability test challenges
- Establishes baseline materials that will enable 1.6/3.2 Tbps rate architectures and lower cost, lower complexity 800G and 400G architectures



OIF-FD-CEI-224G-01.0 published in February 2022

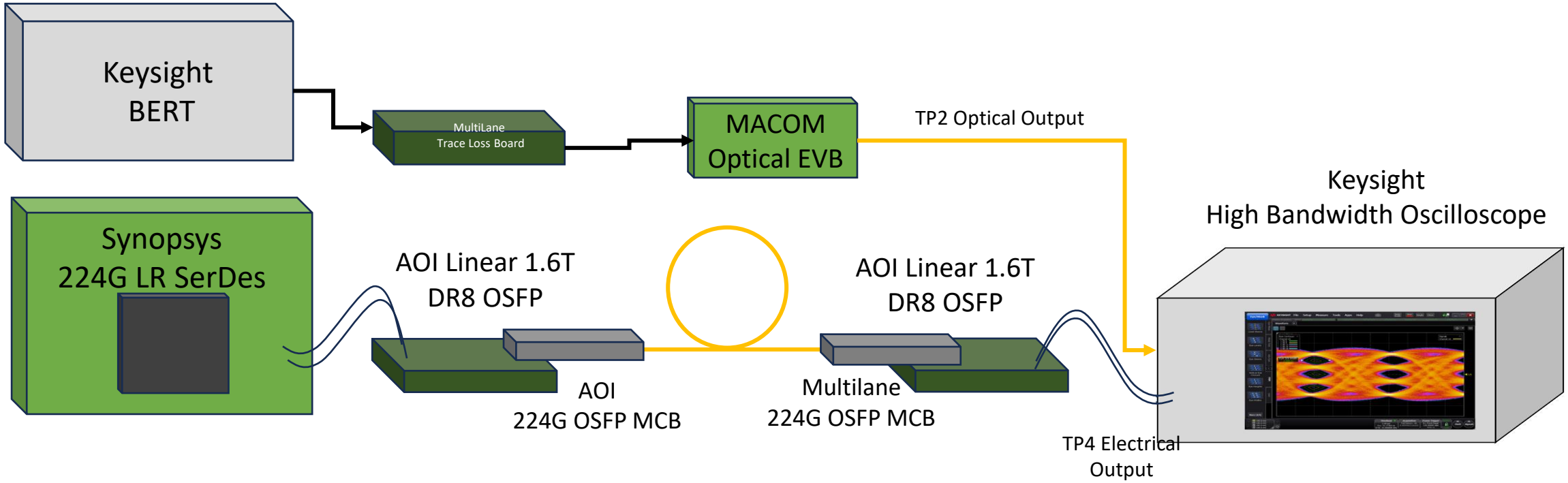
OIF CEI-224G New Project Starts



CEI-224G-LR Draft Specification is currently in review for OIF members

- One SerDes core might not be able to cover multiple applications from XSR to LR
- For short reach applications, simpler and lower power equalizations are desired

CEI-224G-Linear at ECOC 2024

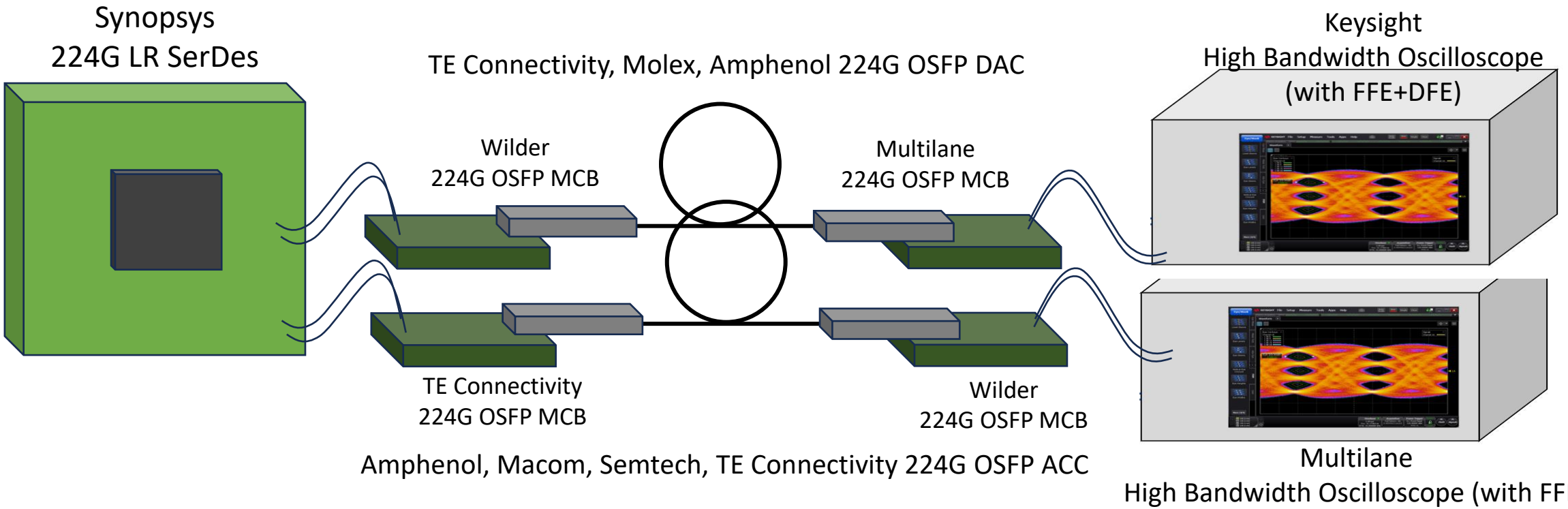


This CEI-224G-Linear demonstration shows test chip silicon sending a PRBS13Q PAM4 212 Gbps signal through a 1.6T DR8 OSFP linear optical module via Module Compliance Board. The optical connection over SMF is then converted to an electrical signal on the partnered DR8 OSFP linear optical module with MCB and communicated to an oscilloscope electrically displaying the resulting far end eye diagram. A second path in the demonstration leverages test equipment to generate a PRBS13Q PAM4 212 Gbps signal which is then sent over a trace loss board. An evaluation board is used to perform linear compensation and convert to an optical signal which is displayed on the oscilloscope

CEI-224G-Linear | Chip — Pluggable Optics |

Linear operation up to 224Gbps-PAM4 interconnects
Without DSP/SERDES in Optical Module
Lower power and cost targets

CEI-224G-LR/MR at ECOC 2024



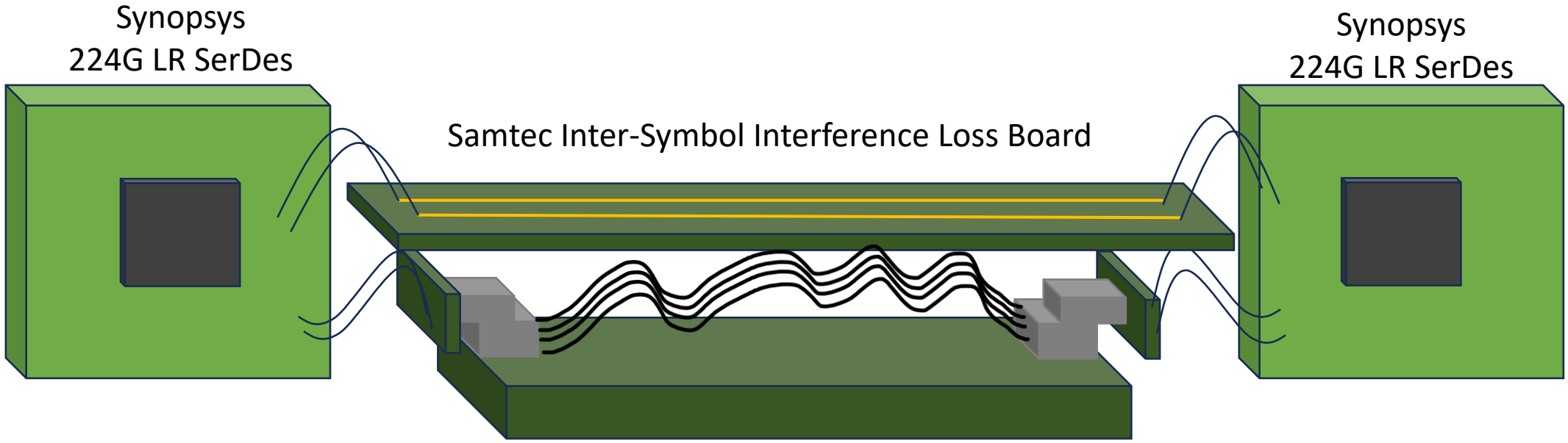
This LR demonstration shows test chip silicon transmitting a PRBS13Q PAM4 212 Gbps signal over a network of multi-vendor connectors/MCBs and copper cabling, both passive (DAC) and re-driven active copper cables (ACC), including break-out test fixturing, totaling over 25 dB of channel loss and 40 dB of insertion loss die to die at 56 GHz. This is a building block for enabling system to system interoperability links, driving 1.6T connectivity in the data center.

CEI-224G-LR

Backplane or Passive / Active Copper Cable

1000mm of host and daughter cards
2 connectors
1e-15 or lower (FEC is allowed)

CEI-224G-LR at OFC 2024



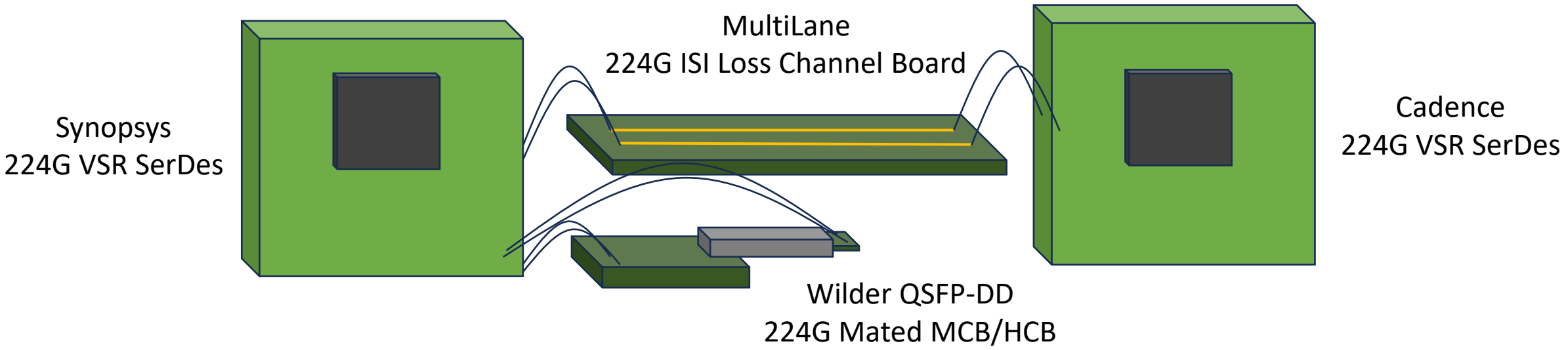
This LR demonstration shows test chip silicon transmitting a PRBS13Q PAM4 212 Gbps signal over a cabled near chip/cabled backplane implementation (750mm) plus break-out test fixturing, totaling over 25 dB of channel loss and 40 dB of insertion loss die to die at 56 GHz. This enables up to a meter of backplane with host and daughter cards, for “line card to line card” or “AI/ML architecture” or “GPU/GPU to switch” interconnectivity.

CEI-224G-LR

Backplane or Passive Copper Cable

1000mm of host and daughter cards
2 connectors
1e-15 or lower (FEC is allowed)

CEI-224G-VSR at ECOC 2024

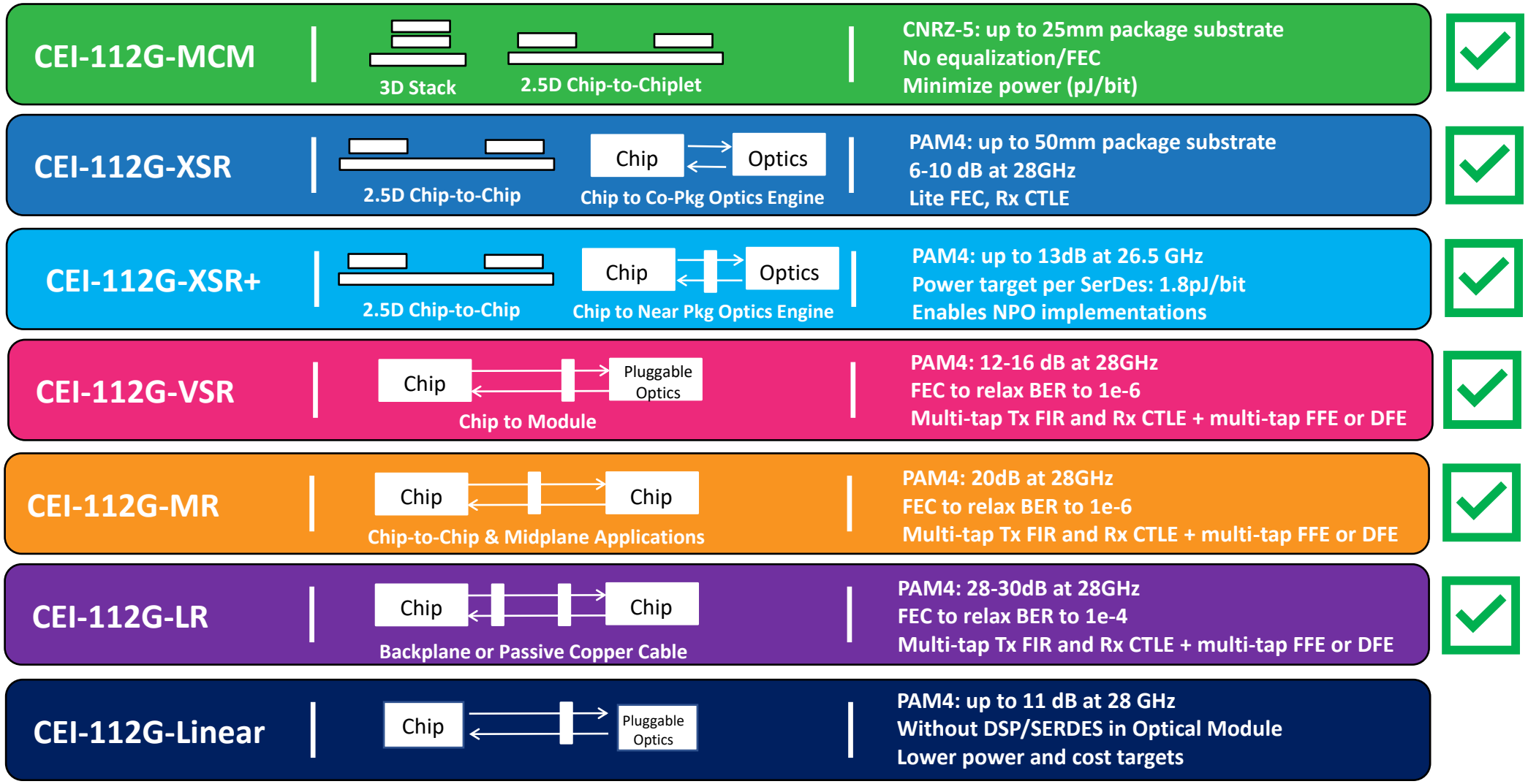


This VSR interoperability demonstration includes test chip silicon from two vendors leveraging a VSR channel operating at 212.5 Gbps PRBS31Q PAM4 with a die-to-die insertion loss of 32 dB at 56 GHz. A second channel is also leveraged in this setup is emulating a Chip to Module channel, such as a switch ASIC to front panel pluggables, enabling 1.6T optical connectivity leveraging a mated Module Compliance Board (MCB) and Host Compliance Board (HCB).

CEI-224G-VSR	Chip → Pluggable Optics (Chip to Module)	200mm of host, 20mm of module 1 connector 1e-15 or lower (FEC is allowed)

OIF CEI-112G Development Application Space

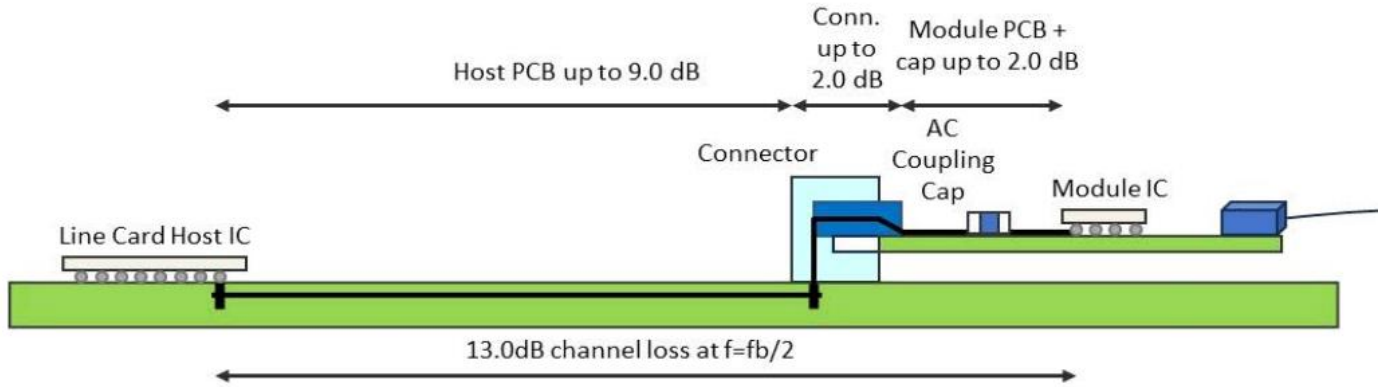
- PAM4 modulation scheme becomes dominant in OIF CEI-112 Gbps interface IA
- One SerDes core is not able to efficiently cover multiple applications from XSR to LR
- For short reach applications, simpler and lower power equalizations are desired



CEI-112G-Linear at ECOC 2024

OIF CEI Interoperability Demonstration Summary
- 24 Unique member participants in the ecosystem in the last three years
- Interoperability use cases demonstrated include
  - 100m MMF Operation
  - 500m SMF Operation
  - Multi-Vendor LPO Modules
  - Multi-Vendor LPO and RTLR Modules
  - Multi-Vendor LPO and DSP Modules
  - Multi-Vendor SerDes Vendors
  - TP1a, TP2, TP4 Compliance

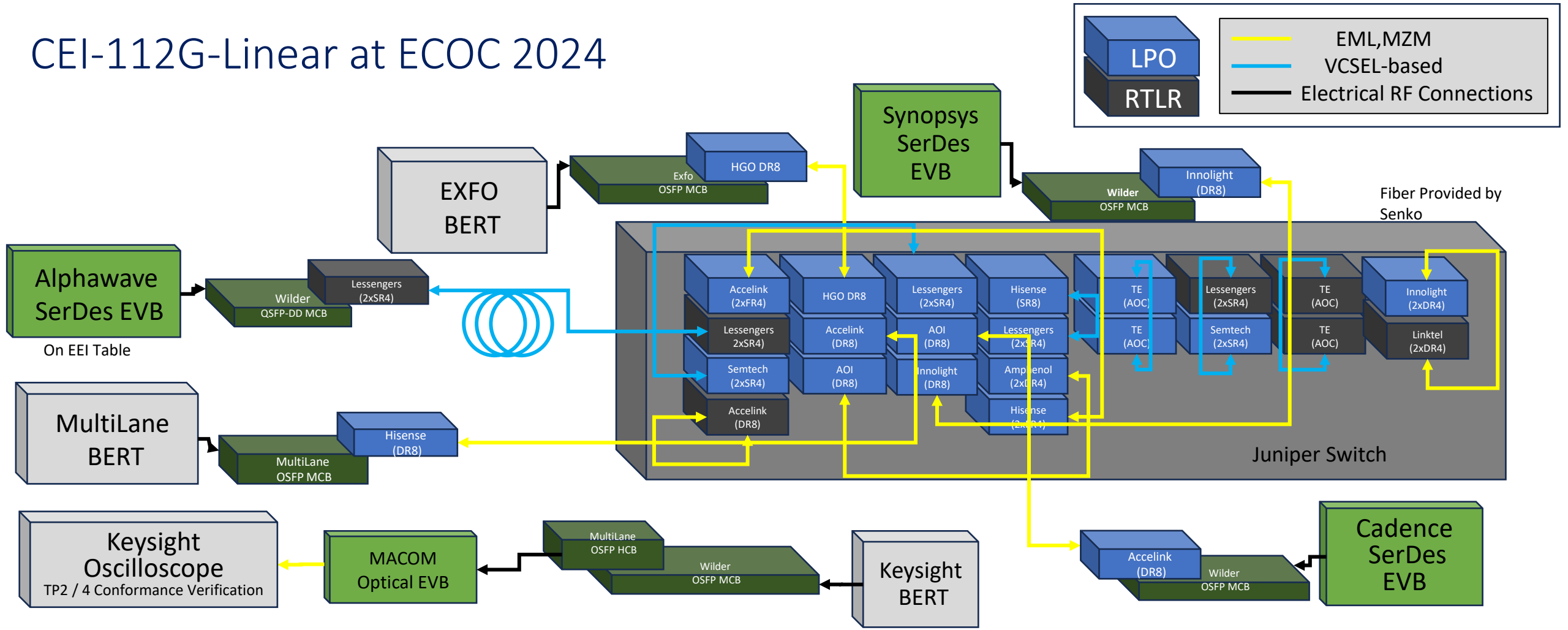
Advantages of LPO:
- Lower Power
  - Up to 50% module power consumption savings compared to traditional retimed modules
- Lower Latency
- Protocol Agnostic
- Keeps sideband functionality and manageability
- Orders of magnitude of BER margin
- Electrical specification (EECQ) alignment with optical specification (TDECQ)



CEI-112G-Linear | Chip → Pluggable Optics |

PAM4: Up to 13 dB at 28GHz
Without DSP/SerDes in Optical Module
Lower Power and Cost Targets

CEI-112G-Linear at ECOC 2024

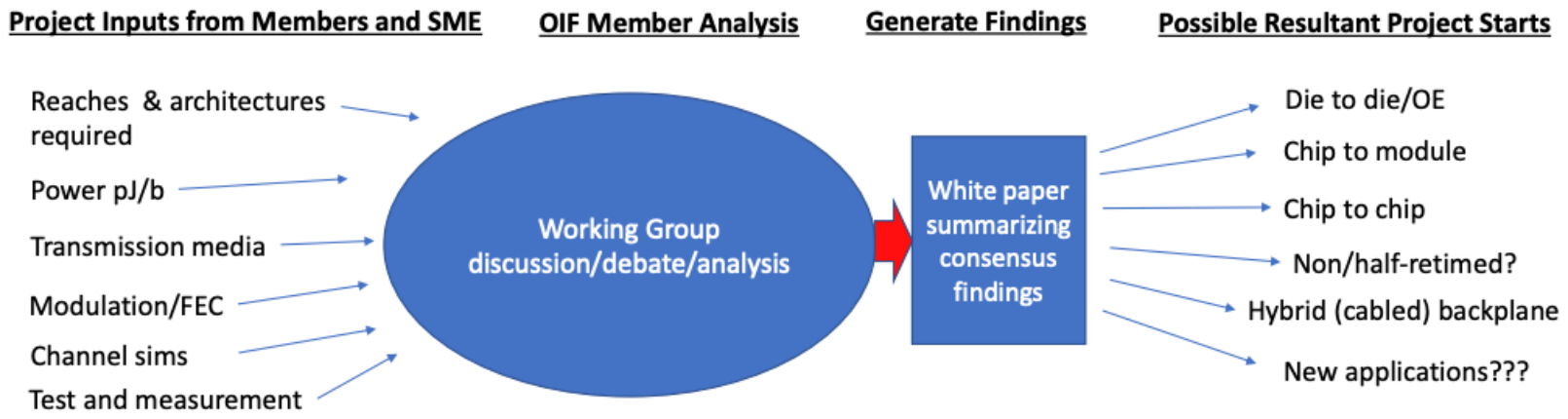


This demonstration encompasses the entire ecosystem enabling multi-vendor CEI-Linear interoperability. A 51.2T Switch along with multi-vendor SerDes represented by test platforms emulating Ethernet devices, driving single mode and multi-mode, multi-vendor Linear Pluggable Optics (LPO's) while demonstrating quality BER with FEC tail margin, at minimal power consumption. Test and measurement equipment provide conformance verification and insight on compliance into stages of the link. Interoperability between LPOs interfacing with RTLR (Retimed Transmit, Linear Receive – new EEI architecture) is also achieved showcasing compatibility between the two pluggable options .

Participating Members

CEI-448G: Framework Document Start

- The OIF has already started the process on considering challenges for new OIF CEI-448G projects
- Identifies key technical challenges for next generation systems
  - Interfaces, reaches, modulations, FEC, test methodologies, etc.
- Investigations by end users and developers will bring critically important channel architecture requirements to the table, along with simulations of channels and device performances
- Establishes baseline materials that will enable 3.2/6.4 Tbps rate architectures and lower cost, lower complexity 800G and 1.6T architectures



OIF-FD-CEI-448G Approved in August 2024

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