OIF Common Electrical I/O (CEI) -112G Interoperability Demo

OFC 2022

March 8-10 – San Diego CA

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OIF's Common Electrical I/O (CEI) Work Has Been a Significant Industry Contributor

Name	Rate per pair	Year	Activities that Adopted, Adapted or were influenced by the OIF CEI
CEI-112G	112Gbps	2022	Seven channel reach projects in progress, IEEE, InfiniBand, T11 (Fibre Channel), Interlaken, ITU.
CEI-56G	56Gbps	2017	IEEE, InfiniBand, T11 (Fibre Channel), Interlaken, ITU
CEI-28G	28 Gbps	2012	InfiniBand EDR, 32GFC, SATA 3.2, SAS-4,100GBASE-KR4, CR4, CAUI4, Interlaken, ITU
CEI-11G	11 Gbps	2008	InfiniBand QDR, 10GBASE-KR, 10GFC, 16GFC, SAS-3, RapidIO v3, Interlaken, ITU
CEI-6G	6 Gbps	2004	4GFC, 8GFC, InfiniBand DDR, SATA 3.0, SAS-2, RapidIO v2, HyperTransport 3.1, Interlaken, ITU
SxI5	3.125 Gbps	2002-3	Interlaken, FC 2G, InfiniBand SDR, XAUI, 10GBASE-KX4, 10GBASE-CX4, SATA 2.0, SAS-1, RapidIO v1, ITU
SPI4, SFI4	1.6 Gbps	2001-2	SPI-4.2, HyperTransport 1.03
SPI3, SFI3	0.800 Gbps	2000	(from PL3)

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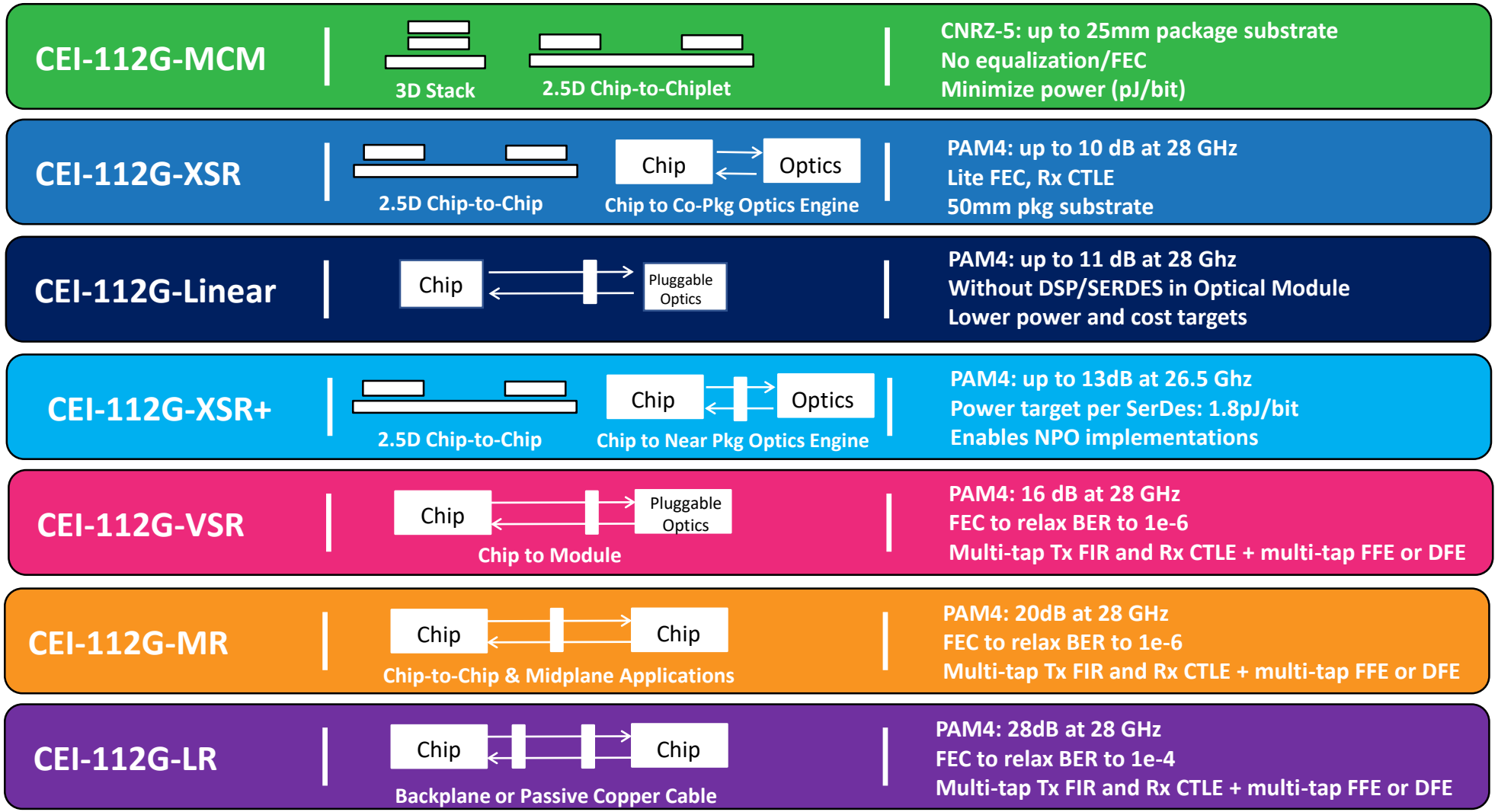
OIF CEI-112G Development Application Space

- PAM4 modulation scheme becomes dominant in OIF CEI-112 Gbps interface IA
- One SerDes core is not able to efficiently cover multiple applications from XSR to LR
- For short reach applications, simpler and lower power equalizations are desired



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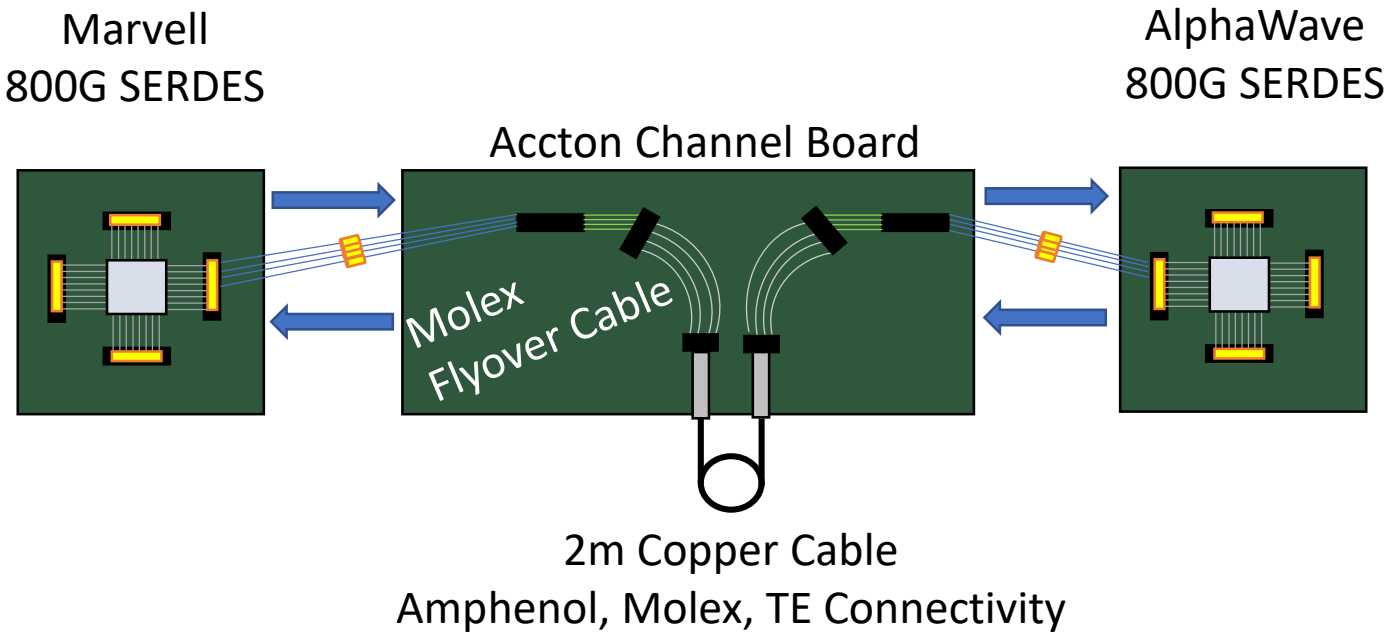
CEI-112G-LR



This interoperability demo consists of multivendor LR silicon transmitting 106.25 Gbps PRBS31Q PAM4 signals over a multivendor LR channel emulating high density 256x100G (25.6T) and 512x100G (51.2T) line card implementations while exceeding the BER target requirements.

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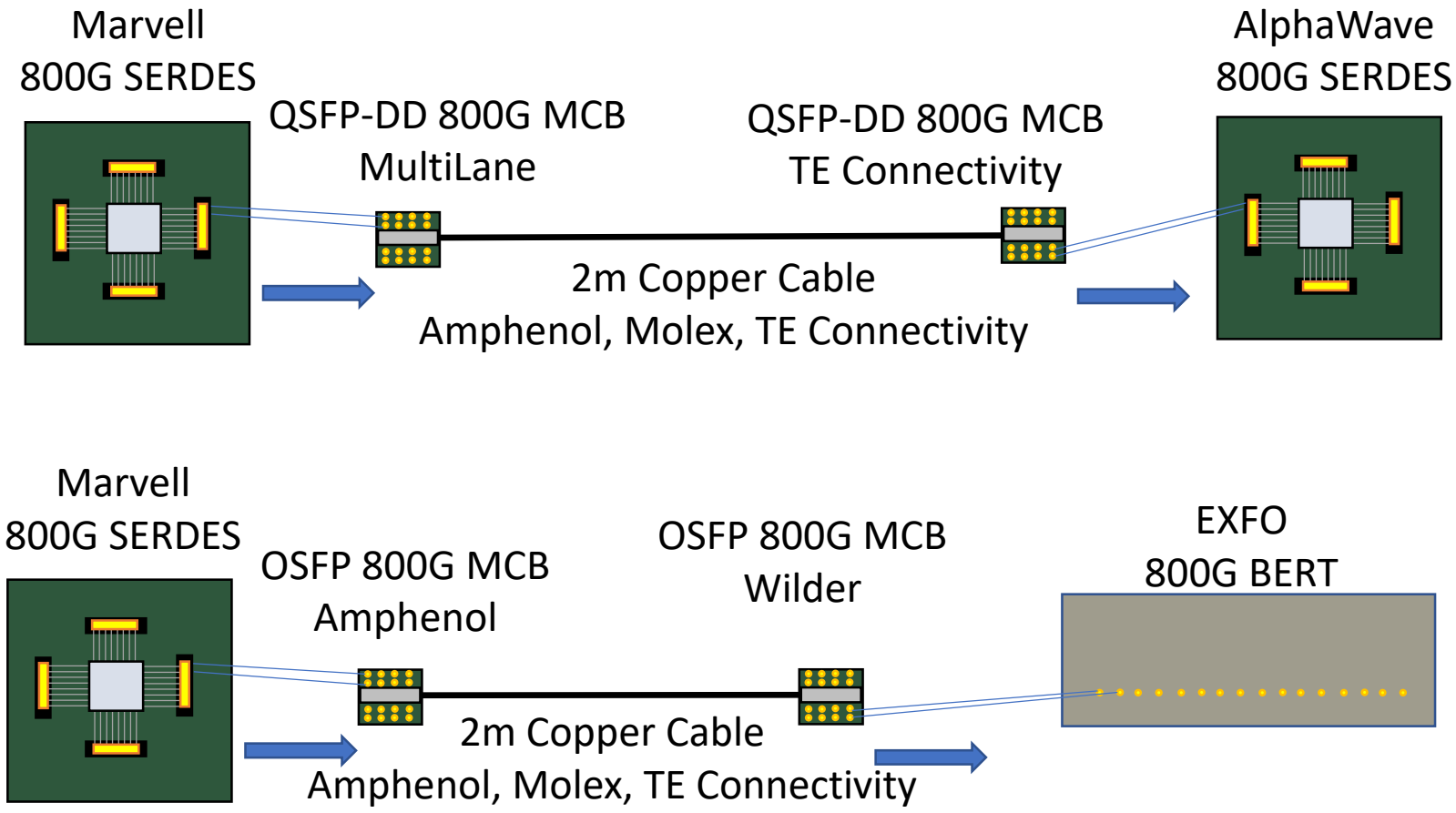
CEI-112G-LR



These interoperability demo's consists of multivendor LR silicon and silicon to test equipment transmitting 106.25 Gbps PRBS31Q PAM4 signals over a 2m Copper Cable and Module Compliance Boards while exceeding the BER target requirements.

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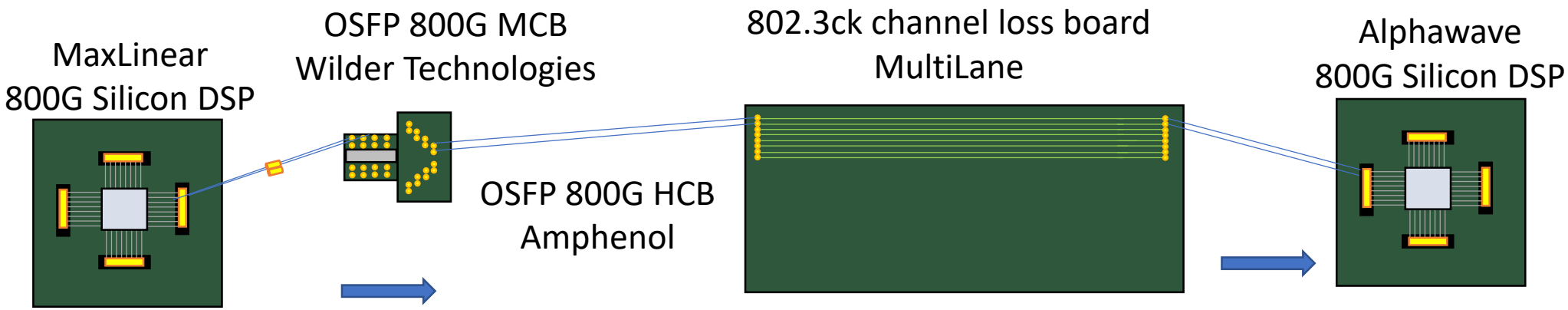
CEI-112G-MR



This interoperability demo consists of multivendor MR silicon transmitting 106.25 Gbps PRBS31Q PAM4 signals over a multivendor MR channel consisting of a mated compliance set of test fixtures and channel loss board at a bit error rate in of 1E-10.

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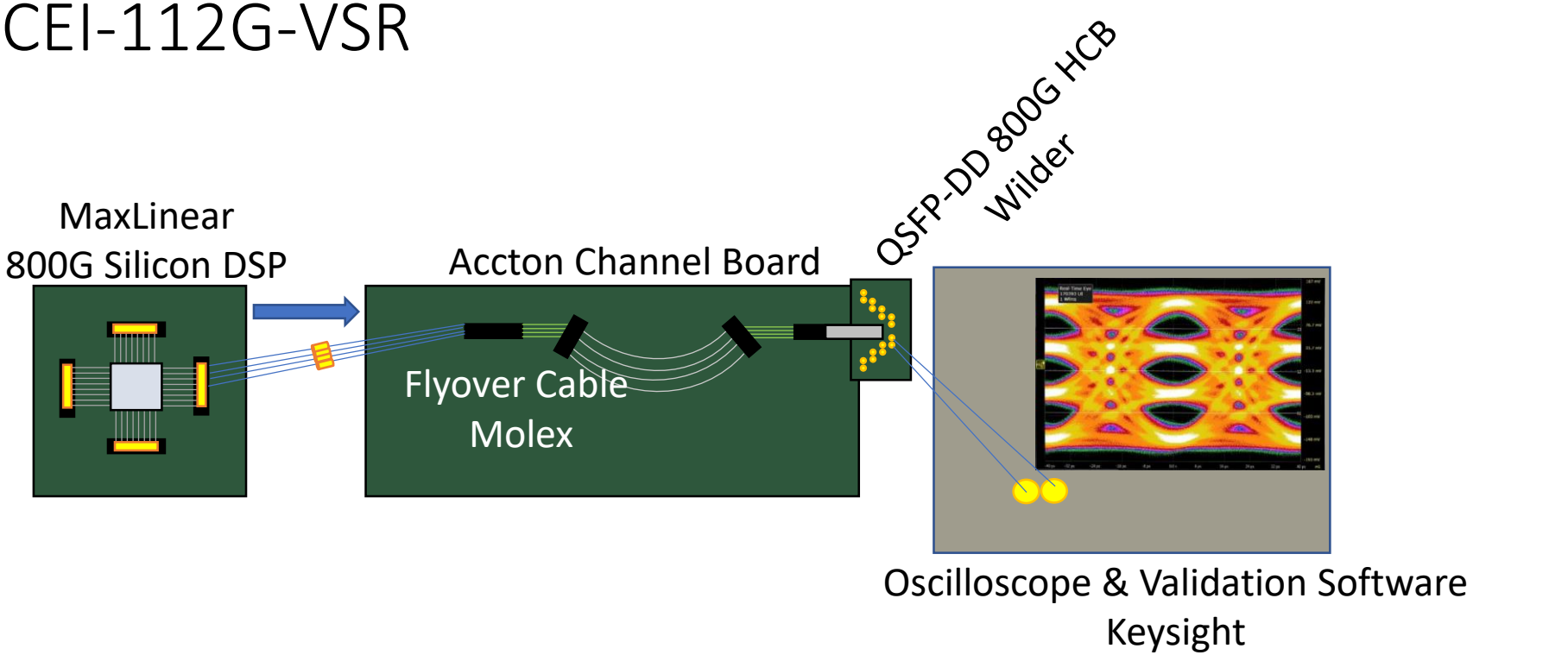
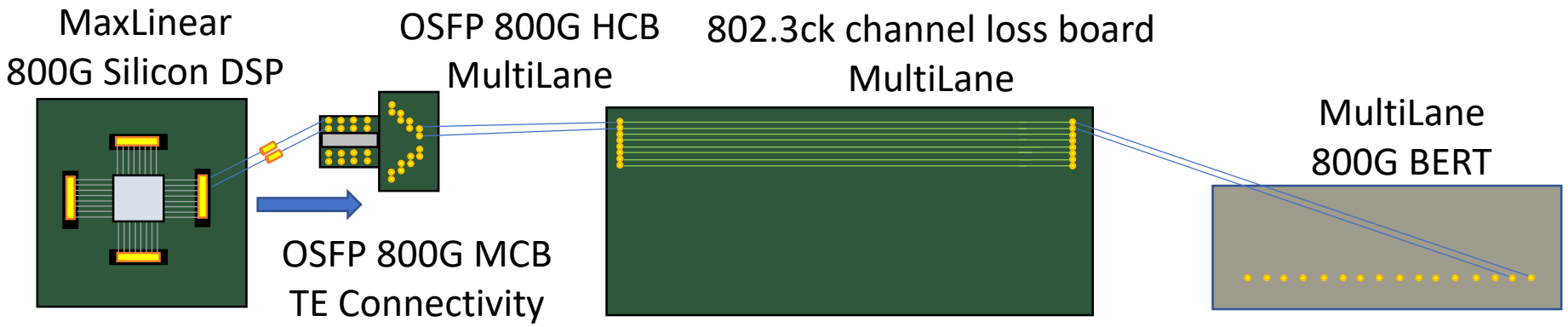
CEI-112G-VSR





This demo uses a DSP/CDR to drive a channel loss emulating high density line card implementations, delivering an eye-opening exceeding target TP1a draft targets.

This demo consists of a single 106.25 Gbps PRBS31Q PAM4 signal being transmitted from silicon traversing a 16dB VSR passive channel terminated by FEC capable test equipment. The VSR channel consists a mated compliance test fixture set and channel loss board. The measured Bit Error Rate is in the 1E-10 range.

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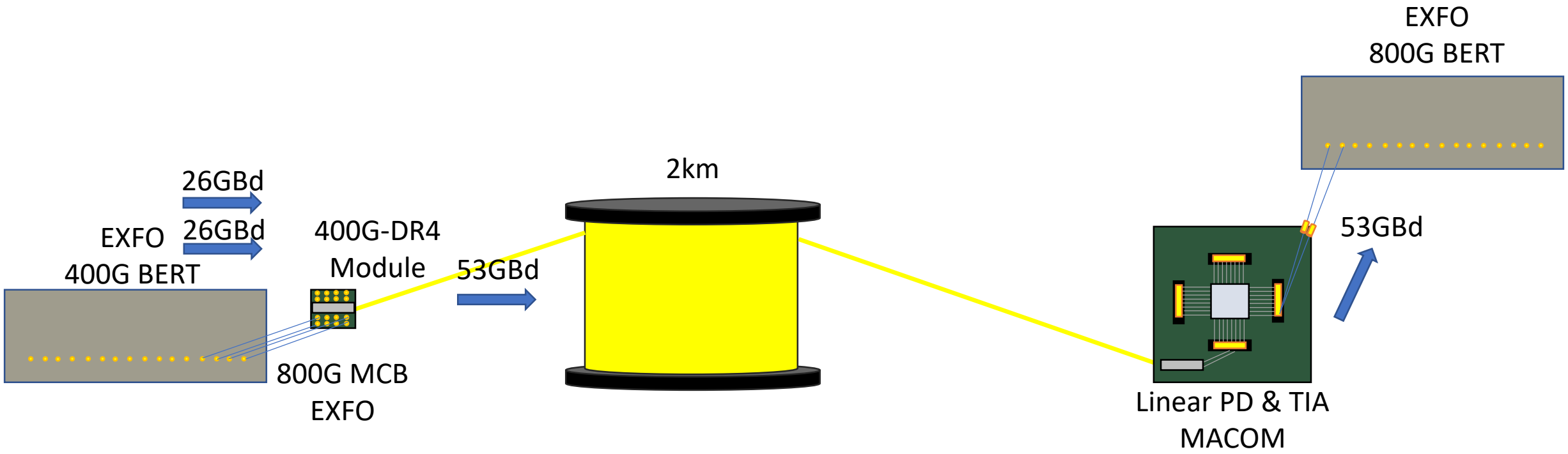
CEI-112G-Linear



This interoperability demo consists of the linear conversion of an optical input from a 400G DR-4 module sent over 2km of SMF to an electrical signal via PD+TIA. The electrical signal is then sent through an OSFP connector to a BERT which integrates receive FFE functionality and achieves a link BER which exceeds standard requirements. There is no discrete DSP in the Rx path before the BERT, saving module power and cost.

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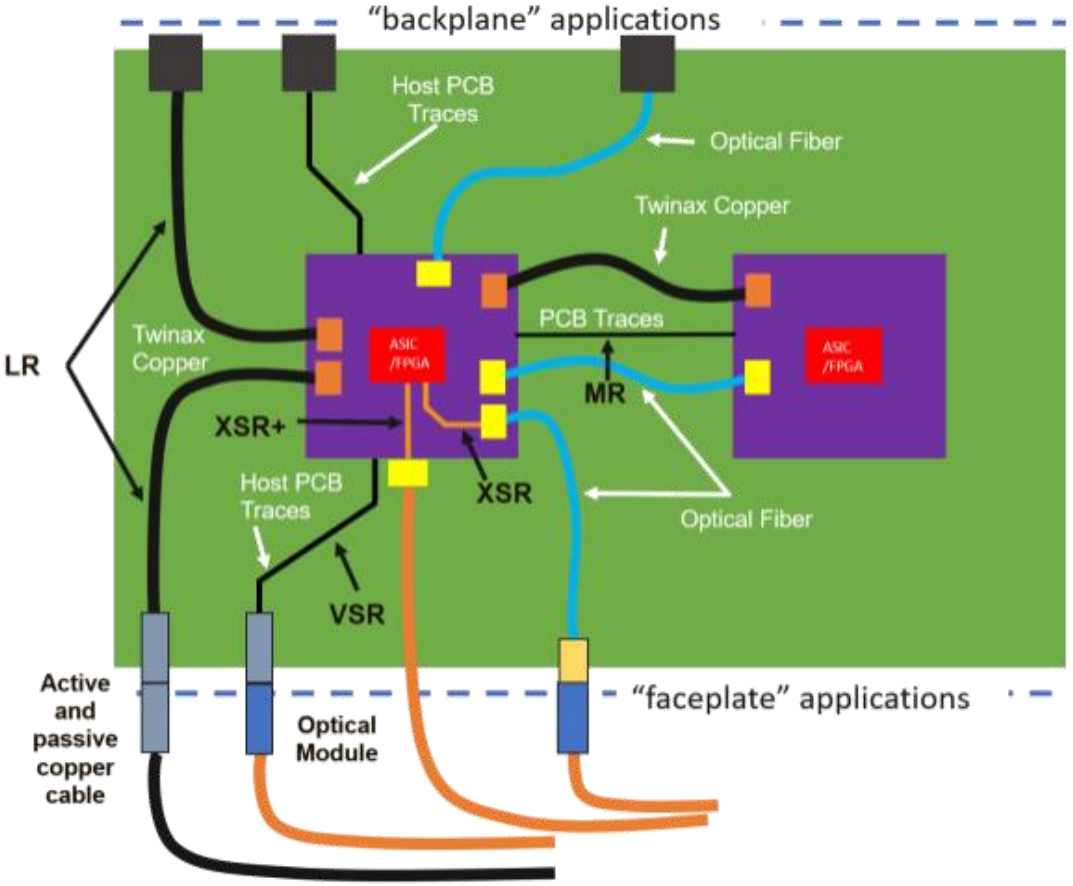
CEI-224G Framework Document

OIF

CONTENTS

- Summarizes the consensus findings and guidance for new OIF CEI-224G projects
- Identifies key technical challenges for next generation systems
  - Power, density, performance, reach and cost
- Defines electrical interconnection applications and discusses some of the interoperability test challenges
- Establishes baseline materials that will enable 1.6/3.2 Tbps rate architectures and lower cost, lower complexity 800G and 400G architectures



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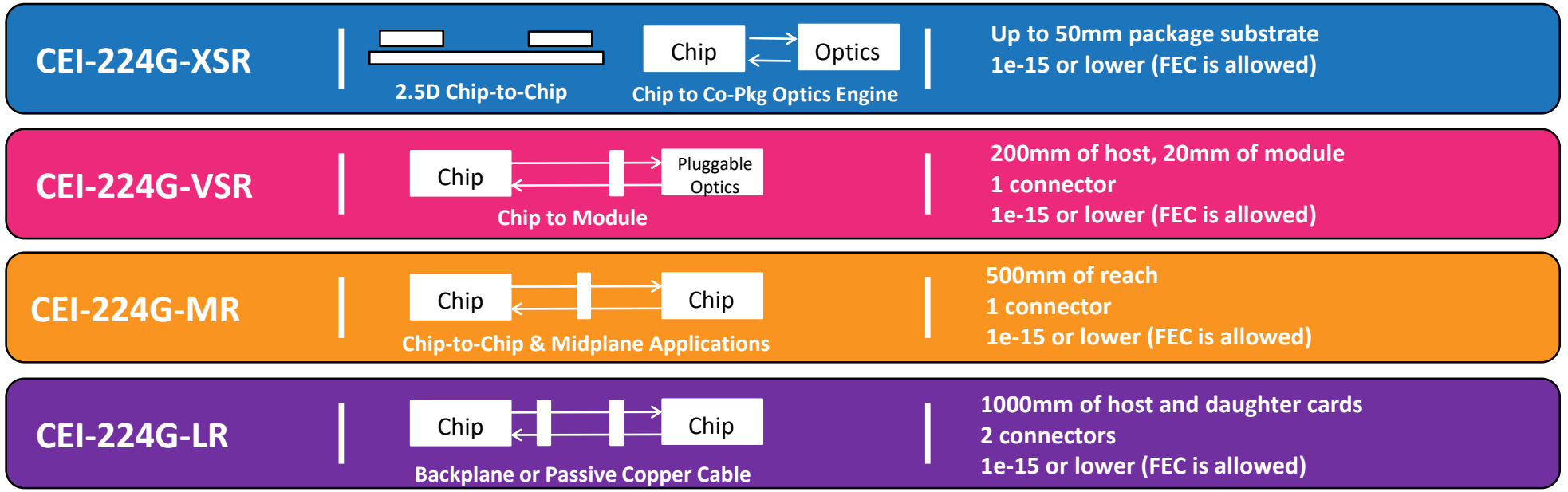
OIF CEI-224G New Project Starts



- New Projects started at OIF Q1 2022 meeting
- One SerDes core might not be able to cover multiple applications from XSR to LR
- For short reach applications, simpler and lower power equalizations are desired

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Participating Members!

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