



CEI-112G and CEI-224G Demos @ OFC 2023

OIF's Common Electrical I/O (CEI) Work Has Been a Significant Industry Contributor

Name	Rate per pair	Year	Activities that Adopted, Adapted or were influenced by the OIF CEI
CEI-224G	224Gbps	202X	Several channel reach projects in progress, kicked off in 2022
CEI-112G	112Gbps	2022	Five channel projects are complete, two channel projects in progress, IEEE, InfiniBand, T11 (Fibre Channel), Interlaken, ITU.
CEI-56G	56Gbps	2017	IEEE, InfiniBand, T11 (Fibre Channel), Interlaken, ITU
CEI-28G	28 Gbps	2012	InfiniBand EDR, 32GFC, SATA 3.2, SAS-4,10GBASE-KR4, CR4, CAUI4, Interlaken, ITU
CEI-11G	11 Gbps	2008	InfiniBand QDR, 10GBASE-KR, 10GFC, 16GFC, SAS-3, RapidIO v3, Interlaken, ITU
CEI-6G	6 Gbps	2004	4GFC, 8GFC, InfiniBand DDR, SATA 3.0, SAS-2, RapidIO v2, HyperTransport 3.1, Interlaken, ITU
SxI5	3.125 Gbps	2002-3	Interlaken, FC 2G, InfiniBand SDR, XAUI, 10GBASE-KX4, 10GBASE-CX4, SATA 2.0, SAS-1, RapidIO v1, ITU
SPI4, SFI4	1.6 Gbps	2001-2	SPI-4.2, HyperTransport 1.03

OIF CEI-112G Development Application Space

- PAM4 modulation scheme becomes dominant in OIF CEI-112 Gbps interface IA
- One SerDes core is not able to efficiently cover multiple applications from XSR to LR
- For short reach applications, simpler and lower power equalizations are desired

CEI-112G-MCM	<p>3D Stack 2.5D Chip-to-Chiplet</p>	CNRZ-5: up to 25mm package substrate No equalization/FEC Minimize power (pJ/bit)	✓
CEI-112G-XSR	<p>2.5D Chip-to-Chip Chip to Co-Pkg Optics Engine</p>	PAM4: up to 50mm package substrate 6-10 dB at 28GHz Lite FEC, Rx CTLE	✓
CEI-112G-XSR+	<p>2.5D Chip-to-Chip Chip to Near Pkg Optics Engine</p>	PAM4: up to 13dB at 26.5 Ghz Power target per SerDes: 1.8pJ/bit Enables NPO implementations	
CEI-112G-VSR	<p>Chip to Module</p>	PAM4: 12-16 dB at 28GHz FEC to relax BER to 1e-6 Multi-tap Tx FIR and Rx CTLE + multi-tap FFE or DFE	✓
CEI-112G-MR	<p>Chip-to-Chip & Midplane Applications</p>	PAM4: 20dB at 28GHz FEC to relax BER to 1e-6 Multi-tap Tx FIR and Rx CTLE + multi-tap FFE or DFE	✓
CEI-112G-LR	<p>Backplane or Passive Copper Cable</p>	PAM4: 28-30dB at 28GHz FEC to relax BER to 1e-4 Multi-tap Tx FIR and Rx CTLE + multi-tap FFE or DFE	✓
CEI-112G-Linear	<p>Chip to Pluggable Optics</p>	PAM4: up to 11 dB at 28 Ghz Without DSP/SERDES in Optical Module Lower power and cost targets	

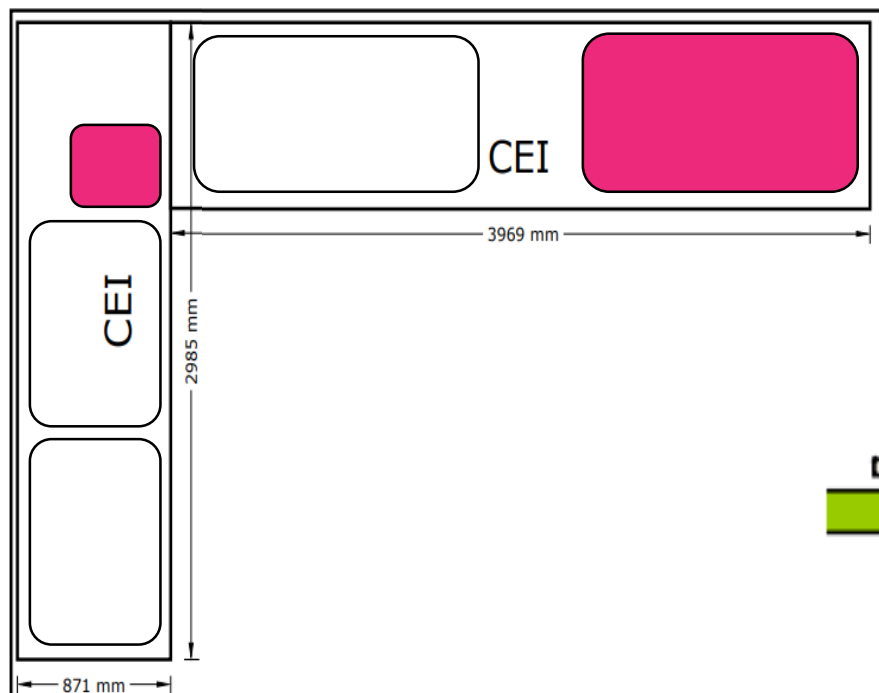
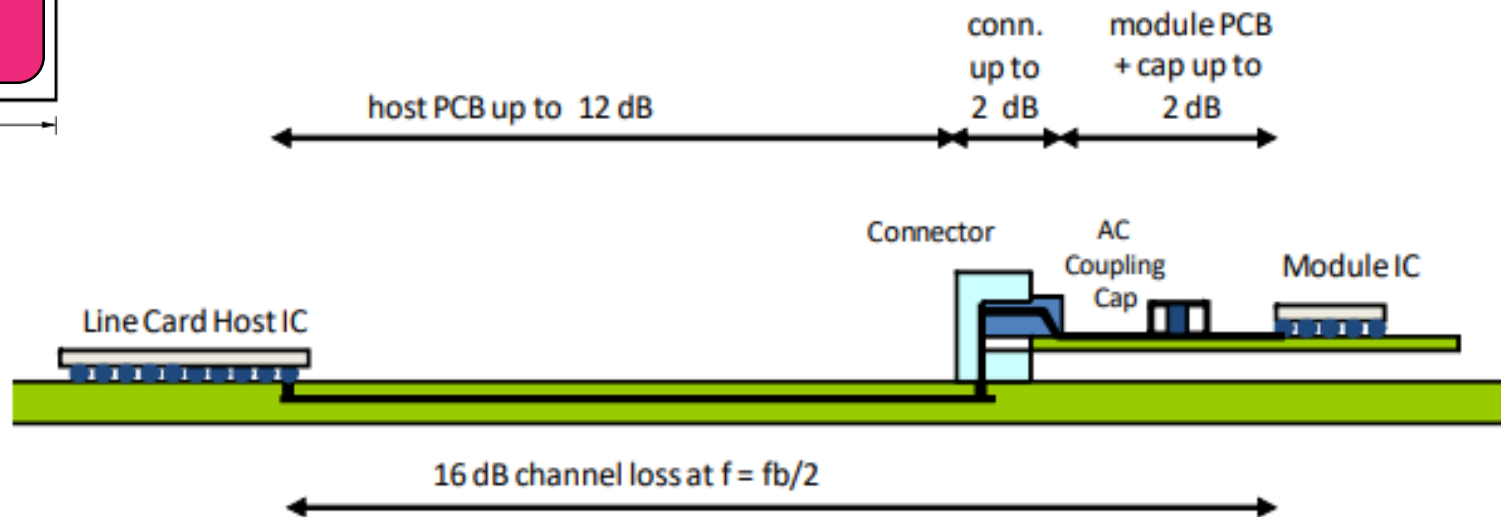


Figure 23-21. CEI-112G-VSR-PAM4 PCB Channel Reference Model



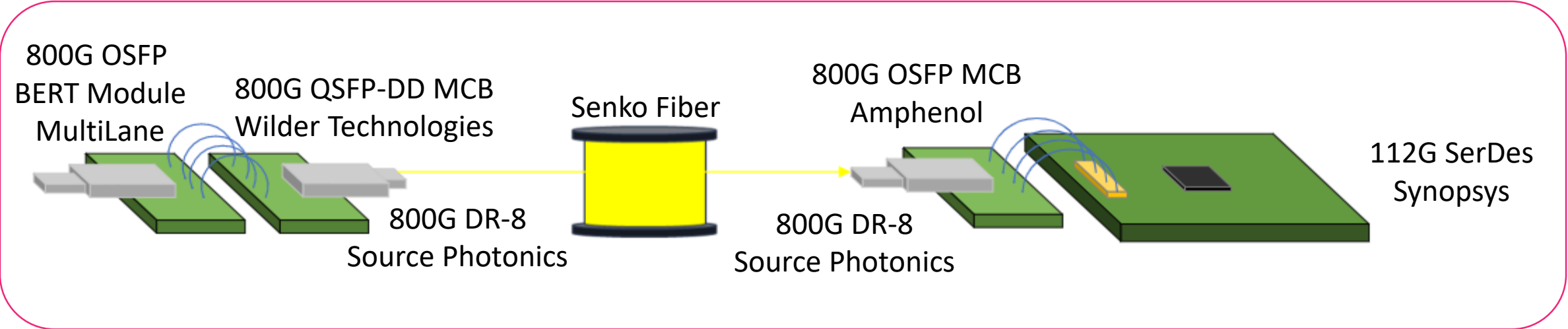
CEI-112G-VSR



PAM4: 12-16 dB at 28GHz
 FEC to relax BER to 1e-6
 Multi-tap Tx FIR and Rx CTLE + multi-tap FFE or DFE

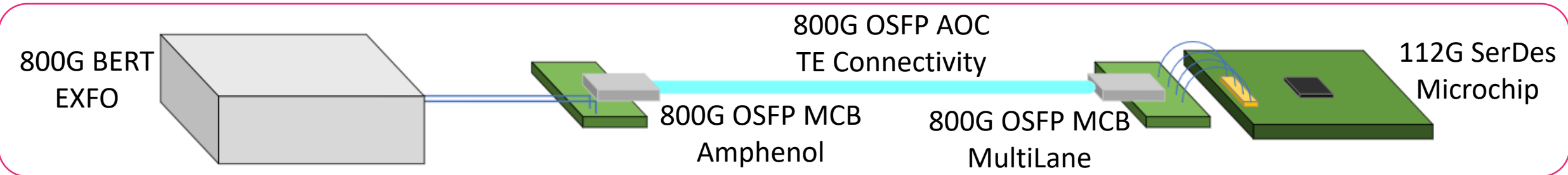
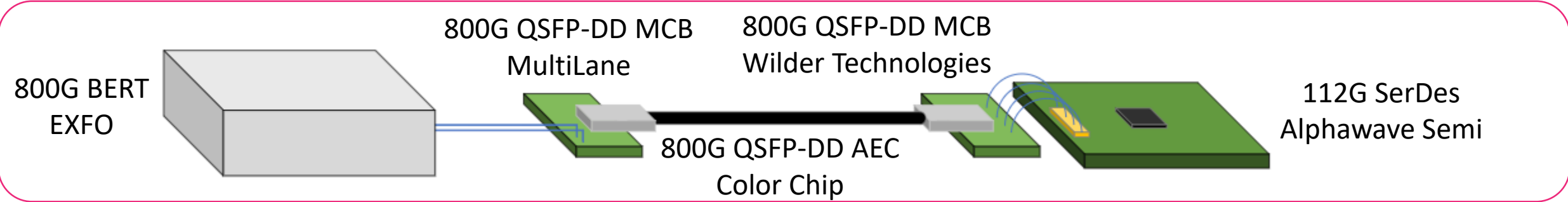
CEI-112G-VSR at OFC 2023

This demo consists of an 800G BERT transmitting a 106.25Gbps PRBS31Q PAM4 signal to an 800Gbps QSFP-DD DR8 optical module mated to a CMIS capable QSFP-DD800 module compliance board interoperating over single mode fiber with another OSFP800 mated-DR8 optical module and mated compliance board ultimately being terminated by a 112G SerDes evaluation platform board.



CEI-112G-VSR at OFC 2023

Re-timers are becoming more present in interconnects to extend their reach. This demonstration consists of an 800G BERT transmitting a 106.25Gbps PRBS31Q PAM4 signal to an 800Gbps QSFP-DD Active Electrical Cable (AEC) mated to QSFP-DD module compliance boards and terminated by a 112G SerDes evaluation board, extending the reach of copper cabling >2m while keeping BER low (1E-9).



This demo consists of an 800G BERT transmitting a 106.25Gbps PRBS31Q PAM4 signal to an 800Gbps OSFP Active Optical Cable (AOC) mated to module compliance boards ultimately being terminated by a 112G SerDes evaluation board, allowing for an even longer reach interconnect.

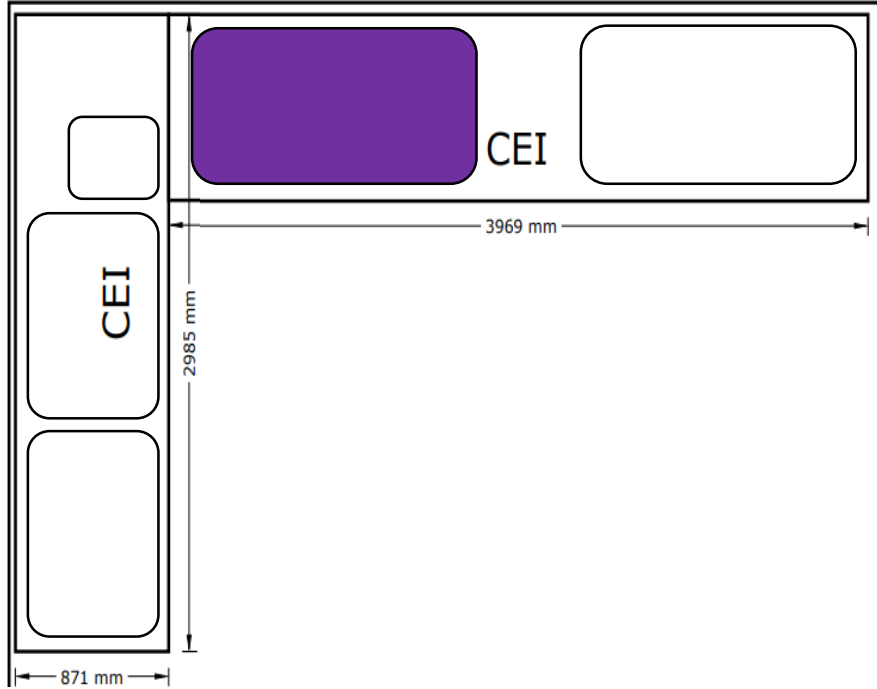
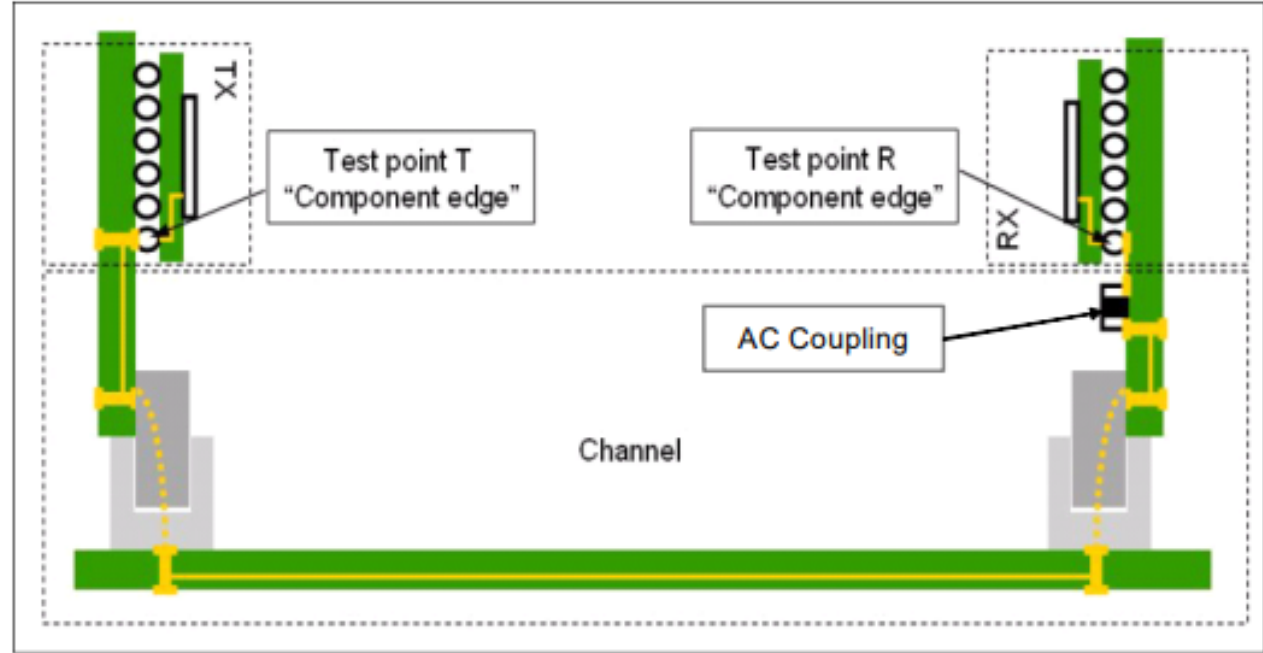


Figure 28-1.CEI-112G-LR-PAM4 Reference Model

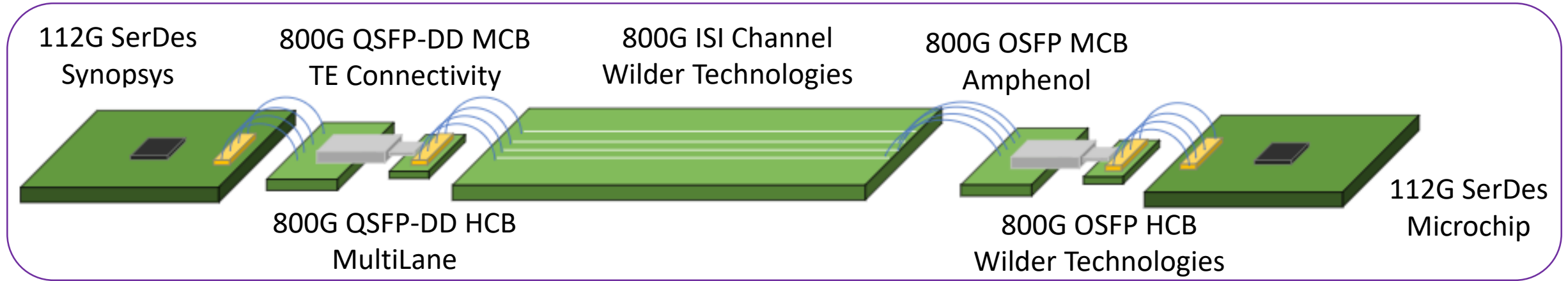


CEI-112G-LR



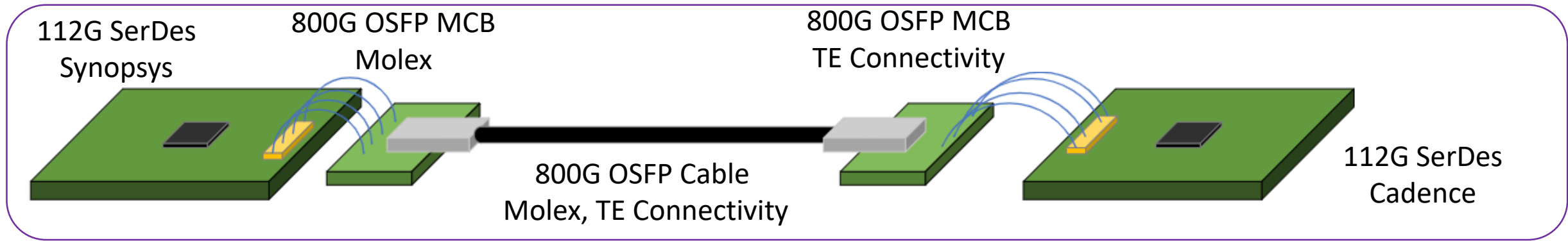
PAM4: 28-30dB at 28GHz
 FEC to relax BER to 1e-4
 Multi-tap Tx FIR and Rx CTLE + multi-tap FFE or DFE

CEI-112G-LR at OFC 2023



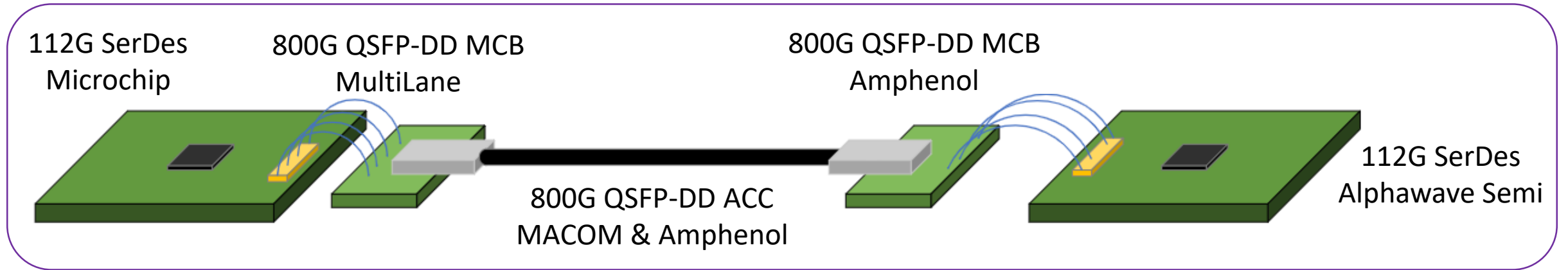
This interoperability demo consists of multivendor LR silicon transmitting 106.25 Gbps PRBS31Q PAM4 signals over a multivendor LR channel consisting of a mated compliance set of test fixtures and channel loss board while exceeding the bit error rate target.

CEI-112G-LR at OFC 2023



This interoperability demo consists of multi-vendor LR-capable silicon transmitting and receiving PRBS31Q traffic at 106.25Gbps PAM4 over a multi-vendor 33.5dB LR loss channel, including a 2m OSFP passive copper cable channel and module compliance boards while exceeding the LR Link BER spec requirements

CEI-112G-LR at OFC 2023



These long reach interoperability demonstrations consist of multivendor LR silicon bi-directional traffic at 106.25 Gbps PRBS31QAM PAM4 signals over Active Copper Cables (ACC), extending the reach compared to passive copper cables, while consuming lower power than retimed active electrical cables. Behaving similarly to LR channels, the insertion loss is >36 dB while BER is well below specification, 1E-9.

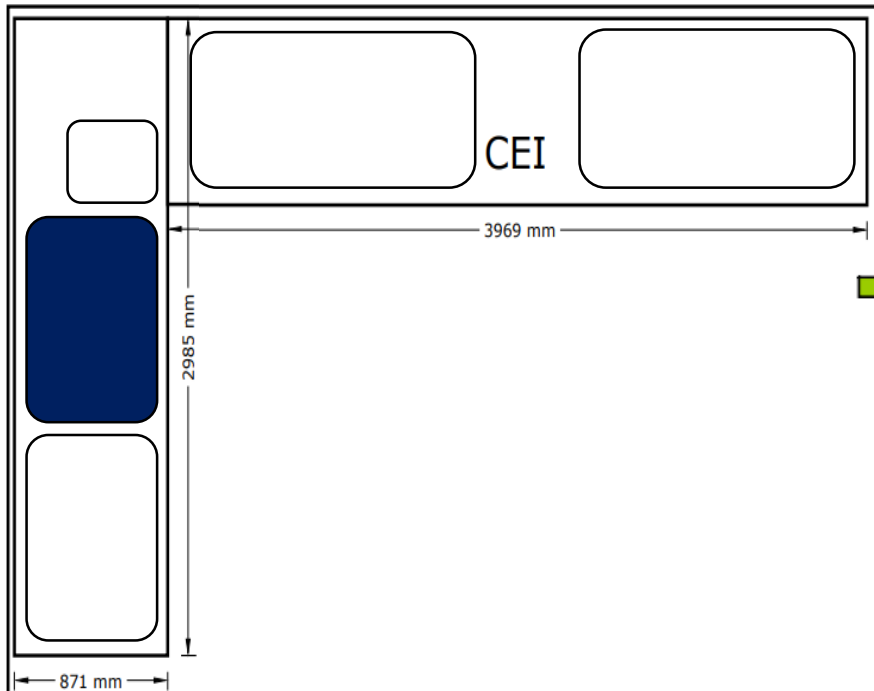


Figure 23-18. CEI-112G-LINEAR-PAM4 PCB Channel Reference Model

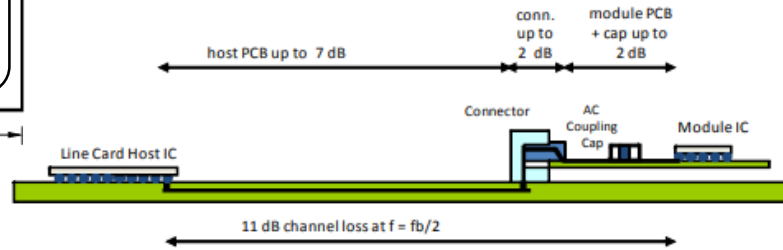


Figure 23-19. CEI-112G-LINEAR-PAM4 Cabled Channel Reference Model

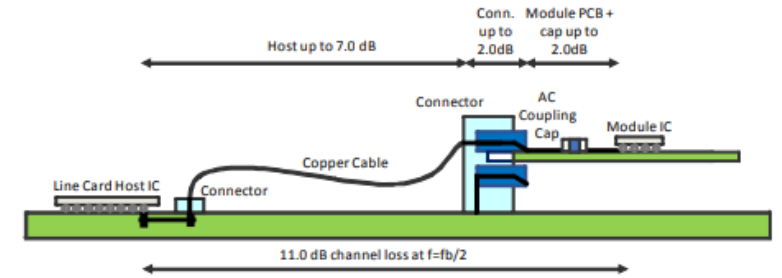


Figure 23-21. CEI-112G-LINEAR-PAM4 Co-Packaged Optics Channel Reference Model

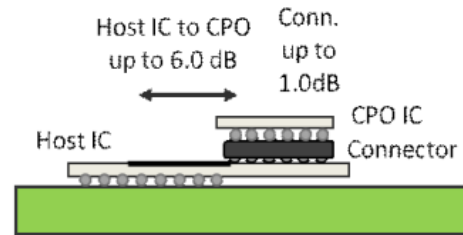
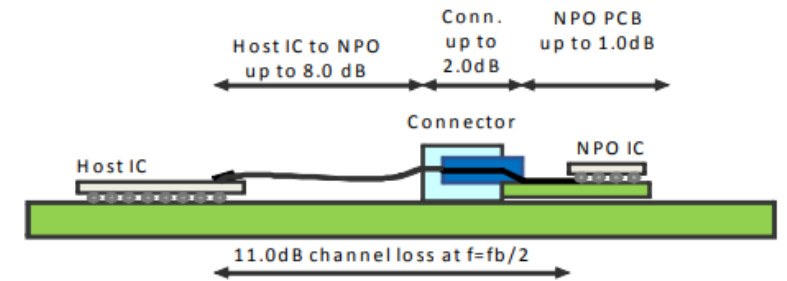


Figure 23-20. CEI-112G-LINEAR-PAM4 Near Package Optics Channel Reference Model

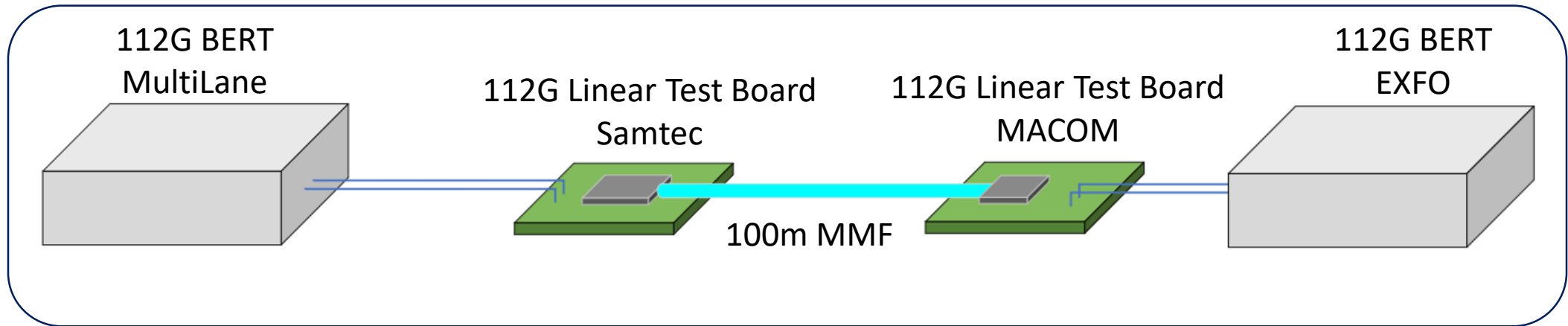


CEI-112G-Linear



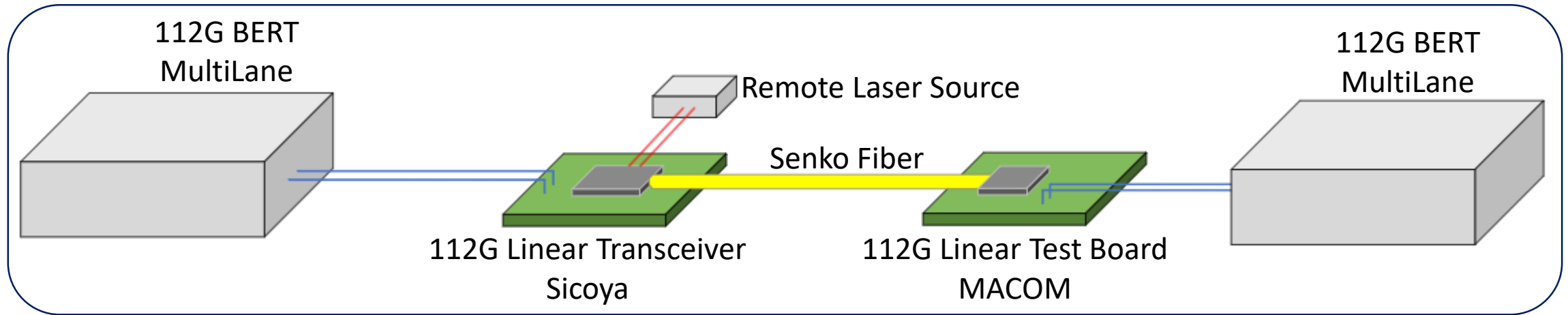
PAM4: up to 11 dB at 28 Ghz
 Without DSP/SERDES in Optical Module
 Lower power and cost targets

CEI-112G-Linear at OFC 2023



This interoperability demo consists of multi-vendor Linear Test boards driven and terminated by LR-capable BERTs, subsequently converted and transmitted over 100m of multimode fiber optically and converted back into an electrical signal. The BERT on the far end integrates receive FFE functionality and achieves a link BER which exceeds standard requirements. There is no discrete DSP in the receive path before the BERT, saving module power and cost.

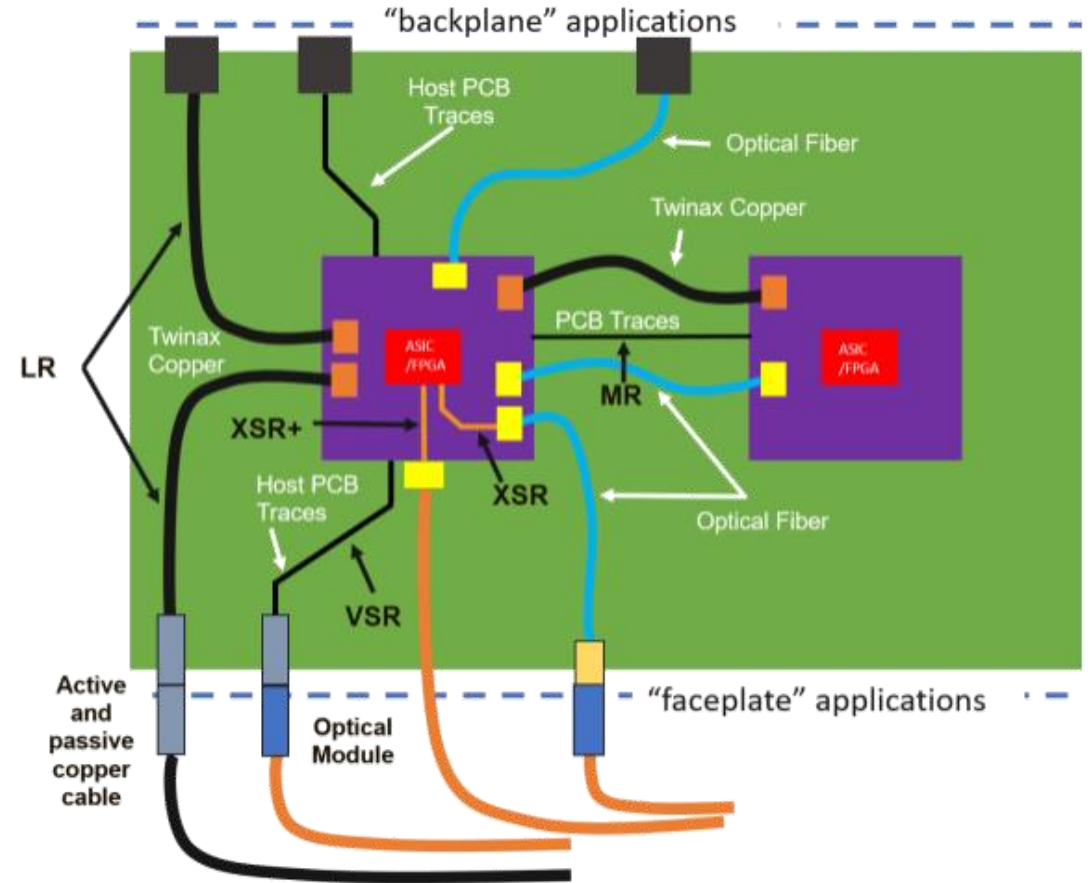
CEI-112G-Linear at OFC 2023



This interoperability demo consists of a 112G co-packaged optical engine driven by a remotely sourced laser transmitting an optical signal across single mode fiber to an electrical signal Linear test board via PD+TIA. The electrical signal is then sent to a BERT which integrates receive FFE functionality and achieves a link BER which exceeds standard requirements. There is no discrete DSP device in the Rx path before the BERT, reducing module power and cost.

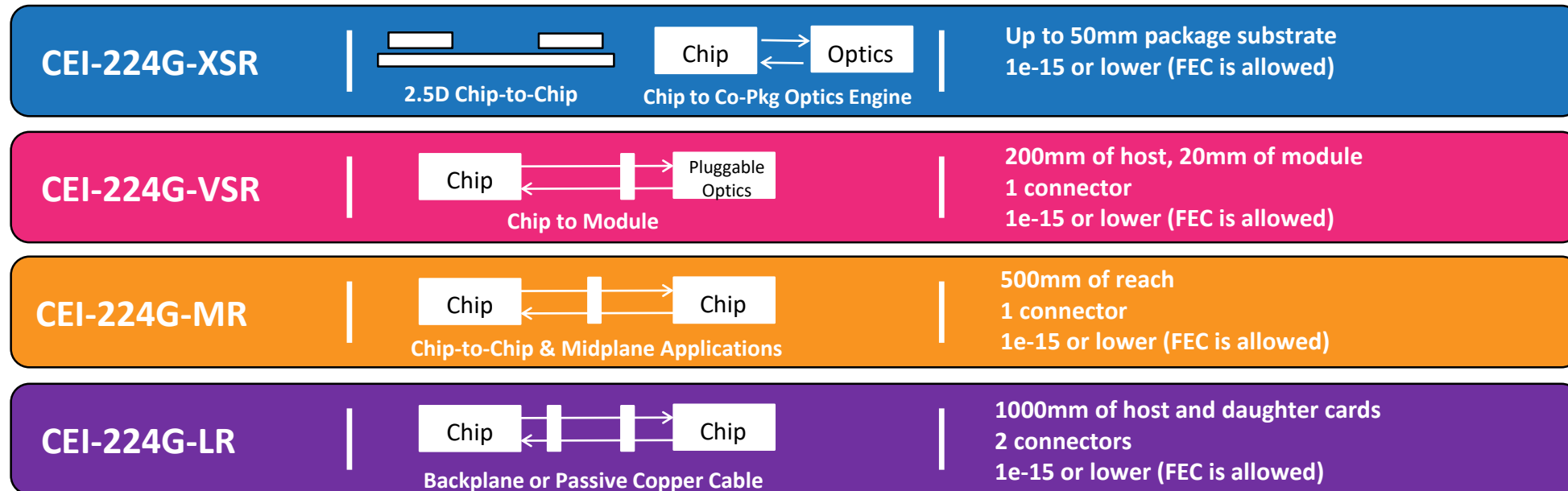
OIF	
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- Summarizes the consensus findings and guidance for new OIF CEI-224G projects
- Identifies key technical challenges for next generation systems
 - Power, density, performance, reach and cost
- Defines electrical interconnection applications and discusses some of the interoperability test challenges
- Establishes baseline materials that will enable 1.6/3.2 Tbps rate architectures and lower cost, lower complexity 800G and 400G architectures



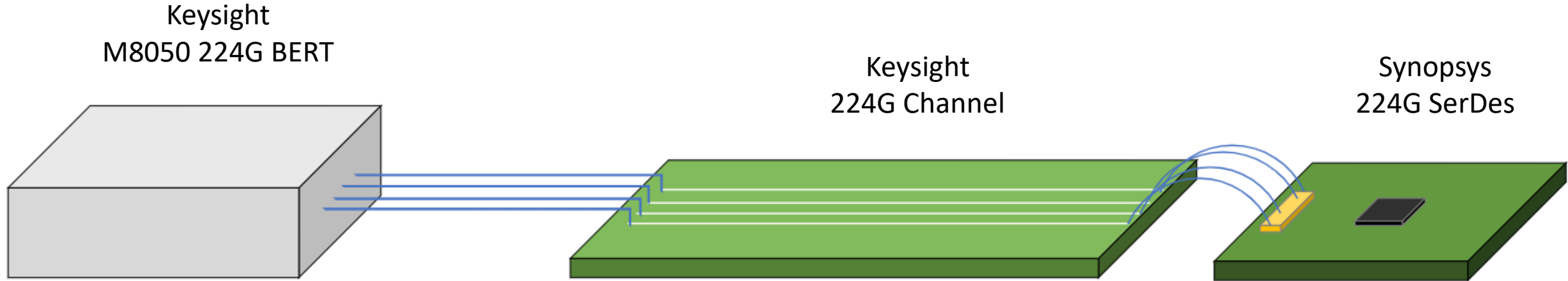
OIF-FD-CEI-224G-01.0 published in February 2022

OIF CEI-224G New Project Starts



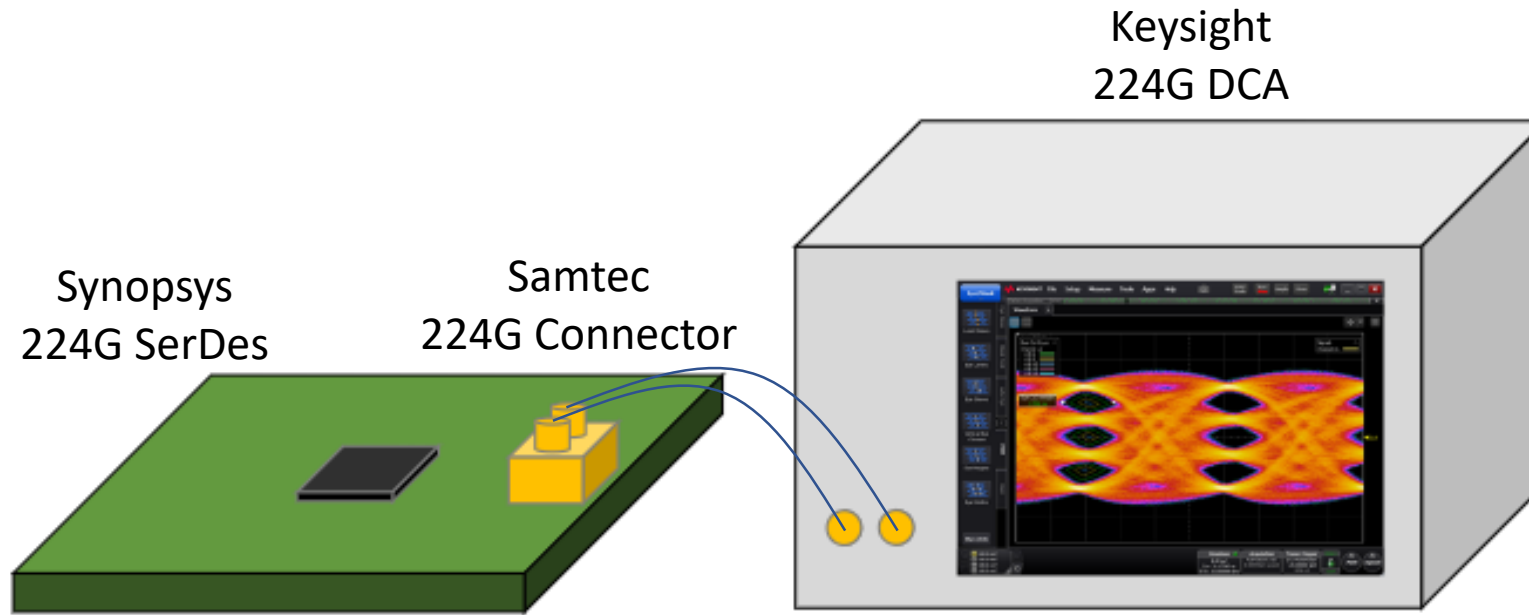
- New Projects started at OIF Q1 2022 meeting
- One SerDes core might not be able to cover multiple applications from XSR to LR
- For short reach applications, simpler and lower power equalizations are desired

CEI-224G-LR at OFC 2023



This demonstration is an operational showcase of 224G LR PHY (112GBd PAM4) from Synopsys being driven by a Keysight M8050 Bit Error Ratio Tester (BERT), through a high bandwidth (120GHz) 1mm based ISI board modeling OIF CEI-LR package and channel losses.

CEI-224G-LR at OFC 2023



This demonstration is an operational showcase of 224G LR PHY (112GBd PAM4) transmit from Synopsys terminated into a Keysight 224G DCA.

CEI Participating Members





OIF

PLL INTEROP DEMO
OFC 2023



Scan for demo info



Wednesday March 8th

"Bringing Order to Chaos – OIF"

3pm-4pm in Theater 3

Moderator: **Stephen Hardy**, *Lightwave*

Panelists:

Karl Gass, OIF PLL WG Optical Vice Chair

Vladimir Kozlov, LightCounting

Sterling Perrin, Heavy Reading;

Nathan Tracy, OIF MA&E Co-Chair PLL, TE Connectivity

Alan Weckel, 650 Group

Celebration Reception

4pm-5pm

Booth #5101