

OIF

OIF PLL Interoperability Demo CEI-112G

ECOC 2022

19-21 September 2022

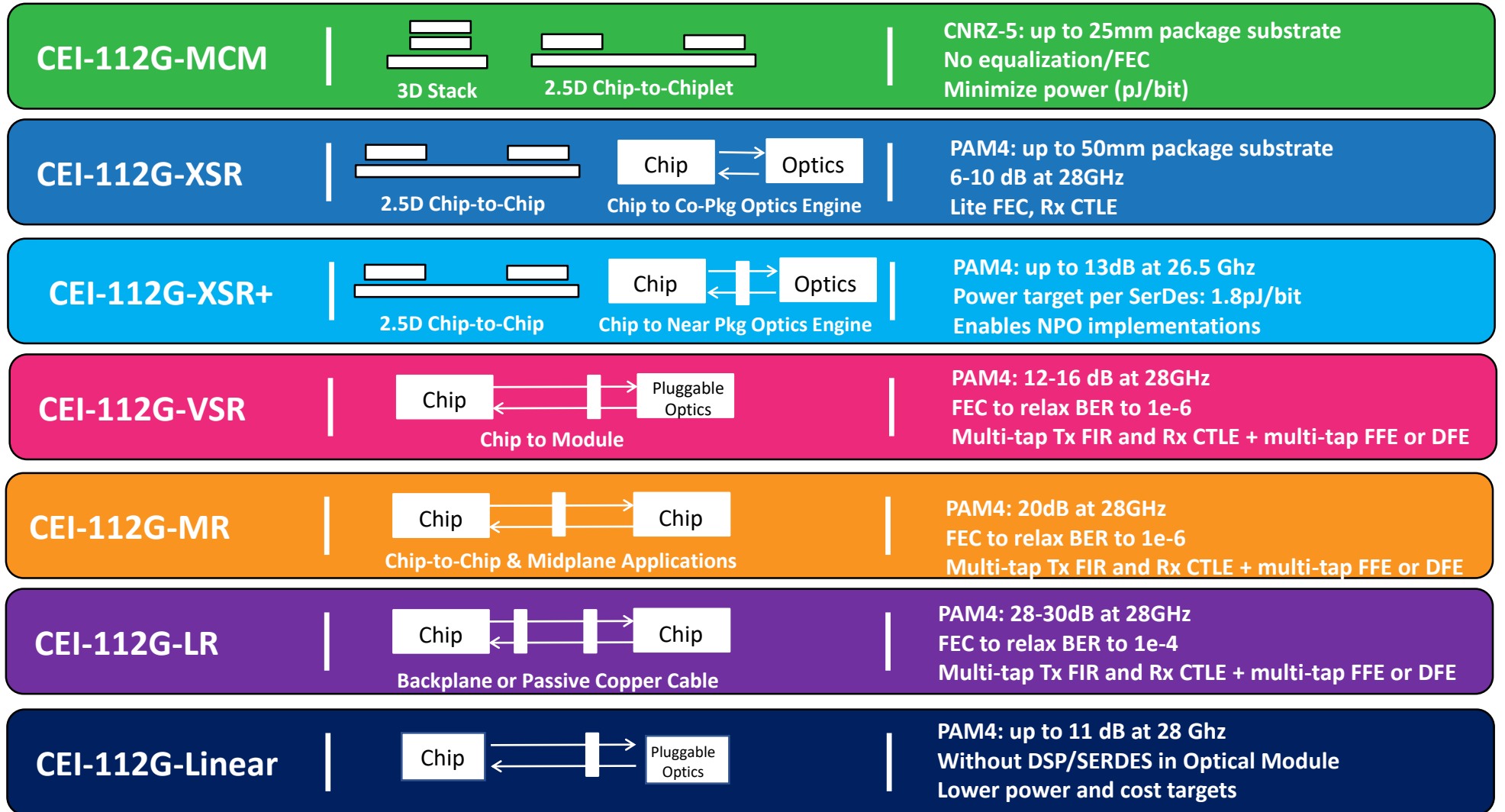
Basel, Switzerland

OIF's Common Electrical I/O (CEI) Work Has Been a Significant Industry Contributor

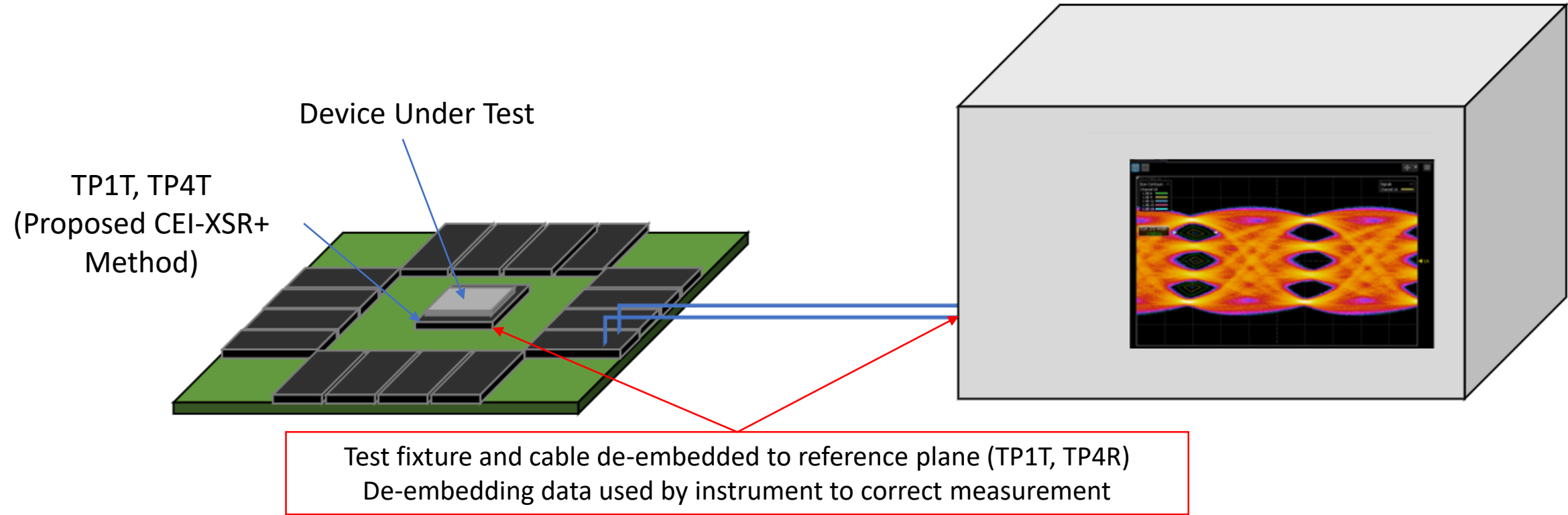
Name	Rate per pair	Year	Activities that Adopted, Adapted or were influenced by the OIF CEI
CEI-112G	112Gbps	2022	Seven channel reach projects in progress, IEEE, InfiniBand, T11 (Fibre Channel), Interlaken, ITU.
CEI-56G	56Gbps	2017	IEEE, InfiniBand, T11 (Fibre Channel), Interlaken, ITU
CEI-28G	28 Gbps	2012	InfiniBand EDR, 32GFC, SATA 3.2, SAS-4, 10GBASE-KR4, CR4, CAUI4, Interlaken, ITU
CEI-11G	11 Gbps	2008	InfiniBand QDR, 10GBASE-KR, 10GFC, 16GFC, SAS-3, RapidIO v3, Interlaken, ITU
CEI-6G	6 Gbps	2004	4GFC, 8GFC, InfiniBand DDR, SATA 3.0, SAS-2, RapidIO v2, HyperTransport 3.1, Interlaken, ITU
SxI5	3.125 Gbps	2002-3	Interlaken, FC 2G, InfiniBand SDR, XAUI, 10GBASE-KX4, 10GBASE-CX4, SATA 2.0, SAS-1, RapidIO v1, ITU
SPI4, SFI4	1.6 Gbps	2001-2	SPI-4.2, HyperTransport 1.03
SPI3, SFI3	0.800 Gbps	2000	(from PL3)

OIF CEI-112G Development Application Space

- PAM4 modulation scheme becomes dominant in OIF CEI-112 Gbps interface IA
- One SerDes core is not able to efficiently cover multiple applications from XSR to LR
- For short reach applications, simpler and lower power equalizations are desired



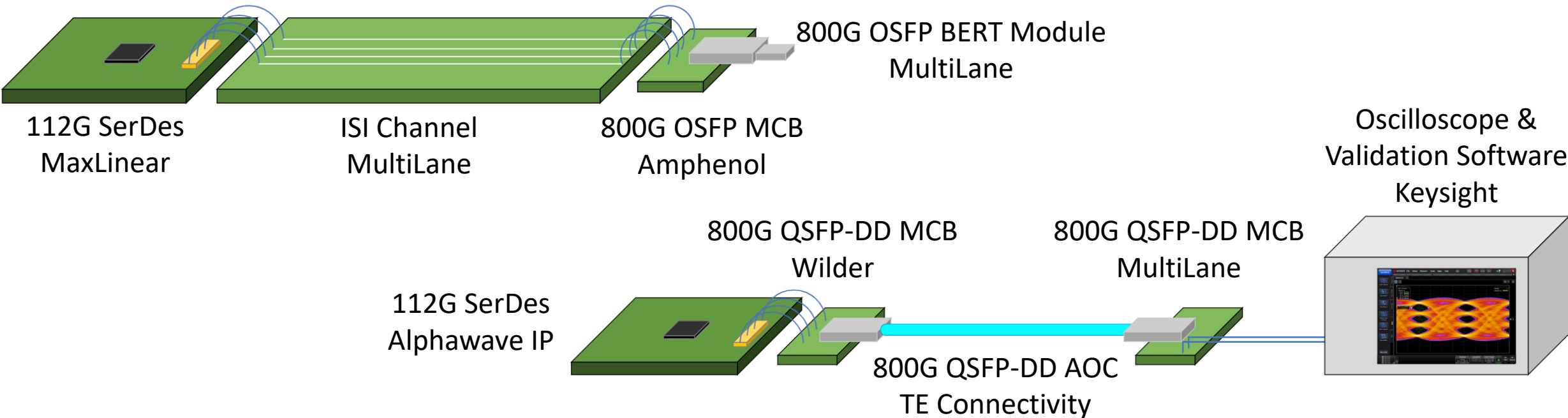
CEI-112G-XSR+ at ECOC 2022



This static display shows a proposed compliance test methodology for applications such as XSR and XSR+ where high bandwidth use cases such as 3.2Tbps for co-packaging can create challenges to traditional compliance methodology. The proposed approach will use Module and Host compliance fixtures similar to those used with CEI-VSR front panel pluggable optics today, but de-embeds the fixture losses to the prescribed test points at the module connector mating plane. This approach is still under OIF member consideration.

CEI-112G-VSR at ECOC 2022

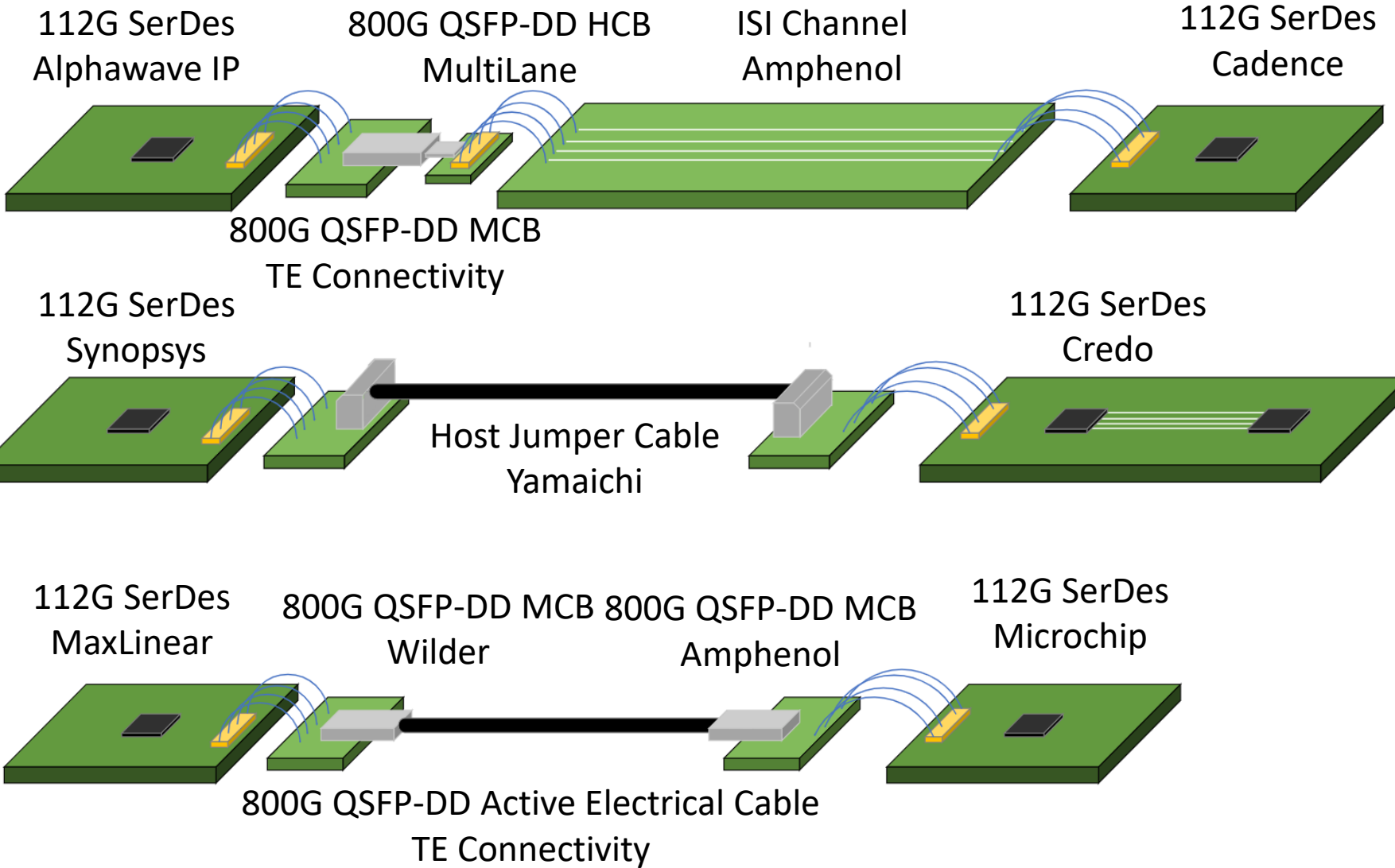
This demo consists of two silicon solutions exchanging bi-directional PRBS31Q traffic at 106.25Gbps PAM4 over full VSR loss paths. The evaluation board is connected to an ISI channel board, which is subsequently routed to an OSFP112 module compliance board, ending with an Active Loopback module, with both nodes reporting live BER.



This demo consists of a 112G silicon chip evaluation board transmitting a 106.25Gbps PRBS31Q PAM4 signal to a CMIS controlled 800Gbps QSFP-DD active optical cable (AOC) mated to a CMIS capable QSFP-DD module compliance board ultimately interconnected to a high-speed oscilloscope showing the resultant eye diagram after equalization.



CEI-112G-MR at ECOC 2022

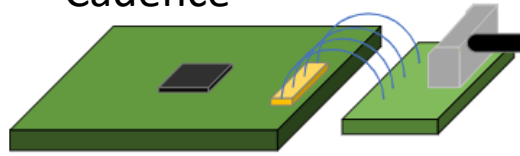


These medium reach interoperability demonstrations consist of multivendor silicon transmitting 106.25 Gbps PRBS31QAM PAM4 signals over an array of channels, from multivendor mated test fixtures, cabled host channels, ISI channels, and active electrical cables. A retimer configuration is also on display, enabling an XSR link on the SerDes board with two instances of functional silicon.

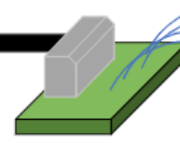


CEI-112G-LR at ECOC 2022

112G SerDes
Cadence



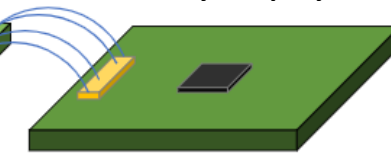
Cabled Backplane
TE Connectivity



ISI Channel
MultiLane



112G SerDes
Synopsys

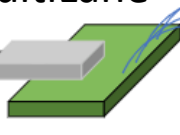


112G SerDes
Microchip



3.5m Active Copper Cable
Amphenol

QSFP-DD 800G MCB
MultiLane



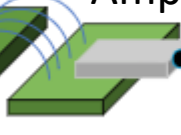
112G SerDes
Alphawave IP



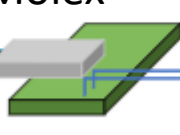
112G SerDes
Microchip



OSFP 800G MCB
Amphenol



OSFP 800G MCB
Molex



2m Copper Cable

Amphenol, Molex, TE Connectivity

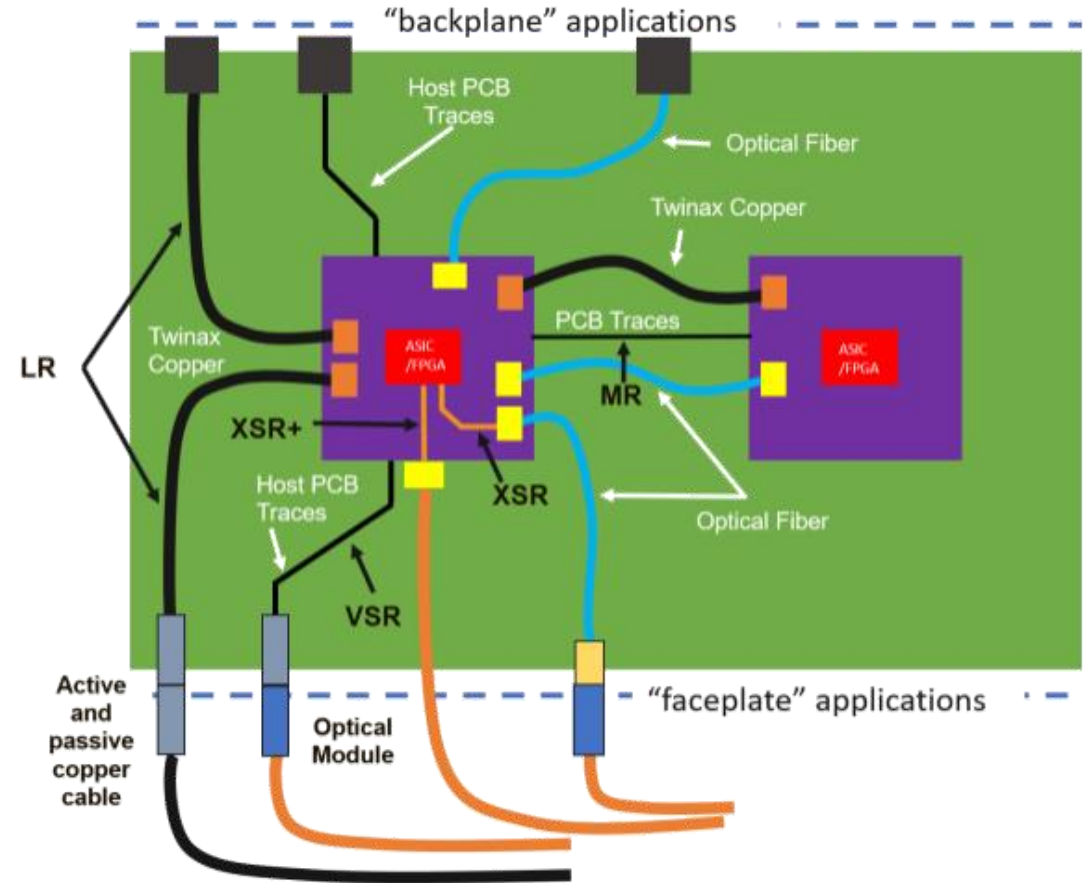
800G BERT
EXFO



These long reach interoperability demonstrations consist of multivendor LR silicon and silicon to test equipment transmitting 106.25 Gbps PRBS31QAM PAM4 signals over an array of channels, from passive copper OSFP cables, cabled backplanes, ISI channels, and active copper cables extending the reach of the link to at least 3.5m.

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- Summarizes the consensus findings and guidance for new OIF CEI-224G projects
- Identifies key technical challenges for next generation systems
 - Power, density, performance, reach and cost
- Defines electrical interconnection applications and discusses some of the interoperability test challenges
- Establishes baseline materials that will enable 1.6/3.2 Tbps rate architectures and lower cost, lower complexity 800G and 400G architectures



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