OIF
PLL INTEROP DEMO
OFC 2024

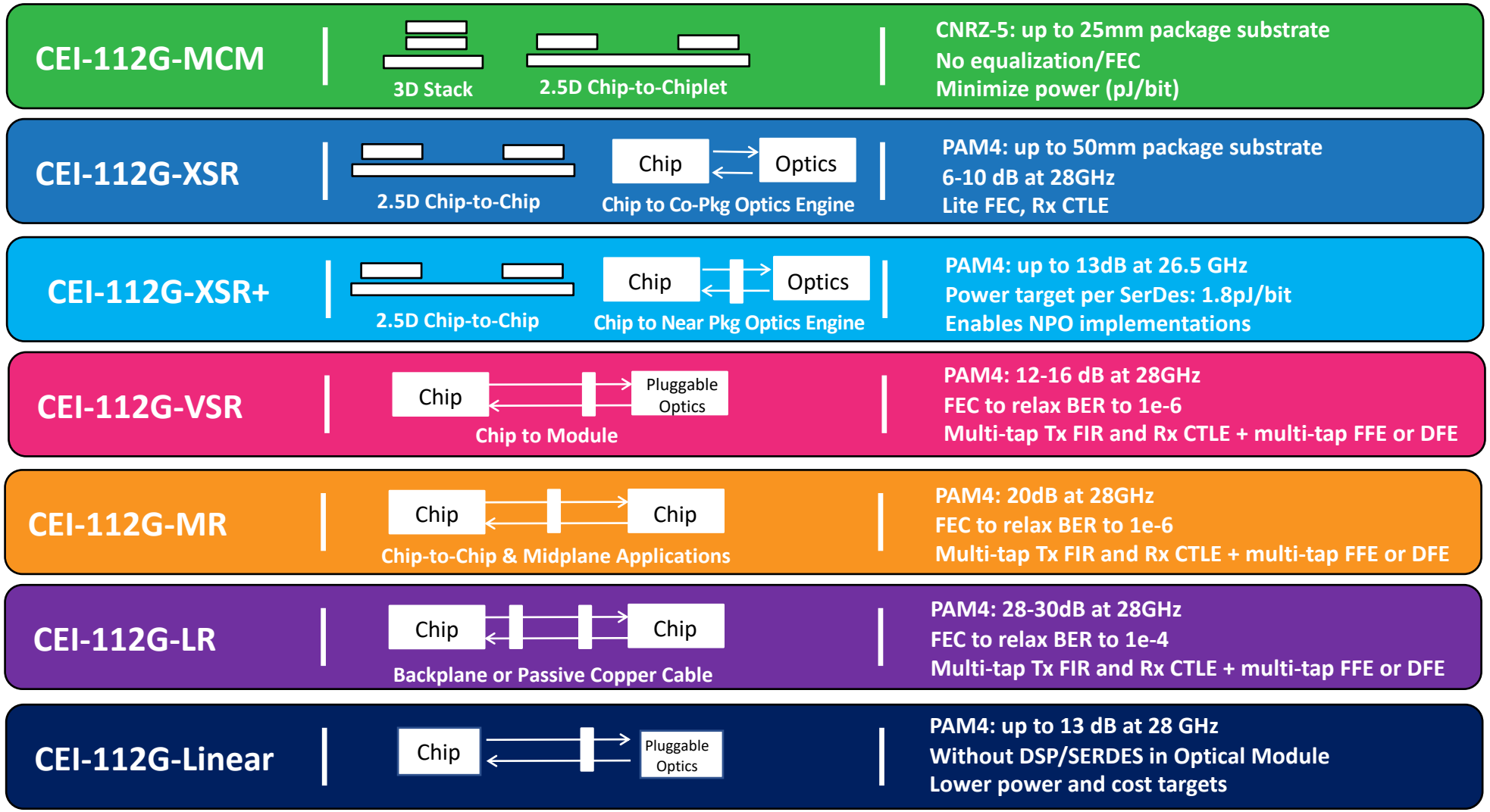
OIF Physical & Link Layer Common Electrical Interface (CEI) Interoperability Demo at OFC 2024

OIF's Common Electrical I/O (CEI) Work Has Been a Significant Industry Contributor

Name	Rate per pair	Year	Activities that Adopted, Adapted or were influenced by the OIF CEI
CEI-224G	224Gbps	202X	Several channel reach projects in progress, kicked off in 2022
CEI-112G	112Gbps	2022	Five channel projects are complete, two channel projects in progress, IEEE, InfiniBand, T11 (Fibre Channel), Interlaken, ITU.
CEI-56G	56Gbps	2017	IEEE, InfiniBand, T11 (Fibre Channel), Interlaken, ITU
CEI-28G	28 Gbps	2012	InfiniBand EDR, 32GFC, SATA 3.2, SAS-4,100GBASE-KR4, CR4, CAUI4, Interlaken, ITU
CEI-11G	11 Gbps	2008	InfiniBand QDR, 10GBASE-KR, 10GFC, 16GFC, SAS-3, RapidIO v3, Interlaken, ITU
CEI-6G	6 Gbps	2004	4GFC, 8GFC, InfiniBand DDR, SATA 3.0, SAS-2, RapidIO v2, HyperTransport 3.1, Interlaken, ITU
SxI5	3.125 Gbps	2002-3	Interlaken, FC 2G, InfiniBand SDR, XAUI, 10GBASE-KX4, 10GBASE-CX4, SATA 2.0, SAS-1, RapidIO v1, ITU
SPI4, SFI4	1.6 Gbps	2001-2	SPI-4.2, HyperTransport 1.03

OIF CEI-112G Development Application Space

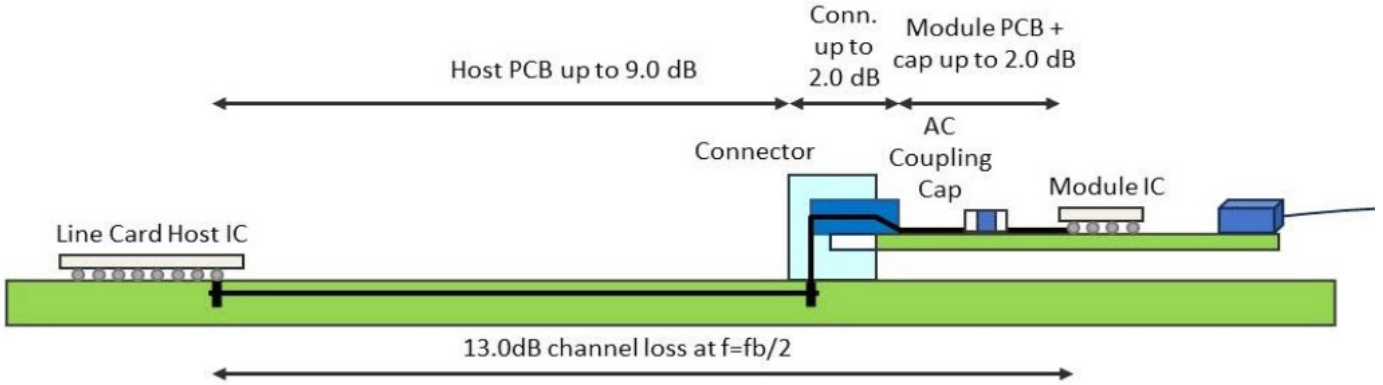
- PAM4 modulation scheme becomes dominant in OIF CEI-112 Gbps interface IA
- One SerDes core is not able to efficiently cover multiple applications from XSR to LR
- For short reach applications, simpler and lower power equalizations are desired

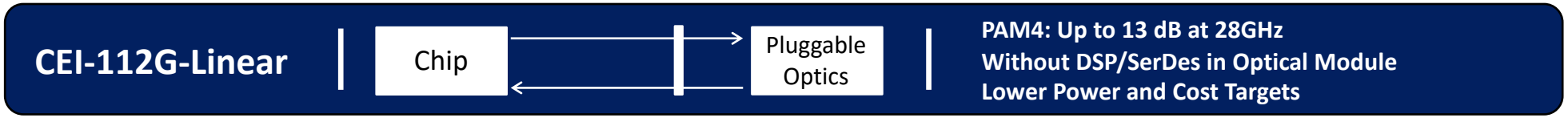


CEI-112G-Linear at OFC 2024

Advantages of Linear Pluggable Optics (LPO):

- Lower Power (up to 50% module power consumption savings compared to traditional retimed modules)
- Lower Latency
- Protocol Agnostic
- Keeps sideband functionality / manageability
- Orders of magnitude of BER margin
- Electrical specification (EECQ) alignment with optical specification (TDECQ)

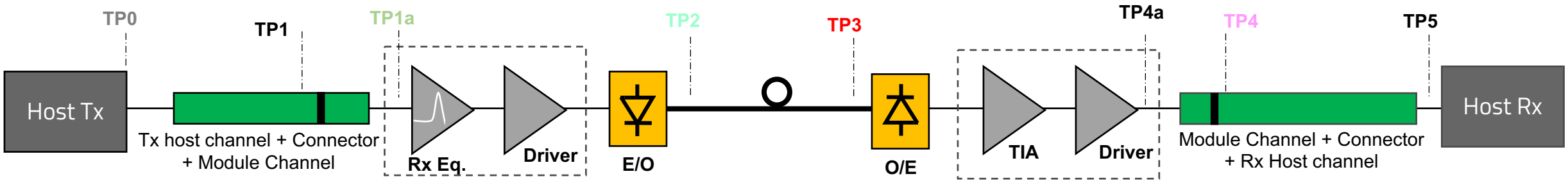




CEI-112G-Linear Test Point Data Driving Interop Results

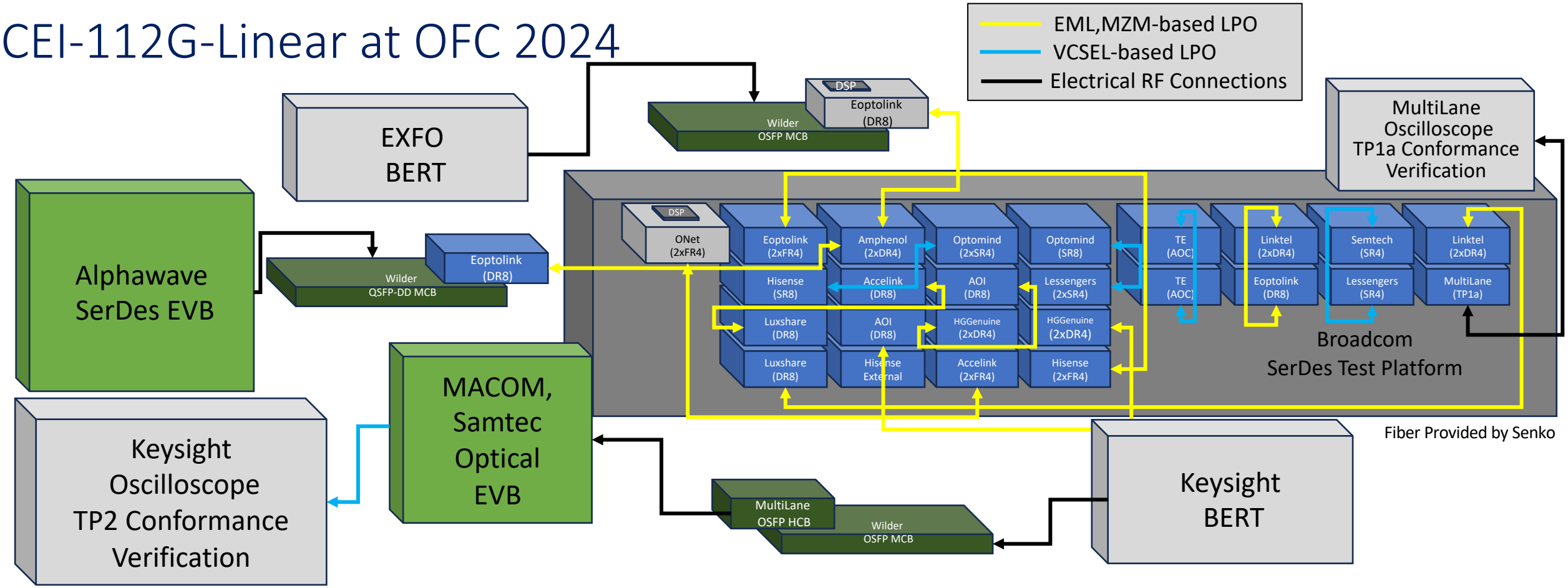
OIF-CEI-Linear Interop results showing key Linear electro/optic test points of a conformant Low Power Optical (LPO)

Generator Output			Channel			TP1a (per CEI-112G-Linear-PAM4)				TP2 (per 802.3db)			TP4 (per CEI-112G-Linear-PAM4)				
Signaling Rate	Pattern	Differential Amplitude	OSFP 112G Fixture		MTF+ Cables Insertion Loss	VMA	EECQ	Ceq	Total Tx Insertion Loss	OMA	TDECQ	Ceq	VMA	EECQ	Ceq	Differential Voltage (D1A)	Linearity RLM
GBd		mV pp	MCB	HCB	dB	mV	dB	dB	dB	dBm	dB	dB	mV	dB	dB	pk-pk	%
53.125	PRBS13Q	500	Wilder TX1	Multilane TX1	7.24	210	1.8	0.02	10.24	1.473	2.62	0.19	349	6.54	0.94	569	0.91
53.125	PRBS13Q	500	Wilder TX1	Multilane TX1	10.2	217	1.62	0.1	13.2	1.5	2.8	1.07	359	6.8	1.1	566	0.91
53.125	PRBS13Q	500	Wilder TX1	Multilane TX1	10.2	217	1.62	0.1	13.2	1.5	2.8	1.07	391	4.04	1.21	551	0.95
53.125	PRBS13Q	500	Wilder TX1	Multilane TX1	13.2	226	1.44	-0.18	16.2	0.78	3.59	1.57	408	5.42	2.44	561	0.95
53.125	PRBS13Q	500	Wilder TX1	Multilane TX1	13.2	226	1.44	-0.18	16.2	0.78	3.59	1.57	447	3.98	4.08	552	0.95



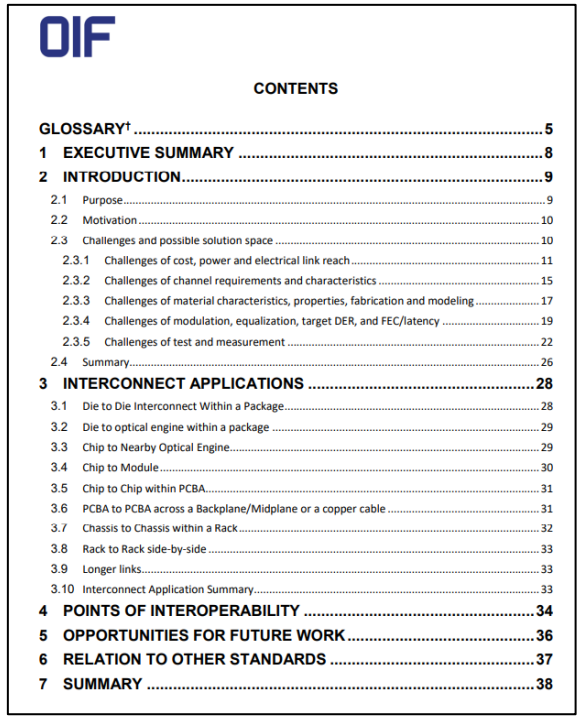
CEI-112G-Linear System Diagram

CEI-112G-Linear at OFC 2024



This demonstration encompasses the entire ecosystem enabling multi-vendor CEI-Linear interoperability. Multi-vendor SerDes represented by test platforms emulating Ethernet devices such as a switch and a test and measurement device drive single mode and multi-mode, multi-form factor and multi-vendor Linear Pluggable Optics (LPO's) while demonstrating quality BER with FEC tail margin, at minimal power consumption. Test and measurement equipment provide conformance verification and insight on compliance into stages of the link. Interoperability between LPOs interfacing with retimed modules is also achieved showcasing compatibility between the two pluggable options.

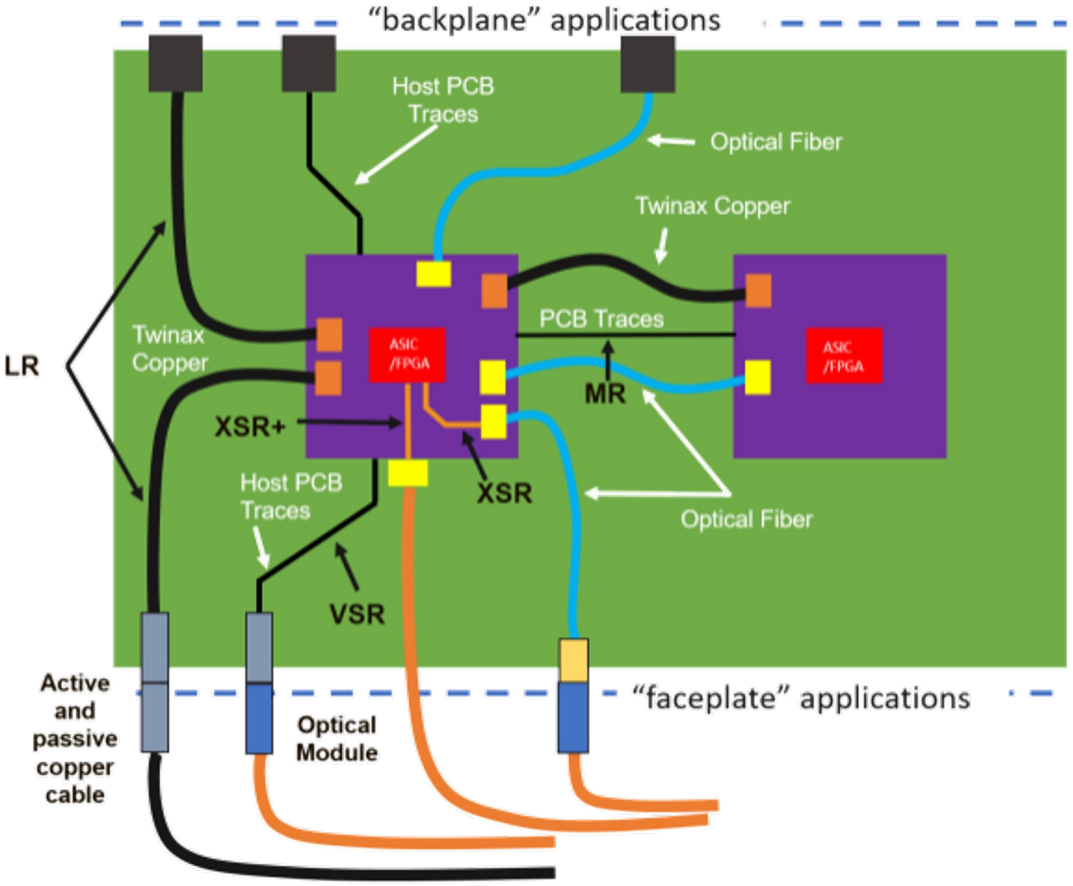
CEI-224G: Framework Document



OIF

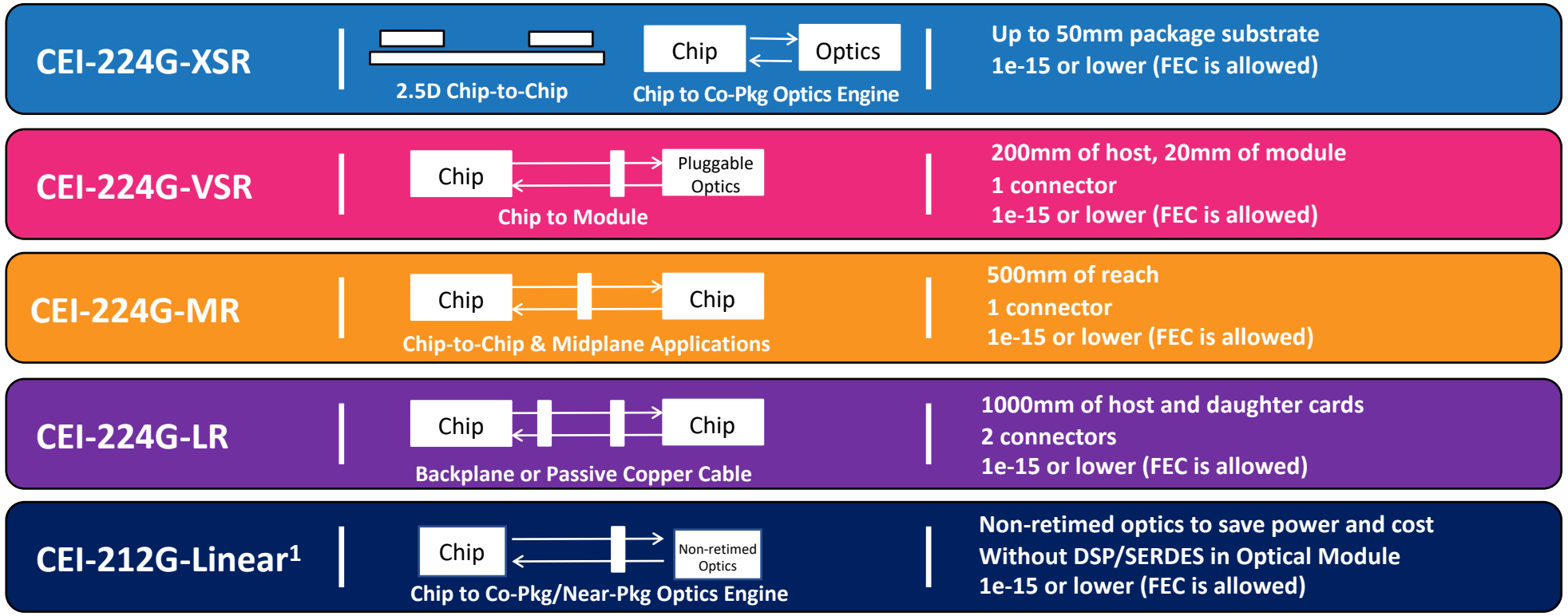
CONTENTS

- Summarizes the consensus findings and guidance for new OIF CEI-224G projects
- Identifies key technical challenges for next generation systems
  - Power, density, performance, reach and cost
- Defines electrical interconnection applications and discusses some of the interoperability test challenges
- Establishes baseline materials that will enable 1.6/3.2 Tbps rate architectures and lower cost, lower complexity 800G and 400G architectures



OIF-FD-CEI-224G-01.0 published in February 2022

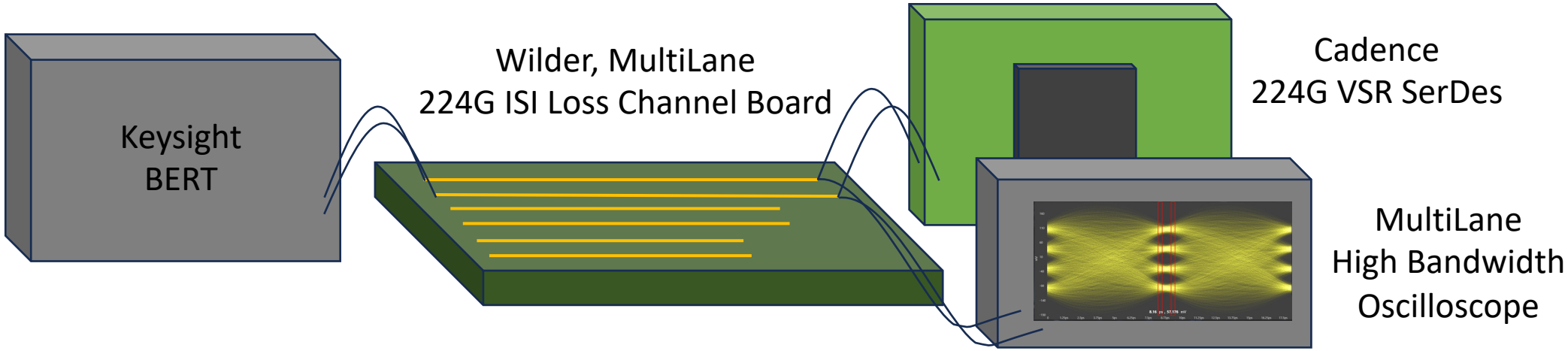
OIF CEI-224G New Project Starts



- CEI-224G-LR Draft Specification is currently in review for OIF members
- New Projects started at OIF Q1 2022 meeting
- One SerDes core might not be able to cover multiple applications from XSR to Linear
- For short reach applications, simpler and lower power equalizations are desired
- Retimed Tx Linear Rx Specs EEI Project Start in OIF Q1 2024 meeting covering 200G/lane over 500m SMF link

[1]Proposal for CEI-212G-Linear Project Discussed in OIF Q1 2024 meeting

CEI-224G-VSR at OFC 2024

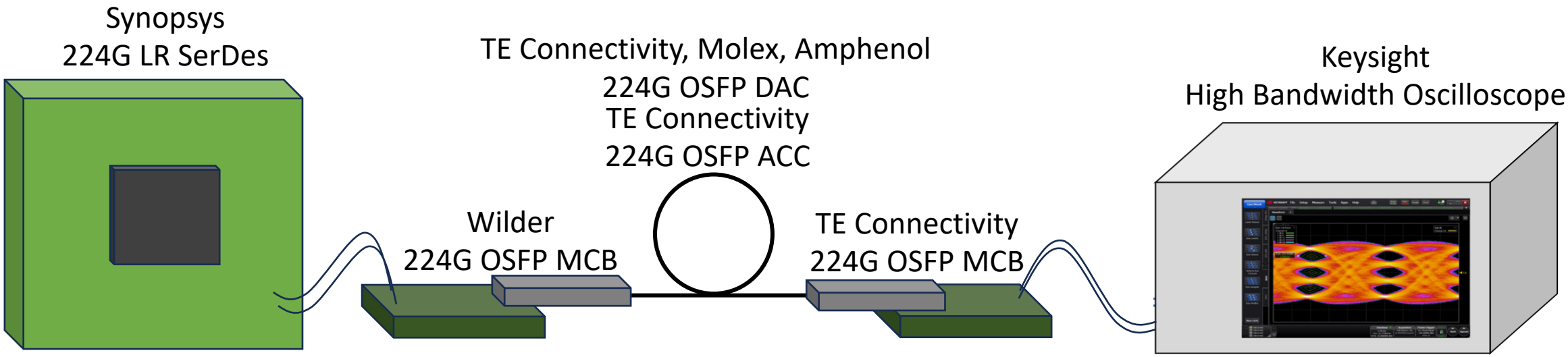


This VSR interoperability demonstration is a snapshot of the current OIF CEI-224G-VSR draft definition for transmitter compliance (VEC) complemented, one metric currently under definition development by measurement science experts, with bit error rate measurement to show what could be expected at the receiver. Transmitter compliance is essential to enabling an ecosystem of interoperability. This demo has test chip silicon receiving PRBS31Q PAM4 212.5 Gbps signals over an ISI test board, with a die-to-die insertion loss of 32 dB at 56 GHz. This setup is emulating a Chip to Module channel, such as a switch ASIC to front panel pluggables, driving 1.6T optical connectivity.

CEI-224G-VSR

200mm of host, 20mm of module
1 connector
1e-15 or lower (FEC is allowed)

CEI-224G-LR at OFC 2024



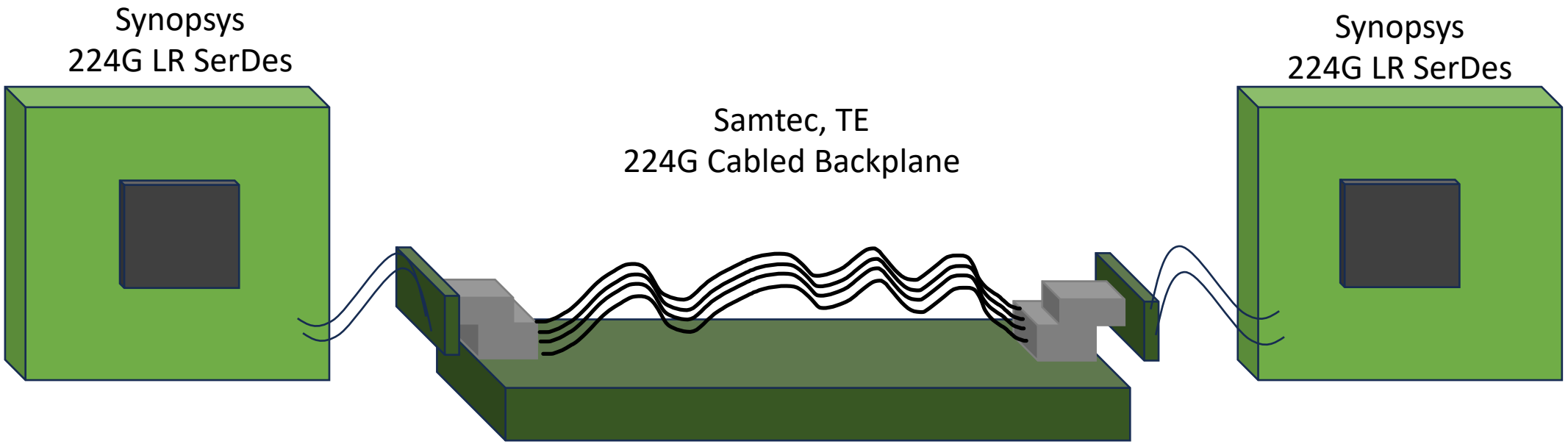
This LR demonstration is shows test chip silicon sending a PRBS13Q PAM4 212 Gbps signal over a network of multi-vendor connectors and direct attach cabling, passive and active, including break-out test fixturing, totaling over 25 dB of channel and 40 dB of insertion loss die to die at 56 GHz. This is a building block for enabling system to system interoperability links, driving 1.6T connectivity in the data center.

CEI-224G-LR

Backplane or Passive Copper Cable

1000mm of host and daughter cards
2 connectors
1e-15 or lower (FEC is allowed)

CEI-224G-LR at OFC 2024



This LR demonstration is test chip silicon sending a PRBS13Q PAM4 212 Gbps signal over a cabled backplane implementation including break-out test fixturing, totaling over 25 dB of channel loss and 40 dB of insertion loss die to die at 56 GHz. This enables up to a meter of backplane with host and daughter cards, for PCBA to PCBA across a Backplane/Midplane interconnectivity.

CEI-224G-LR

Backplane or Passive Copper Cable

1000mm of host and daughter cards
2 connectors
1e-15 or lower (FEC is allowed)

Participating Members

Special thanks to MACOM for hosting pre-testing event!

OIF

PLL INTEROP DEMO

OFC 2024

SCAN ME

www.oiforum.com