OIF
PLL INTEROP DEMO
OFC 2025

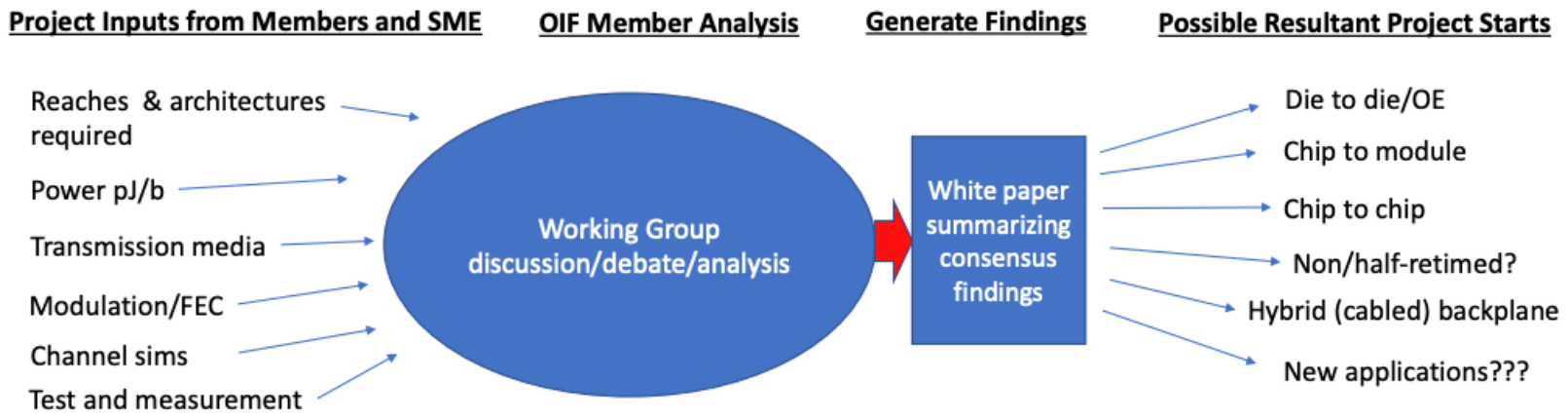
448G, 224G, 112G CEI Interoperability Demo
OFC 2025

OIF's Common Electrical I/O (CEI) Work Has Been a Significant Industry Contributor

Name	Rate per pair	Year	Activities that Adopted, Adapted or were influenced by the OIF CEI
CEI-448G	??? Gbps	202X	Initiated the process considering the many challenges for new OIF CEI-448G projects
CEI-224G	224 Gbps	202X	Several channel reach projects in progress, kicked off in 2022
CEI-112G	112 Gbps	2022	Five channel projects are complete, two channel projects in progress, IEEE, InfiniBand, T11 (Fibre Channel), Interlaken, ITU.
CEI-56G	56 Gbps	2017	IEEE, InfiniBand, T11 (Fibre Channel), Interlaken, ITU
CEI-28G	28 Gbps	2012	InfiniBand EDR, 32GFC, SATA 3.2, SAS-4,100GBASE-KR4, CR4, CAUI4, Interlaken, ITU
CEI-11G	11 Gbps	2008	InfiniBand QDR, 10GBASE-KR, 10GFC, 16GFC, SAS-3, RapidIO v3, Interlaken, ITU
CEI-6G	6 Gbps	2004	4GFC, 8GFC, InfiniBand DDR, SATA 3.0, SAS-2, RapidIO v2, HyperTransport 3.1, Interlaken, ITU
SxI5	3.125 Gbps	2002-3	Interlaken, FC 2G, InfiniBand SDR, XAUI, 10GBASE-KX4, 10GBASE-CX4, SATA 2.0, SAS-1, RapidIO v1, ITU
SPI4, SFI4	1.6 Gbps	2001-2	SPI-4.2, HyperTransport 1.03

CEI-448G: Framework Document Start [under development]

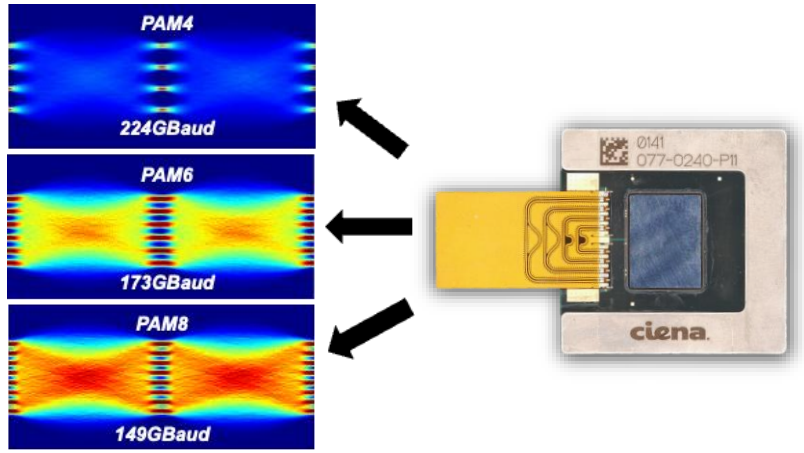
- The OIF has already started the process on considering challenges for new OIF CEI-448G projects
- Identifies key technical challenges for next generation systems
  - Interfaces, reaches, modulations, FEC, test methodologies, etc.
- Investigations by end users and developers will bring critically important channel architecture requirements to the table, along with simulations of channels and device performances
- Establishes baseline materials that will enable 3.2/6.4 Tbps rate architectures and lower cost, lower complexity 800G and 1.6T architectures

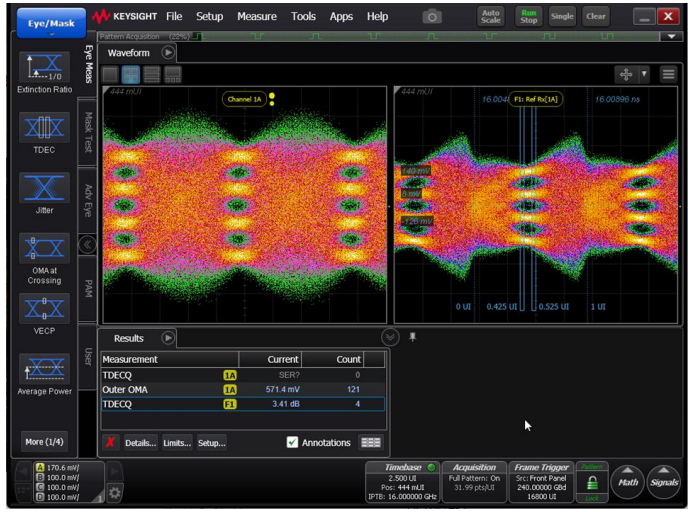


OIF-FD-CEI-448G Approved in August 2024

448G – A common electrical interface for AI/ML

- Discussions and demonstrations addressing the challenges of 448G including:
  - Modulation
    - Live 448G electrical demo at selectable PAM4 (224GBaud), PAM6 (173GBaud) or PAM8 (149GBaud) modulation formats
  - Required SNR
  - Pre-FEC BER and FEC Requirements
    - Latency, Coding Gain, Power
  - Channel Loss
  - Connectorizations
  - Power profiles
  - Test & Measurement Capabilities
- Contributions for pathfinding requested to the industry
- OIF will be hosting Bay Area 400G AI Signaling Workshop April 15th and 16th

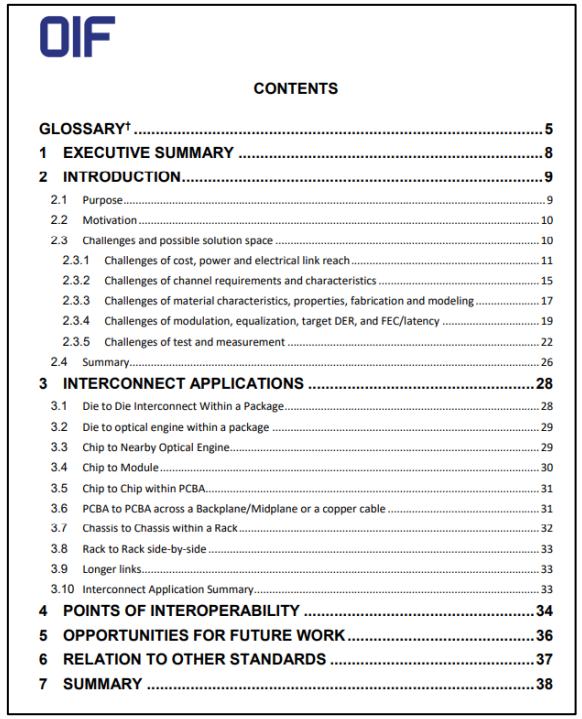




OIF 448Gbps Signaling for AI Workshop

- https://www.oiforum.com/meetings-events/oif-448gbps-signaling-for-ai-workshop-reg/
- Hosted by OIF and co-sponsored by the Ethernet Alliance, Open Compute Project, SNIA, Ultra Ethernet Consortium and Ultra Accelerator Link Consortium
- Two-day workshop will serve as a forum for hyperscalers, system vendors, semiconductor companies, optics manufacturers, electrical and optical interconnect and channel suppliers, and test and measurement vendors to align on the challenges and innovations related to 400G/lane electrical and optical interconnects, system architectures, modulations and equalization tradeoffs

CEI-224G: Framework Document



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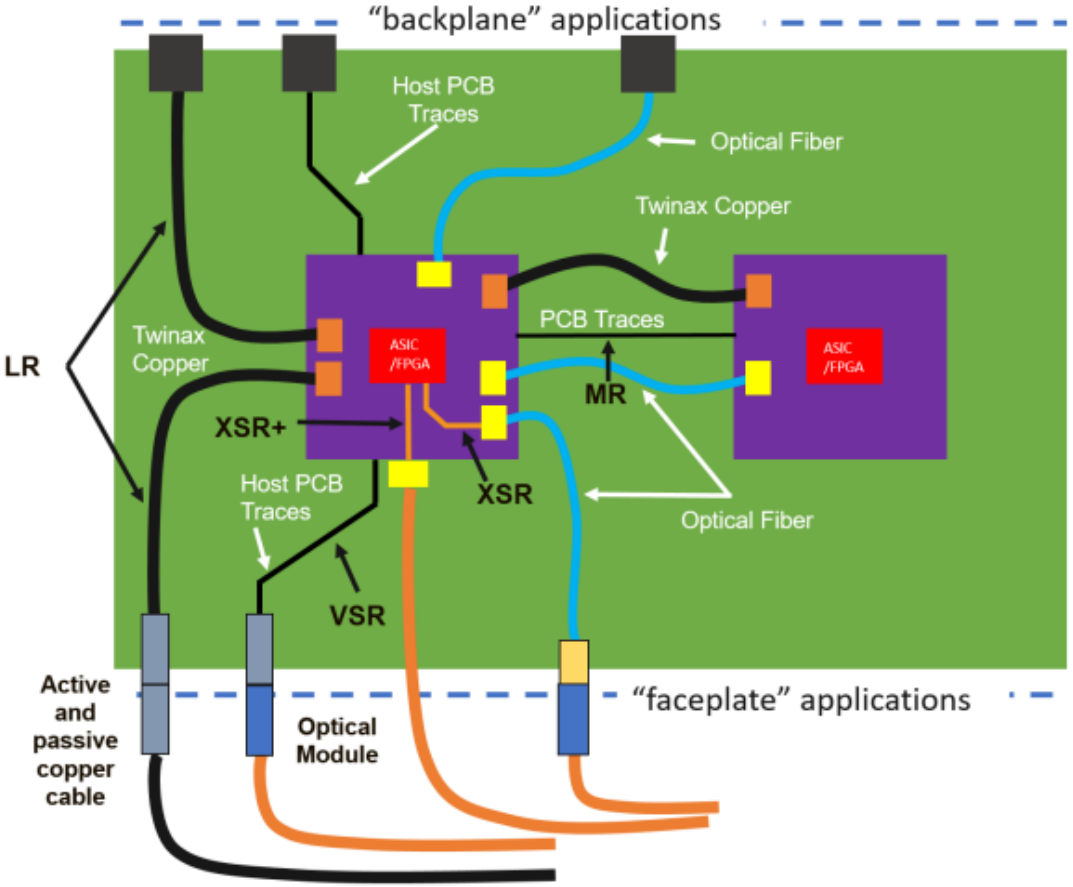
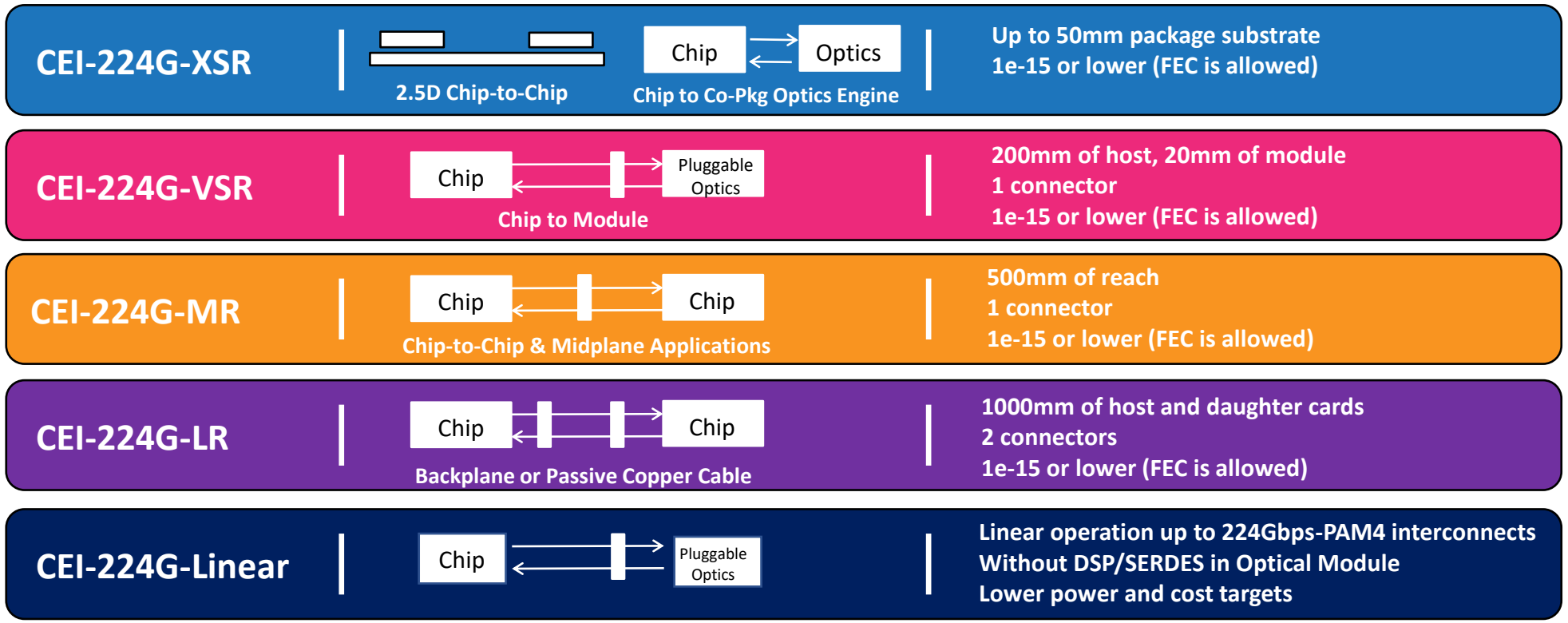
CONTENTS

- Summarizes the consensus findings and guidance for new OIF CEI-224G projects
- Identifies key technical challenges for next generation systems
  - Power, density, performance, reach and cost
- Defines electrical interconnection applications and discusses some of the interoperability test challenges
- Establishes baseline materials that will enable 1.6/3.2 Tbps rate architectures and lower cost, lower complexity 800G and 400G architectures



OIF-FD-CEI-224G-01.0 published in February 2022

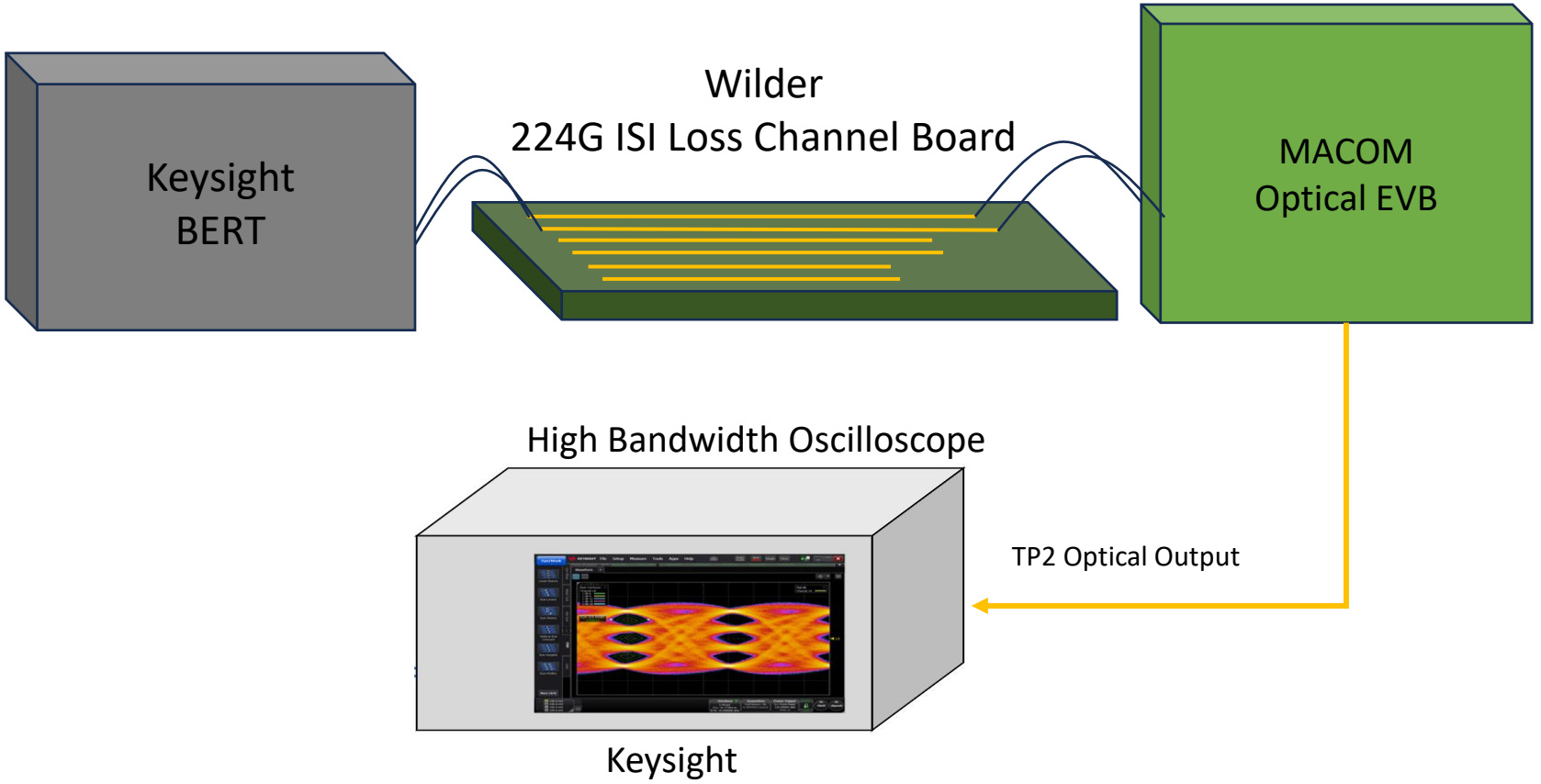
OIF CEI-224G New Project Starts

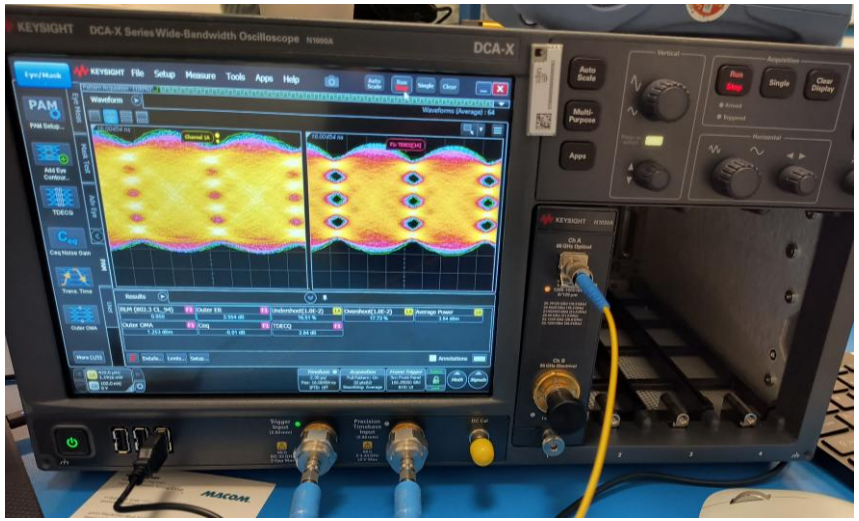


CEI-224G-LR, MR Draft Specifications currently in review for OIF members

- One SerDes core might not be able to cover multiple applications from XSR to LR
- For short reach applications, simpler and lower power equalizations are desired

CEI-224G-Linear at OFC 2025





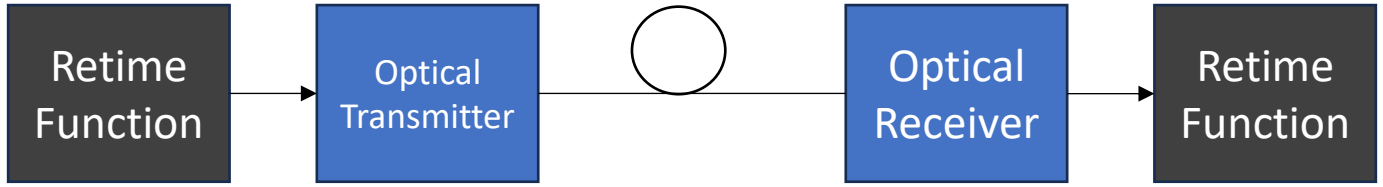
CEI-224G-Linear | Chip ⟷ Pluggable Optics |

Linear operation up to 224Gbps-PAM4 interconnects
Without DSP/SERDES in Optical Module
Lower power and cost targets

RTLR (Retimed Transmitter, Linear Receiver)

Fully Retimed Optical Link: Highest Power, Longest Reach

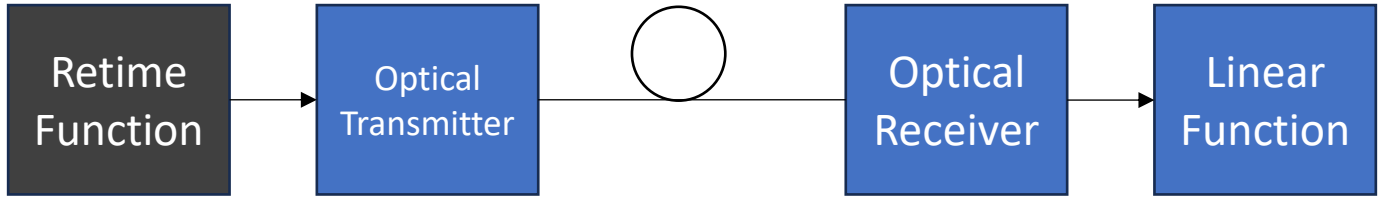
DSP/retimer module OIF-CEI-224G-VSR-PAM4 supports TBD channel on egress with some optical output compliance expectation



Ingress path includes DSP/retimer in the module and supports TBD channel to Host ASIC

Retimed Transmit Linear Receiver (RTLR) Optical Link: Balance of Reach, Power

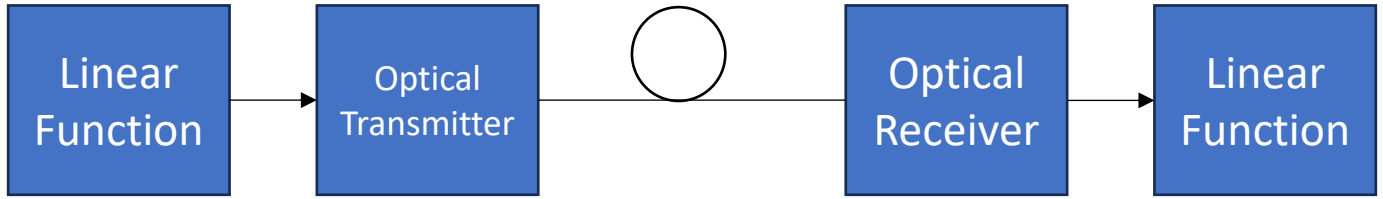
OIF-EEI-224G-RTLR is meant to be identical to above on the egress channel



Ingress path removes the DSP/retimer in the module and uses an enhanced version of OIF CEI-224G-Linear-PAM4 specifications by utilizing host ASIC DSP SerDes capability

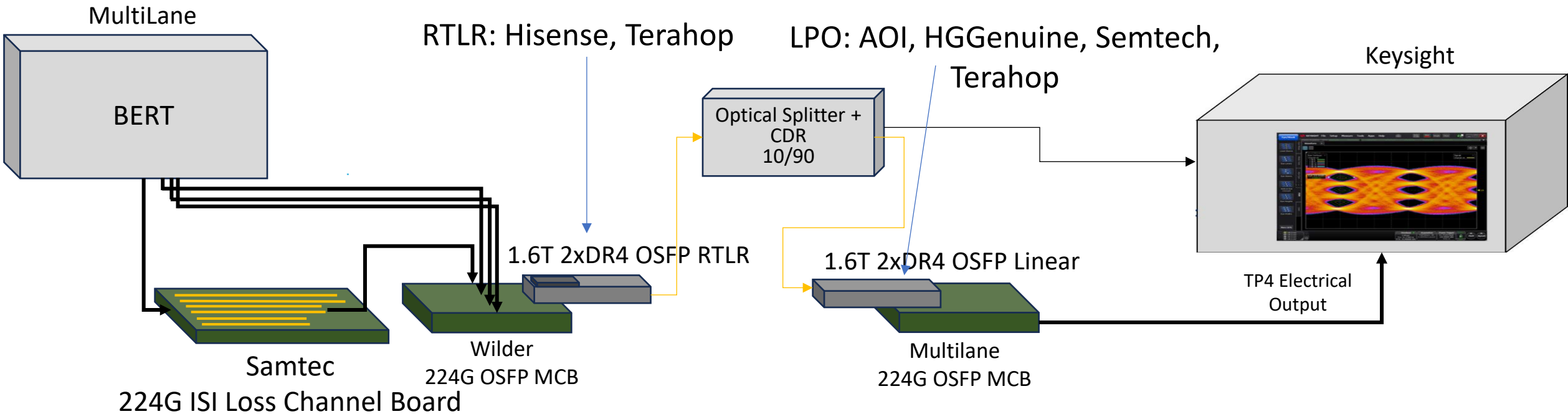
Linear Unretimed Optical Link: Lowest Power, Shortest Reach

Egress path removes the DSP/retimer in the module and uses OIF CEI-224G-Linear-PAM4 specifications by utilizing host ASIC DSP SerDes capability



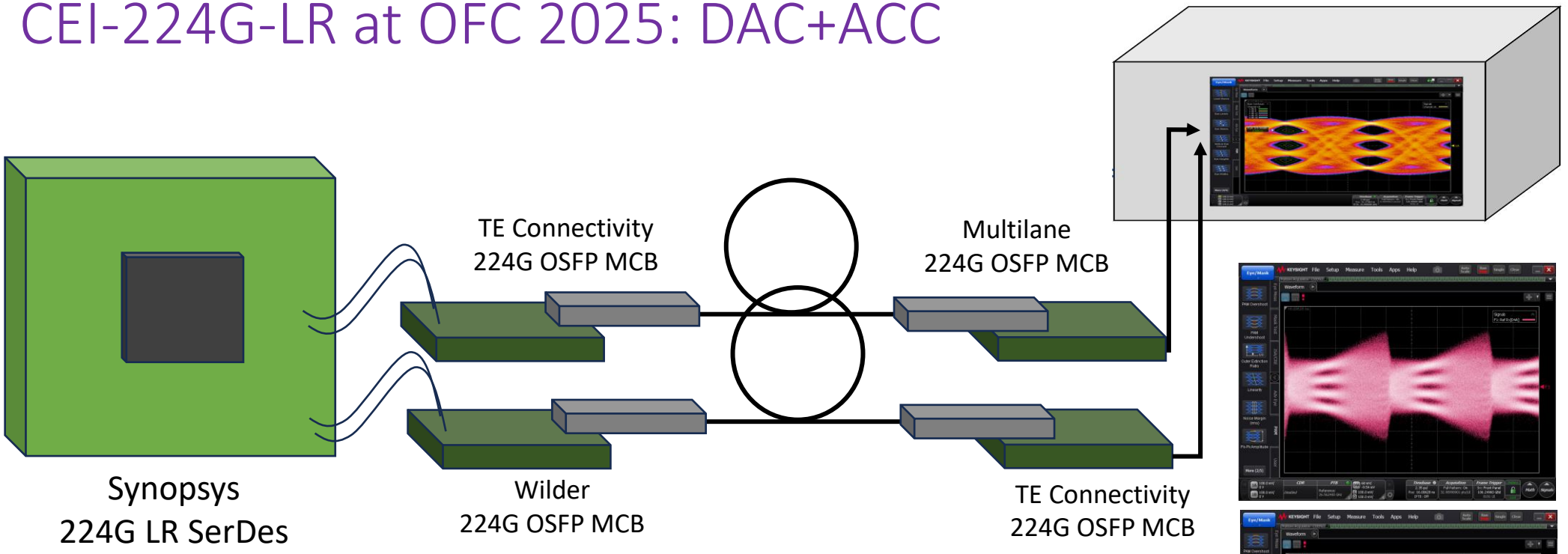
Ingress path removes the DSP/retimer in the module and uses OIF CEI-224G-Linear-PAM4 specifications by utilizing host ASIC DSP SerDes capability

CEI-224G-Linear & EEI-224G-RTLR at OFC 2025

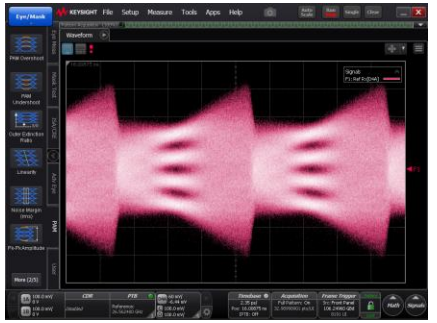


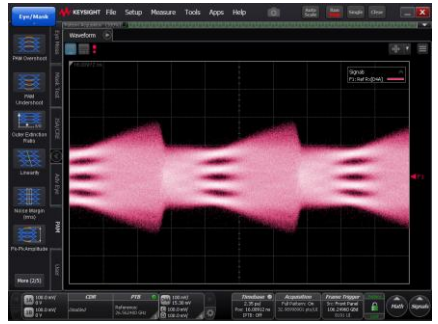


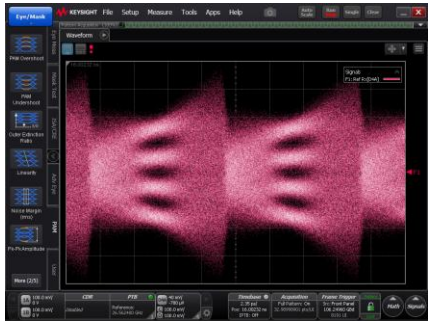

CEI-224G-LR at OFC 2025: DAC+ACC



High Bandwidth Oscilloscope + Adaptive EQ Keysight







MACOM, Semtech, TE Connectivity, Molex
224G OSFP ACC

TE Connectivity, Molex
224G OSFP DAC

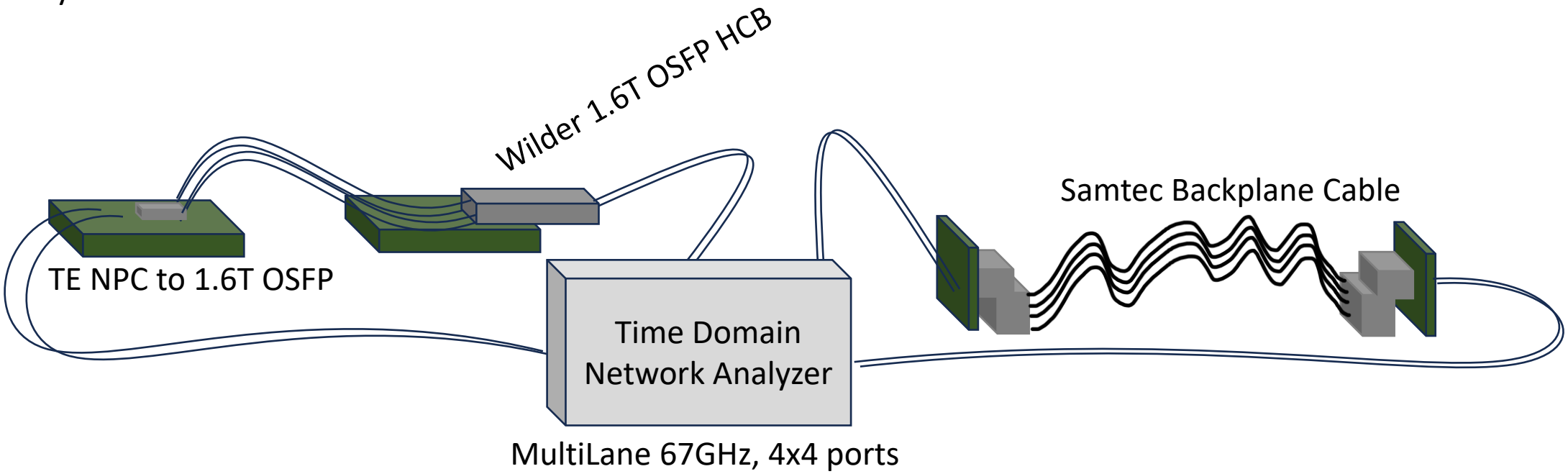
CEI-224G-LR

Backplane or Passive / Active Copper Cable

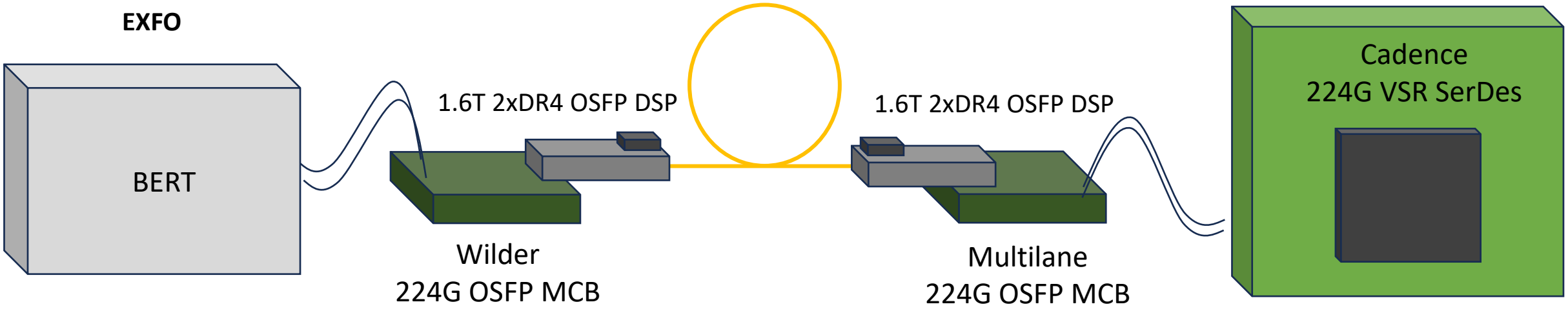
1000mm of host and daughter cards
2 connectors
1e-15 or lower (FEC is allowed)

CEI-224G at OFC 2025: T&M Channel Insights

This demonstration uses a Time Domain Network Analyzer to show channel characteristics of a cabled near chip and cabled host connectivity (XXmm) plus OSFP break-out test fixturing, totaling over 20 dB of channel loss as well as a cabled backplane (XXmm). These architectural examples are leveraged to extend the interoperable ecosystem to 224G and enable a meter of backplane with host and daughter cards, for “line card to line card” or “AI/ML architecture” or “GPU/GPU to switch” interconnectivity.

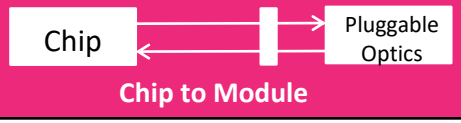


CEI-224G-VSR at OFC 2025



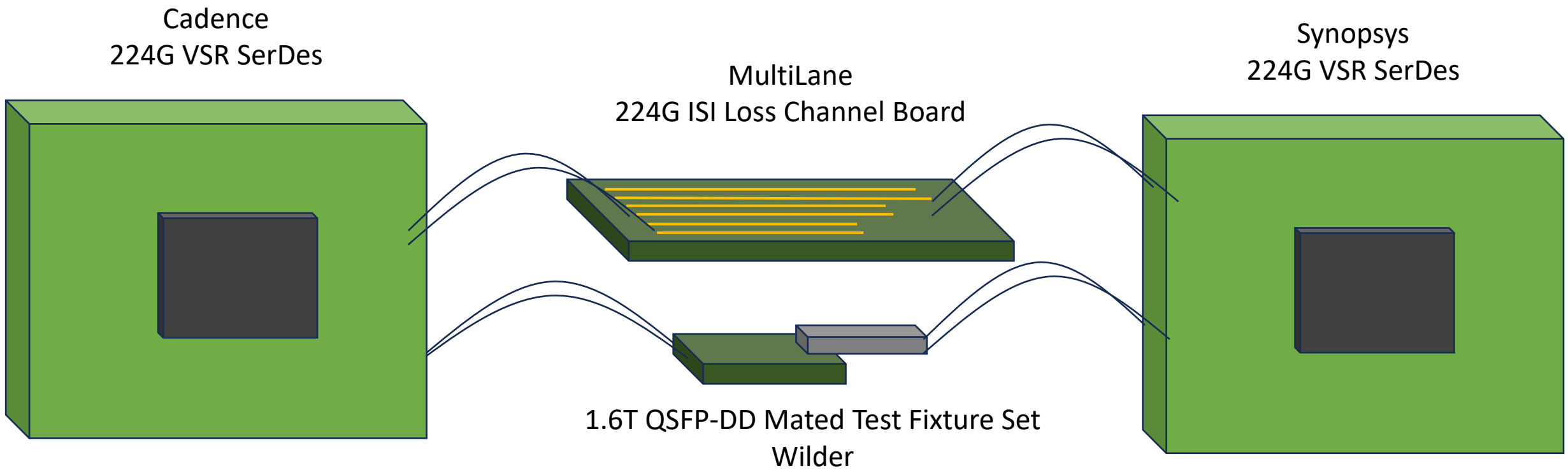
1.6T Optics: Accelink, HGGenuine, Terahop, Hisense

CEI-224G-VSR



200mm of host, 20mm of module
1 connector
1e-15 or lower (FEC is allowed)

CEI-224G-VSR at OFC 2025



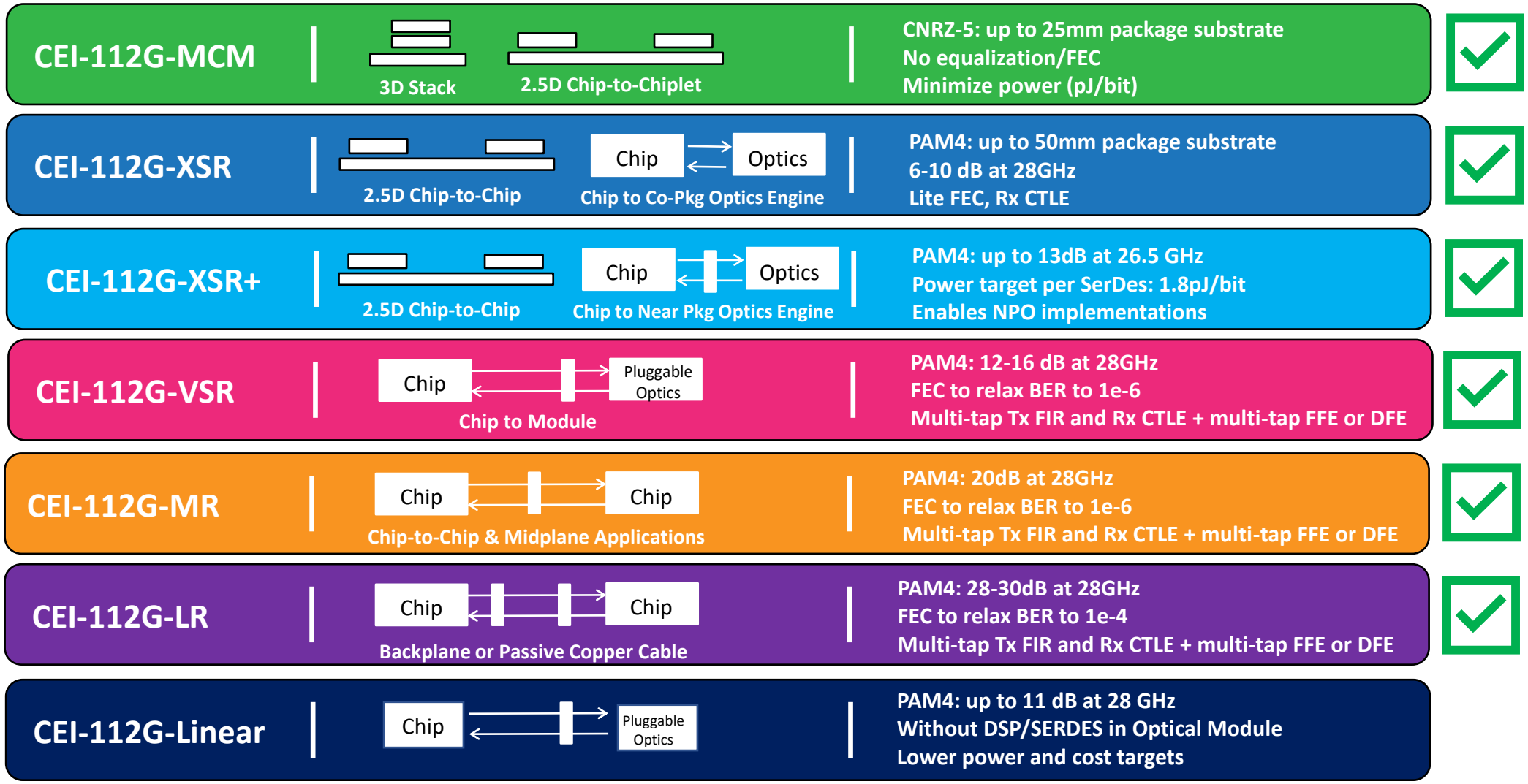
CEI-224G-VSR

Chip to Module

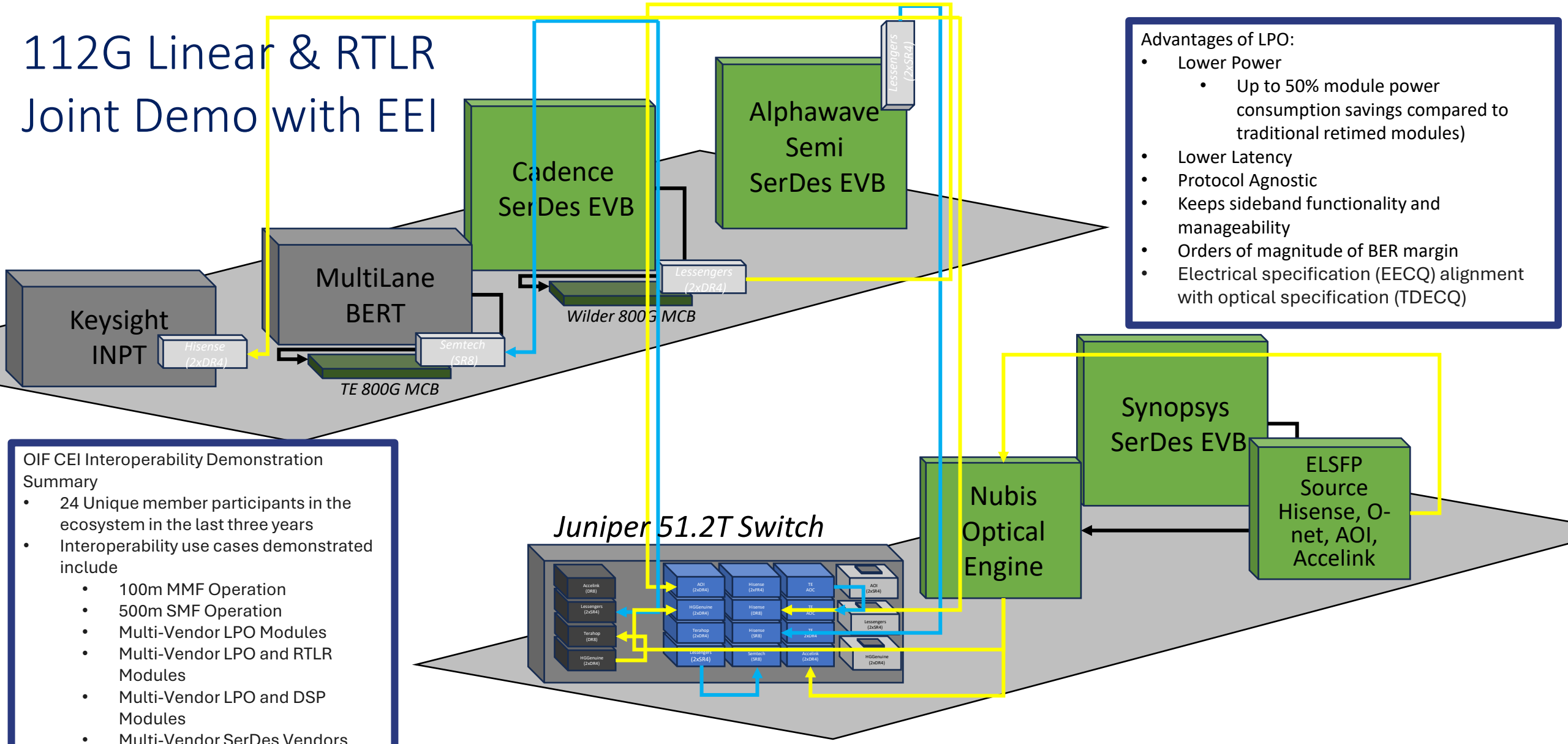
200mm of host, 20mm of module
1 connector
1e-15 or lower (FEC is allowed)

OIF CEI-112G Development Application Space

- PAM4 modulation scheme becomes dominant in OIF CEI-112 Gbps interface IA
- One SerDes core is not able to efficiently cover multiple applications from XSR to LR
- For short reach applications, simpler and lower power equalizations are desired



112G Linear & RTLR Joint Demo with EEI



Advantages of LPO:

- Lower Power
  - Up to 50% module power consumption savings compared to traditional retimed modules)
- Lower Latency
- Protocol Agnostic
- Keeps sideband functionality and manageability
- Orders of magnitude of BER margin
- Electrical specification (EECQ) alignment with optical specification (TDECQ)

OIF CEI Interoperability Demonstration Summary

- 24 Unique member participants in the ecosystem in the last three years
- Interoperability use cases demonstrated include
  - 100m MMF Operation
  - 500m SMF Operation
  - Multi-Vendor LPO Modules
  - Multi-Vendor LPO and RTLR Modules
  - Multi-Vendor LPO and DSP Modules
  - Multi-Vendor SerDes Vendors
  - TP1a, TP2, TP4 Compliance

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PLL INTEROP DEMO

OFC 2025

SCAN ME