CMIS Data Path State Machine (DPSM) and Application Advertising

OIF Webinar

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Presenters

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Future Sessions
- VDM – Todd Rope, Marvell – Feb 28
- CDB/FW Upgrades – TBD – April 3
- NPSM – TBD – TBD
- Others?

Webinar Overview

- Review of CMIS: What is CMIS? How is CMIS structured.
- DPSM and Data Paths
  - What is the Data Path State Machine (DPSM)?
  - DPSM Transition Diagram and State Definition
  - DPSM Provisioning & Commissioning
- Application Advertisements and AppSels
  - How are Applications advertised in CMIS
  - Where to check Application ID codes
  - Application Configuration – Data Path Control Sets
  - Application Examples

Review: What is CMIS ?

CMIS = **C**ommon **M**anagement **I**nterface **S**pecification

Electrical [Host]

(OIF CEI, IEEE, etc)

Optical/Copper [Media]

Host (switch/router)

Pluggable Module

(IEEE, MSAs, OIF)

Management

- configure
- initialize
- monitor

= “the forgotten interface”

Review: What is CMIS?

Common **M**anagement **I**nterface **S**pecification (**CMIS**) is a management interface for optical modules and cable assemblies based on a range of industry form factors such as QSFP-DD and OSFP.

CMIS provides a defined set of registers and functions for standard module management including:

- Inventory data
- Module and traffic configuration
- Module monitoring (alarms/defects, performance monitoring)
- Capability advertising

CMIS is intended to manage a wide range of range of interconnects such as passive copper cables, 1300 nm client plugs, 400ZR coherent modules, etc.

CMIS is written to operate over a two wire interface but can be implemented on other physical interfaces

Review: How is CMIS structured?

CMIS has grown from a single document to a collection of documents. CMIS is the core and is supported by a set of supplements for specific applications.

- C-CMIS – Coherent CMIS – Provides extensions to CMIS to manage modules with coherent interfaces
- CMIS-FF* – CMIS Form Factor – Provides details of HW pins and related registers for different module form factors.
- CMIS- ELSFP* – CMIS External Laser Small Form Factor Pluggable – Provides details for managing Co-Packaging and ELSFP modules.
- CMIS-LT* – CMIS Link Training – Provides details for managing host side link training on CMIS modules.
- CMIS-VCS* – CMIS Versatile Control Set – Provides details for managing electrical characteristics of host interfaces.

CMIS works in conjunction with other industry standards like SFF-8024 and hardware MSAs.

*Some CMIS extensions are under development and have not been published yet.

Review: CMIS Data Path State Machine (DPSM)

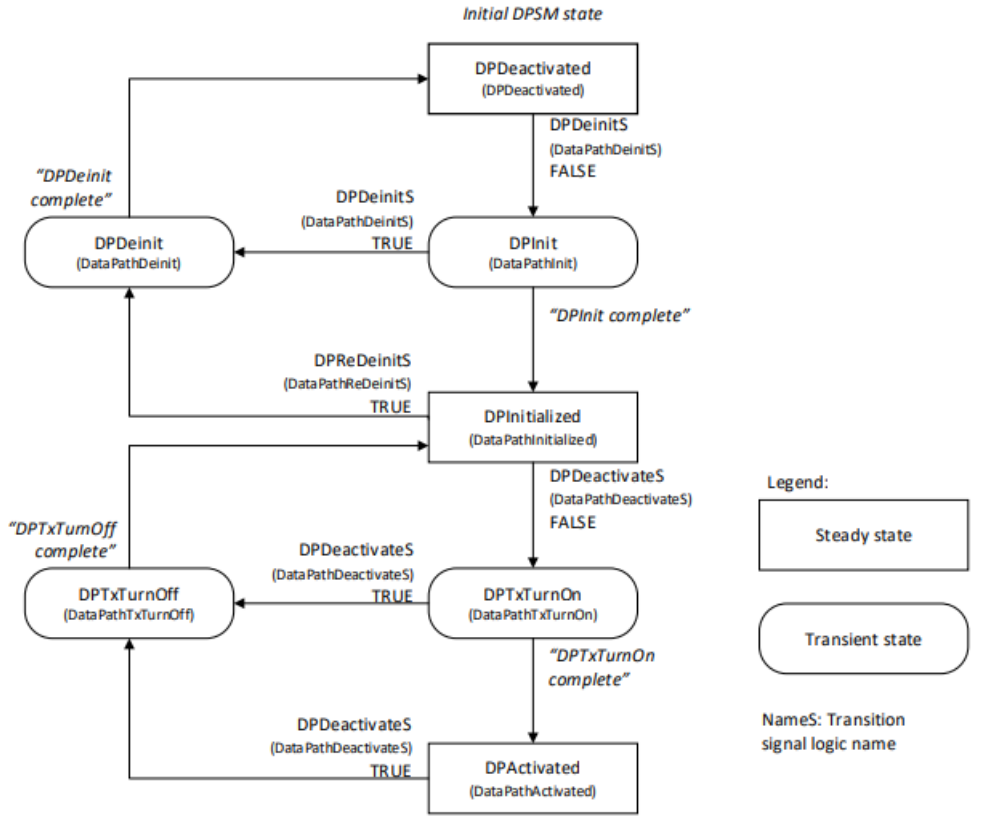
DPSM — **Used to progress the module from DP_Deactivated (laser off) to DP_Activated (laser on)**

Use

Separate from the module state machine

CMIS module uses the DPSM in the same way

The Host can write one DPSM driver that can be used on all the CMIS modules



Review: CMIS APPSEL Code

APPSEL

Application Select codes are used to provision a module
A module advertises a set of supported APPSEL codes that can be applied to the module

Example

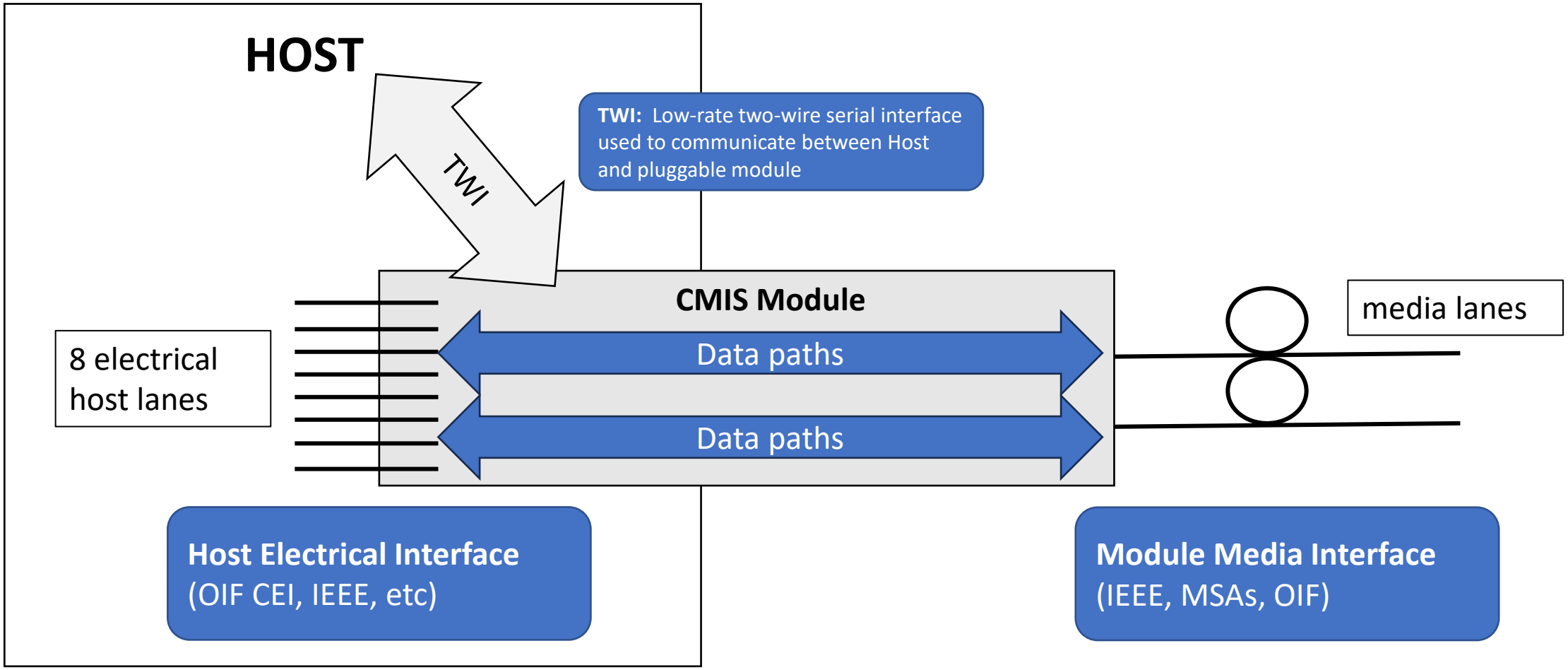
Table shows the two supported APPSEL codes for a 400ZR module

Also shows the start of APPSEL 3 where FF indicates this is the end of supported APPSEL codes

86	Appl sel 1 Host Elec IF ID	11	ID from Table 4-5 SFF-8024: 400GAUI-8 C2M
87	Appl sel 1 module media if id	3E	ID from Table 4-7 SFF-8024: 400GBZR
88	appl sel 1 lane count	81	Host Lane Count: 8
			Media Lane Count: 1
89	Appl sel 1 host lane assignment opt	1	Application allowed to start on host lane 1. Refer to Section 6.2.1.1 for details
90	Appl sel 2 host elec if id	D	ID from Table 4-5 SFF-8024: 100GAUI-2 C2M
91	Appl sel 2 module media if id	3E	ID from Table 4-7 SFF-8024: 400GZR
92	Appl sel 2 lane count	21	Host Lane Count: 2
			Media Lane Count: 1
93	Appl sel 2 host lane assignment opt	55	Application allowed to start on host lane 1. Refer to Section 6.2.1.1
94	Host interface ID app 3	FF	first unused ApSel code

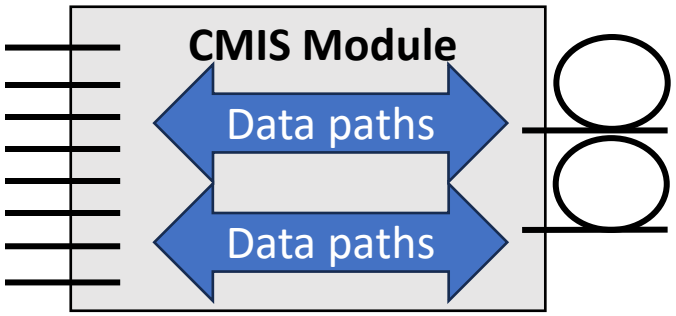
Today's Focus

Data Paths (DPSM) and Applications



What is the Data Path State Machine (DPSM)?

The **D**ata **P**ath **S**tate **M**achine (**DPSM**) is an instance that describes Data Path-specific behaviors and properties that are related to the configuration of the Data Path, as managed by the Host.



A Data Path is a bidirectional combination of

- One or more host lanes
- One or more media lanes
- A set of internal module resources implementing the Application that is described in an associated Application Descriptor.

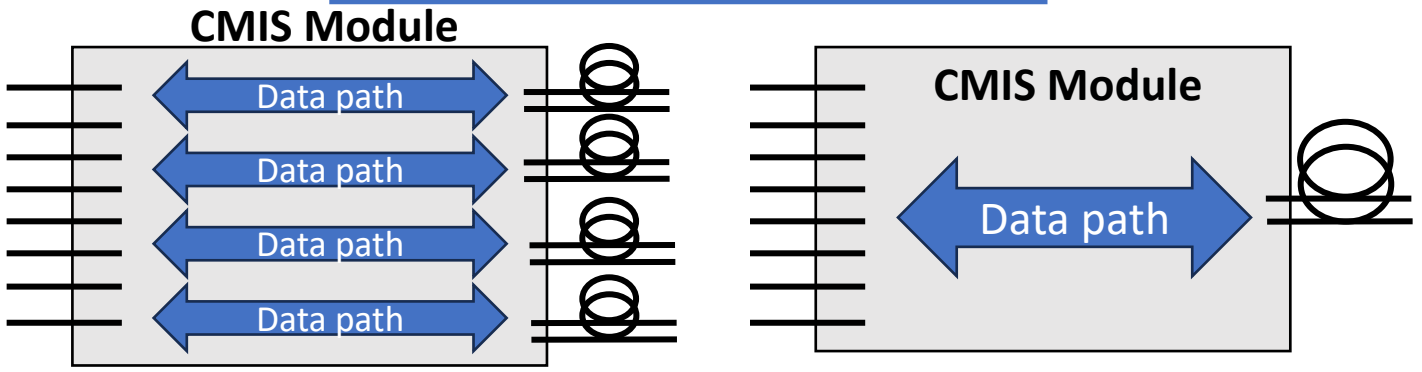
The DPSM state represents a management or configuration realization status of a Data Path, representing the effects of certain host configuration commands and of module reactions to those commands.

Why have a DPSM?

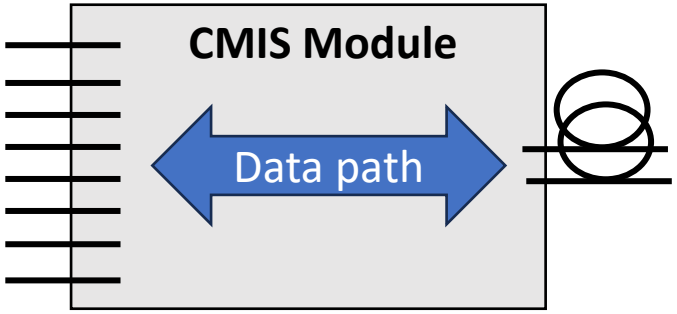
The DPSM Purpose: Coordinating communication and management between the Host and module to initialize traffic

Example of different Data Paths (media – electrical)

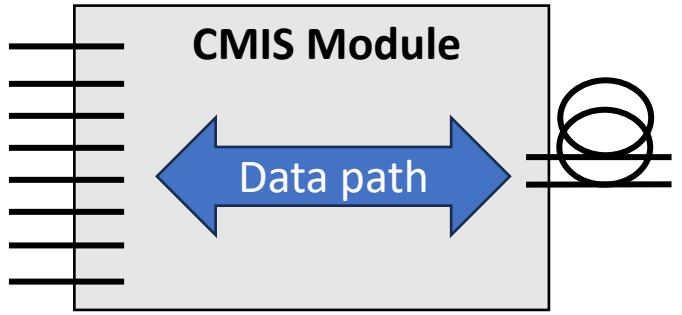
IMDD DR4 Module (4-4 or 1-1)



Coherent 400ZR Module (1-1)



IMDD FR4 Module (1-1)



Where is the DPSM used?

The DPSM registers were introduced in CMIS 4.0

Page 10h: Lane Control and Data Path Control

Byte	Size (bytes)	Subject Area	Description
128	1	Data Path Control	Data Path control bits for each lane, controlling associated Data Path State machines
129-142	14	Lane-Specific Control	Fields to control lane attributes independent of the Data Path State machine or control sets
143-177	35	Staged Control Set 0	Fields to select Applications and signal integrity settings
178-212	35	Staged Control Set 1	Fields to select Applications and signal integrity settings
213-232	20	Lane-Specific Masks	Masks to suppress Interrupts from lane-related Flags
233-239	7	-	**Reserved[7]**
240-255	16	-	**Custom[16]**

Page 11h: Lane Status and Data Path Status

Byte	Size (bytes)	Subject Area	Description
128-131	4	Data Path States	State of Data Path State Machine associated with each lane
132-133	2	Lane Output Status	Output signal validity status (per lane)
134-153	20	Lane-specific Flags	Flags per lane or per Data Path
154-201	48	Lane-specific Monitors	Generic media side monitors for optical power and laser bias
202-205	4	Configuration Status	Status of configuration commands (Apply register writes)
206-234	29	Active Control Set	Nominal or actual Data Path configuration. See section 6.2.3
235-239	5	Data Path Conditions	Dynamic condition indications
240-255	16	Media Lane to media wavelengths and fibers mapping	Indicates the mapping of Media Lanes to Media Wavelengths and Fibers

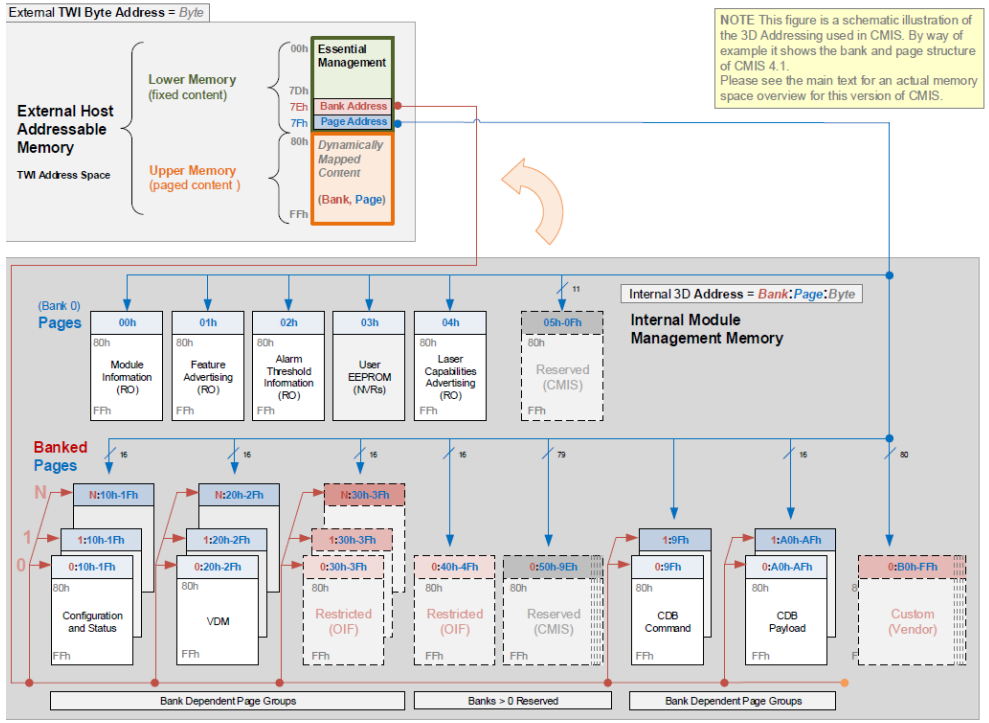


Figure 8-1 CMIS Module Memory Map (Conceptual View)

Page 12h: Tunable Laser Control and Status

Byte	Size (bytes)	Subject Area
128-135	8	Grid Spacings
136-151	8 x 2	Channel Offset Numbers
152-167	8 x 2	Fine Tuning Offsets
168-199	8 x 4	Laser Frequencies
200-215	8 x 2	Target Output Power
216-221	6	-
222-229	8	Status Indicators
230	1	Flag Summary
231-238	8	Flags
239-246	8	Masks (default: 1)
247-255	9	-

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MAIN DPSM CTRL

Stage Ctrl 0

Data Path Control Registers

Host control for Data Path State Machine DPSM

- 128 = DPDeinitLane<i>

Example Stage Control 0 Registers:

- Staged Control Set 0, **Apply Triggers**
  - 143 = ApplyDPInitLane<i>
  - 144 = ApplyImmediateLane<i>
- Staged Control Set 0, **Data Path Configuration Application assignments**
  - 145-152 = DPConfigLane<i>
- Staged Control Set 0, Tx Controls

  Host-to-Module signal integrity settings per lane
  - 153 = AdaptiveInputEqEnableTx<i>
  - 154-155 = AdaptiveInputEqRecallTx<i>
  - 156-159 = FixedInputEqTargetTx<i>
  - 160 = CDREnableTx<i>
- Staged Control Set 0, Rx Controls

  Module-to-Host signal integrity settings per lane
  - 161 = CDREnableRx<i>
  - 162-165 = OutputEqPreCursorTargetRx<i>
  - 166-169 = OutputEqPostCursorTargetRx<i>
  - 170-173 = OutputAmplitudeTargetRx<i>
- Staged Control Set 0, Unidirectional Apply Triggers
  - 176 = ApplyImmediateTx<i>
  - 177 = ApplyImmediateRx<i>

<i> is variable designated for each lane

Where is the DPSM used?

Page 10h: Lane Control and Data Path Control

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DP Status

Page 11h Data Path Status:

- Data Path States
  Module reported DPSM status
  - 128-131 = DPStateHostLane<i>
- Lane-Specific State Changed Flags
  Reporting Data Path status changes
  - 134 = DPStateChangedFlag<i>
- Configuration Command Status registers
  Reporting Data Path configuration CMD status
  - 202-205 = ConfigStatusLane<i>
- Active Control Set, Provisioned Data Path Configuration
  Active application
  - 206-213 = ACS::DPConfigLane<i>
- Active Control Set, Provisioned Tx Controls
  Active Host-to-Module signal integrity settings per lane
  - 214 = ACS::AdaptiveInputEqEnableTx<i>
  - 215-216 = ACS::AdaptiveInputEqRecalledTx<i>
  - 217-220 = ACS::FixedInputEqTargetTx<i>
  - 221 = ACS::CDREnableTx<i>
- Active Control Set, Provisioned Rx Controls
  Module-to-Host signal integrity settings per lane
  - 222 = ACS::CDREnableRx<i>
  - 223-226 = ACS::OutputEqPreCursorTargetRx<i>
  - 227-230 = ACS::OutputEqPostCursorTargetRx<i>
  - 231-234 = ACS::OutputAmplitudeTargetRx<i>
- Data Path Conditions
  - 235 = ACS::DPConfigLane<i>

(<i> is variable designated for each lane)

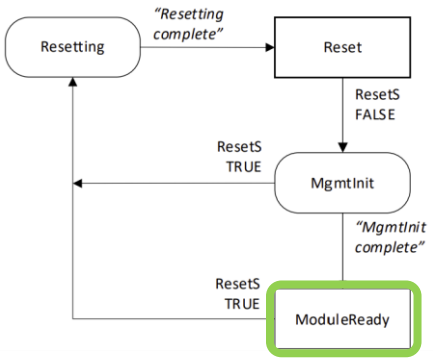
Encoding	State
0h	**Reserved**
1h	DPDeactivated (or unused lane)
2h	DPInit
3h	DPDeinit
4h	DPActivated
5h	DPTxTurnOn
6h	DPTxTurnOff
7h	DPInitialized
8h-Fh	**Reserved**

DPSM Transition Diagram and State Definition

MSM — **Is in Ready State**

Register 3, bits 3-1

Code	Module State
000b	-
001b	ModuleLowPwr
010b	ModulePwrUp
011b	ModuleReady
100b	ModulePwrDn
101b	ModuleFault
110b	-
111b	-



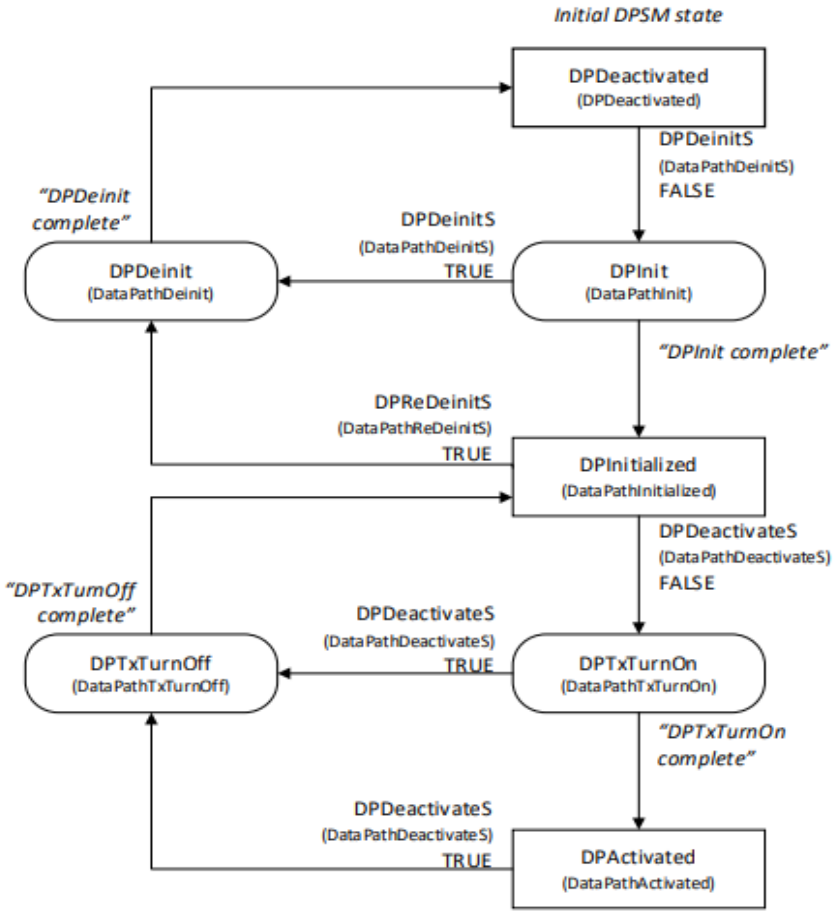
DPSM — **Used to progress the module from DP_Deactivated (laser off) to DP_Activated (laser on)**
Plus Module Provisioning and Commissioning!

Page 11h Data Path State Machine Status

- 128-131 = DPStateHostLane<i>

Encoding	State
0h	**Reserved**
1h	DPDeactivated (or unused lane)
2h	DPInit
3h	DPDeinit
4h	DPActivated
5h	DPTxTurnOn
6h	DPTxTurnOff
7h	DPInitialized
8h-Fh	**Reserved**

SteadyState **Transition States**



DPSM Transition Diagram and State Definition

DPSM State Definitions

The DPSM has two types of States:

- **Steady States: the module is maintaining a condition and waiting for the Host to initiate action**
- **Transition States: the module is performing an action and automatically performs a state transition upon completion**

  Module advertises max duration for transition states

States:

- **State 1h – DPDeactivated – The data path is not active and the Host can configure the data path lane**
- **State 2h – DPInit - The module is initializing the data path**
- **State 3h – DPDeinit - The module is deactivating the data path**
- **State 4h – DPActivated - The data path is fully functional and ready to pass traffic**
- **State 5h – DPTxTurnOn - The module unmutes the Tx media lane ('laser' turns on)**
- **State 6h – DPTxTurnOff - The module disables or squelches the Tx media lane**
- **State 7h – DPInitialized - All functional resources of the data path have been allocated, but the Host has squelched or disabled the Tx media lane**

- By default, all Data Paths will begin initializing when the Module State reaches ModuleReady.
- The Host can prevent this auto-initialization behavior by setting all DPDeinit bits while the module is in the ModuleLowPwr state.
- Multiple Data Paths are mutually independent. They may be initialized or deinitialized at the same time or at different times.
- The number of lanes in any specific Data Path is a characteristic of the currently active Application that is selected by the AppSel code in the Active Control Set.
- Max duration advertisements for DPInit & DPDeinit are located on Page01h, register 144

DPSM Provisioning: Application Modes

Data Path Configuration Fields

1. **AppSelCode<i> is the AppSel Number that the module advertises in the Low Memory Page and Upper Memory Page 01h**
2. **DataPathID<i> is the Data Path lane assigned**
3. **Explicit Control: If lane is unused, the field is ignored**
   - **0b: Use Application-dependent settings for lane**
   - **1b: Use Staged Control Set 0 control values for lane**

- The Host configures different applications by selecting an Appsel Code based on the module's advertisements
- Each Data Path lane is individually configured
- The Host can configure the Data Path lane(s) when the DPSM is in State 1h – DPDeactivated

Don't Forget! Data Path configurations of a Staged Control Set have no effect on the behavior of a lane until the Host has successfully triggered ApplyDPInit for the lane.

Upper Memory Page 10h

Table 8-65 Staged Control Set 0, Data Path Configuration (Page 10h)

Byte	Bits	Field Name	Register Description	Type
145	7-4	AppSelCodeLane1	**SCS0::DPConfigLane1** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane1		
	0	ExplicitControlLane1		
146	7-4	AppSelCodeLane2	**SCS0::DPConfigLane2** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane2		
	0	ExplicitControlLane2		
147	7-4	AppSelCodeLane3	**SCS0::DPConfigLane3** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane3		
	0	ExplicitControlLane3		
148	7-4	AppSelCodeLane4	**SCS0::DPConfigLane4** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane4		
	0	ExplicitControlLane4		
149	7-4	AppSelCodeLane5	**SCS0::DPConfigLane5** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane5		
	0	ExplicitControlLane5		
150	7-4	AppSelCodeLane6	**SCS0::DPConfigLane6** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane6		
	0	ExplicitControlLane6		
151	7-4	AppSelCodeLane7	**SCS0::DPConfigLane7** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane7		
	0	ExplicitControlLane7		
152	7-4	AppSelCodeLane8	**SCS0::DPConfigLane8** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane8		
	0	ExplicitControlLane8		

DPSM Provisioning: Application Modes

Example of provisioning a 400G DR Applications

AppSel 2

Host Electrical Interface: 400GAUI-8 C2M ; 0x11

Module Media Interface: 400G DR4; 0x1C

Byte	Bits	Field Name	Bit Value	Hex Value
145	7-4	AppSelCodeLane1	0010	0x20
	3-1	DataPathIDLane1	000	
	0	ExplicitControlLane1	0	
146	7-4	AppSelCodeLane2	0010	0x20
	3-1	DataPathIDLane2	000	
	0	ExplicitControlLane2	0	
147	7-4	AppSelCodeLane3	0010	0x20
	3-1	DataPathIDLane3	000	
	0	ExplicitControlLane3	0	
148	7-4	AppSelCodeLane4	0010	0x20
	3-1	DataPathIDLane4	000	
	0	ExplicitControlLane4	0	
149	7-4	AppSelCodeLane5	0010	0x20
	3-1	DataPathIDLane5	000	
	0	ExplicitControlLane5	0	

400GE

Upper Memory Page 10h

Table 8-65 Staged Control Set 0, Data Path Configuration (Page 10h)

Byte	Bits	Field Name	Register Description	Type
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	3-1	DataPathIDLane1		
	0	ExplicitControlLane1		
146	7-4	AppSelCodeLane2	**SCS0::DPConfigLane2** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane2		
	0	ExplicitControlLane2		
147	7-4	AppSelCodeLane3	**SCS0::DPConfigLane3** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane3		
	0	ExplicitControlLane3		
148	7-4	AppSelCodeLane4	**SCS0::DPConfigLane4** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane4		
	0	ExplicitControlLane4		
149	7-4	AppSelCodeLane5	**SCS0::DPConfigLane5** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane5		
	0	ExplicitControlLane5		
150	7-4	AppSelCodeLane6	**SCS0::DPConfigLane6** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane6		
	0	ExplicitControlLane6		
151	7-4	AppSelCodeLane7	**SCS0::DPConfigLane7** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane7		
	0	ExplicitControlLane7		
152	7-4	AppSelCodeLane8	**SCS0::DPConfigLane8** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane8		
	0	ExplicitControlLane8		

DPSM Provisioning: Application Modes

Example of provisioning a 4x 100G DR Applications

AppSel 3

Host Electrical Interface: 100GAUI-2 C2M ; 0x0D

Module Media Interface: 100GBASE-DR; 0x14

Byte	Bits	Field Name	Bit Value	Hex Value
145	7-4	AppSelCodeLane1	0011	0x30
	3-1	DataPathIDLane1	000	
	0	ExplicitControlLane1	0	
146	7-4	AppSelCodeLane2	0011	0x30
	3-1	DataPathIDLane2	000	
	0	ExplicitControlLane2	0	
147	7-4	AppSelCodeLane3	0011	0x34
	3-1	DataPathIDLane3	010	
	0	ExplicitControlLane3	0	
148	7-4	AppSelCodeLane4	0011	0x34
	3-1	DataPathIDLane4	010	
	0	ExplicitControlLane4	0	
149	7-4	AppSelCodeLane5	0011	0x38
	3-1	DataPathIDLane5	100	
	0	ExplicitControlLane5	0	

100GE

100GE

Upper Memory Page 10h

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	3-1	DataPathIDLane1		
	0	ExplicitControlLane1		
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	3-1	DataPathIDLane2		
	0	ExplicitControlLane2		
147	7-4	AppSelCodeLane3	**SCS0::DPConfigLane3** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane3		
	0	ExplicitControlLane3		
148	7-4	AppSelCodeLane4	**SCS0::DPConfigLane4** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane4		
	0	ExplicitControlLane4		
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	3-1	DataPathIDLane5		
	0	ExplicitControlLane5		
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	3-1	DataPathIDLane6		
	0	ExplicitControlLane6		
151	7-4	AppSelCodeLane7	**SCS0::DPConfigLane7** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane7		
	0	ExplicitControlLane7		
152	7-4	AppSelCodeLane8	**SCS0::DPConfigLane8** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane8		
	0	ExplicitControlLane8		

DPSM Provisioning: Signal Integrity Controls

Data Path Signal Integrity Related Controls

Electrical Interface Signal Control options are available and controlled through the Stage Control Set mechanisms.

Control Options:

1. **Tx Input Equalization Control**
   - **Adaptive Equalization**
   - **Fixed Equalization**
2. **Rx Output Equalization Control**
   - **Adaptive Equalization**
   - **Fixed Equalization**
3. **Rx Output Amplitude Control**
4. **CDR**

Upper Memory Page 10h

Tx Controls: 153-160

Table 8-66 Staged Control Set 0, Tx Controls (Page 10h)

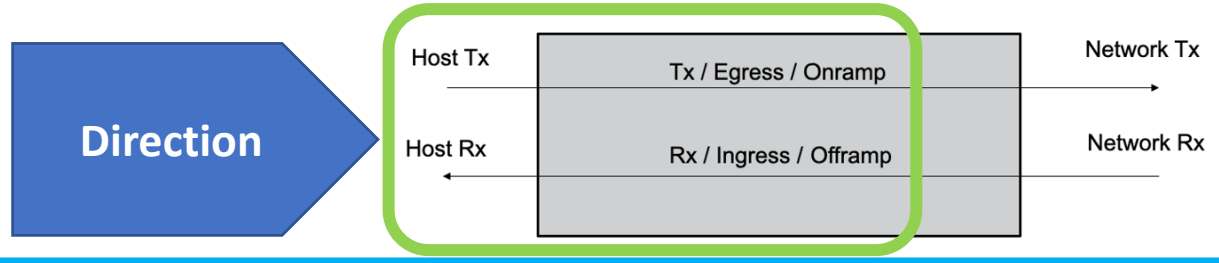
Byte	Bits	Field Name	Register Description	Type
153	7	AdaptiveInputEqEnableTx8	**SCS0::AdaptiveInputEqEnableTx<i>**	RW
	6	AdaptiveInputEqEnableTx7	Adaptive input equalizer for host lane <i>	Adv.
	5	AdaptiveInputEqEnableTx6	1b: Enable adaptive Tx input equalization	
	4	AdaptiveInputEqEnableTx5	0b: Disable (use manual fixed equalizer)	
	3	AdaptiveInputEqEnableTx4		
	2	AdaptiveInputEqEnableTx3	Advertisement: 01h:161.3	
	1	AdaptiveInputEqEnableTx2		
	0	AdaptiveInputEqEnableTx1		
154	7-6	AdaptiveInputEqRecallTx4	**SCS0::AdaptiveInputEqRecallTx<i>**	RW
	5-4	AdaptiveInputEqRecallTx3	Recall stored Tx input equalizer adaptation settings for host	Adv.
	3-2	AdaptiveInputEqRecallTx2	lane <i> when Staged Control Set is copied to Active	
	1-0	AdaptiveInputEqRecallTx1	Control Set. *See section 6.2.5.4 for Store/Recall mechanism*	
155	7-6	AdaptiveInputEqRecallTx8	00b: do not recall	RW
	5-4	AdaptiveInputEqRecallTx7	01b: recall buffer 1	Adv.
	3-2	AdaptiveInputEqRecallTx6	10b: recall buffer 2	
	1-0	AdaptiveInputEqRecallTx5	11b: reserved	
			Advertisement: 01h:161.6-5	
156	7-4	FixedInputEqTargetTx2	**SCS0::FixedInputEqTargetTx<i>**	RW
	3-0	FixedInputEqTargetTx1	Manual fixed Tx input equalizer control	Adv.
157	7-4	FixedInputEqTargetTx4		RW
	3-0	FixedInputEqTargetTx3	Advertisement: 01h:161.2	Adv.
158	7-4	FixedInputEqTargetTx6		RW
	3-0	FixedInputEqTargetTx5		Adv.
159	7-4	FixedInputEqTargetTx8		RW
	3-0	FixedInputEqTargetTx7		Adv.
160	7	CDREnableTx8	**SCS0::CDREnableTx<i>**	RW
	6	CDREnableTx7	1b: CDR enabled	Adv.
	5	CDREnableTx6	0b: CDR bypassed	
	4	CDREnableTx5		
	3	CDREnableTx4	Advertisement: 01h:161.0-1	
	2	CDREnableTx3		
	1	CDREnableTx2		
	0	CDREnableTx1		

Rx Controls: 153-160

Table 8-67 Staged Control Set 0, Rx Controls (Page 10h)

Byte	Bits	Name	Register Description	Type
161	7	CDREnableRx8	**SCS0::CDREnableRx<i>**	RW
	6	CDREnableRx7	1b: CDR enabled	Adv.
	5	CDREnableRx6	0b: CDR bypassed	
	4	CDREnableRx5		
	3	CDREnableRx4	Advertisement: 01h:162.0-1	
	2	CDREnableRx3		
	1	CDREnableRx2		
	0	CDREnableRx1		
162	7-4	OutputEqPreCursorTargetRx2	**SCS0::OutputEqPreCursorTargetRx<i>**	RW
	3-0	OutputEqPreCursorTargetRx1	Rx output equalization pre-cursor target	Adv.
163	7-4	OutputEqPreCursorTargetRx4	See Table 6-7	RW
	3-0	OutputEqPreCursorTargetRx3		Adv.
164	7-4	OutputEqPreCursorTargetRx6	Advertisement: 01h:162.4-3	RW
	3-0	OutputEqPreCursorTargetRx5		Adv.
165	7-4	OutputEqPreCursorTargetRx8		RW
	3-0	OutputEqPreCursorTargetRx7		Adv.
166	7-4	OutputEqPostCursorTargetRx2	**SCS0::OutputEqPostCursorTargetRx<i>**	RW
	3-0	OutputEqPostCursorTargetRx1	Rx output equalization post-cursor target	Adv.
167	7-4	OutputEqPostCursorTargetRx4	See Table 6-7	RW
	3-0	OutputEqPostCursorTargetRx3		Adv.
168	7-4	OutputEqPostCursorTargetRx6	Advertisement: 01h:162.4-3	RW
	3-0	OutputEqPostCursorTargetRx5		Adv.
169	7-4	OutputEqPostCursorTargetRx8		RW
	3-0	OutputEqPostCursorTargetRx7		Adv.
170	7-4	OutputAmplitudeTargetRx2	**SCS0::OutputAmplitudeTargetRx<i>**	RW
	3-0	OutputAmplitudeTargetRx1	Rx output amplitude target	Adv.
171	7-4	OutputAmplitudeTargetRx4	See Table 6-8	RW
	3-0	OutputAmplitudeTargetRx3		Adv.
172	7-4	OutputAmplitudeTargetRx6	Advertisement: 01h:162.2	RW
	3-0	OutputAmplitudeTargetRx5		Adv.
173	7-4	OutputAmplitudeTargetRx8		RW
	3-0	OutputAmplitudeTargetRx7		Adv.
174-175	All	-	**Reserved[2]**	RO

Don't Forget! Data Path configurations of a Staged Control Set have no effect on the behavior of a lane until the Host has successfully triggered ApplyDPInit for the lane.



DPSM Provisioning and Commissioning

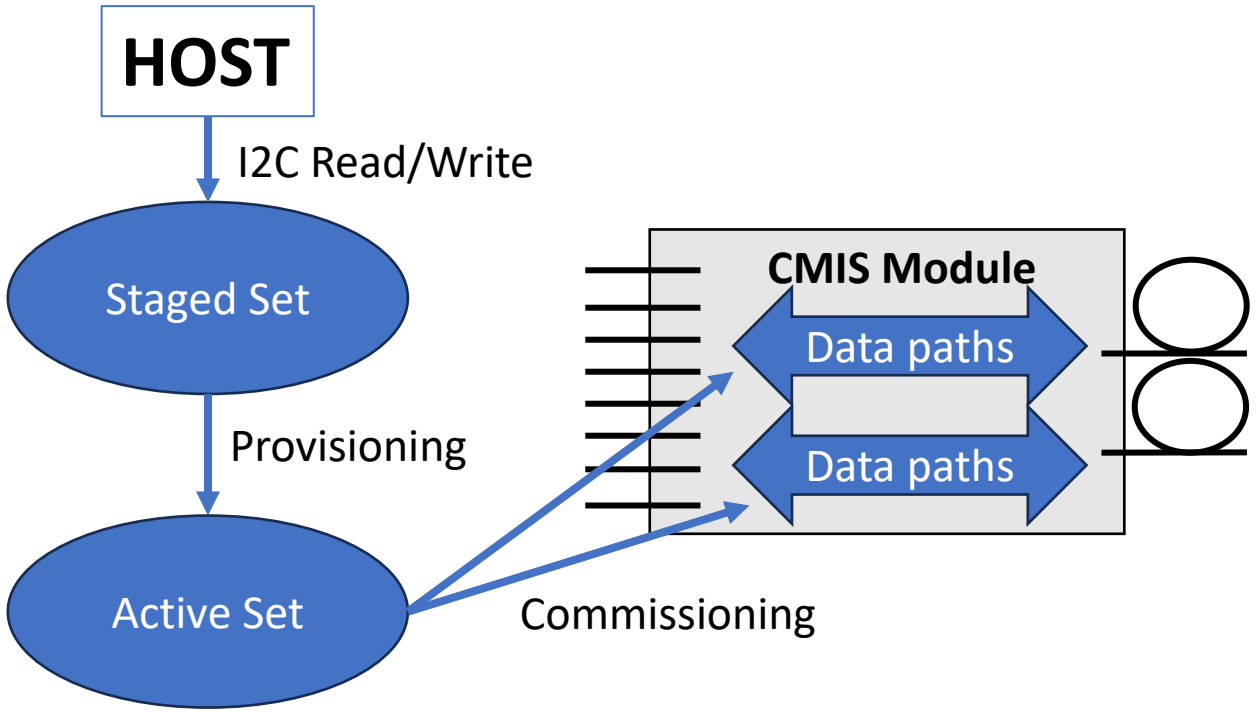
The DPSM is the key to configure the module by providing a controlled communication sequence between host and module.

The configuration includes options to change the active Application, the Lane assignments, and manage the signal integrity.

Key Terms

1. **Staged Set = a Host configurable set**
2. **Active Set = a valid configuration set**

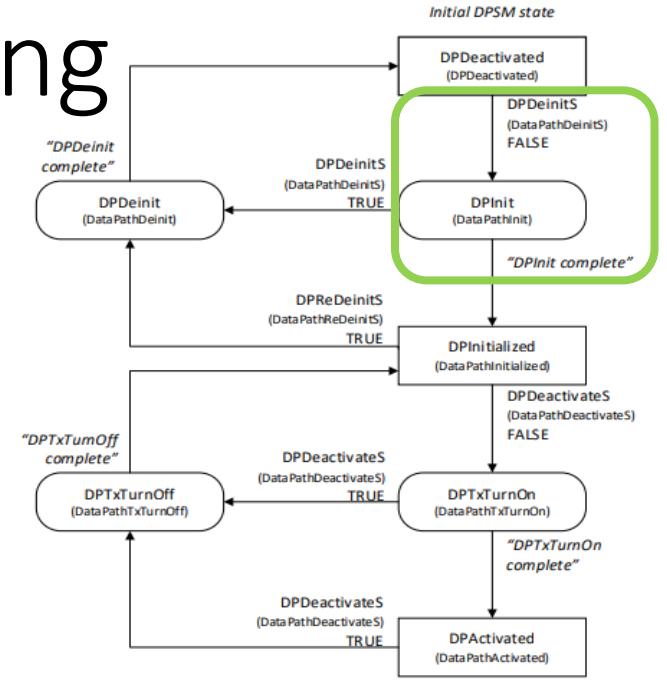
3. **Provisioning = the Host requests the module copy the Stage Set configuration into the Active Set, then modules validates the configuration and copies a valid configuration into the Active Set**
   "The host tells the module what it wants & modules validates"
4. **Commissioning = upon the module entering the DPSM state DPInit, the module initializes the Data path based on the Active Set configuration by allocating HW resources**
   "The module acts on the Active Set!"



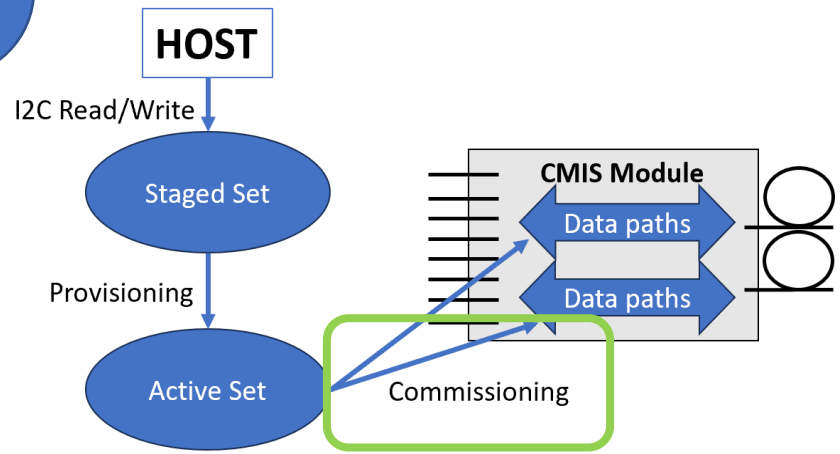
DPSM Provisioning and Commissioning

How to trigger the Provisioning and Commissioning Process

- The Host can configure the Data Paths when the DPSM is in State 1h – DPDeactivated.
- Changes to Data Path configurations of a Staged Control Set have no effect on the behavior of the Active Set until the Host has successfully triggered ApplyDPInit per Data Path.
- If the module rejects the Stage Set configuration during Provisioning, then the Active Set remains unchanged.
- Provisioning feedback is provided by the module in
- An Example: CMIS 5.2 Appendix D.1.3 Software Configuration and Initialization

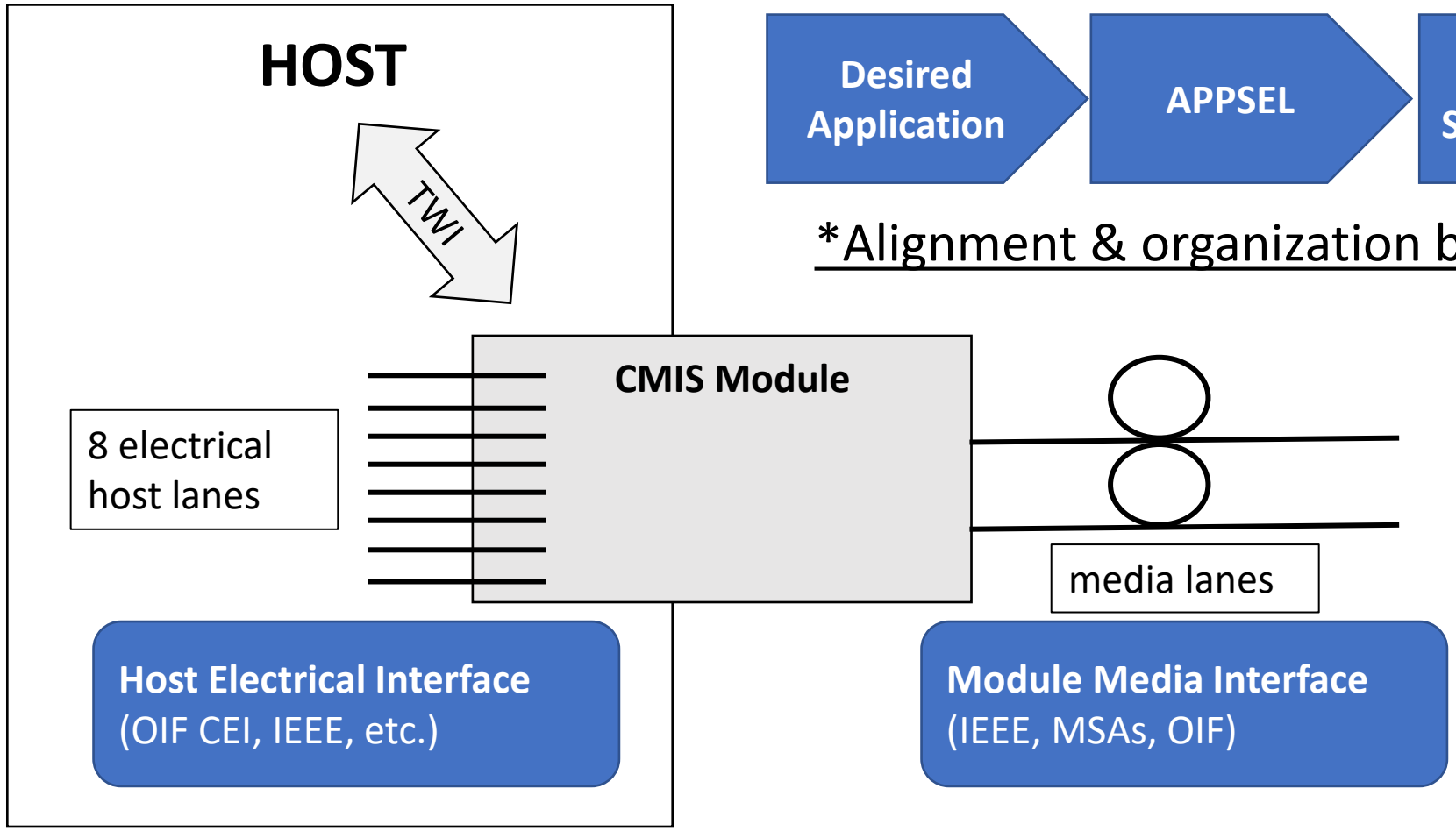


Control Command	Data Path State	Host Requests	Modules Reaction
ApplyDPInit (Stage Ctrl 0 = 10h:143)	DPDeactivated	Apply = "Provision only", afterwards the Host initializes the Data path	Module validates the Stage Set& copies into the Active Set, then waits on the Host to "commission" the configuration into HW during DPInit state



*An alternative method to trigger a new lane configuration is with ApplyImmediate

How are Applications advertised in CMIS?



Desired Application → APPSEL → Data Path Stage Control → Module utilizes Application

Alignment & organization between all points is needed

Application Code definitions:
Standard Host and Media Interface ID codes are referenced in SFF-8024
Vendor Specific/Custom MediainterfaceID codes are assigned C0h-FFh

The Anatomy of an Appsel

Appsel are a list of addresses held within the module which advertise the device's different application capability.
Each Appsel is composed of Application Descriptors that provide information to the Host on each Application option.
The Appsel list can be quickly interpreted by the Host to produce a clear list of Application capabilities.

Application Descriptors come in Five Parts

1. **HostInterfaceID: the Host (to Module) interface including signal rate, modulation format, and lane count(s)**
2. **MediaInterfaceID: the module media interface signaling rate, modulation format, and standard-defined lane count(s)**
3. **Lane Counts: the number of host and media lanes per application**
4. **HostLaneAssignmentOptions: the lanes where the application is supported on the module's host interface**
5. **MediaLaneAssignmentOptions: the number of media lanes supported in that application**

1 3 4 2 5

App. Code	Electr. Code [Hex]	Application Name	Host LC	Lane Ass. [Hex]	Media Code [Hex]	Application Name	Media LC
1	0011	400GAUI-8 C2M	8	0001	003E	400ZR, DWDM	1
2	0011	400GAUI-8 C2M	8	0001	003F	400ZR,SW,unampl.	1
3	000D	100GAUI-2 C2M	2	0055	003E	400ZR, DWDM	1
4	0011	400GAUI-8 C2M	8	0001	00C5	Custom	1
5	0011	400GAUI-8 C2M	8	0001	00C0	Custom	1
6	000D	100GAUI-2 C2M	2	0055	00C0	Custom	1
7	000D	100GAUI-2 C2M	2	0055	00C1	Custom	1
8	000D	100GAUI-2 C2M	2	0055	00C2	Custom	1
9	0041	CAUI-4 C2M noFec	4	0011	00C2	Custom	1
10	000D	100GAUI-2 C2M	2	0055	00C4	Custom	1
11	0041	CAUI-4 C2M noFec	4	0011	00C4	Custom	1
12	0011	400GAUI-8 C2M	8	0001	00C1	Custom	1
13	0041	CAUI-4 C2M noFec	4	0011	00CD	Custom	1
14	0011	400GAUI-8 C2M	8	0001	00C7	Custom	1
15	00D0	Custom	0	0000	00D0	Custom	0

Where to check Application Descriptors and Appsels?

The Appsel list has a defined location in the CMIS memory map.

Low Memory Page

Table 8-4 Lower Memory Overview

Address	Size	Subject Area	Description
0–2	3	Management Characteristics	Basic Information about how this module is managed
3	1	Global Status Information	Current state of Module, Interrupt signal status
4–7	4	Flags Summary	Summary of Flags set on specific Pages (and Banks)
8-13	6	Module-Level Flags	Flags that are not lane or Data Path specific
14-25	12	Module-Level Monitors	Monitors that are not lane or Data Path specific
26-30	5	Module-Level Controls	Controls applicable to the module as a whole
31-36	6	Module-Level Masks	Mask bits for the Module-Level Flags
37-38	2	CDB Command Status	Status of current CDB command
39-40	2	Module Active Firmware Version	Module Active Firmware Version number
41	1	Fault Information	Fault cause for entering ModuleFault state
42-63	22	-	**Reserved[22]**
64-84	21	-	**Custom[21]**
85-117	33	Supported Applications Advertising	Applications supported by module Data Path(s)
118-125	8	Password Facilities	Password Entry and Change (mechanism only)
126-127	2	Page Mapping	Page mapping into host addressable Upper Memory

Specific Registers

Table 8-20 Application Descriptor Registers Bytes 1-4 (Lower Memory)

Byte	Bits	Field Name	Register Description	Type
86	7-0	HostInterfaceIDApp1	**AppDescriptor1** AppSel 1 (0001b) See Table 8-19	RO Rqd.
87	7-0	MediaInterfaceIDApp1		
88	7-4	HostLaneCountApp1		
	3-0	MediaLaneCountApp1		
89	7-0	HostLaneAssignmentOptionsApp1		
90	7-0	HostInterfaceIDApp2	**AppDescriptor2** AppSel 2 (0010b) See Table 8-19	RO Rqd.
91	7-0	MediaInterfaceIDApp2		
92	7-4	HostLaneCountApp2		
	3-0	MediaLaneCountApp2		
93	7-0	HostLaneAssignmentOptionsApp2		
94	7-0	HostInterfaceIDApp3	**AppDescriptor3** AppSel 3 (0011b) See Table 8-19	RO Cnd.
95	7-0	MediaInterfaceIDApp3		
96	7-4	HostLaneCountApp3		
	3-0	MediaLaneCountApp3		
97	7-0	HostLaneAssignmentOptionsApp3		
98	7-0	HostInterfaceIDApp4	**AppDescriptor4** AppSel 4 (0100b) See Table 8-19	RO Cnd.
99	7-0	MediaInterfaceIDApp4		
100	7-4	HostLaneCountApp4		
	3-0	MediaLaneCountApp4		
101	7-0	HostLaneAssignmentOptionsApp4		
102	7-0	HostInterfaceIDApp5	**AppDescriptor5** AppSel 5 (0101b) See Table 8-19	RO Cnd.
103	7-0	MediaInterfaceIDApp5		
104	7-4	HostLaneCountApp5		
	3-0	MediaLaneCountApp5		
105	7-0	HostLaneAssignmentOptionsApp5		
106	7-0	HostInterfaceIDApp6	**AppDescriptor6** AppSel 6 (0110b) See Table 8-19	RO Cnd.
107	7-0	MediaInterfaceIDApp6		
108	7-4	HostLaneCountApp6		
	3-0	MediaLaneCountApp6		
109	7-0	HostLaneAssignmentOptionsApp6		
110	7-0	HostInterfaceIDApp7	**AppDescriptor7** AppSel 7 (0111b) See Table 8-19	RO Cnd.
111	7-0	MediaInterfaceIDApp7		
112	7-4	HostLaneCountApp7		
	3-0	MediaLaneCountApp7		
113	7-0	HostLaneAssignmentOptionsApp7		
114	7-0	HostInterfaceIDApp8	**AppDescriptor8** AppSel 8 (1000b) See Table 8-19	RO Cnd.
115	7-0	MediaInterfaceIDApp8		
116	7-4	HostLaneCountApp8		
	3-0	MediaLaneCountApp8		
117	7-0	HostLaneAssignmentOptionsApp8		

Where to check Application Descriptors and Appsels?

The Appsel list has a defined location in the CMIS memory map.

Upper Memory Page 01h

Table 8-37 Page 01h Overview

Byte	Size (bytes)	Subject Area	Description
128-131	4	Inactive Firmware and Hardware revisions	Inactive FW revision and HW revision
132-137	6	Supported link length	Supported lengths of various fiber media
138-141	4	Wavelength Information	(for single wavelength modules)
142	1	Supported Pages	
143-144	2	Durations Advertisements	
145-154	10	Module Characteristics	
155-156	2	Supported Controls	
157-158	2	Supported Flags	
159-160	2	Supported Monitors	
161-162	2	Supported Signal Integrity Controls	
163-166	4	Supported CDB Functionality	
167-169	3	Additional Durations Advertisements	
170-175	7	-	**Reserved[7]**
176-190	15	Media Lane advertising	
191-222	32	-	**Custom[32]**
223-250	28	Additional Application Descriptors	
251-254	4	-	**Reserved[4]**
255	1	Page Checksum	Page Checksum of bytes 130-254[1]

Specific Registers

Table 8-53 Additional Application Descriptor Registers (Page 01h)

Byte	Bits	Field Name	Register Description	Type
223	7-0	HostInterfaceIDApp9	**AppDescriptor9** AppSel 9 (1001b) See Table 8-19	RO Cnd.
224	7-0	MediaInterfaceIDApp9		
225	7-4	HostLaneCountApp9		
	3-0	MediaLaneCountApp9		
226	7-0	HostLaneAssignmentOptionsApp9		
227	7-0	HostInterfaceIDApp10	**AppDescriptor10** AppSel 10 (1010b) See Table 8-19	RO Cnd.
228	7-0	MediaInterfaceIDApp10		
229	7-4	HostLaneCountApp10		
	3-0	MediaLaneCountApp10		
230	7-0	HostLaneAssignmentOptionsApp10		
231	7-0	HostInterfaceIDApp11	**AppDescriptor11** AppSel 11 (1011b) See Table 8-19	RO Cnd.
232	7-0	MediaInterfaceIDApp11		
233	7-4	HostLaneCountApp11		
	3-0	MediaLaneCountApp11		
234	7-0	HostLaneAssignmentOptionsApp11		
235	7-0	HostInterfaceIDApp12	**AppDescriptor12** AppSel 12 (1100b) See Table 8-19	RO Cnd.
236	7-0	MediaInterfaceIDApp12		
237	7-4	HostLaneCountApp12		
	3-0	MediaLaneCountApp12		
238	7-0	HostLaneAssignmentOptionsApp12		
239	7-0	HostInterfaceIDApp13	**AppDescriptor13** AppSel 13 (1101b) See Table 8-19	RO Cnd.
240	7-0	MediaInterfaceIDApp13		
241	7-4	HostLaneCountApp13		
	3-0	MediaLaneCountApp13		
242	7-0	HostLaneAssignmentOptionsApp13		
243	7-0	HostInterfaceIDApp14	**AppDescriptor14** AppSel 14 (1110b) See Table 8-19	RO Cnd.
244	7-0	MediaInterfaceIDApp14		
245	7-4	HostLaneCountApp14		
	3-0	MediaLaneCountApp14		
246	7-0	HostLaneAssignmentOptionsApp14		
247	7-0	HostInterfaceIDApp15	**AppDescriptor15** AppSel 15 (1111b) See Table 8-19	RO Cnd.
248	7-0	MediaInterfaceIDApp15		
249	7-4	HostLaneCountApp15		
	3-0	MediaLaneCountApp15		
250	7-0	HostLaneAssignmentOptionsApp15		

Same as Data Path Provisioning!

Application Configuration – Data Path Control Sets

Data Path Configuration Fields

1. **AppSelCode<i> is the AppSel Number that the module advertises in the Low Memory Page and Upper Memory Page 01h**
2. **DataPathID<i> is the Data Path lane assigned**
3. **Explicit Control: If lane is unused, the field is ignored**
   - **0b: Use Application-dependent settings for lane**
   - **1b: Use Staged Control Set 0 control values for lane**

- The Host configures different applications by selecting an Appsel Code based on the module's advertisements
- Each Data Path lane is individually configured
- The Host can configure the Data Path lane(s) when the DPSM is in State 1h – DPDeactivated

Don't Forget! Data Path configurations of a Staged Control Set have no effect on the behavior of a lane until the Host has successfully triggered ApplyDPInit for the lane.

Upper Memory Page 10h

Table 8-65 Staged Control Set 0, Data Path Configuration (Page 10h)

Byte	Bits	Field Name	Register Description	Type
145	7-4	AppSelCodeLane1	**SCS0::DPConfigLane1** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane1		
	0	ExplicitControlLane1		
146	7-4	AppSelCodeLane2	**SCS0::DPConfigLane2** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane2		
	0	ExplicitControlLane2		
147	7-4	AppSelCodeLane3	**SCS0::DPConfigLane3** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane3		
	0	ExplicitControlLane3		
148	7-4	AppSelCodeLane4	**SCS0::DPConfigLane4** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane4		
	0	ExplicitControlLane4		
149	7-4	AppSelCodeLane5	**SCS0::DPConfigLane5** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane5		
	0	ExplicitControlLane5		
150	7-4	AppSelCodeLane6	**SCS0::DPConfigLane6** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane6		
	0	ExplicitControlLane6		
151	7-4	AppSelCodeLane7	**SCS0::DPConfigLane7** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane7		
	0	ExplicitControlLane7		
152	7-4	AppSelCodeLane8	**SCS0::DPConfigLane8** See Table 8-64	RW Rqd.
	3-1	DataPathIDLane8		
	0	ExplicitControlLane8		

Application Examples

Coherent Module

App. Code	Electr. Code [Hex]	Application Name	Host LC	Lane Ass. [Hex]	Media Code [Hex]	Application Name	Media LC
1	001D	400G CR8	8	0001	003E	400ZR, DWDM	1
2	0011	400GAUI-8 C2M	8	0001	003E	400ZR, DWDM	1
3	000F	200GAUI-4 C2M	4	0011	003E	400ZR, DWDM	1
4	000D	100GAUI-2 C2M	2	0055	003E	400ZR, DWDM	1
5	000A	50GAUI-1 C2M	1	00FF	003E	400ZR, DWDM	1
6	003C	FOIC1.2	2	0055	003E	400ZR, DWDM	1
7	0040	FOIC4.8	8	0001	003E	400ZR, DWDM	1
8	000E	200GAUI-8 C2M	8	0001	003E	400ZR, DWDM	1
9	003B	FOIC1.4	4	0011	003E	400ZR, DWDM	1
10	003E	FOIC2.4	4	0011	003E	400ZR, DWDM	1
11	0046	100GBASE-CR1	1	00FF	003E	400ZR, DWDM	1
12	0047	200GBASE-CR2	2	0055	003E	400ZR, DWDM	1
13	0048	400GBASE-CR4	4	0011	003E	400ZR, DWDM	1
14	0049	800GBASE-CR8	8	0001	003E	400ZR, DWDM	1
15	00FF	End of List	0	0000	0000	Undefined	0

Coherent 400ZR Module

App. Code	Electr. Code [Hex]	Application Name	Host LC	Lane Ass. [Hex]	Media Code [Hex]	Application Name	Media LC
1	0011	400GAUI-8 C2M	8	0001	003E	400ZR, DWDM	1
2	0011	400GAUI-8 C2M	8	0001	003F	400ZR,SW,unampl.	1
3	000D	100GAUI-2 C2M	2	0055	003E	400ZR, DWDM	1
4	0011	400GAUI-8 C2M	8	0001	00C5	Custom	1
5	0011	400GAUI-8 C2M	8	0001	00C0	Custom	1
6	000D	100GAUI-2 C2M	2	0055	00C0	Custom	1
7	000D	100GAUI-2 C2M	2	0055	00C1	Custom	1
8	000D	100GAUI-2 C2M	2	0055	00C2	Custom	1
9	0041	CAUI-4 C2M noFec	4	0011	00C2	Custom	1
10	000D	100GAUI-2 C2M	2	0055	00C4	Custom	1
11	0041	CAUI-4 C2M noFec	4	0011	00C4	Custom	1
12	0011	400GAUI-8 C2M	8	0001	00C1	Custom	1
13	0041	CAUI-4 C2M noFec	4	0011	00CD	Custom	1
14	0011	400GAUI-8 C2M	8	0001	00C7	Custom	1
15	00D0	Custom	0	0000	00D0	Custom	0

IMDD DR4 Module

App. Code	Electr. Code [Hex]	Application Name	Host LC	Lane Ass. [Hex]	Media Code [Hex]	Application Name	Media LC
1	000D	100GAUI-2 C2M	2	0055	0015	100G-FR	1
2	0011	400GAUI-8 C2M	8	0001	001C	400GBASE-DR4	4
3	00FF	End of List	0	0000	0000	Undefined	0
4	0000	Undefined	0	0000	0000	Undefined	0
5	0000	Undefined	0	0000	0000	Undefined	0
6	0000	Undefined	0	0000	0000	Undefined	0
7	0000	Undefined	0	0000	0000	Undefined	0
8	0000	Undefined	0	0000	0000	Undefined	0
9	0000	Undefined	0	0000	0000	Undefined	0
10	0000	Undefined	0	0000	0000	Undefined	0
11	0000	Undefined	0	0000	0000	Undefined	0
12	0000	Undefined	0	0000	0000	Undefined	0
13	0000	Undefined	0	0000	0000	Undefined	0
14	0000	Undefined	0	0000	0000	Undefined	0
15	0000	Undefined	0	0000	0000	Undefined	0

IMDD FR4 Module

App. Code	Electr. Code [Hex]	Application Name	Host LC	Lane Ass. [Hex]	Media Code [Hex]	Application Name	Media LC
1	0011	400GAUI-8 C2M	8	0001	001D	400G-FR4	4
2	00FF	End of List	0	0000	0000	Undefined	0
3	0000	Undefined	0	0000	0000	Undefined	0
4	0000	Undefined	0	0000	0000	Undefined	0
5	0000	Undefined	0	0000	0000	Undefined	0
6	0000	Undefined	0	0000	0000	Undefined	0
7	0000	Undefined	0	0000	0000	Undefined	0
8	0000	Undefined	0	0000	0000	Undefined	0
9	0000	Undefined	0	0000	0000	Undefined	0
10	0000	Undefined	0	0000	0000	Undefined	0
11	0000	Undefined	0	0000	0000	Undefined	0
12	0000	Undefined	0	0000	0000	Undefined	0
13	0000	Undefined	0	0000	0000	Undefined	0
14	0000	Undefined	0	0000	0000	Undefined	0
15	0000	Undefined	0	0000	0000	Undefined	0

Copper Modules

QSFP passive copper cable assy (byte 85=03h) – 1 AppSel
- Host code – 48h – 400GBASE-CR4
- TX Lanes – 4
- Host Lane assign opt = 01h
- Media code – 01h – copper cable
- Meda lanes - 4

QSFP-DD passive copper cable assy (byte 85=03h) – 1 AppSel
- Host code – 49h – 800GBASE-CR8
- TX Lanes – 8
- Host Lane assign opt = 01h
- Media code – 01h – copper cable
- Meda lanes - 8

Thank You