448G Signaling: Trade-offs between SNR, FEC, and channel loss

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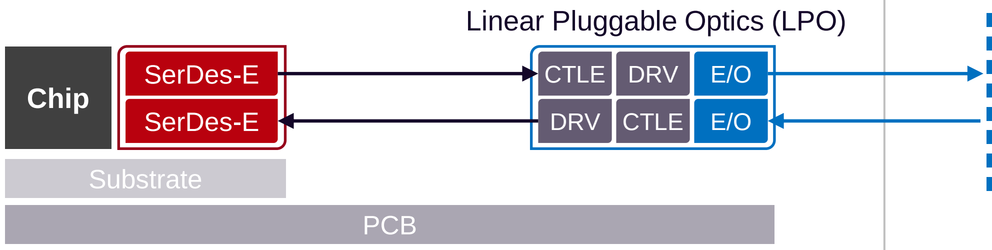
Agenda

1. Silicon results for 448Gb/s at PAM4, PAM6, PAM8
2. FEC and SNR trade-offs vs. cardinality (PAM4, PAM6, PAM8)
3. 50dB Channel compensation vs DSP, FEC
4. Microstrip flex interconnect
5. 3.2T 8x448G DR8 and FR8

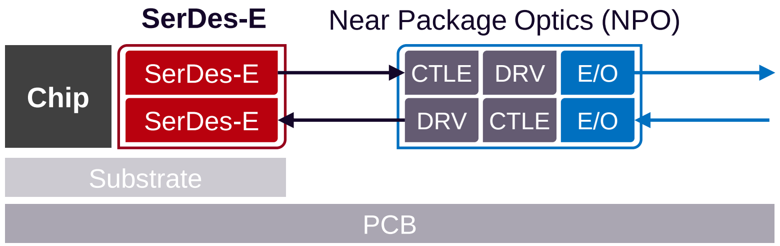
448G SerDes Applications

Possible implementation options

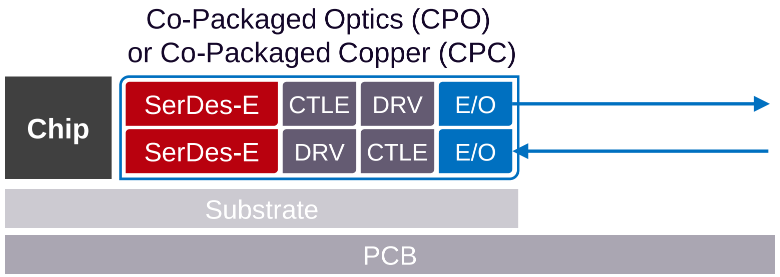
Chip to Pluggable Modules (LPO)



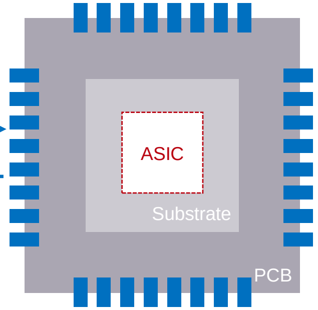
Chip to Pluggable Modules (NPO)

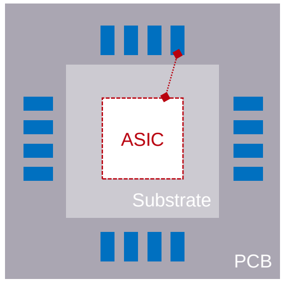


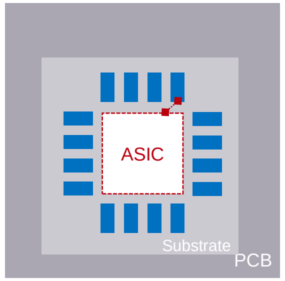
Chip to Nearby Optical/Electrical Engine (CPO/CPC)

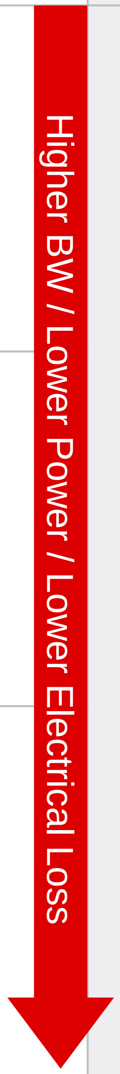


Top-view





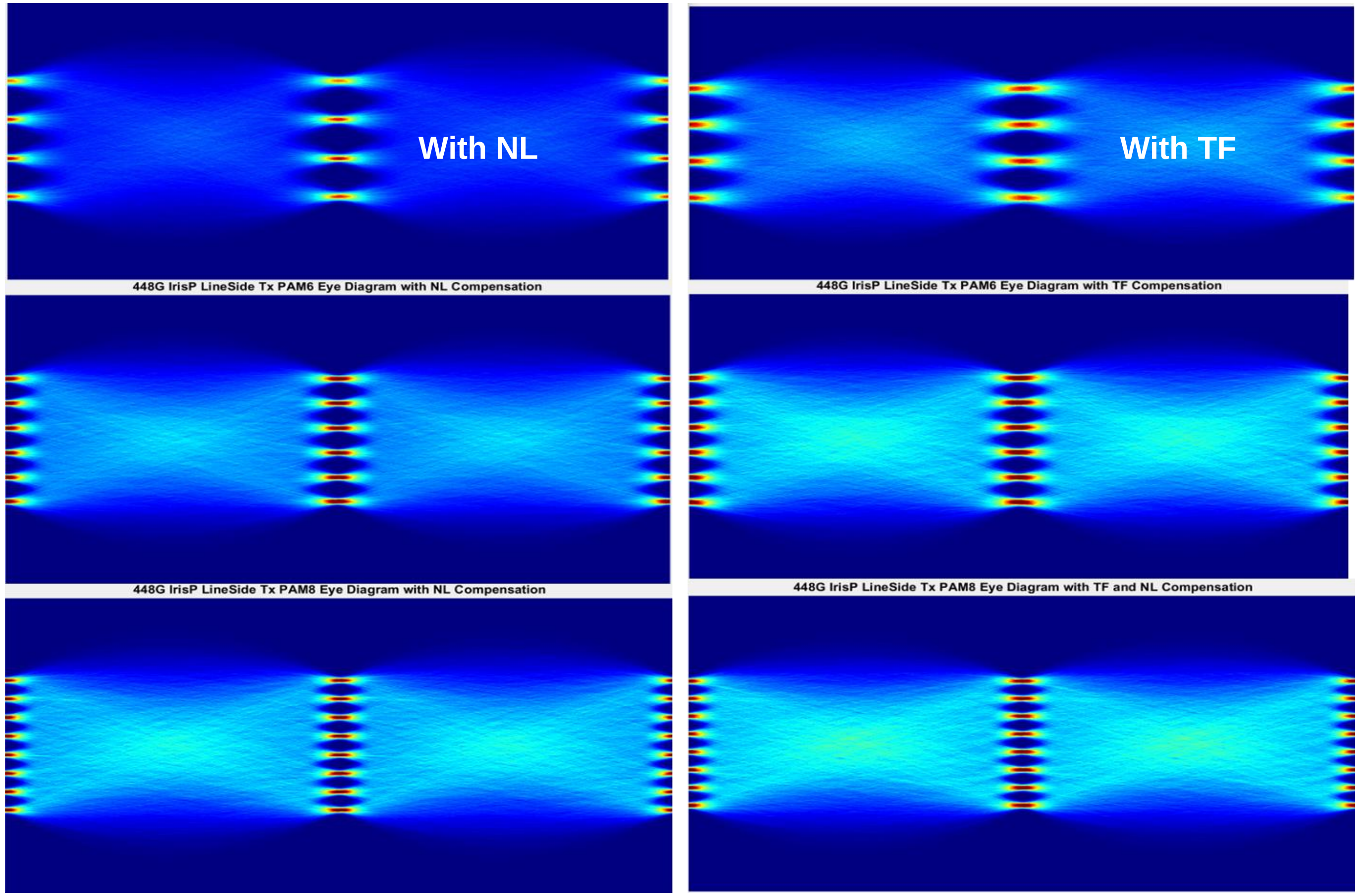




Problem Statement

- Loss profile increases significantly moving from 224 to 448G
- Trade-off between Electrical BW and FEC performance is required
- Two key dimensions:
  - Moving the interface close to the I/O increases available options e.g. CPO
  - Looking at different technologies to use the link budget in the most optical way e.g. Microstrip flex

Measured Tx Eyes for 448Gb/s in PAM4/6/8



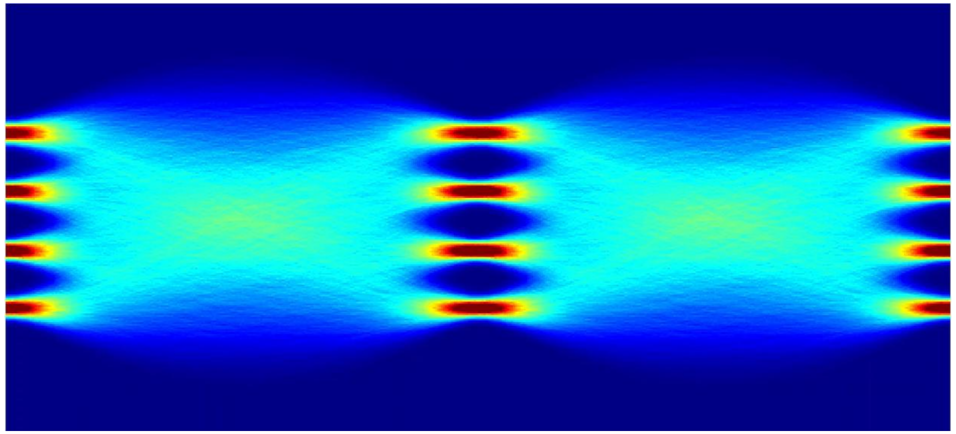
PAM4
Baud rate: 225G
SNDR: 25.6dB

PAM6
Baud rate: 175G
SNDR: 27.9dB

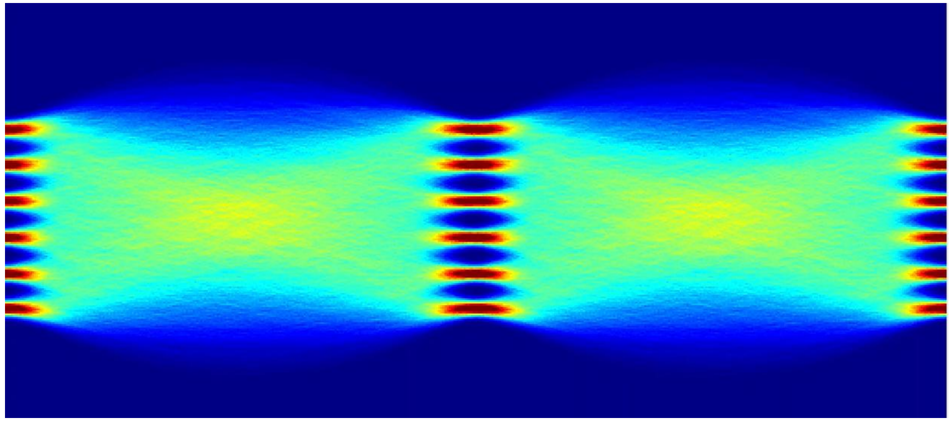
PAM8
Baud rate: 150G
SNDR: 28.5dB

Improvement of SNR does not justify the increase in cardinality

Loop back 448G eye diagrams: Tx to Rx



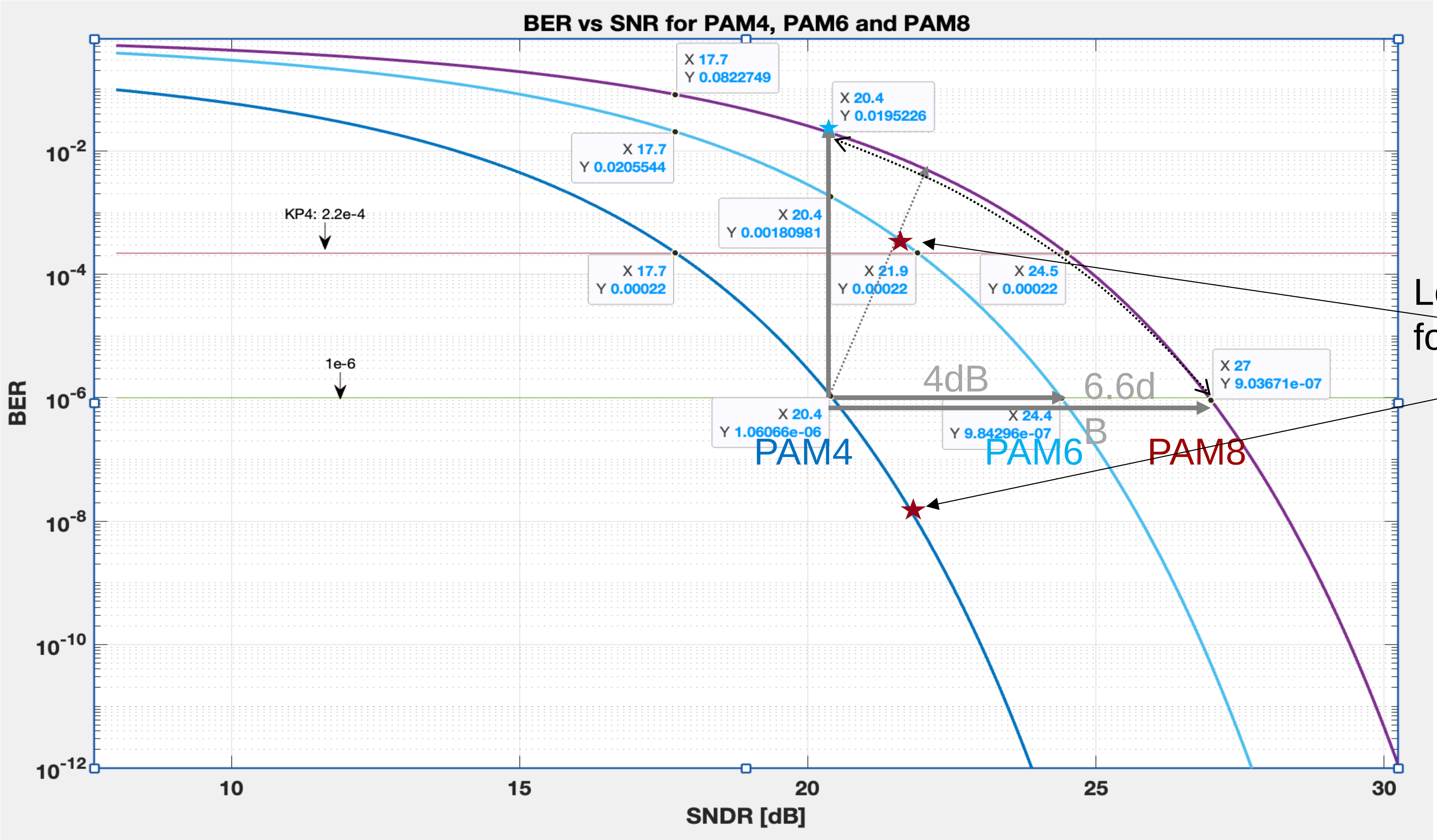
PAM4: 448Gb/s Received eye diagram
Baud rate: 224G



PAM6: 448Gb/s Received eye diagram
Baud rate: 173.4G

PAM4 is performing better than PAM6 in a loop back with 25dB channel

BER vs SNR for PAM4-6-8



Loopback performance for PAM6 and PAM4

448Gb/s: PAM4/6/8

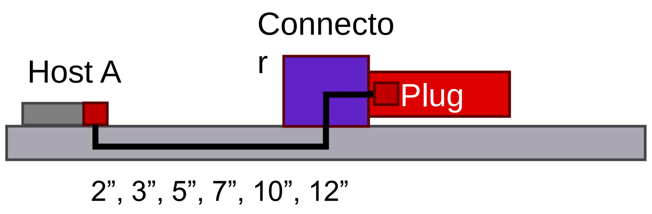
Figure of Merit		PAM-4	PAM-6	PAM-8
Constant BER	Baud rate	224G	173G	150G
	SNR [dB]	20.4	24.4	27
	BER	1e-6	1e-6	1e-6
	Latency	KP4	KP4	KP4
Constant SNR	Baud	224G	200G?	190G?
	SNR	17.7	17.7	17.7
	BER	2.2e-4	2e-2 [OFEC]	8.2e-2
	Latency	KP4	1us [OFEC]	-
	FEC power [pJ/bit]	0.25	~2 [OFEC]	-

Power → For long reach SerDes requiring a larger number of taps, advanced and efficient DSP implementation are required. Frequency domain filtering is a possibility

Latency → Advanced FEC adds to the latency, but it can be minimized

448G SerDes Simulation for Bump-to-Bump

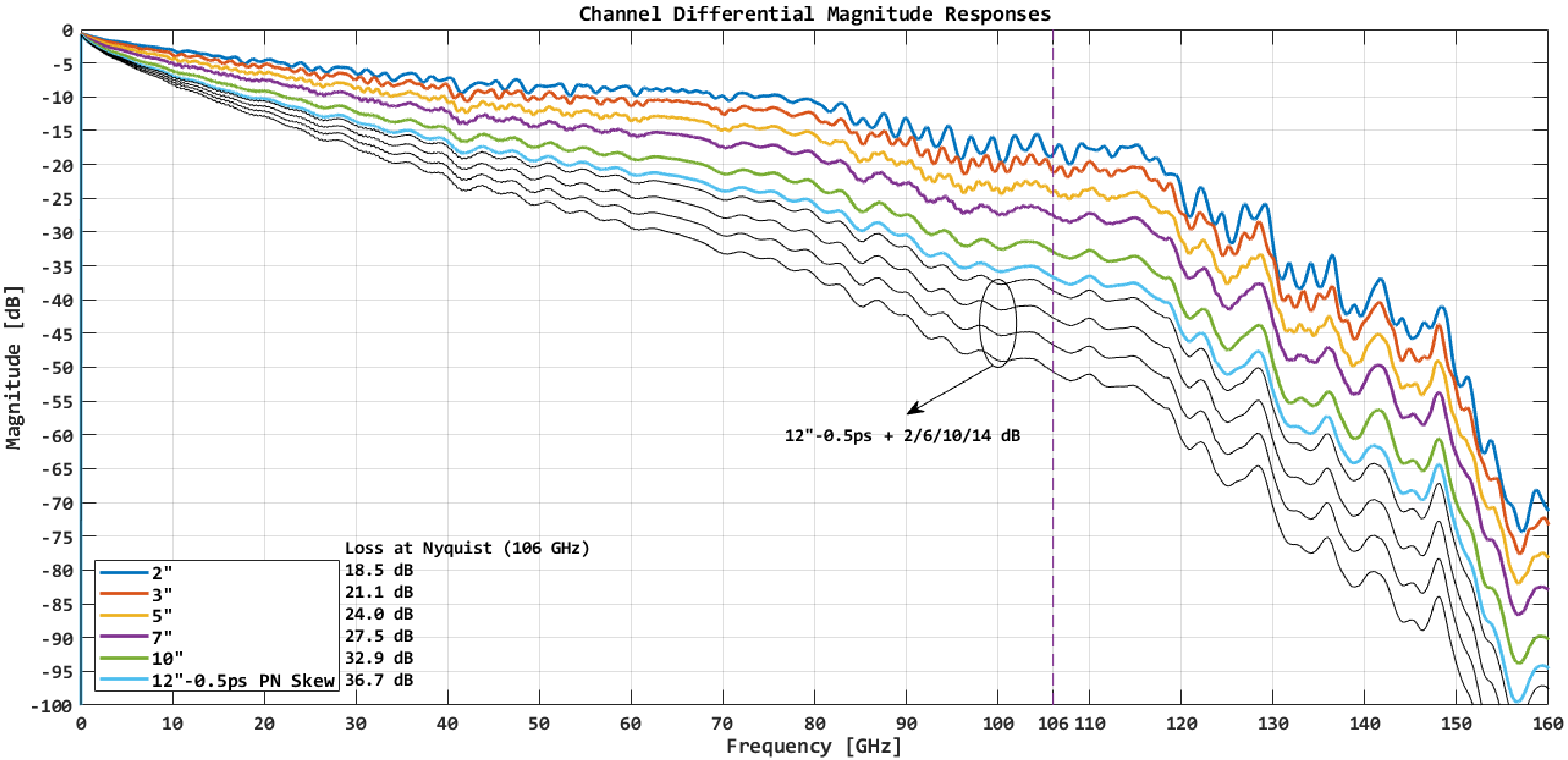
Parameter	Value	Unit
Application	VSR --- C2M	
Baud	212	GBd
Modulation	4PAM	
# Symbols	1,048,576	
Tx Launch Vpp (P2P-Limited)	1,200	mV
Channel	2”, 3”, 5”, 7”, 10”, 12” --- Bump-to-Bump: Package+Thru	
DAC RLM	98	%
DAC White Jitter	60	fs
Tx SNDR (Output of DAC)	28	dB
ADC SNDR	29	dB
ADC White Jitter	50	fs
EQ Taps	70 over 128 UI	



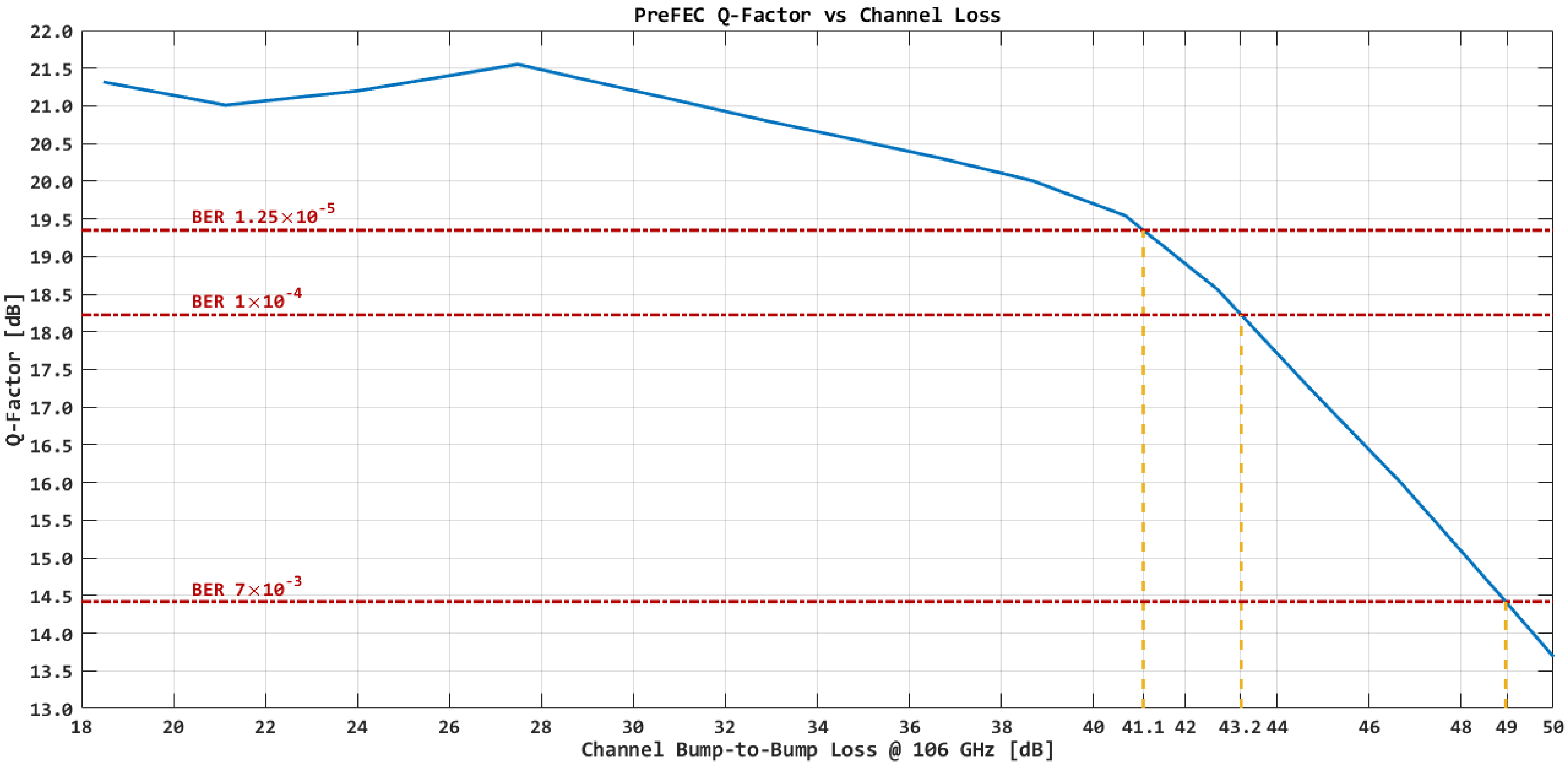
Notes:

1) Channel models are projected from 224 Gbps to 424 Gbps using frequency scaling. Additional dB-linear droop was added to 12” for extra loss at Nyquist (106 GHz) up to about 50 dB.
2) AFE (Analog Front-End) model is projected from 224 Gbps to 424 Gbps by scaling frequency to 424/224, and scaling dB-magnitude to ~2/3.

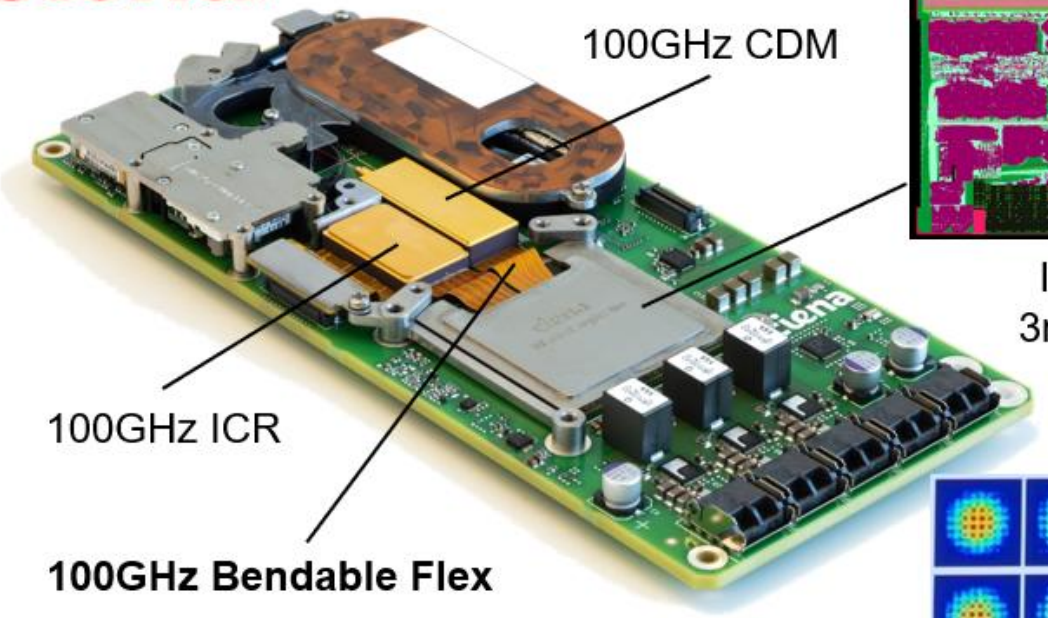
448G SerDes extrapolated channels



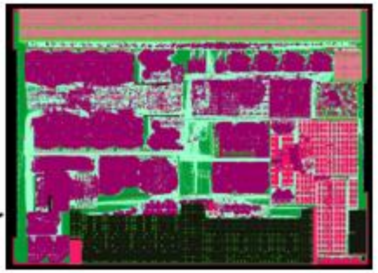
448G SerDes Result vs Channel Loss



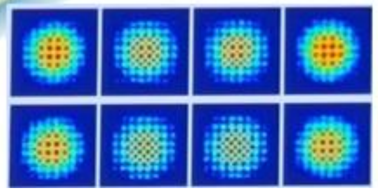
WL6e: 1.6T DSP chip and Flex interconnect

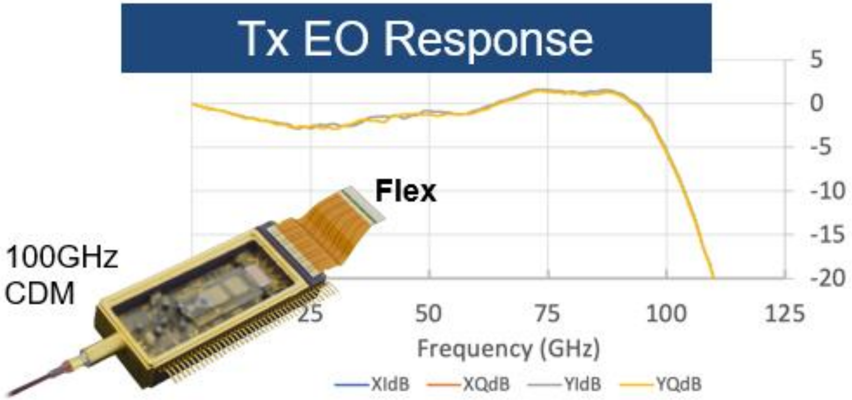


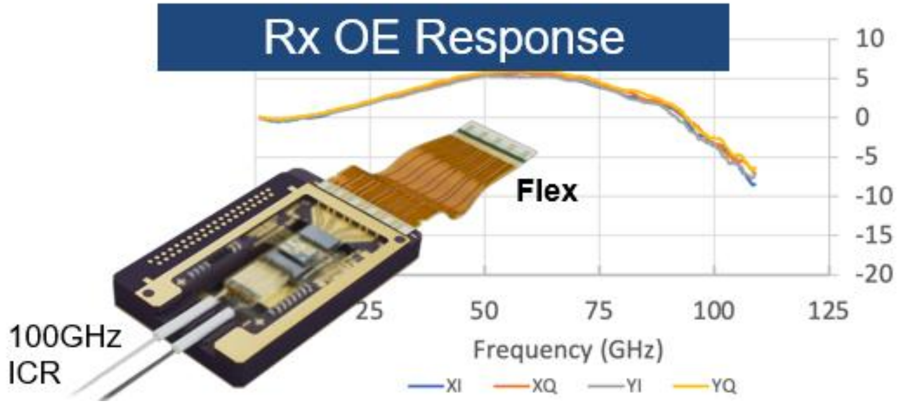
(Remove SI bottleneck of BGA transitions)



Industry's 1st 3nm Coherent DSP chip







- 1.6 Tb/s WL6 Photonics products: First 200GBaud product
- Use of Flex interfaces to minimize interconnect losses and crosstalk

448Gbps Channel Loss Considerations

- Conventional routing through PCB is limited at high frequencies
  - Use of relatively large PCB vias & BGA balls
  - Stripline structures have high dielectric loss

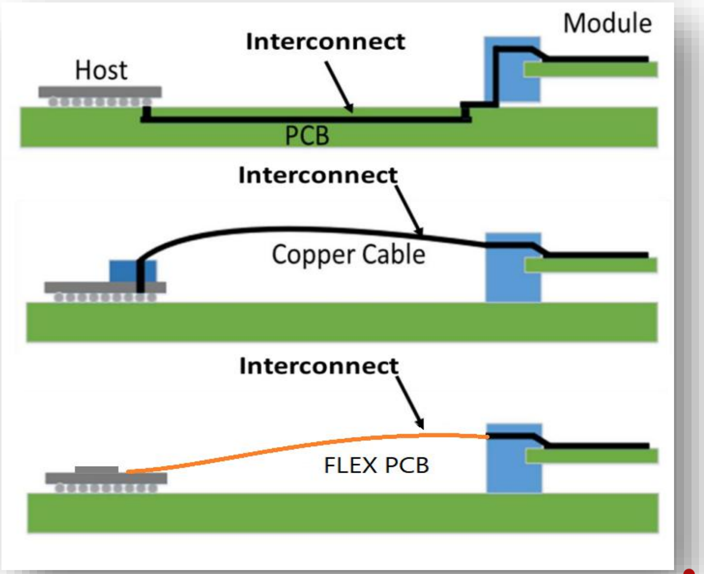
- Low-loss flex PCB is effective at 100+ GHz (Ciena results)
  - Low cost & volume manufacturing friendly
  - Mechanically advantageous for dense designs

- Manufacturing spread & tolerances need to be considered
  - Statistical analysis of loss budgets becomes increasingly more important at higher Nyquist Freq
  - Need to budget worst-case channel loss vs material vs manufacturing tolerances
    - Early testing, analysis & validation on each portion of transmission line is key
    - Sampling via high-frequency coupons should be done to ensure loss is bounded

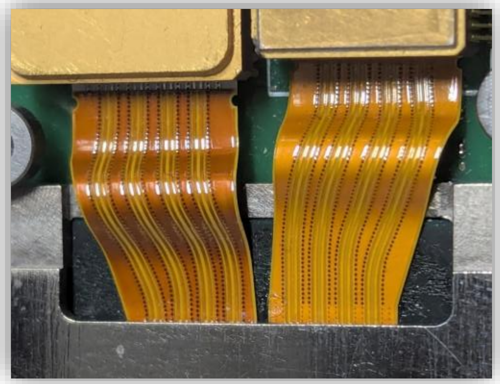
Measured PCB Insertion Losses for 448Gbps

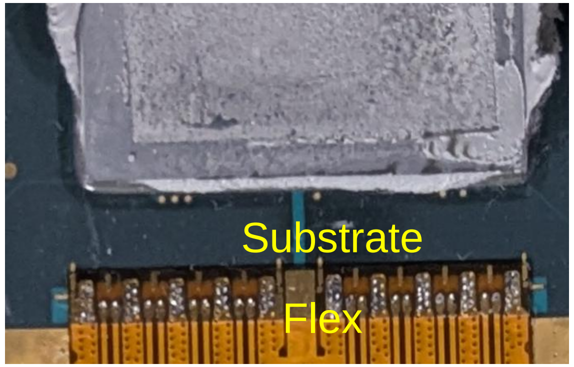
	PAM8	PAM6	PAM4
Nyquist Frequency (GHz)	74.6	86.8	112
Microstrip PCB loss (dB/inch)	3.4	3.8	4.8
Stripline PCB loss (dB/inch)	5.0	5.5	6.4
Microstrip Flex (dB/inch)	1.3	1.6	2.2

Measured Data

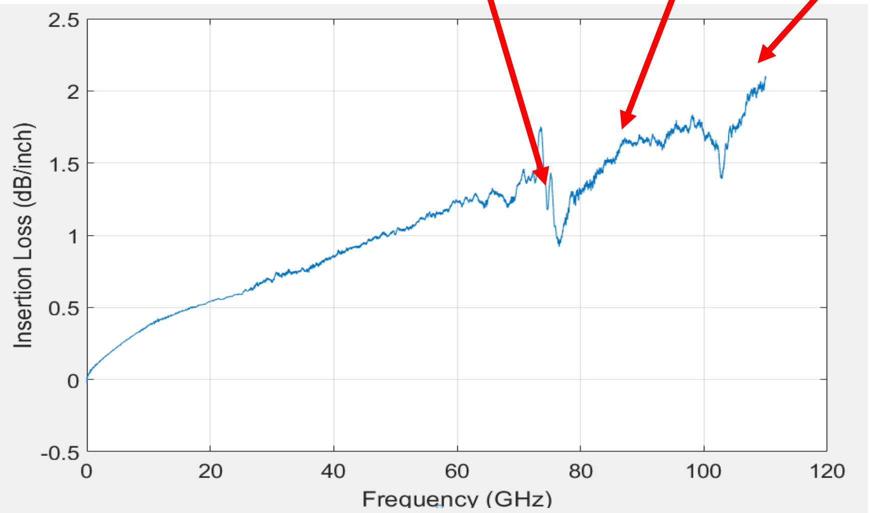


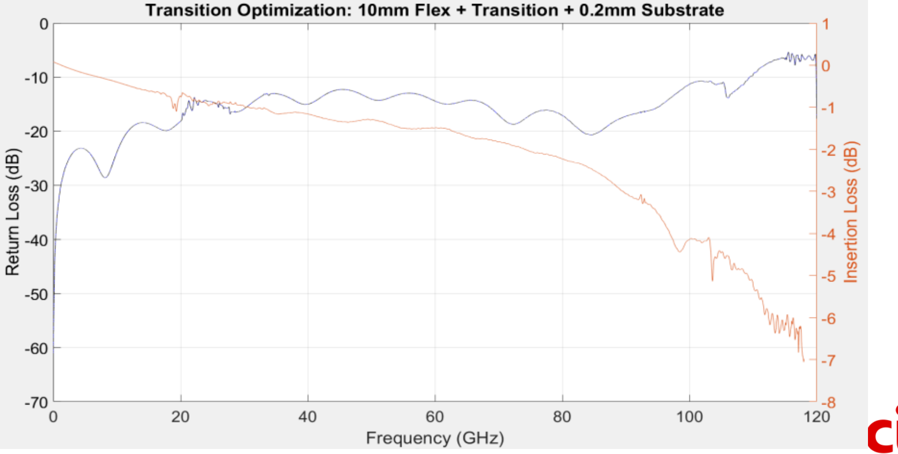
Example Implementation: Flex Microstrip





448G Signaling	PAM8	PAM6	PAM4
Nyquist Frequency (GHz)	74.6	86.8	112
Insertion loss (dB/inch)	1.3	1.6	2.2



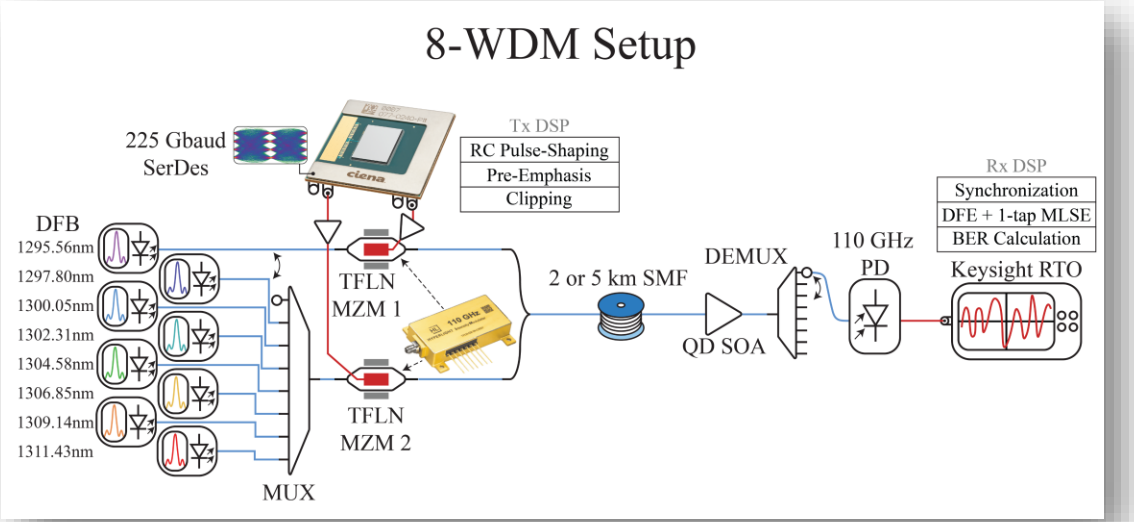


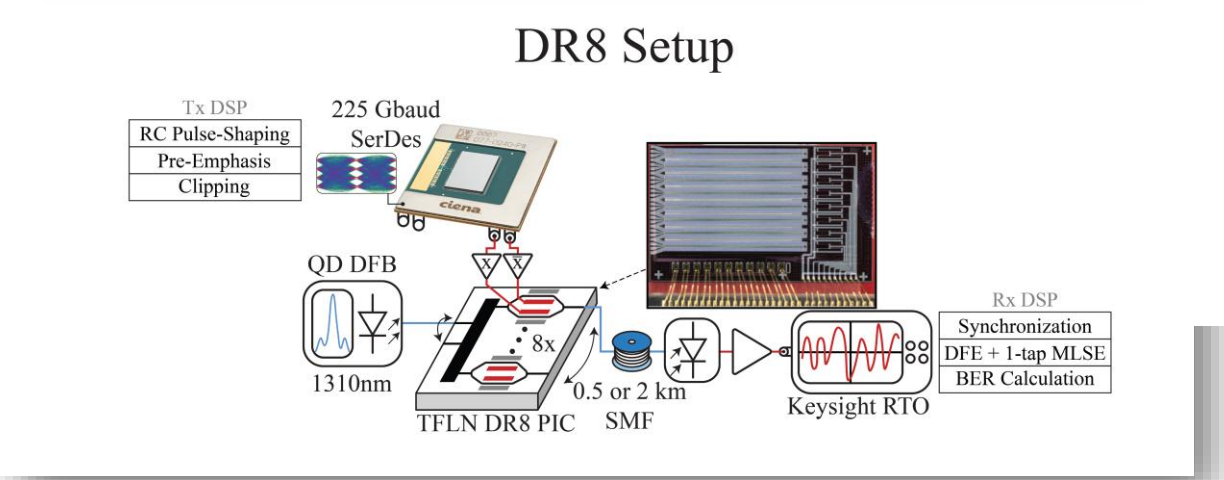
Measured Data

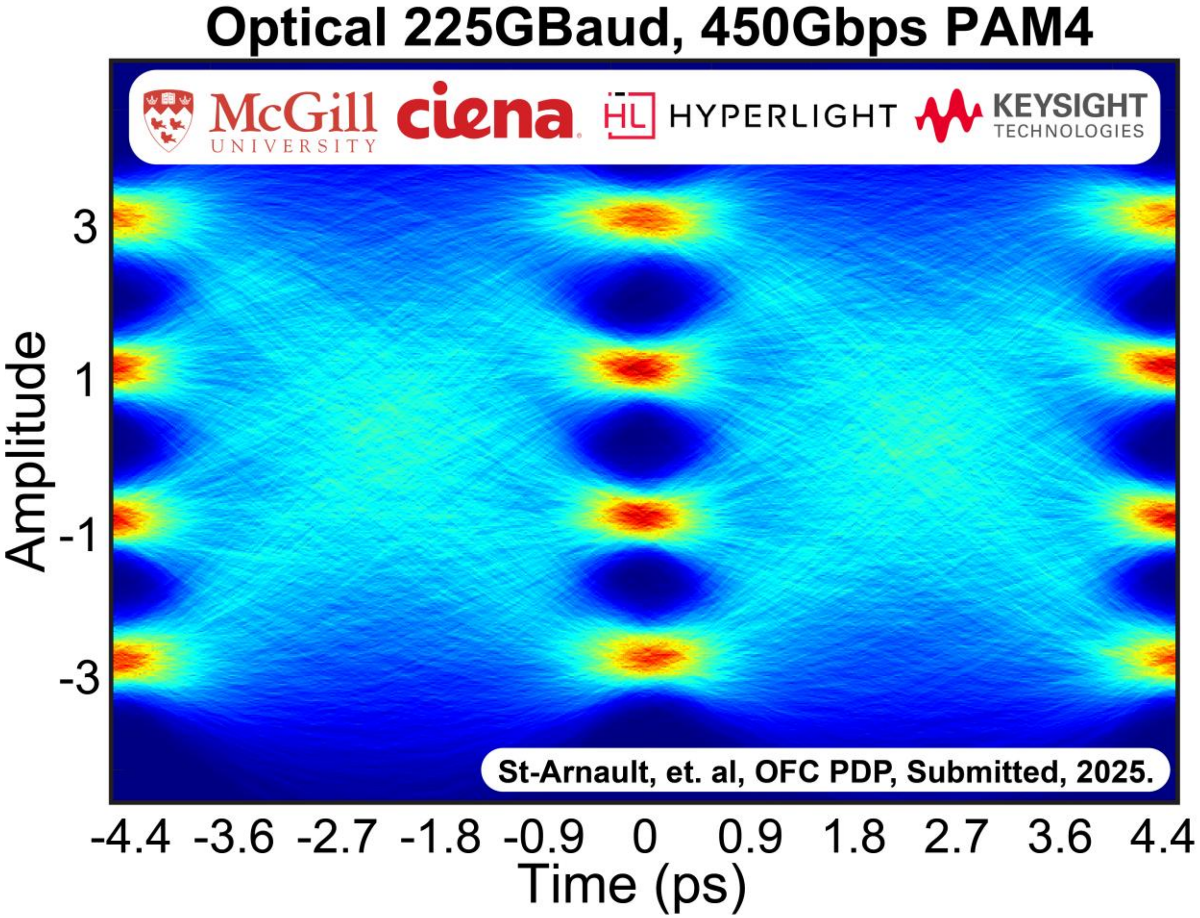
- Allows for a low-loss interconnect between chip and module
  - 2.5dB insertion loss from ASIC substrate to Flex at 100GHz
  - 10dB return loss at 100GHz
- Soldered directly onto the ASIC substrate
  - No BGA balls & PCB blind via to stripline structure
- Improves the insertion loss by > 4dB/inch @ 112GHz vs conventional stripline PCB
- Path to a 1Tb/mm beachfront density

Higher cardinality may solve the interconnect problem at the expense of higher required SNR

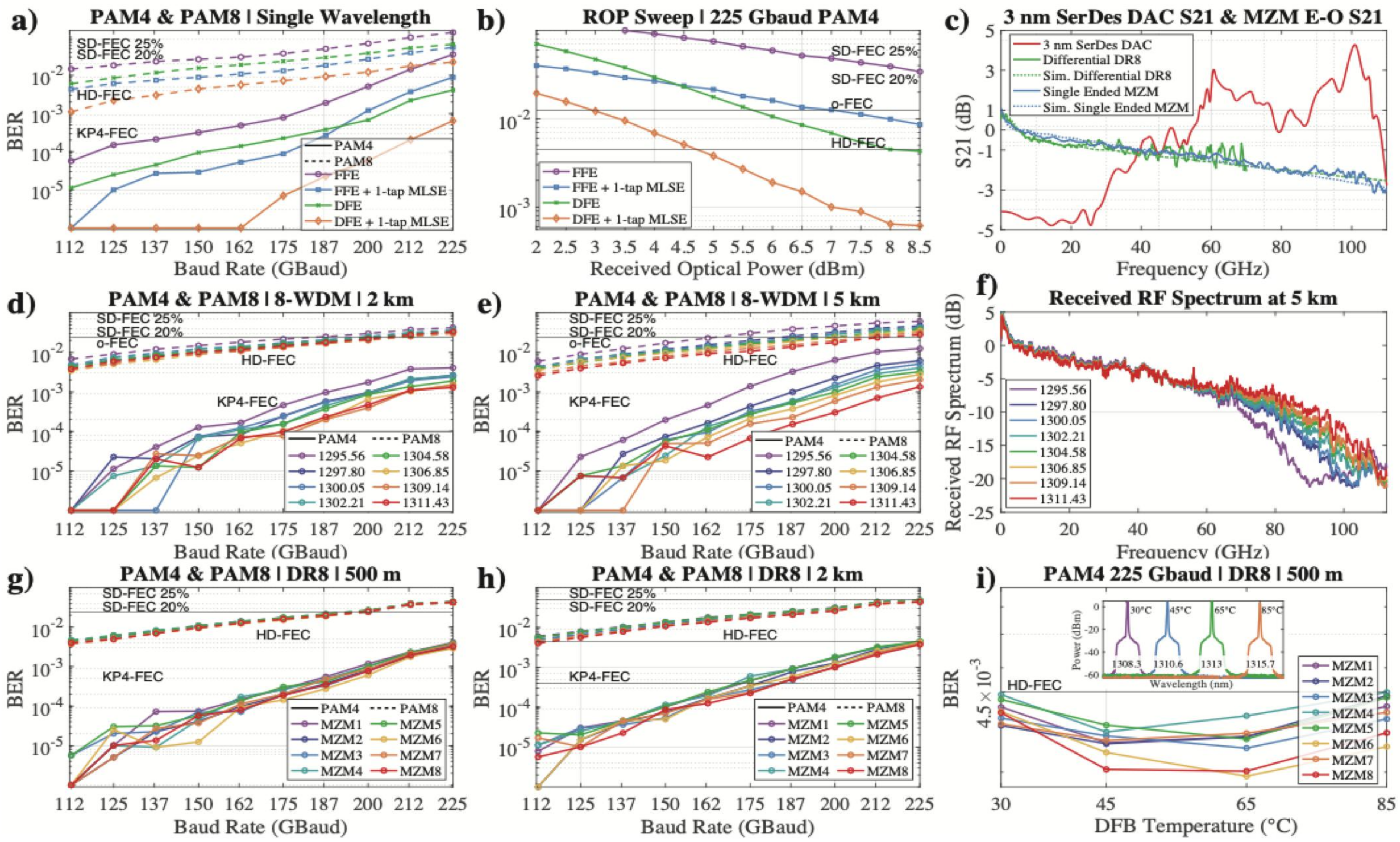
Ciena, HyperLight, and McGill University Achieve First 3.2Tb/s, 448Gb/s Per-Lane IMDD 2km Transmission







PAM4/6/8 Optical propagation



ciena

PAM4/6/8 Optical propagation

Table 1: Summary of achieved net data rates

BER Threshold	FEC Overhead	Symbol Rate / Modulation Format	Net Rate (Gbps)	Aggregate Rate (Tbps)
Single Wavelength (1310 nm) B2B				
4.5×10^{-3}	7%	225 Gbaud / PAM4	420.5	-
2.4×10^{-2}	20%	225 Gbaud / PAM8	562.5	-
DR8 (500m), DR8+ and 8-WDM (2km)				
4.5×10^{-3}	7%	225 Gbaud / PAM4	8×420.5	3.36
5×10^{-2}	25%	225 Gbaud / PAM8	8×540	4.32
8-WDM (5km)				
2.4×10^{-2}	20%	225 Gbaud / PAM4	8×375	3.0
5×10^{-2}	25%	200 Gbaud / PAM8	8×480	3.84

The first demonstration of 2km 225 Gbaud PAM4-8 for 3.2-4.2 Tbps IM/DD using 8-WDM and DR8 configurations was presented at OFC 2025 PDP

Net 3.2 Tbps 225 Gbaud PAM4 O-Band IM/DD 2 km Transmission Using FR8 and DR8 with a CMOS 3 nm SerDes and TFLN Modulators, Charles Saint Arnault et all, OFC 2025

Conclusion

- 3nm silicon can deliver 448Gb/s
- PAM4 is the lead option from SNR perspective despite the need for higher baud
- FEC improvement is needed:
  - 1-3dB coding gain for PAM4
  - 5-6dB coding gain for PAM6
  - 9-10dB coding gain for PAM8
- We see a path for 50dB channel loss
  - With the right FEC/DSP and good SNR
- We can overcome 50dB channel and connector loss
  - We opted for microstrip flex interconnect for our 200Gbaud coherent solution (WL6e: 1.6Tb/s)
  - We need to solve the connector challenge
- We show a path for a 3.2T optical solution at 8x448Gb/s

Thank You