



Energy Efficient Interfaces

Driving Optical Interconnect Specs for AI

19 March 2026

Speakers



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OIF President of the Board

Agenda

1	Overview of OIF's work on Energy Efficient Interfaces (EEI)	Jeff Hutchins, Ranovus OIF PLL WG EEI Vice Chair
2	Compute Optics Interface Energy Efficient Interfaces for Scale-up for AI	Mike Klempa, Qualcomm OIF Board Member OIF PLL Interoperability WG Chair
3	High-Density Connectors for Energy Efficient Interfaces	Nathan Tracy, TE Connectivity OIF Board President
4	Exploring the next data rate: 448G	Cathy Liu, Broadcom OIF Board Member
5	Q/A Panel Discussion	

Accelerating Market Adoption of Optical Networking Technologies

170+ Member Companies

▶ 25+ Years of Service

▶ Member Driven Global Organization

COHERENT OPTICAL



Multi-Vendor Interoperability in Client Form Factors

1600ZR+

- <1000km Multi-Span Coherent DWDM

1600LR, 800LR

- <10km Coherent Point-to-Point

1600ZR, 800ZR, 400ZR

- >80km Coherent DWDM

ELECTRO-OPTICAL



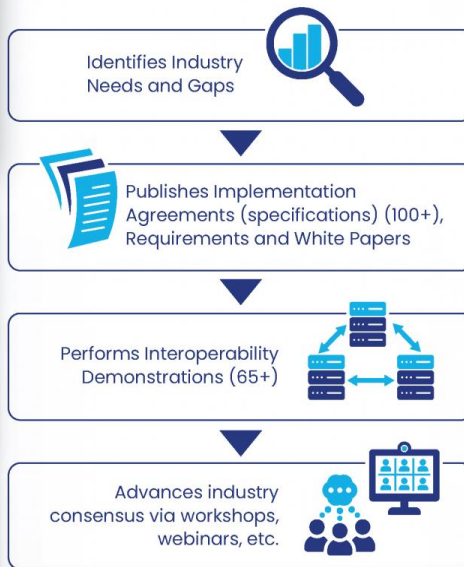
Energy Efficient Interfaces (EEI) –Low Latency/ Optimized Energy Interfaces for AI/ML

- Compute Optics Interface (COI)
- Retimed Tx, Linear Rx (RTLX)
- External Laser Sources (ELSFP)
- Co-Packaged Modules (3.2T)

Common Electrical I/O (CEI)

- High-Speed Building Blocks
- 448G, 224G, 112G, 56G, 28G
- LR, MR, VSR, XSR+, XSR, MCM, Linear
- Protocol Agnostic Link Training

OIF



MANAGEMENT



Common Management Interface Specification (CMIS)

- Single Solution Ranging From Copper to Coherent
- Simplified Bring up Between Host and Module
- Supports Standard and Custom Interfaces

Transport SDN APIs

- Automation, Programmability

Enhanced Network Operations

- Artificial Intelligence
- Digital Twin
- DC Storage and Optical Multi-Layer Coordination

PROTOCOL



Flex Ethernet (FlexE)

- 800 Gb/s Ethernet PHY support

For more information, visit www.oiforum.com

What are Energy Efficient Interfaces (EEI)?

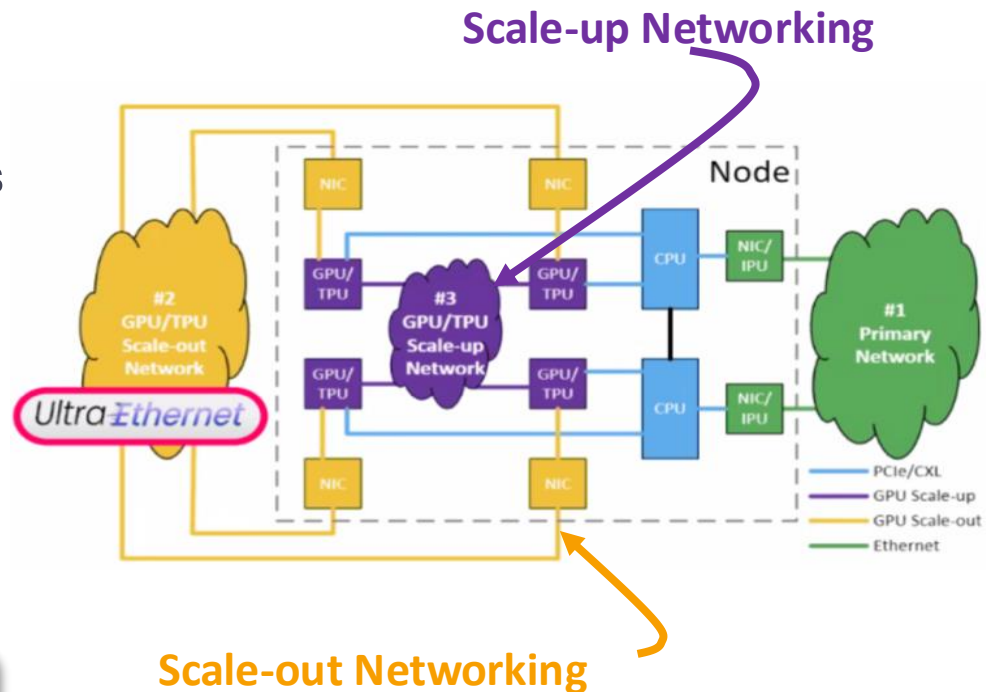
Scale-out links

- ▶ Reaches of 100s of meters
- ▶ Currently using pluggable optics

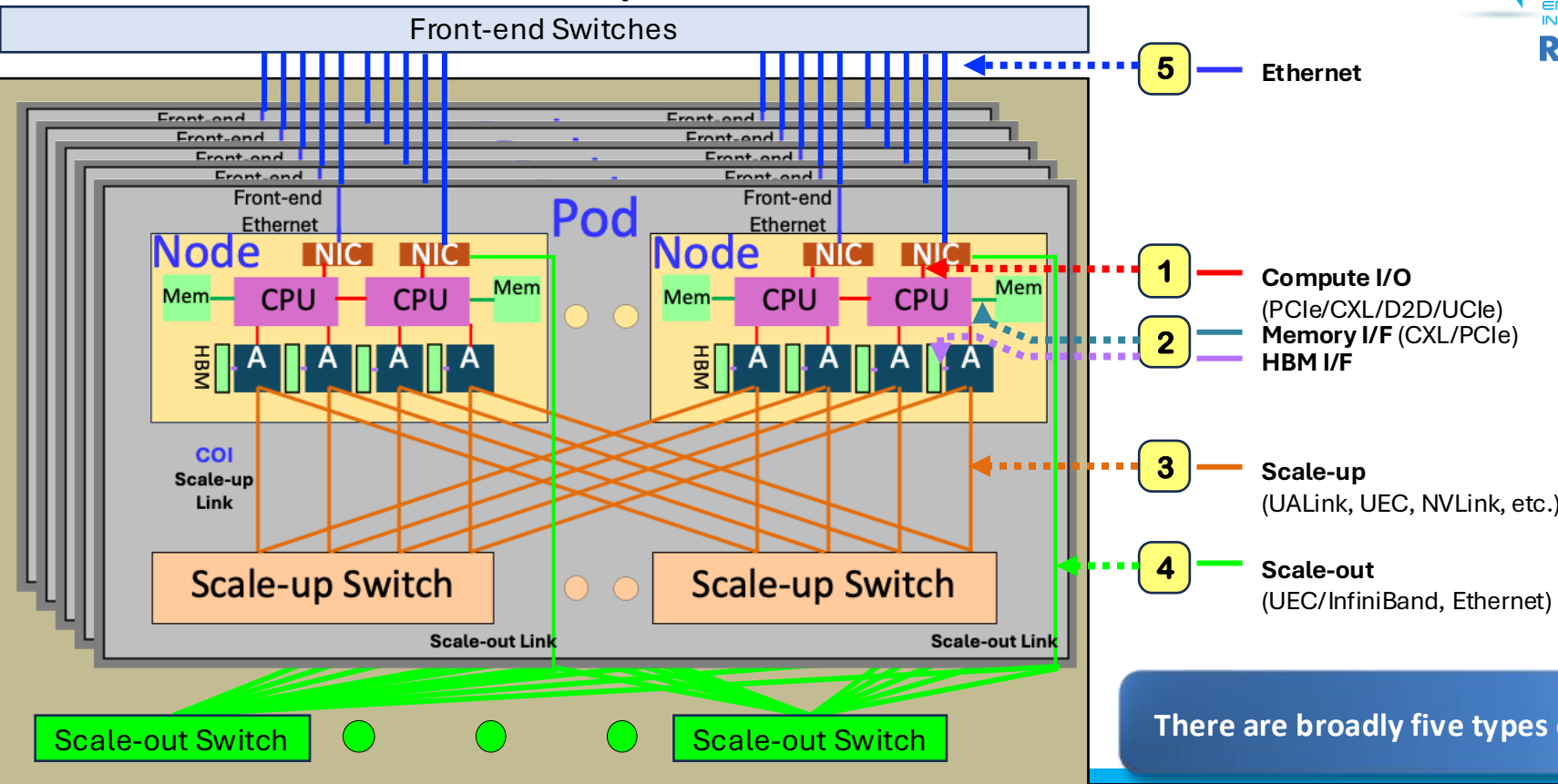
Scale-up links

- ▶ Reaches 20 up to 100 meters
- ▶ ~ 10x the BW of scale-out
- ▶ More sensitive to latency
- ▶ Currently using passive copper

Energy efficiency (power usage) is a key requirement for training Pods

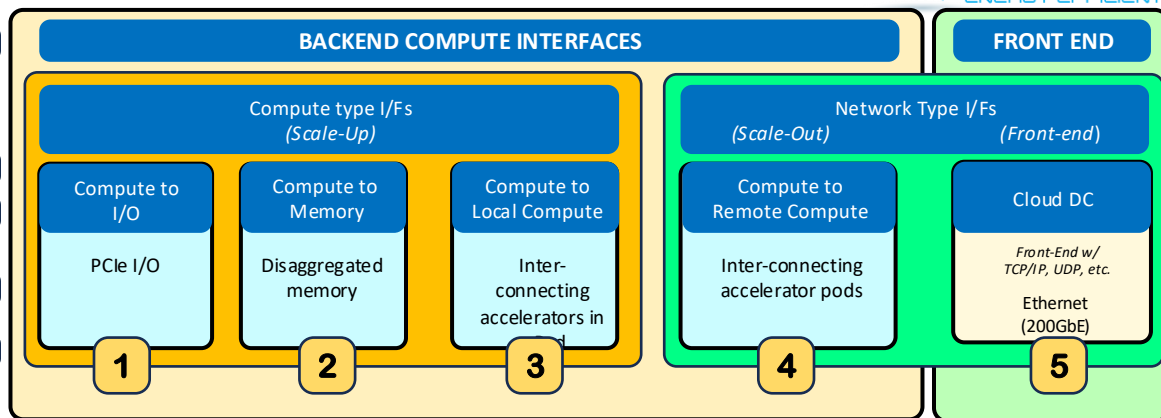
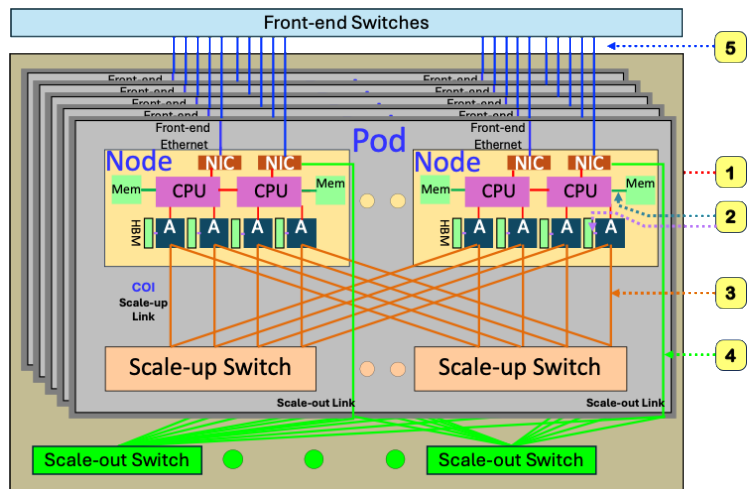


What does AI Compute look like?



There are broadly five types of links

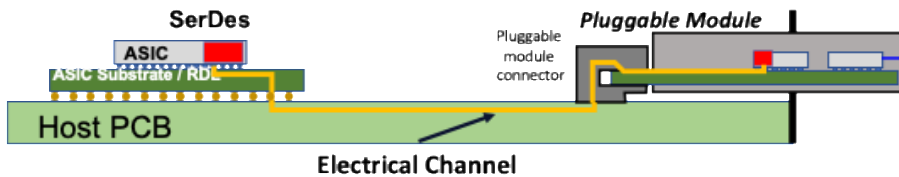
The various links have different requirements



Key requirements from hyperscalers are summarized in the table

Parameter	3: COI: Scale-up Compute - Local	4: Scale-out Compute - Network	5: Front-end Compute Servers
Scale	Local	10's of racks	Data center
Reach [m]	~ 20 – 100	~ 100	~ 1000
ASIC BW Edge Escape Density [Tbs/m m] (Tx + Rx)/(edge width)	> 2.0	> 2.0	Std Ethernet
Transceiver Latency (Tx + Rx) [ns]	latency-A: < 5 latency-B: < 100	latency-A: < 60 latency-B: <100	< 100
Energy Utilization [pJ/b] (Tx + Rx with lasers)	EU-A: < 4 EU-B: < 12	EU-A: < 10 EU-B: < 12	< 12
Reliability (link errors)	very high	high	same as std Ethernet
Reliability (hw failures)	inside: very high front panel: high	inside: very high front panel: high	same as std Ethernet

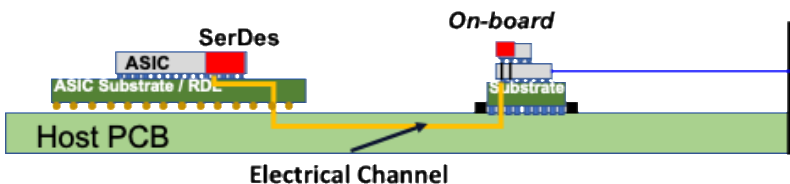
Various approaches for EEI Links



Pluggable

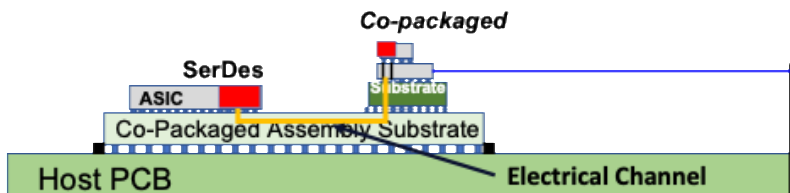
Replaceable modules:

- Non-retimed (e.g. LPO, LINEAR, passive copper)
- Tx-retimed (e.g. RTL, LRO) (Tx diagnostics)
- Fully-retimed (full diagnostics)



On-Board

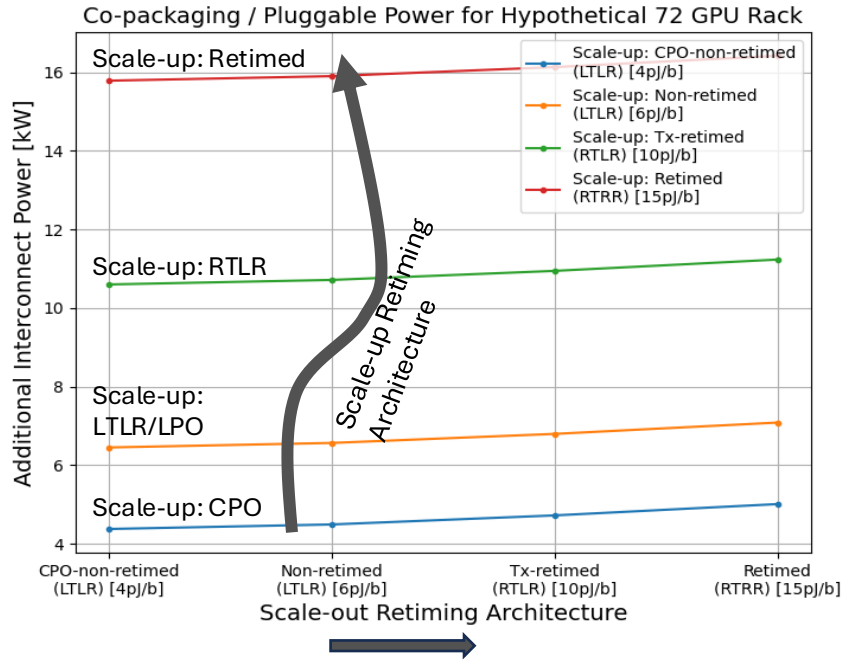
- Increased density
- Shorter electrical channel
- Replacement requires card removal



Co-packaged

- Highest density
- Shortest electrical channel
- Replacement requires repair of ASIC's package
- Configured during ASIC packaging

Scale-up systems benefit from energy efficiency



- ▶ Scale-up networking bandwidth is about ~10x that of scale-out networks
- ▶ Scale-up dominates the rack interconnect power consumption
- ▶ The lowest power solutions for optical connectivity will leverage co-packaging or linear/LTLR/LPO for scale-up

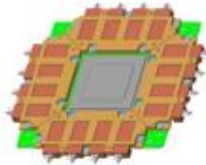
Scale-up dominates the rack interconnect power, energy efficient solutions (CPO, LTLR) are lowest power

The OIF is tackling improved energy efficiency

OIF's Co-Packaging Projects

✓ Co-packaging Framework Project

[OIF-Co-Packaging-FD-01.0 – Co-Packaging Framework Document](#)

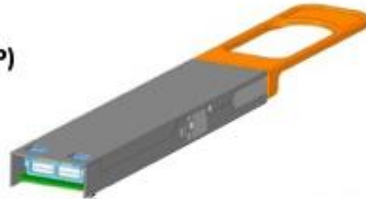


✓ 3.2T Co-packaged Engine

[OIF-Co-Packaging-3.2T-Module-01.0 – Implementation Agreement for a 3.2Tb/s Co-Packaged \(CPO\) Module](#)

✓ External Laser Source (ELSFP)

[External Laser Small Form Factor Pluggable \(ELSFP\) Implementation Agreement \(August 2023\)](#)



✓ Management Interface for ELSFP

[OIF-ELSFP-CMIS-01.0 – Implementation Agreement for External Laser Small Form Factor Pluggable \(ELSFP\) CMIS](#)

Energy Efficient Interfaces for AI

✓ System Vendor Requirements for Energy Efficient Interfaces

- Document the EEI requirements as provided by the end-users for AI/ML optical and electrical links

Energy Efficient Interface Framework

- Study and initiate new standards for dense, low power, low latency links for AI/ML

RTLr Project (Retimed Transmitter, Linear Receiver)

- Address lower latency and low power applications utilizing transmit retimed optical transceivers (e.g. Ethernet, UEC, etc.)

CEI-Linear (Non-Retimed Interface)

- Low power optical interface (LPO, CPO, & NPO)

COI Project (Compute Optics Interface)

- Address energy efficient, low latency photonic interfaces for transport of traffic for AI scale-up applications

High-Density Connector Project

- Defining requirements for next generation connectors

OIF's New Documents



448G Framework



COI WP



EEI Framework

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AI is Driving a New Interconnect Era

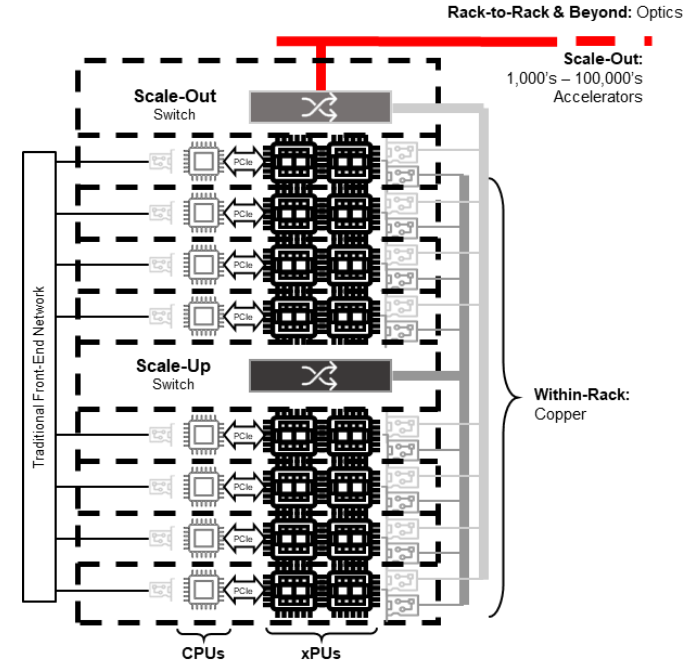
Frontier AI model size growing $\sim 4\times$ annually, driving demand for higher memory, compute, and bandwidth

Frontier AI models exceed single-accelerator memory, requiring multi-accelerator clusters with hierarchical interconnects:

- Scale-up (intra-node)
 - Electrical
- Scale-out (inter-node)
 - Optical
- Front-end (I/O)

Maximizing accelerators per scale-up domain requires compact rack design

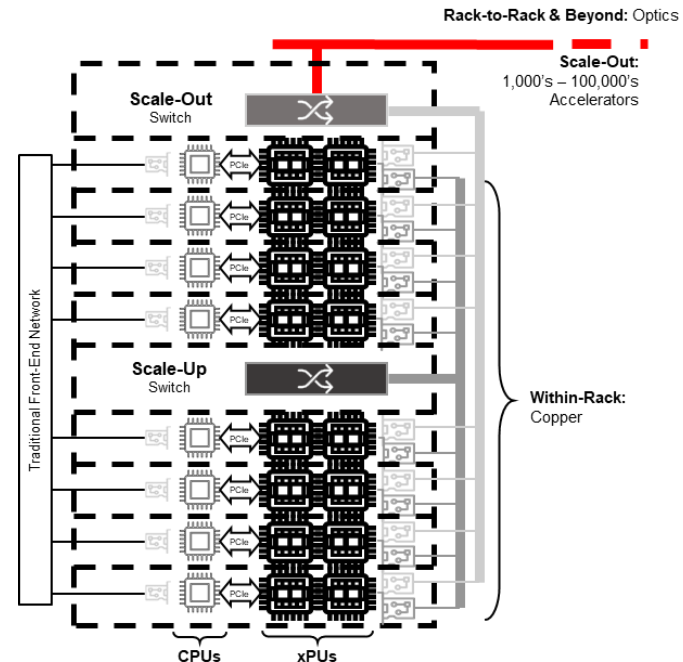
- Density is Imperative



AI is Driving a New Interconnect Era

And the historical evolution of the OIF's CEI-LR Projects

OIF CEI Projects	CEI-56G-LR	CEI-112G-LR	CEI-224G-LR	CEI-448G-LR
Timeline	2014-2017	2017-2021	2021-	2026-
Modulation	PAM4	PAM4	PAM4	TBD
Insertion Loss	30 dB at 14 GHz (Ball – Ball)	28 dB at 28 GHz (Ball – Ball)	40 dB at 56 GHz (Bump – Bump)	TBD
Reach Objectives	3m copper cable	2m copper cable	1m copper cable	TBD



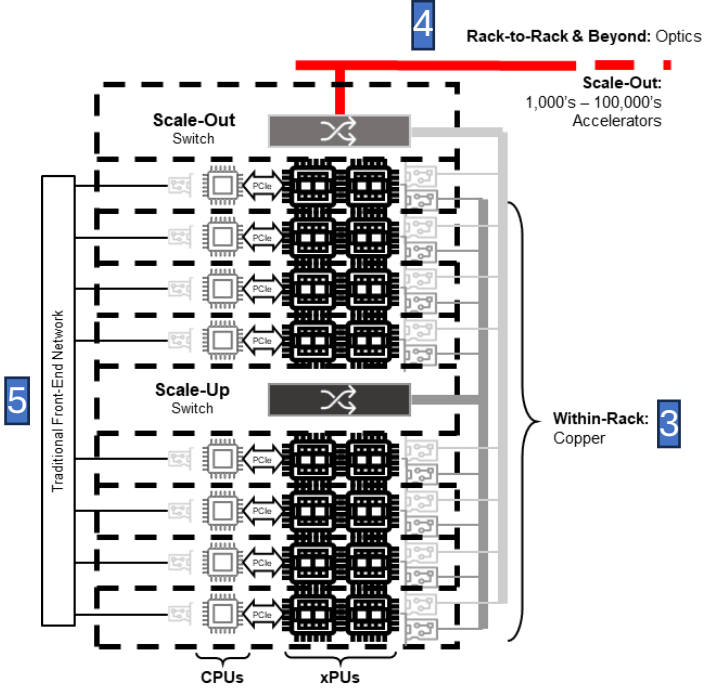
AI Scale-up Dominated by Copper (for now)



And the historical evolution of the OIF's CEI-LR Projects



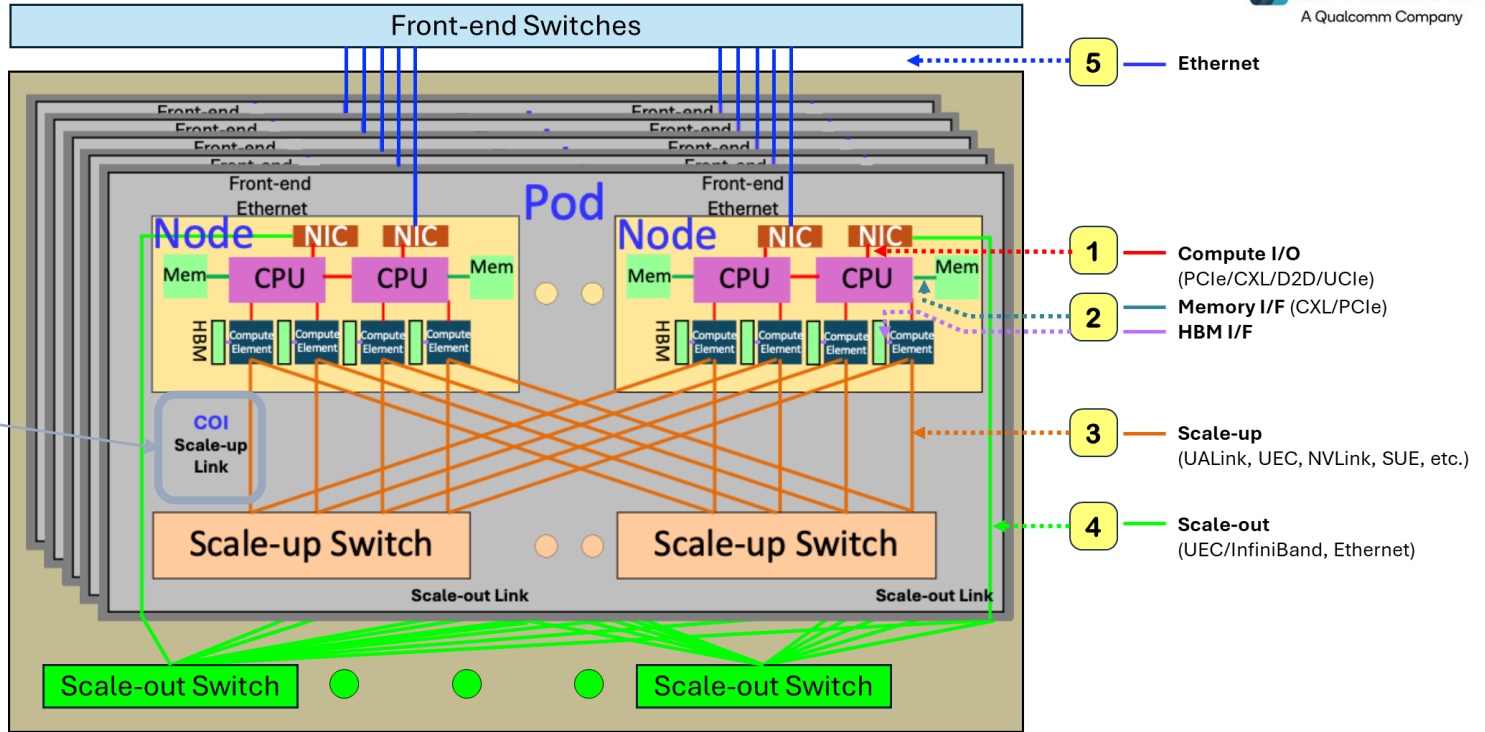
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Minimum Reach (m)	~ 20 - 100	~ 100	~ 1000



Links in an AI Compute Pod

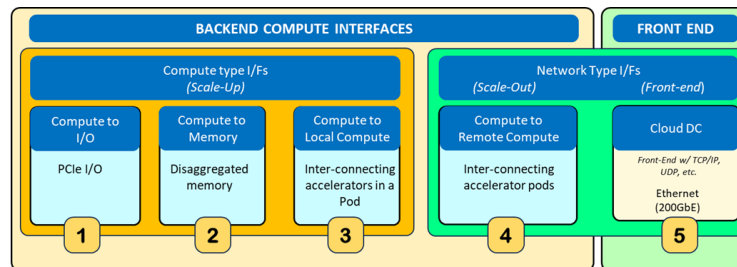
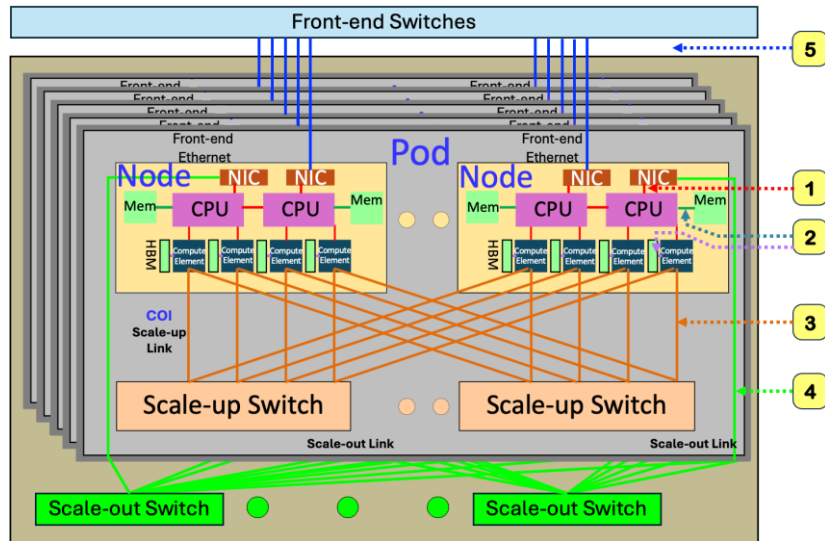
5 Types of Links Used in an AI Compute Pod

Compute Optics Interface (COI):
Energy Efficient
Photonic
Interconnects for AI
Compute Scale-up



AI Compute Requirements

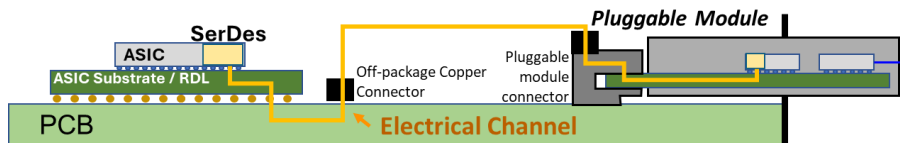
AI Compute Architecture, Pod Structure and Link info



Parameter	3: COI: Scale-up Compute - Local	4: Scale-out Compute - Network	5: Front-end Compute Servers
Scale	Local	10's of racks	Data center
Minimum Reach [m]	20 - 100	~ 100	~ 1000
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Next Gen AI Scale-up Connectivity Options

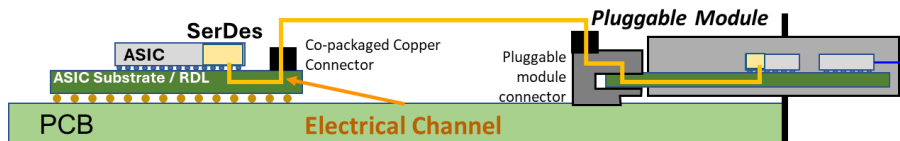
How to move the compute to other elements



Pluggable with Off-package Copper

Replaceable modules:

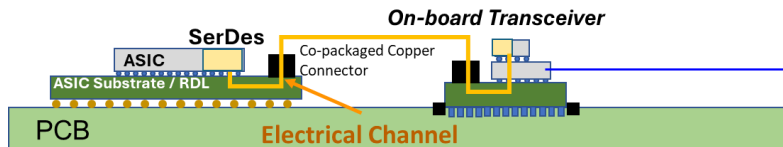
- Non-retimed (e.g. LPO, LINEAR, passive copper)
- Tx-retimed (e.g. RTL, LRO) (Tx diagnostics)
- Fully-retimed (full diagnostics)



Pluggable with Co-packaged Copper

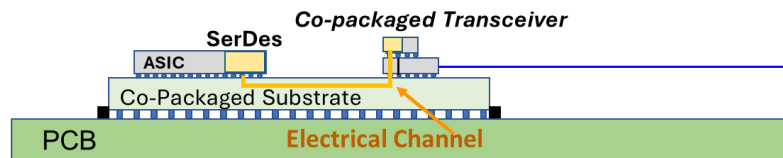
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- Tx-retimed (e.g. RTL, LRO) (Tx diagnostics)
- Fully-retimed (full diagnostics)



On-Board with Co-packaged Copper

- Retimed, Tx-retimed, or non-retimed interface
- Increased density
- Shorter electrical channel
- Replacement requires card removal

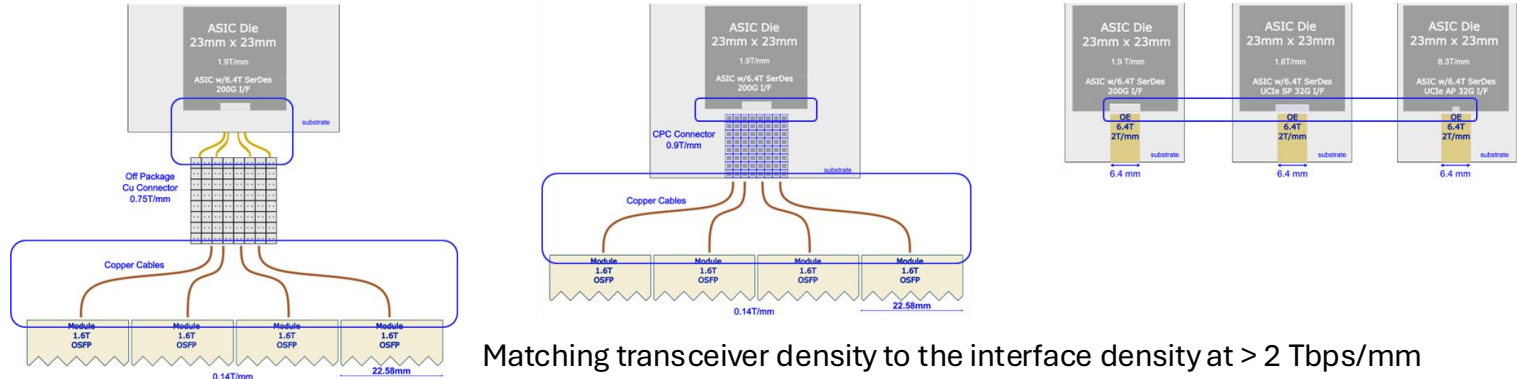


Co-packaged

- Non-retimed or slow/wide interface
- Highest density, shortest electrical channel
- Replacement requires repair of ASIC's package
- Configured during ASIC packaging

ASIC Escape Bandwidth Edge Density Requirements for AI Compute

Retiming Architecture	Electrical Interface (ASIC to Transceiver)	Optical Transceiver Location (2.0 T/mm)	Achievable ASIC Bandwidth Escape Density [T/mm]	ASIC Bandwidth Escape Density Limiting Factor	Net Interface Energy Utilization [pJ/b]	Max Electrical Channel Reach
Passive Copper	200G	N/A	~ 0.9	Co-packaged Copper Connector	0	~ 1.5 m
Retimed (RTRR)	200G	Pluggable or			15 - 19	> 35 dB
Tx Retimed (RTL, LRO, TRO)		On-board			10 - 12	~ 26 dB
Non-retimed (LTLR, linear)	200G	Co-packaged	~ 2.0	Transceiver	4 - 5	22 dB
Non-retimed (LTLR, linear)	200G		~ 1.8	D2D Interface	5 - 6	25 mm
Slow-Wide	D2D-D2D standard		~ 2.0	Transceiver	4 - 5	2 mm
Slow-Wide	D2D-D2D advanced					

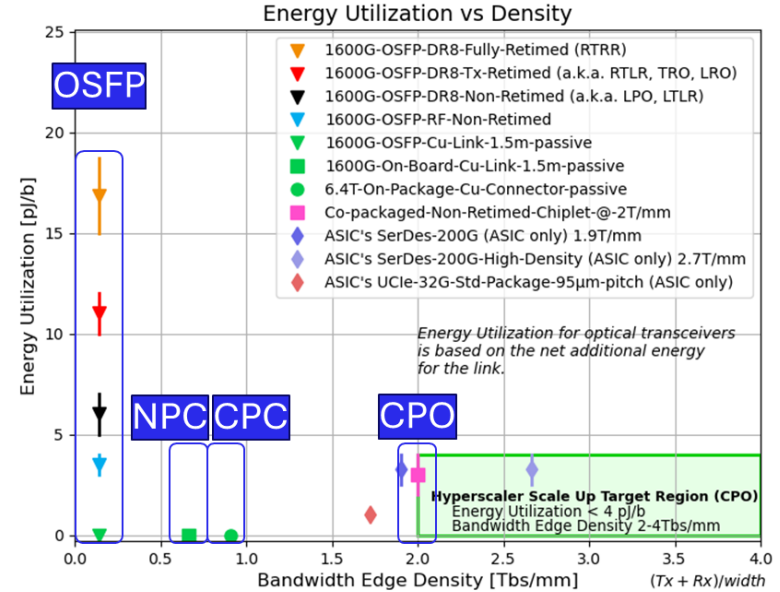


Matching transceiver density to the interface density at > 2 Tbps/mm

ASIC Signaling Energy Efficiency and Reach Requirements for AI Compute

Trading off Energy Utilization and Max Electrical Reach at the Shoreline

Retiming Architecture	Net Interface Energy Utilization [pJ/b]	Max Electrical Channel Reach
Passive Copper	0	~ 1.5 m
Retimed (RTRR)	15 - 19	> 35 dB
Tx Retimed (RTL, LRO, TRO)	10 - 12	~ 26 dB
Non-retimed (LTLR, linear)	5 - 6	22 dB
Non-retimed (LTLR, linear)	4 - 5	22 dB
D2D Standard Package	5 - 6	25 mm
D2D Advanced Package	4 - 5	2 mm



Summary

- ▶ The next generation of AI Compute will need larger Pods
 - Optical links can enable these larger pods

- ▶ The OIF is working with its members from across the ecosystem to find the best solutions among the various trade offs while balancing scalability and manufacturing for energy-efficient, high-bandwidth, low-latency reliable optical interconnects in next-generation AI compute systems
 - CPO vs CPC
 - Minimizing Latency
 - Lower Energy Utilization
 - Improved Hardware and Link Reliability
- ▶ [OIF-EEI-COI-WP-01.0.pdf](#)

OIF

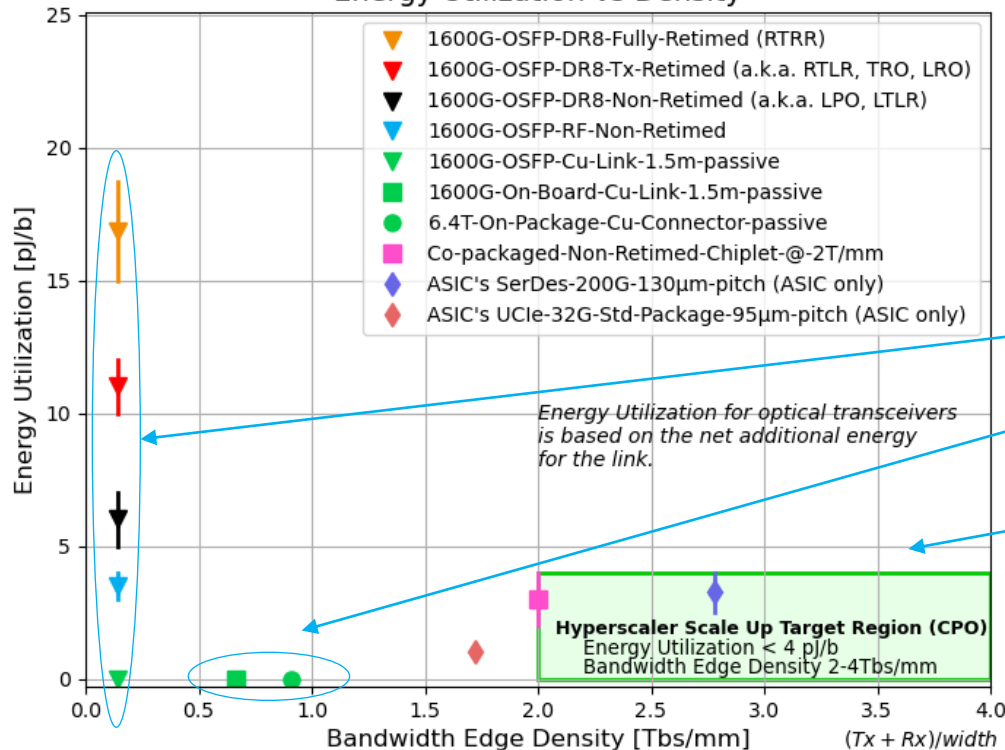
Compute Optics Interface (COI): Energy Efficient
Photonic Interconnects for AI Compute Scale-up

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Motivations for an HD Connector

Energy Utilization vs Density



Driven by demands for Energy Efficiency

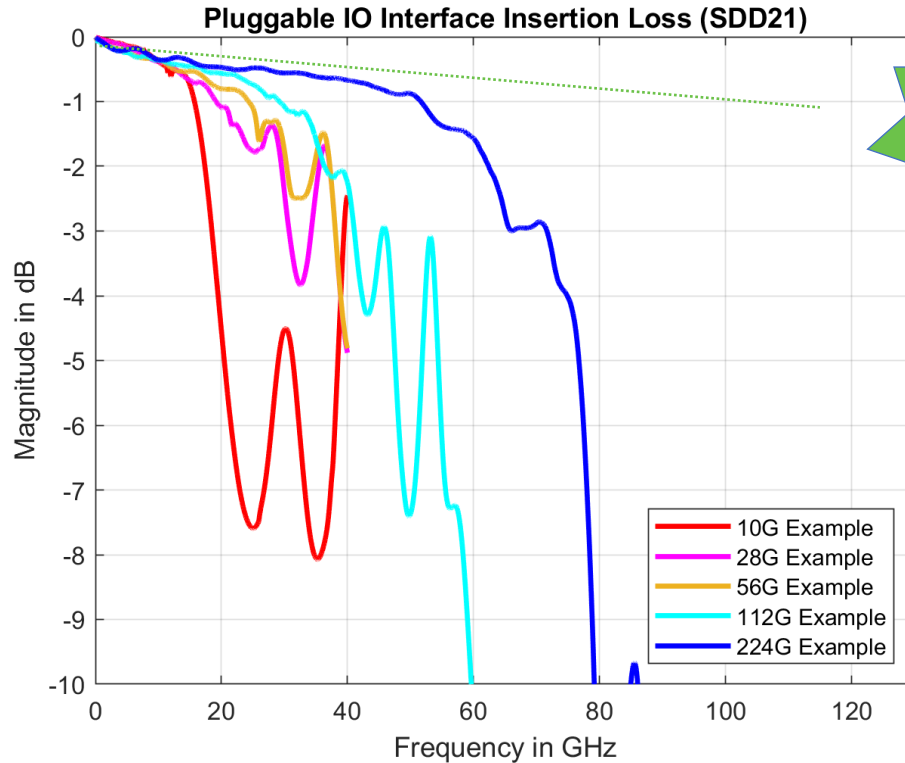
Bandwidth is limited by I/O

OSFP (x8) Generational Limits

Industry CPC and NPC solutions

Anything 5 pJ/b or below is non-retimed.

What is an HD Connector?



“448G”

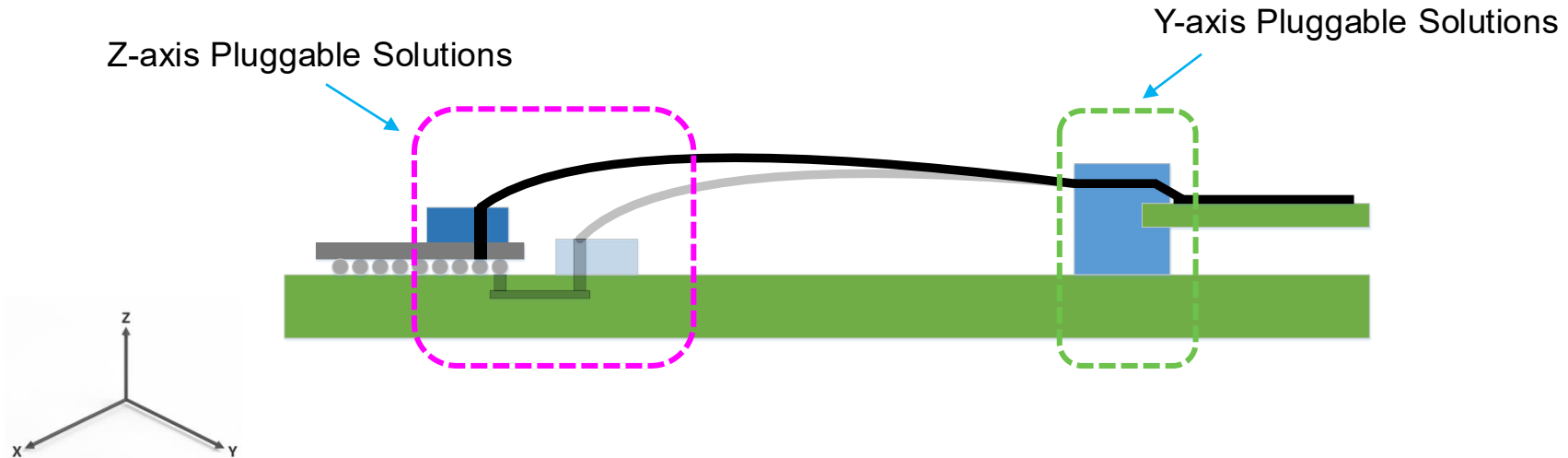
Form Factor Bandwidth is
Data Rate x Density (# of lanes)

Both are critical for HD Connector

- ← 10G Example SFP
- ← 28G Example QSFP, SFP
- ← 56G Example QSFP-DD, QSFP, SFP
- ← 112G Example OSFP, QSFP-DD, QSFP, SFP
- ← 224G Example OSFP, QSFP-DD, QSFP, SFP

What is an HD Connector?

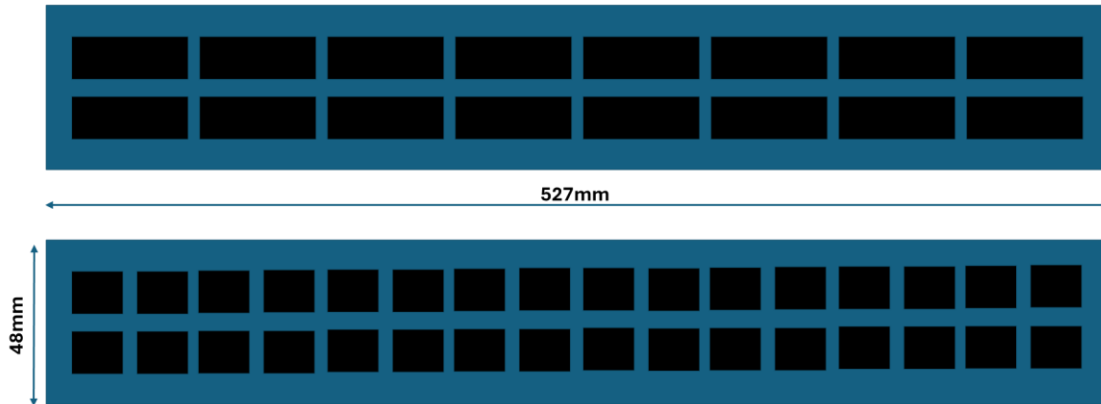
1. Provide modular connectivity transporting high-speed, management, power signals
2. Enable translation from electrical to optical domain
3. Support necessary cooling implementation techniques
4. Improve upon Tbs/mm of existing industry solutions that meet the criteria above



Y-Axis Pluggable I/O Solutions

Target is 1024 Lanes across appliance faceplate

Optimization of space is critical for HD Connector



1 OU (Open Unit) height:
~1.89 inches (48mm)*

Usable dimensions: 98% of 1 OU:
47.6 mm by 527 mm

Faceplate Space per module:

- 16 Modules (8 x 2) = 53 mm / module
- 32 Modules (16 x 2) = 26 mm / module
- 64 Modules: power/thermal prohibitive

* Defined by Open Compute Project

Y-Axis Pluggable I/O Solutions

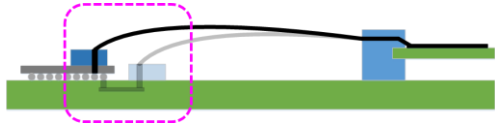


HD = High Power, Thermal management is critical

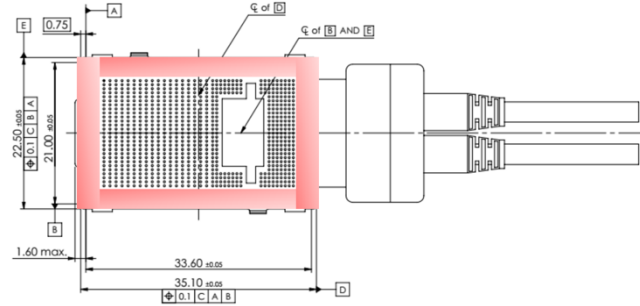
Module mechanical interface needs to be DC-friendly

		Bandwidth Density			
		QSFP-DD	OSFP	OSFP-XD	Y-Axis HD Pluggable
Per Lane Bandwidth	100Gb/s	0.04 Tb/mm	0.035 Tb/mm	0.07 Tb/mm	0.13 Tb/mm
	200Gb/s	0.08 Tb/mm	0.07 Tb/mm	0.14 Tb/mm	0.25 Tb/mm
	400Gb/s	0.16 Tb/mm	0.14 Tb/mm	0.28 Tb/mm	0.49 Tb/mm

Z-Axis Pluggable I/O Solutions



OIF 3.2T was industry's first Z-axis IA
Improved system integration is critical



		Bandwidth Density	
		OIF3.2T	Z-Axis HD Pluggable
Per Lane Bandwidth	100Gb/s	0.14 Tb/mm	0.25 Tb/mm
	200Gb/s	0.28 Tb/mm	0.49 Tb/mm
	400Gb/s	0.56 Tb/mm	0.98 Tb/mm

Key Takeaways for HD Connector



HD Connector aims to improve Tbs/mm efficiency for both Y-axis and Z-axis solutions

HD Connector may include different solutions supporting different applications

Ongoing considerations include:

- Form factor compatibility for copper and optical solutions
- Mechanical interface definition
- Optical interface requirements
- Thermal management considerations

AGENDA

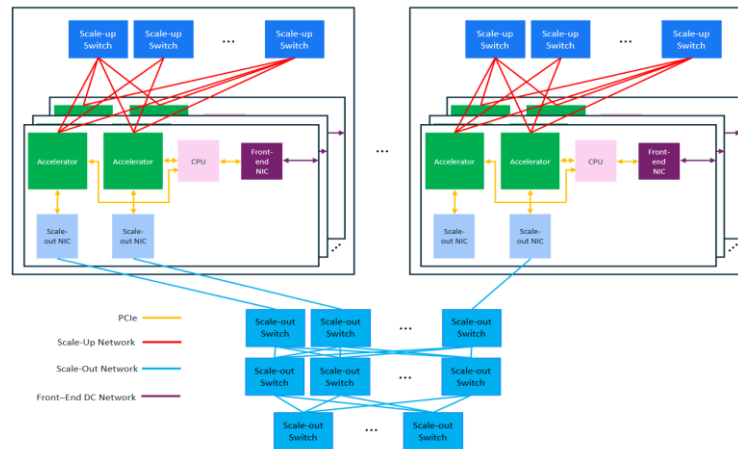
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Shift to 448G

Interconnects are an essential part of AI infrastructure

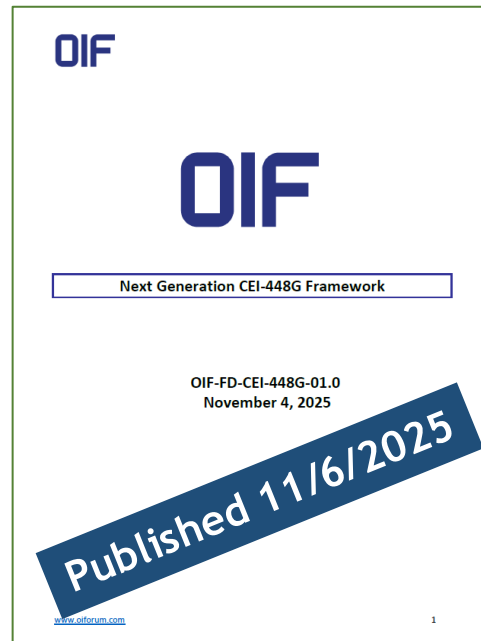
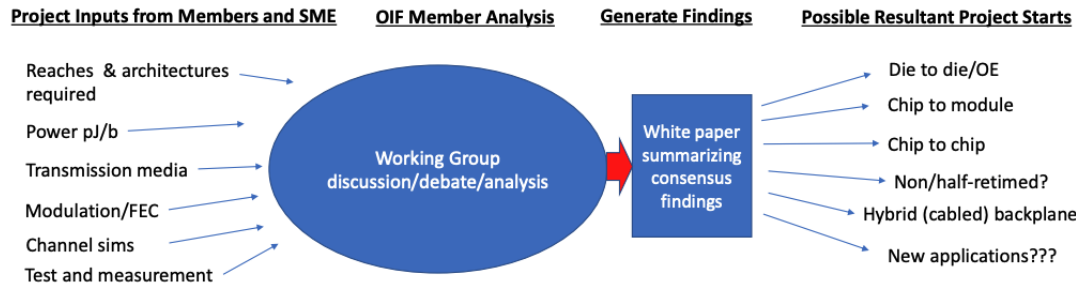
Copper remains as primary interconnect for scale-up network today

To keep pace with the growth in AI model parameters size, OIF created the CEI-448G framework



	Scale-Up		Scale-Out	
	State of Art Today	Next Generation	State of Art Today	Next Generation
# of Accelerator Nodes	~100	~1k	100k+	>>100k
Physical Size	Rack	Rack to Row	Datacenter	Datacenter
Network Properties	Lossless, Low Latency		Large scale	
Primary Interconnect Type	Passive PCB Twinax Backplane: within rack AEC: between adjacent racks	Twinax Backplane: within rack AEC: between adjacent racks Optical: within row	Optical	Optical

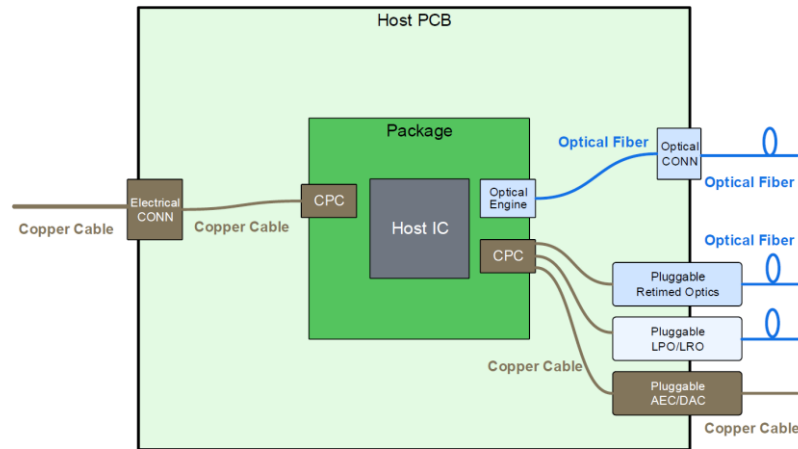
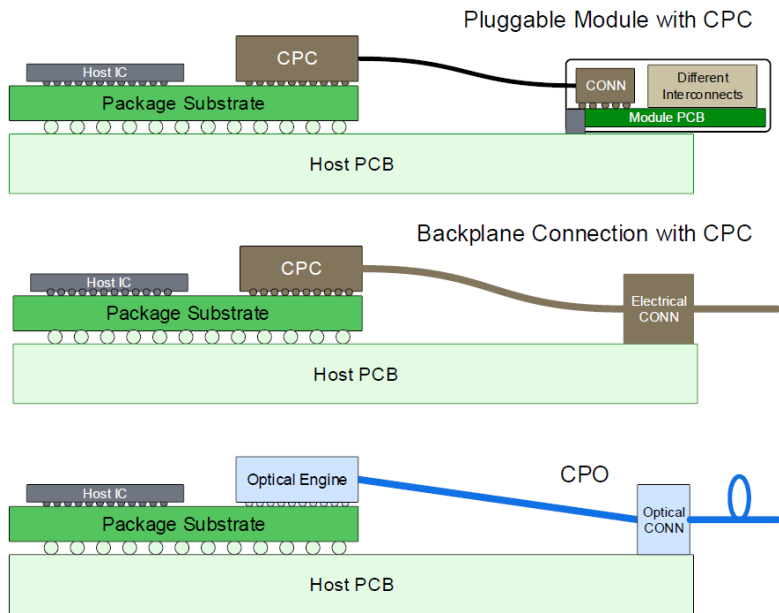
448G Next Generation Framework



OIF CEI-448G Framework Project Start in August 2024

Access the OIF 448G Framework
Document here: <https://www.oiforum.com/wp-content/uploads/OIF-FD-CEI-448G-01.0.pdf>

Typical 448G Electrical Applications



CPC: Co-packaged Copper

LPO/Linear: Linear Pluggable Optics

DAC: Direct Attach Copper Cables

CPO: Co-packaged Optics

LRO/RTLRO: Linear Receiver Optics

AEC: Active Electrical Cables

Channel Requirements and Characteristics

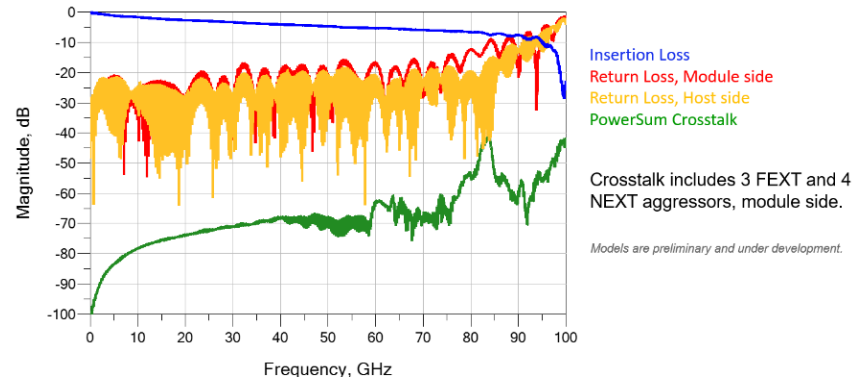
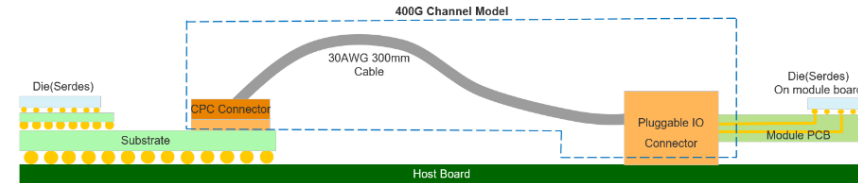
Increasing data rates lead to degradation in SNR due to increased conductive and dielectric losses, and noise from reflections and crosstalk

Increased I/O density exacerbates crosstalk concerns

Intra-pair skew can amplify jitter and inter-symbol interference, degrading the eye diagram

Current channel bandwidth is limited to approximately 90 GHz, largely due to connector technology, making PAM4 challenging for 448G

VSR Channel



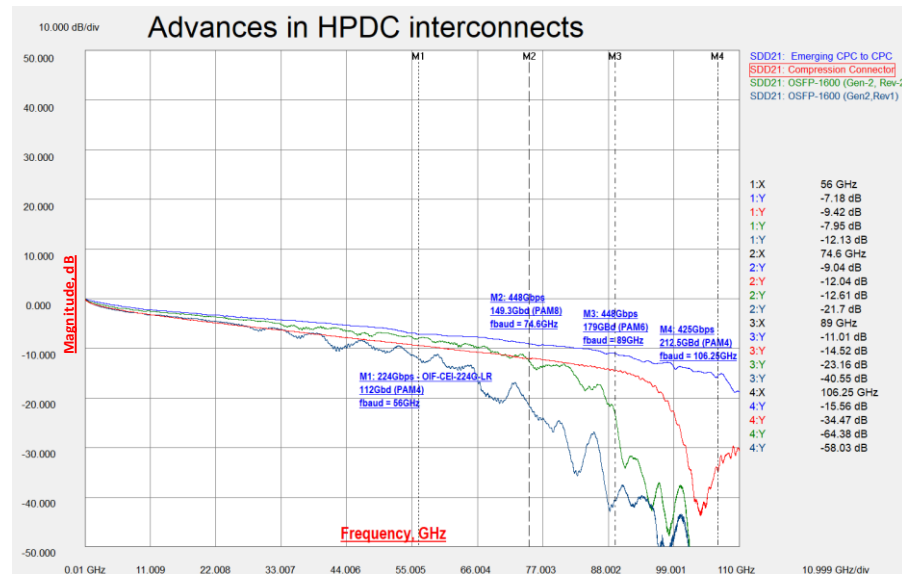
Channel Advancements

Meanwhile, emerging interconnect technologies and ongoing advancements in connector design offer promising pathways to overcome these bandwidth limitations.

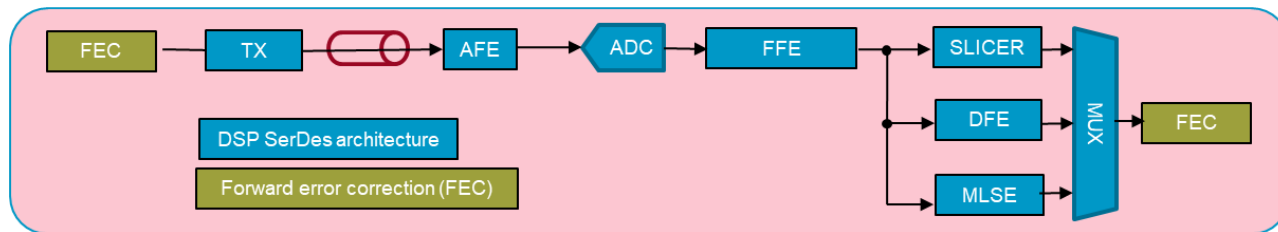
However, what if these existing connector/channel bandwidth limitations persist longer?

To meet fast pace of AI network demanding

- ▶ Short-term: Maximize existing infrastructure
 - Requires higher order modulation
- ▶ Mid-term: Address channel limitations without full-scale replacement
 - Use PAM4 where possible, e.g. XSR
 - Use higher order modulation where required, e.g. LR
- ▶ Long-term: Full-scale hardware transition
 - Full transition to lowest possible modulation
 - Use higher order modulation for longer reach or faster speed (e.g. > 448 Gbps)



SerDes Toolbox



Data rate per lane, Gb/s	10	25	50	100	200	400
Modulation	PAM-2	PAM-2	PAM-4	PAM-4	PAM-4	?
Nominal cable reach, m	7	5	3	2	1-2 ¹	?
Technology added	DFE	RS FEC	Stronger RS FEC	Floating-tap DFE	MLSD	Inner FEC?
Year²	2007	2014	2018	2022	2026 (est.)	?

¹ Nominal cable reach is a function of host class

² Year of publication of the IEEE802.3 Ethernet standard

New tools pulled from the toolbox with each generation
Used to address challenges presented by doubling the data rates

448G Interconnect Applications

Interconnect Application	Distance Up To	Types of interfaces	Potential CEI projects
Die to Die in a Package	~25mm	Electrical	XSR
Die to Optical Engine in a Package	~50 mm	Electrical	XSR/XSR+, Linear, RTL
Chip to nearby optical Engine	~150 mm	Electrical	XSR/XSR+, Linear(?), RTL(?)
Chip to pluggable module	~250 mm	Electrical	VSR, Linear(?), RTL(?)
Chip to chip within PCBA	~50 cm	Electrical or Optical	MR
PCBA to PCBA across a backplane/midplane/cable	~1 m	Electrical or Optical	LR
Chassis to Chassis within a rack	~1 m	Electrical or Optical	LR

CEI-448G-FD identified potential CEI-448G electrical interconnection applications

CEI-448G-VSR and CEI-448G-LR new projects start in February 2026

AGENDA

1	Overview of OIF's work on Energy Efficient Interfaces (EEI)	Jeff Hutchins, Ranovus OIF PLL WG EEI Vice Chair
2	Compute Optics Interface Energy Efficient Interfaces for Scale-up for AI	Mike Klempa, Qualcomm OIF Board Member OIF PLL Interoperability WG Chair
3	High-Density Connectors for Energy Efficient Interfaces	Nathan Tracy, TE Connectivity OIF Board President
4	Exploring the next data rate: 448G	Cathy Liu, Broadcom OIF Board Member
5	Q/A Panel Discussion	

Thank-you!

Mike Klempa, Panelist (OIF and Qualcomm)
Nathan Tracy, Panelist, (OIF and TE Connectivity)
Cathy Liu, Panelist (OIF and Broadcom)
Jeff Hutchins, Moderator (OIF and Ranovus)